Advanced Type-1c FLL for Enhancing Converters Synchronization During Frequency Drift

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***Abstract*—This paper introduces a novel out-loop compensation scheme with a selective filtering stage for Type-1 Frequency Locked Loop (FLL) to obtain the same features of Type-2 FLL in response to frequency drift. The proposed scheme can eliminate the phase angle error during frequency drift without compromising its benefits of the low order control system. The performance of the proposed Type1-c FLL is evaluated with alternatively employed Delayed Signal Cancellation (DSC), Low Pass Filter (LPF) with selective harmonics filtering and multiple second-order generalized integrator (MSOGI) as a pre-filtering stage under the various grid disturbances. The effects of each filtering scheme on the dynamic response and harmonics mitigation are identified. As each filter has a distinct advantage in response to each grid disturbance, a selective control approach is used to insert the most suitable filter based on the severity of the grid disturbance to achieve the best performance. A comprehensive study is conducted to demonstrate the superior performance of the proposed schemes with both simulation and experimental validation. In addition, the potential application of the proposed Type-1c FLL for enhancing the islanded microgrid operation has been presented and verified.**

***Index Terms*—Frequency-locked loop (FLL), frequency estimation and phase estimation, distortion elimination.**

I. Introduction

THE dynamic response and the accurateness of the grid voltage phase angle and frequency estimations under ideal and non-ideal grid conditions are crucial considerations for controlling most of the grid-connected power electronics devices [1]–[6]. The frequency variation and phase jump associated with the severe system disturbances may result in instability or improper response of the power converters [7]. For example, the nonlinear response of the synchronous reference frame (SRF-PLL) in a power converter failed to maintain the synchronism with the power grid due to the existence of multiple equilibrium points at post fault conditions. Therefore, an adaptive synchronization SRF-PLL is introduced with the capability of realizing the first-order PLL during the transient condition to ensure fast synchronization to the power grid. However, the phase jump and the steady-state phase angle error caused by frequency drift may result in degrading the performance of the power converter due to the improper active and reactive power control [7]. For example, in the islanded microgrid, the frequency is not fixed, and it varies in response to the loading conditions based on the deployed droop controllers for the inverter-based devices and the diesel generator. Therefore, the frequency may ramp up or down during the off-peak or peak loads, respectively. Thus, the existing synchronization schemes of PLLs and FLLs suffer from the steady-stage phase angle error as well as the phase jump during the frequency ramp. In addition, the asymmetrical operation of the PLL/FLL imposes another challenge during the frequency ramp/drift. Consequently, it may lead to islanded microgrid instability due to the improper active and reactive power flow [9]. Several researches proposed higher-order synchronization schemes such as Type-3 PLL/Type-2 FLL to compensate for the phase angle error during the frequency ramp. However, these schemes degrade the system stability and the transient response [9], [10]. The synchronous reference frame phase-locked loop (SRF-PLL) is widely used as a synchronization scheme, and can be looked at a second-order closed-loop control system [11]. Many PLLs are categorized based on their open-loop transfer function as Type-1, Type-2, and Type-3 PLLs. Type-1 PLL is characterized by having only one integrator in its control loop resulting in fast dynamic response and high stability margin [11]. However, both Type-1 and Type-2 PLLs cannot achieve zero average steady-state phase-error in the presence of frequency drifts [10]–[13]. The phase angle steady-state error during frequency drift is tackled by introducing Type-3 PLL with three cascaded integrators resulting in degradations in both the dynamic response and the stability margin [11], [14]–[17].

The pre-filters are essential to mitigate the influence of grid disturbances on the PLL response. The recent research focus on adding in-loop or pre-loop filters such as conventional Low Pass Filter (LPF) [18], Moving Average Filter (MAF) [16], [17], [19], Notch Filter [20], [21], Second-Order Generalized Integrator (SOGI) [22]–[24], Complex-Coefficient Filter [25], and Delayed Signal Cancellation [26]–[28]. Using in-loop pre-filters improves the PLL/FLL immunity to disturbance but results in a large phase delay and thus, degrading the PLL dynamic response [11], [16]. Many approaches have been suggested to reduce the

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influence of the pre-filters on the PLL dynamic response with effective distortion elimination such as using PID-Type LPF [16], lead compensator [19] and Quasi-Type-1(QT1) structure [11]. Alternatively, placing the pre-filters such as MAF in a stationary frame (out-loop) will enhance the distortion elimination of the PLL without a significant delay effect [11], [17]. The Notch Filter (NF) is another filter type for the PLLs that can be classified into cascade and parallel topologies based on their frequency estimation part [11]. The cascade topology implements each NF own with an individual frequency estimator [20], while for the parallel topology, all NFs have the same frequency estimator [21]. Moreover, the harmonics rejection selectivity is the main advantage of NF, which is achieved by using multiple NFs with different notch frequency setting "ω_g" (e.g.,: $2\omega_g,\ 6\omega_g,$ etc.) [11], [20]. Also, SOGI, known as dual QSG-SOGI-based PLL (DSOGI-PLL), is one of the commonly used integrated schemes for PLL [24]. Multiple SOGI (MSOGI-PLL) is introduced to mitigate a wide range of harmonics where multiple QSG-SOGIs are tuned at different harmonic frequencies [29]. The drawback of using notch filters and SOGI based filters is their high computational efforts when digitally implemented. The DSC is another type of filter that has a distinct preference compared to other filters due to its wide range of harmonics mitigation with a single-stage [11]. However, the in-loop DSC filter introduces a significant delay to the PLL dynamics response. This by delay can be reduced by relocating the DSC filter outside the PLL closed-loop (pre-loop) at the cost of adding more complexity and computational efforts [11], [28]. Another approach for estimating the frequency and the phase angle is recently presented in [9] and [30] for locking to the frequency of the input signals instead of tracking the phase angle. This type is known as a frequency-locked loop (FLL). Accordingly, the phase angle is estimated outside the control loop by using orthogonal voltage decomposition. A comprehensive analysis of high order FLL addressing its advantages and disadvantages is conducted in [31]. It is concluded that PLLs and FLLs are analogous systems but each is implemented in different reference frames. A review of recent advanced three-phase FLLs along with a study of the in-loop filter implementation for advanced FLLs can be found in [32]. In summary, several types of FLL are developed to tackle certain disturbance issues. Type -1 FLL is the simplest one that experiences a finite steady-state phase angle error during the frequency ramp [30]. To eliminate the phase angle steady-state error in response to the frequency ramp, a Type-2 FLL is proposed in [9]. Similarly, Type-3 PLL is introduced to resolve the same frequency ramp issue and recently, a new Type-2 PLL is introduced to obtain the feature of Type-3 PLL by introducing a unit delay to the forward loop without the need to increase the PLL order type [33].

In this paper, a new Type-1c FLL is developed to obtain the performance of Type-2 FLL without increasing the FLL order. The proposed Type-1c FLL has a potential application for the control and operation of the islanded microgrid. As the operation of the islanded microgrid relies on droop controllers for the coordination and power-sharing between the renewable-based generation units, battery energy storage systems (BESS) and diesel generator, the frequency varies within an operating range according to the IEEE Standard 1547-2018 [8]. Consequently, the islanded microgrid experiences a frequency ramp up or down at off-peak or peak-loads, respectively. This frequency ramp creates a challenging operation for the existing PLLs/FLLs such as the standard Type-1 FLL and Type-2 PLL due to the existence of the steady-state phase-angle error during the frequency ramp as well as a larger phase angle jump during disturbances [9]. Several synchronization schemes have been recently introduced aiming to compensate the steady-state phase-angle error such as Type-3 PLL/Type-2 FLL. Although Type-3 PLL and Type-2 FLL eliminate the phase angle steady-state error, they face several challenges regarding the stability and transient response as well as the immunity to grid disturbances [9], [14], [32]. To increase the immunity to grid disturbances, the proposed Type-1c FLL is augmented with a selective pre-filtering stage. The novelty of this scheme is mainly the seamless impact of the angle compensation on the closed-loop dynamic response since the compensation scheme of the phase angle is located outside the closed-loop control unlike the other schemes presented in [14], [32]. In addition, the proposed selective pre-filtering stage is dynamically changed depending on the grid disturbances to achieve the best performance in response to all grid dynamics and harmonics distortion individually as well as to a combined contingency of frequency ramp, voltage dip, etc.

II. Type-1 FLL Structure

The basic concept of the FLL under ideal grid condition depends on extracting the phase angle of the voltage vector from its orthogonal component in the stationary $\alpha\beta$ frame. The $\alpha\beta$-voltage coordinates can be expressed as:

$$\begin{cases} V_\alpha = V\sin(\omega t + \emptyset) \\ V_\beta = -V\cos(\omega t + \emptyset) \end{cases} \tag{1}$$

where V and $\emptyset$ are the amplitude and phase angle of the grid voltage vector. The grid frequency can be estimated by using the derivative of the orthogonal signal in (1) as follows:

$$\begin{cases} \frac{dV_\alpha}{dt} = \omega V\cos(\omega t + \emptyset) \\ \frac{dV_\beta}{dt} = \omega V\sin(\omega t + \emptyset) \end{cases} \tag{2}$$

By considering a balanced sinusoidal grid and normalizing (2) using the nominal grid voltage *V (V = 1 pu)*, the frequency can be calculated as follows:

$$\omega = \sqrt{\left(\frac{dV_\alpha}{dt}\right)^2 + \left(\frac{dV_\beta}{dt}\right)^2} \tag{3}$$

The time derivatives of (3) can be calculated for the discrete implementation purpose using backward differentiation assuming linear variation between two consecutive samples as follows:

$$\left(\frac{dV_\alpha}{dt}\right)^2 + \left(\frac{dV_\beta}{dt}\right)^2 \approx \omega^2 - \frac{\omega^4 {T_s}^2}{12} \tag{4}$$

where the term $\frac{\omega^4 {T_s}^2}{12}$ presents the discrete derivation error compensation that has been obtained using Maclaurin series as described in [30].

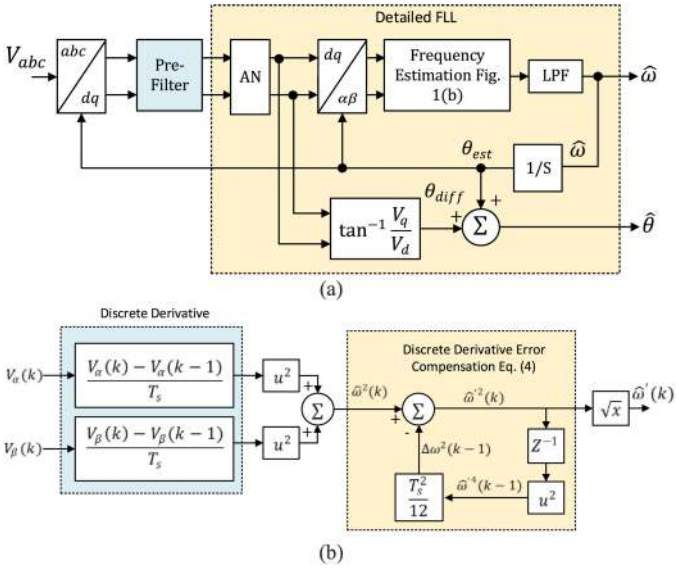

Fig. 1. (a) Detailed FLL scheme. (b) Frequency estimation loop.

The implementation of conventional FLL in dq-frame with a pre-filter stage is shown in Fig. 1. The pre-loop filter stage can be CDSC filter [26], pre-filter [30] or MSOGI filter [29]. The amplitude normalization block (AN) is employed to avoid frequency estimation errors [30]. A LPF is used with an error compensation scheme to enhance the distortion elimination capability shown in Fig. 1(b). As the tracking speed of the FLL depends on which the delay introduced by the LPF, a delay in the frequency estimation is experienced. Consequently, the estimated phase angle will not be perfectly locked to the grid voltage phase angle. To compensate the phase angle error, the difference between the positive-sequence grid voltage phase angle (θ_{diff}) and the estimated angle (θ_{est}) must be added to the estimate the phase angle ($\hat{\theta}$) in the dq-frame as expressed in (5):

$$\begin{cases} \theta_{diff} = \tan^{-1}\left(\frac{V_q}{V_d}\right) \\ \hat{\theta} = \theta_{est} + \theta_{diff} \end{cases} \tag{5}$$

The frequency can be estimated based on the FLL model shown in Fig. 1 with neglecting the input and output LPFs effect, using (1), (2), and (3), as follows [30]:

$$\hat{\omega}'^2(k) = \hat{\omega}^2(k) + \Delta\omega^2(k-1) \tag{6}$$

where k is the discrete-time domain number of samples,

If the input and output LPFs are considered, the mathematical model of Type-1 FLL with described in (6) can be presented in Fig. 2. Similarly, the mathematical model of the phase angle estimation loop can be represented as shown in Fig. 3 where θ_{diff} is expressed in the Laplace domain as follows:

$$\theta_{diff}(s) = G_{pf} \times \mathcal{L}aplace\left(\tan^{-1}\left(\frac{V_q}{V_d}\right)\right) \tag{7}$$

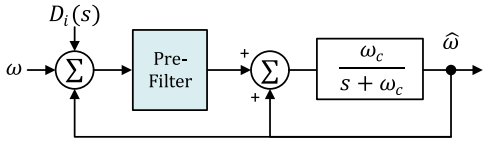

Fig. 2. Mathematical model frequency estimation loop [30].

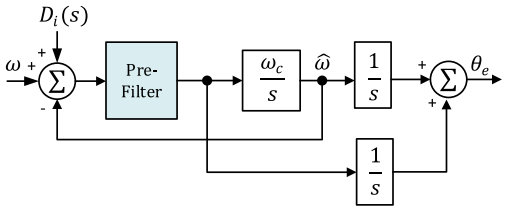

Fig. 3. Mathematical model of the phase angle estimation loop.

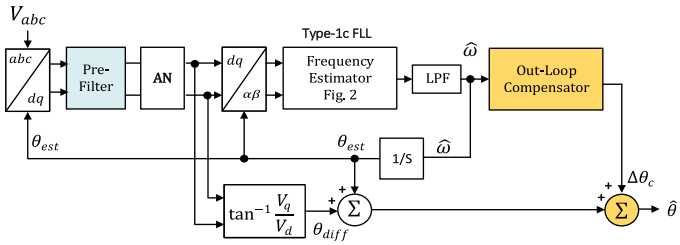

Fig. 4. Generalized scheme for the proposed Type-1c FLL scheme with a pre-filter and out-loop phase angle error compensation.

Substituting for V_d and V_q in (7) gives:

$$\theta_{diff}(s) = G_{pf} \times \mathcal{L}aplace\left(\tan^{-1}\left(\frac{\sin(\Delta\omega t)}{\cos(\Delta\omega t)}\right)\right) \tag{8}$$

If $\Delta\omega t$ is very small, the terms $\sin(\Delta\omega t) = \Delta\omega t$ and $\cos(\Delta\omega t) = 1$, hence $\frac{\sin(\Delta\omega t)}{\cos(\Delta\omega t)}$ is reduced to $\Delta\omega t$, and the Laplace transformation in (8) is obtained as $\frac{\Delta\omega}{s}$.

III. Proposed Out-Loop Phase Angle Compensation Scheme With Various Pre-Filters Types

The steady-state phase angle error during the frequency ramp is a chronic issue for Type-1 FLL as discussed in [30]. To obtain the same features of Type-2 FLL, a novel out-loop phase angle compensation scheme is introduced to the Type-1 FLL as shown in Fig. 4. The out-loop compensation concept has many advantages such as simplicity of implementation, preserving Type-1 FLL conventional structure order, and keeping the same dynamic response. As a result, the overall performance of the Type-1 FLL is improved. The angle compensation term should be calculated for each pre-loop filter type. In this context, different pre-loop filters are evaluated in this paper to identify the best one in response to various disturbances. In this section, the implementation of each filter and the corresponding angle compensation term are discussed for three main pre-filters types as follows:

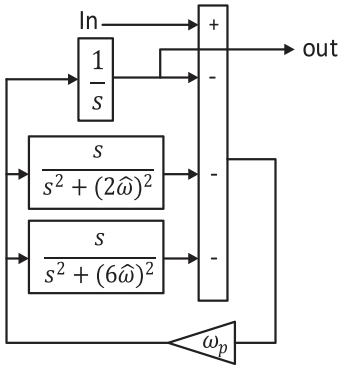

Fig. 5. Modified SLPF pre-filter basic structure.

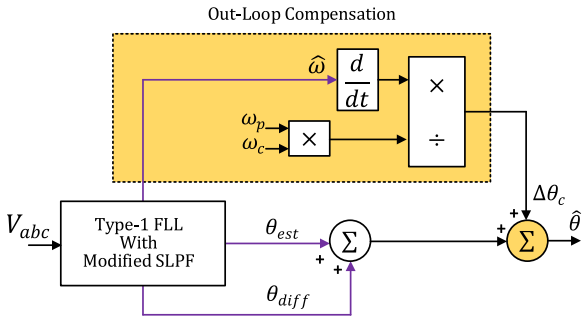

Fig. 6. Type-1c FLL out-loop compensation scheme with modified selective LPF pre-filter.

A. Modified Selective Harmonics LPF Compensation Angle Estimation

The modified Selective Low Pass Filer (SLPF) scheme acting as a pre-filter is shown in Fig. 5 where SLPF design avoids reducing the cut-off frequency under a heavily distorted grid to permit a faster response [30]. The related compensation angle can be calculated using the mathematical model shown in Fig. 3 and in response to a frequency ramp input ($\frac{\Delta\dot{\omega}}{S^3}$), where $\Delta\dot{\omega}$ is the frequency ramp rate in rad/s^2. Let's consider $\Delta\dot{\omega} = \Delta\delta$, the steady-state phase angle is obtained as follows:

$$\theta_e(s) = \frac{\Delta\delta}{s^3 + \omega_p s^2 + \omega_p\omega_c s} \tag{9}$$

The pre-filter is presented by a first-order transfer function as,

$$\frac{\omega_p}{s+\omega_p} \tag{10}$$

By applying the final value theorem to (9), the steady-state phase angle error is calculated as:

$$\theta_{e,ss} = \lim_{s\to 0} s\frac{\Delta\delta}{s^3 + \omega_p s^2 + \omega_p\omega_c s} = \frac{\Delta\delta}{\omega_p\omega_c} \tag{11}$$

As $\theta_{e,ss}$ presents the steady-state error during the grid frequency drift period, it can be used to compensate for the phase angle as shown in Fig. 6.

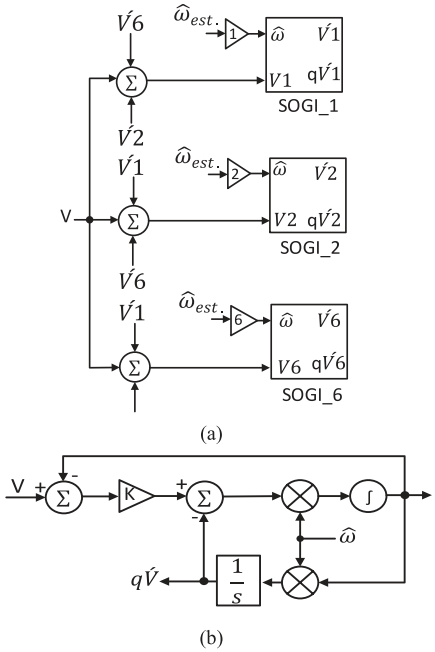

Fig. 7. MSOGI block diagram. (a) Basic structure. (b) SOGI block.

B. MSOGI Pre-Filter Compensation Angle Estimation

The block diagram of the MSOGI filter is shown in Fig. 7. The MSOGI consists of multiple SOGI blocks which are individually tuned at a specific frequency to improve the performance of the DSOGI filter especially under highly distorted grid conditions [35], [36]. The MSOGI requires two additional SOGI blocks with a cross-feedback scheme for each harmonic order 'h'. The basic structure of SOGI is shown in Fig. 7(b), and its characteristic transfer functions are expressed as follows:

$$\begin{cases} D(s) = \frac{V'(s)}{V(s)} = \frac{k\hat{\omega}s}{s^2+k\hat{\omega}s+\hat{\omega}^2} \\ Q(s) = \frac{qV'(s)}{V(s)} = \frac{k\hat{\omega}}{s^2+k\hat{\omega}s+\hat{\omega}^2} \end{cases} \tag{12}$$

where k is the damping factor, and $\hat{\omega}$ is the estimated fundamental frequency. V' and qV' are the direct and quadrature components of the input signal 'V', respectively.

It is worth mentioning that the value of k in each DSOGI-QSG is divided by the corresponding harmonic order to keep the product $k\hat{\omega}$ constant so that the same bandwidth is guaranteed for all DSOGI-QSGs. The compensation angle $\Delta\theta_c$ is calculated by applying the final value theorem to the closed-loop T.F as follows:

$$\theta_{e,ss}(s) = \lim_{s\to 0} s\frac{1}{1+G_{\theta_{ol}}}\theta(s) = \frac{\Delta\delta}{2s^3 + k\hat{\omega}s^2 + k\omega_c\hat{\omega}s} = \frac{2\Delta\delta}{k\omega_c\hat{\omega}} \tag{13}$$

According to (13), the phase angle error compensation term is,

$$\Delta\theta_c = \theta_{e,ss} = \frac{2\Delta\delta}{k\omega_c\hat{\omega}} \tag{14}$$

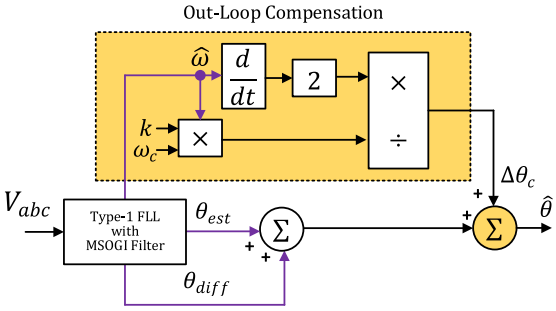

Fig. 8. Type-1c FLL out-loop compensation scheme with MSOGI pre-filter.

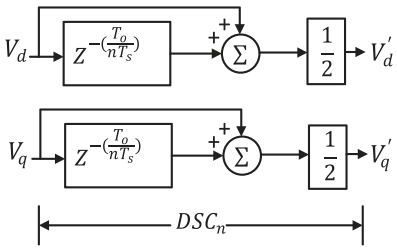

Fig. 9. Generalized DSC with delay factor n.

The corresponding Out-Loop compensation scheme is shown in Fig. 8

C. DCS Pre-Filter Compensation Angle Estimation

The DSC filter's basic idea is to add the signal to its delayed version to cancel a specific range of harmonics [27]. The DSC generalized scheme, shown in Fig. 9, has a selective feature for canceling specific harmonics through its delay factor 'n'. Different DSC orders can be connected in cascaded mode (CDSC) to increase the harmonics filtering capability. DSC can be approximated by a simple first-order T.F as follows [26]:

$$CDSC_{n_1,n_2,\ldots n_m}(s) = \frac{1}{\underbrace{\frac{1}{2}T_o\left(\frac{1}{n_1}+\frac{1}{n_2}+\cdots\frac{1}{n_m}\right)}_{T_d}s+1} \tag{15}$$

where $n_1,\ n_2,\ n_3,\ \ldots\ n_m\ \in\{2,4,8,16,\ldots\}$, and T_d is the equivalent time delay introduced by the CDSC, which can be calculated as follows:

$$T_d = \sum_{n=2,4,8,\ldots}\frac{T_o}{n} \tag{16}$$

It is common to implement DSC with a delay factor equals to 4 (DSC4) to cancel the negative sequence and the 5th, and 7th harmonics. The delay time for DSC4 can be obtained from (16) equals to $\frac{T_o}{4}$. The mathematical model of the phase angle estimation loop using a generic DSCn is shown in Fig. 10(a), while the reduced model is shown in Fig. 10(b). Based on the closed-loop system shown in Fig. 10, the phase angle error

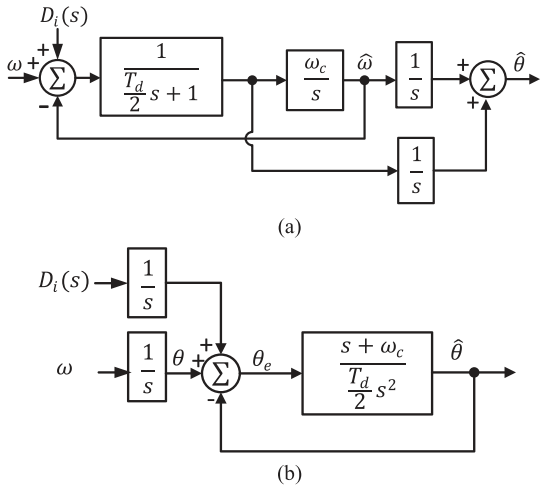

Fig. 10. Phase angle estimation loop. (a) Exact model. (b) Reduced model.

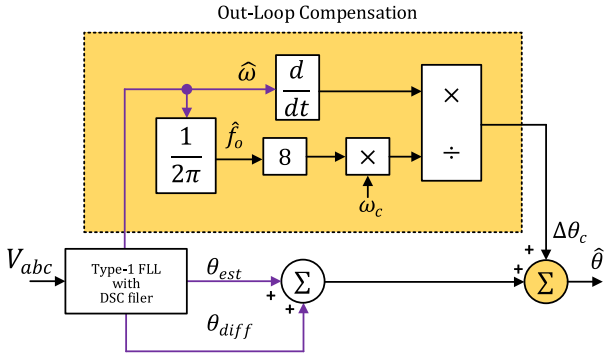

Fig. 11. Type-1c FLL out-loop Compensation scheme with DSC4 pre-filter.

transfer function in response to a frequency ramp input is:

$$\theta_e(s) = \frac{1}{1+G_{\theta_{ol}}}\theta(s) = \frac{\frac{T_d}{2}\Delta\delta}{\frac{T_d}{2}s^3+s^2+\omega_c s} \tag{17}$$

Applying the final value theorem to (17):

$$\theta_{e,ss} = \lim_{s\to 0} s\frac{\frac{T_d}{2}\Delta\delta}{\frac{T_d}{2}s^3+s^2+\omega_c s} = \frac{T_d\,\Delta\delta}{2\omega_c} \tag{18}$$

The phase angle error compensation term for DSC4 is obtained from (18) by using $T_d = \frac{T_o}{4}$ as follows:

$$\Delta\theta_c = \theta_{e,ss} = \frac{T_d\,\Delta\delta}{2\omega_c} = \frac{T_o\,\Delta\delta}{8\omega_c} \tag{19}$$

The corresponding Out-Loop compensation scheme is shown in Fig. 11.

IV. Proposed Selective Pre-Filter Scheme

Each of the presented pre-filter schemes has distinct features in response to the different disturbances. Therefore, there is a need to select the optimum selective pre-filter stage to obtain the best performance. To improve the distortion elimination of the proposed Type-1c FLL while obtaining the desired response, it is

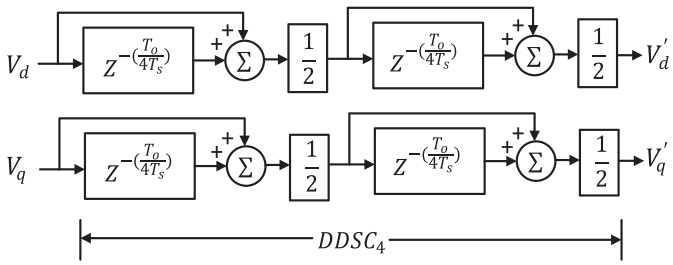

Fig. 12. DDSC4 block diagram.

proposed to use two identical DSC4 in cascade mode (DDSC4) as shown in Fig. 12. The compensation angle can be calculated following the same steps as described by (15) to (19) as follows:

$$G_{DDSC}(s) = \frac{1}{\frac{T_o}{2}\left(\frac{1}{4}+\frac{1}{4}\right)s+1} = \frac{1}{\frac{T_o}{4}s+1} \tag{20}$$

The corresponding phase angle error can be calculated as:

$$\theta_{e(DDSC)} = \frac{1}{1+G_\theta} = \frac{\frac{T_d}{2}s^2}{\frac{T_d}{2}s^2+s+\omega_c} \tag{21}$$

By applying the frequency ramp $= \frac{\Delta\dot{\omega}}{s^3}$ to (21):

$$\theta_e(s) = \frac{\frac{T_d}{2}\Delta\delta}{\frac{T_d}{2}\left(s^3+s^2+\omega_c s\right)} \tag{22}$$

Applying final value theorem lead to:

$$\theta_{e,ss}(s) = \lim_{s\to 0} s\frac{\frac{T_d}{2}\Delta\delta}{\frac{T_d}{2}s^3+s^2+\omega_c s} = \frac{\frac{T_d}{2}\Delta\delta}{\omega_c} = \frac{T_o\Delta\delta}{4\omega_c} \tag{23}$$

As a result, the angle compensation term is calculated as:

$$\Delta\theta_c = \theta_{e,ss} = \frac{T_o\Delta\delta}{4\omega_c} \tag{24}$$

It is proposed to have a pre-filter selective scheme for Type-1c FLL as shown in Fig. 13. The proposed scheme uses frequency adaptive DSC type and two different angle compensation terms for DSC and DDSC based on (19) and (24). The selection logic shown in Fig. 13(b) is implemented to obtain the best performance depending on the disturbance type. The selective control scheme inserts the DDSC4 pre-filter once the estimated grid frequency starts to drift in the presence of grid disturbance while in other cases, the DSC4 is activated. It is observed that both DSC4 and DDSC4 have similar steady-state performances when the grid frequency is fixed. On the contrary, when the grid frequency starts to drift, both filters behave differently accordingly. Thus, the proper pre-filter is inserted. The selective controller relies on detecting both grid disturbances and frequency deviation to latch the switching logic.

V. Stability Assessment of the Proposed Scheme

This section aims to analyze the frequency and the phase estimation loops in terms of the gain and phase margin with selected parameters. As previously mentioned, the dynamic response of the FLL depends on the time constant of the output filter (T_c). Therefore, it will be fixed for all FLLs schemes to

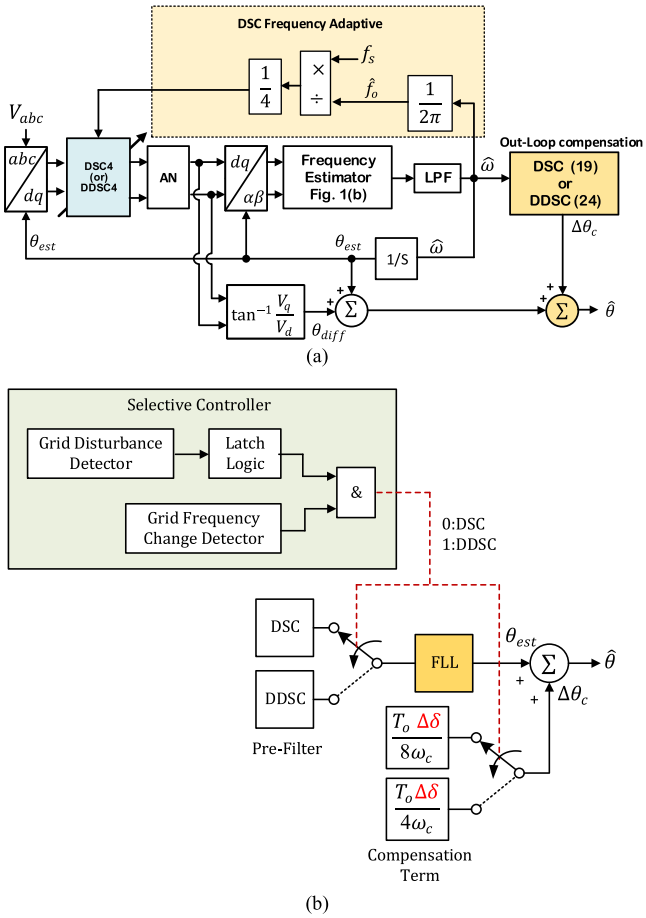

Fig. 13. Proposed Type-1c FLL scheme. (a) Entire scheme. (b) Selective control scheme.

(1/133). The open-loop and closed-loop transfer functions of the frequency estimation loop can be expressed as follows:

$$G_{\omega_{ol}} = G\_pf \times \frac{\omega_c}{s} \tag{25}$$

$$G_{\omega_{cl}} = \frac{G_{\omega_{ol}}}{1+G_{\omega_{ol}}} \tag{26}$$

By using (25) and (26), the open-loop and the closed-loop transfer functions of the frequency estimation loop of FLLs with DDSC4 can be written as follows:

$$G_{\omega\,(DSC)_{ol}} = \frac{\omega_c}{\frac{T_d}{2}s^2+s} \tag{27}$$

$$G_{\omega(DSC)_{cl}} = \frac{\omega_c}{\frac{T_d}{2}s^2+s+\omega_c} \tag{28}$$

The transfer function, presented by (28), is presented in the standard second-order form as follows:

$$G_{\omega(DSc)_{cl}} = \frac{{\omega_n}^2}{s^2+2\zeta\omega_n s+{\omega_n}^2} \tag{29}$$

Using (15), the time delay T_d introduced by DSC4 and DDSC4 equals to $\frac{T_o}{4}$ and $\frac{T_o}{2}$, respectively. Using (28), the damping factors (ζ_{DSC4} and ζ_{DDSC4}) when alternatively employing DSC4 and DDSC4 considering $\omega_c = 133$ and $T_o = 20$ ms are 0.87 and 0.61, respectively, which indicates that both

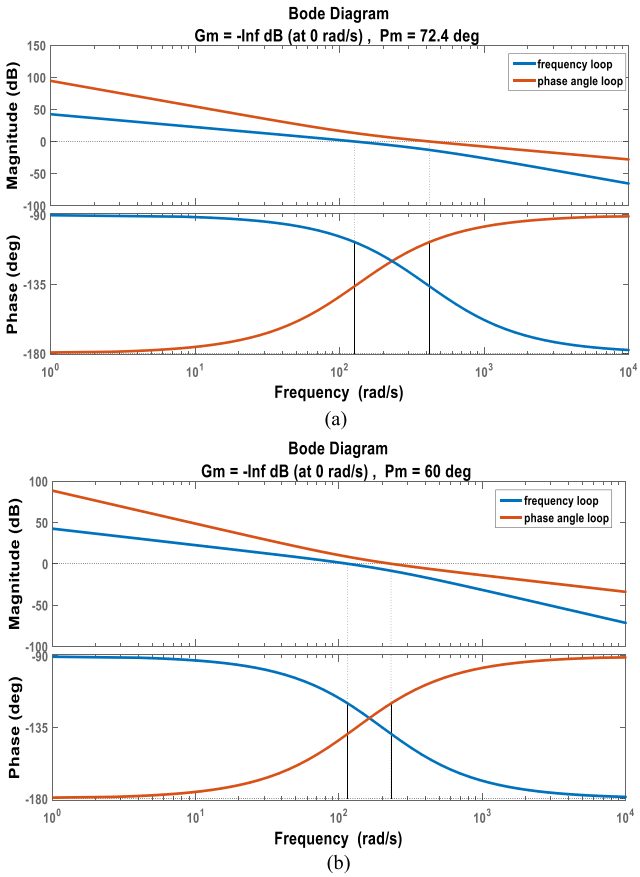

Fig. 14. Bode plot of the open-loop transfer function. (a) DSC-FLL. (b) DDSC-FLL.

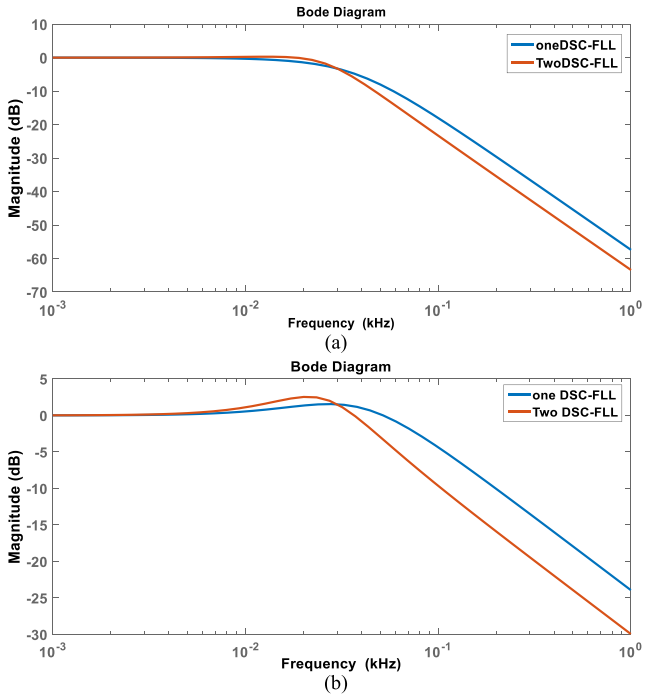

Fig. 15. Closed-loop magnitude response. (a) frequency estimation loop. (b) phase angle estimation loop.

schemes are underdamped. Also, the DSC4 scheme will have a lower overshoot value and less settling time. The bode plots of the open-loop transfer functions of the frequency and phase angle estimation loops with selected control parameters for both DSC-FLL and DDSC-FLL are shown in Fig. 14. It can be noticed that both schemes have infinity gain margin and phase margins of 72° and 60° for DSC-FLL and DDSC-FLL, respectively. A higher phase margin indicates that DSC-FLL will have a lower overshoot during the phase-angle jump. Also, the phase margin degradation is expected due to the additional delay introduced by DDSC4 scheme. It can be observed from Fig. 15 that both schemes have the same bandwidth for the frequency estimation loop whereas, for angle estimation loop, the DSC-FLL has a wider bandwidth.

On the other hand, the DDSC-FLL provides a higher attenuation for the estimated frequency and phase angle amplitudes than the DSC-FLL resulting in a higher filtering capability.

VI. Experimental Results

The performance of the proposed Type-1c FLL with different pre-loop filters such as DSC4, modified SLPF pre-filter, and MSOGI is evaluated using dSPACE-DS1103 Digital Signal Processor (DSP). The performance of the compensation scheme with different pre-filters is evaluated in response to a frequency ramp under three scenarios. The effectiveness of the proposed scheme is verified by comparing the performance of conventional Type-1 FLL with the proposed Type-1c FLL. The comparative results are illustrated in Table I to demonstrate the superior performance of Type-1c FLL in response to various grid disturbances.

TABLE I
Comparison of the Proposed Schemes Under Various Test Conditions

	DSC4	Modified SLPF	MSOGI	DDSC4
2 Hz Frequency ramp				
-phase angle error without compensation	**0.07°**	0.109°	0.161°	0.14°
- compensation time	**23 ms**	43.6 ms	70.9 ms	59.2 ms
- compensated angle error overshoot	**−0.0047°**	0.0205°	0.036°	0.021°
10 % voltage dip with -2 Hz Frequency ramp				
-peak angle error during frequency ramp	0.0014°	0.0047°	0.0056°	**0°**
-peak angle error during constant frequency	**0°**	0.0008°	0.0011°	**0°**
5th harmonics with -2 Hz frequency ramp				
- Compensated peak-to-peak phase angle error	0.2189°	0.2353°	0.4337°	≅ 0°
-un-compensated peak-to-peak phase angle error	0.04392°	0.03096°	0.04368°	≅ 0°

A. Frequency Ramp Test

In this test, the grid frequency ramps down from 50 Hz to 48 Hz in 200 ms as shown in Fig. 16. It can be observed that the DSC-FLL, modified SLPF pre-filter-FLL, MSOGI-FLL, DDSC- FLL show almost 0.07°, 0.109°, 0.161°, and 0.14° phase angle error without the compensation scheme during the frequency ramp period, respectively. Alternatively, with the proposed compensation scheme, the error is compensated with a response time of 23 ms, 43.6 ms, 70.9 ms, and 59.2 ms, respectively with acceptable transient overshoots as shown in Fig. 16.

B. Frequency Ramp With Asymmetrical Voltage Dip Test

The performance of the proposed compensation scheme under 10% voltage dip of phase A with grid frequency ramping from 50 Hz to 48 Hz (ramp time: 200 ms) is shown in Fig. 17.

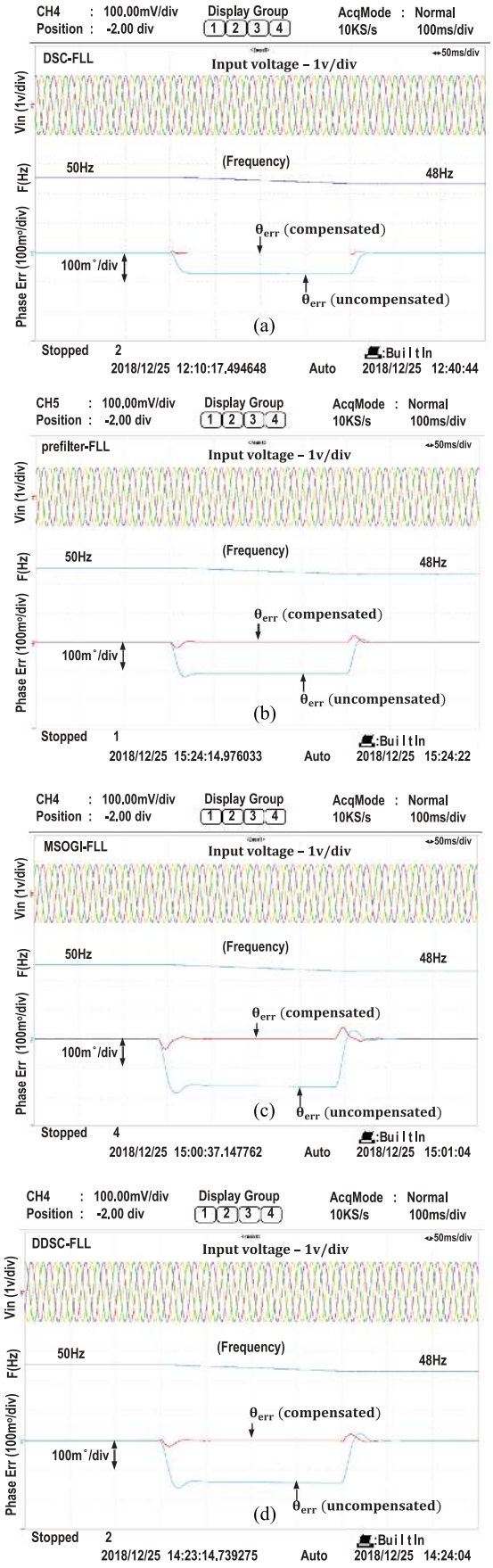

Fig. 16. Frequency ramp test. (a) DSC4 (b) SLPF pre-filter (c) MSOGI. (d) DDSC4.

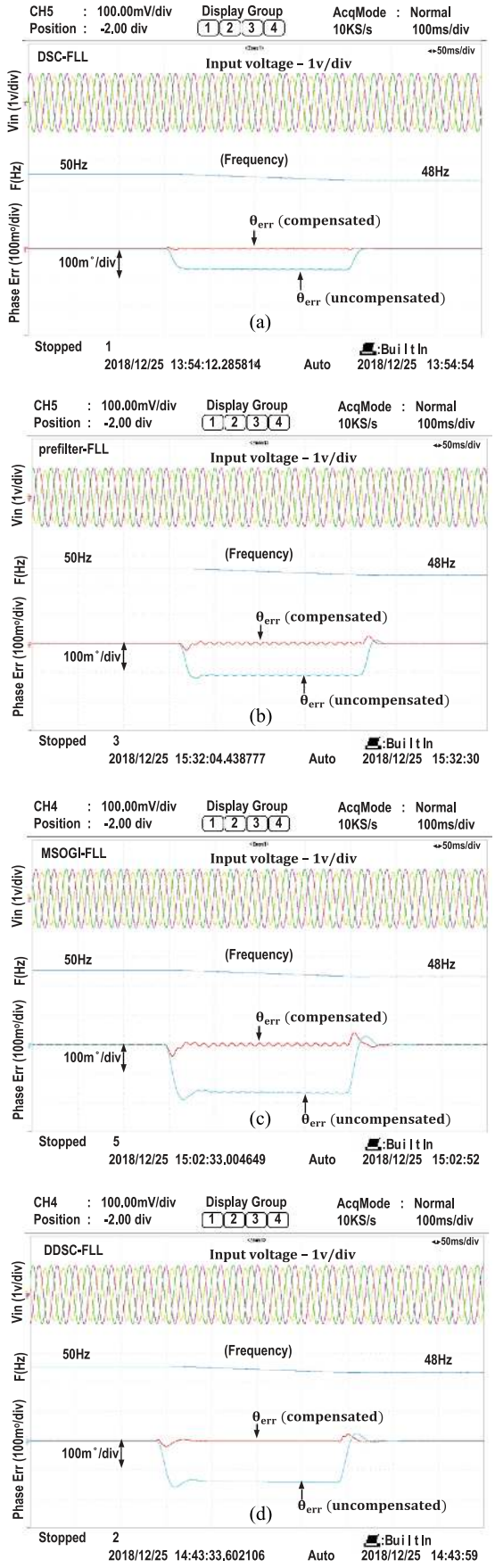

Fig. 17. 10% voltage dip + Frequency ramp test. (a) DSC4. (b) Modified SLPF pre-filter. (c) MSOGI. (d) DDSC4.

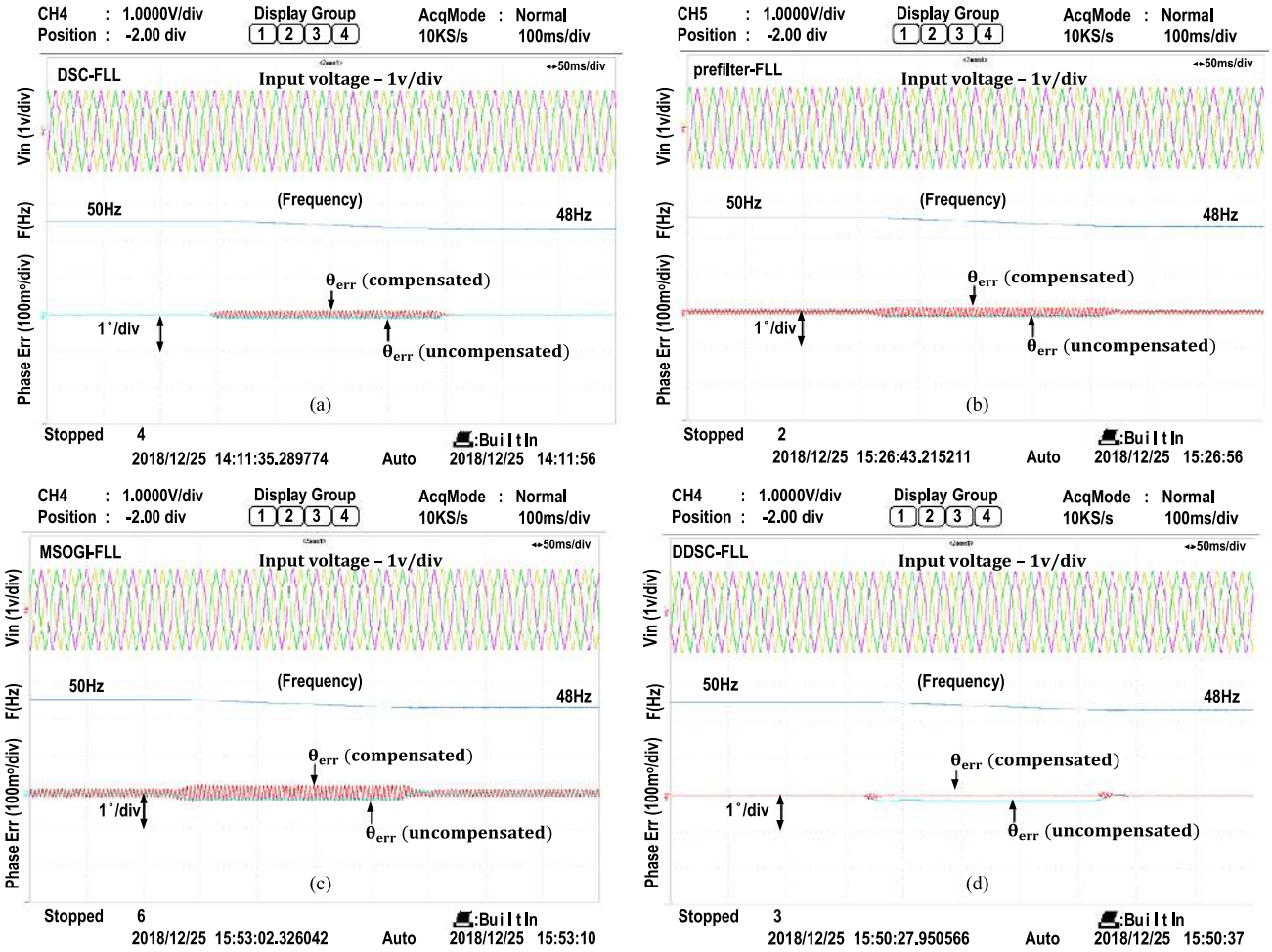

Fig. 18. 5th Harmonic with frequency ramp test. (a) DSC4. (b) Modified SLPF pre-filter. (c) MSOGI. (d) DDSC4.

DDSC-FLL schemes demonstrate superior performance on mitigating the residual oscillations as shown in Fig. 17(d). The response of the other filters schemes contained sustained oscillation as shown in Fig. 17(a) and Fig. 17(c).

C. Frequency Ramp With the 5th Order Harmonic Test

The performance of the proposed compensation scheme is evaluated in response to a combined contingency of frequency ramp from 50 Hz to 48 Hz in 200 ms and 10% of the 5th order harmonics as shown in Fig. 18. The steady-state phase angle error for all schemes, except for the Type-1c FLL with the DDSC4 scheme, starts to have oscillations during the frequency ramp period. It can be noticed that the peak to peak oscillations of 0.0439 °, 0.031°, 0.0437°, and $\approx 0°$ are recorded for DSC-FLL, modified SLPF pre-filter-FLL, MSOGI-FLL, and DDSC-FLL, respectively.

Considerable oscillations appear in the phase angle error while employing the compensation scheme as illustrated in Table I.

D. Selective Filter Scheme Performance Test

The performance of the proposed selective filter scheme (DSC4/DDSC4) for Type-1c FLL is tested with a grid contaminated with 10% of the 5th order harmonics and 40% phase A voltage dip to demonstrate the superior performance of the proposed Type-1c FLL with the selective filter as shown in Fig. 19. The results demonstrate the effectiveness of the selective scheme in mitigating the steady-state phase angle error. The best performance for the combined contingency is obtained by on-line altering the pre-filter stage from DSC4 to DDSC4 when frequency ramp is detected. The proposed Type-1c FLL scheme outperforms the performance of other schemes that fail to demonstrate acceptable performance under all test cases.

VII. Implementation of the Out-Loop Compensation Scheme to Type-2 PLL

In this section, the out-loop compensation scheme is also augmented with Type-2 PLL (referred to as Type-2c PLL) to show the generalized implementation of the proposed compensation scheme. Type-2 PLL is known for its inability to track a frequency ramp input. Increasing the order of

Type-2 PLL, which is known as Type-3 PLL, will result in eliminating the phase angle error during the frequency ramp period that can mainly be avoided by augmenting the proposed out-loop compensation scheme. The detailed analysis of the compensated Type-2 PLL is carried out by using the

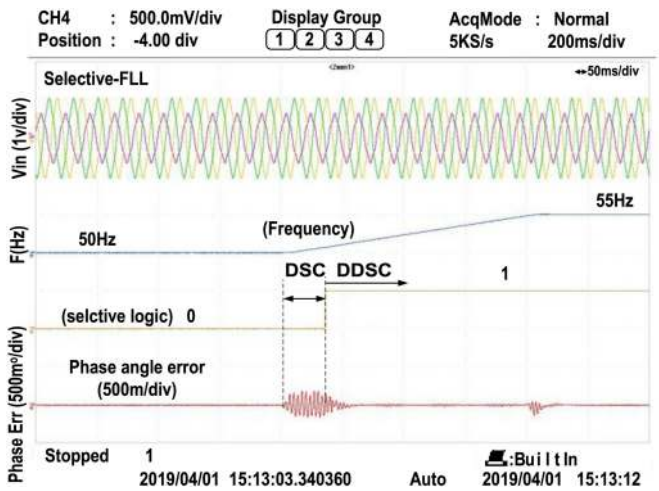

Fig. 19. Performance of the selective filter with the compensation scheme.

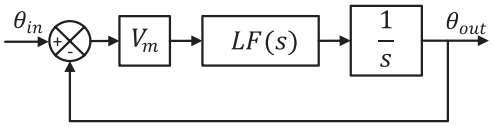

Fig. 20. Small-signal model of Type-2-PLL.

conventional small-signal model shown in Fig. 20, where loop filter $LF(s)$ is commonly a standard PI controller. The system response to a frequency ramp input can be analyzed with considering the closed-loop T.F of Type-2 PLL as follows:

$$\theta_{out}(s) = \frac{s}{s + LF(s)\,V_m}\theta_{in}(s) \tag{30}$$

where $\theta_{in}(s)$ represents the grid frequency change. If the frequency changes as a ramp, function, the s-domain presentation of the input signal is then given by $\frac{\Delta\delta}{s^3}$. Using (30), the phase angle error can be calculated as follows:

$$\theta_{out}(s) = \frac{s}{s + LF(s)\ V_m}\frac{\Delta\delta}{s^3} = \frac{\Delta\delta}{s + LF(s)\ V_m}\cdot\frac{1}{s^2} \tag{31}$$

Substituting $LF(s)$ with the standard PI controller transfer function ($\frac{k_p s + k_i}{s}$) yields:

$$\theta_{out}(s) = \frac{\Delta\delta}{s + \left(\frac{k_p s + k_i}{s}\right)\ V_m}\cdot\frac{1}{s^2} \tag{32}$$

The final value theorem is used to calculate the steady-state phase angle error as follows:

$$\theta_{e,ss} = \lim_{s\to 0} s\,\theta_{out}(s) = \lim_{s\to 0}\ s\frac{\Delta\delta}{s + \left(\frac{k_p s + k_i}{s}\right)\ V_m}\cdot\frac{1}{s^2} \tag{33}$$

The compensation angle $\Delta\theta_c$ can be obtained by evaluating (33) as follows:

$$\Delta\theta_c = \theta_{e,ss} = \frac{\Delta\delta}{V_m\ k_i} \tag{34}$$

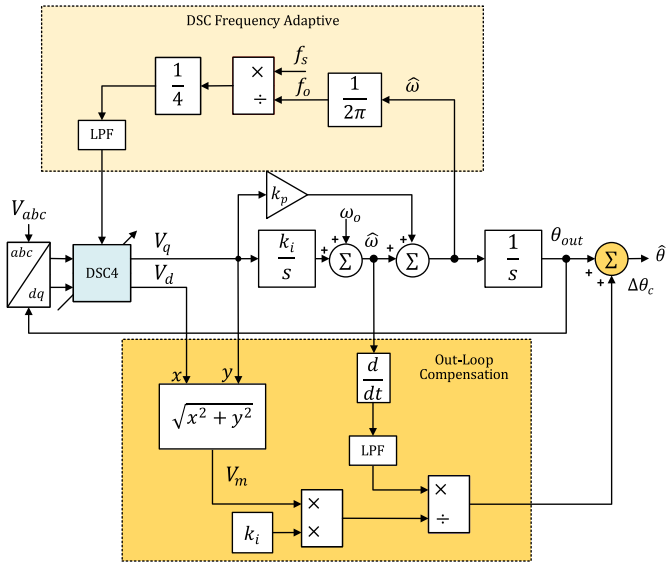

Fig. 21. Proposed Type-2c PLL.

TABLE II
*DESIGN PARAMETERS [14], [28]

Type2-c PLL		Type-3 PLL	
Design loop delay for DSC4 'T_d'	2.5 ms	Phase Margin (PM)	47°
Proportional gain 'k_p'	166	Cutoff frequency (ω_c)	2π17.78
Integral gain 'k_i'	11372	c_{n0}	187277.5
Open loop bandwidth 'ω_c'	165 rad/sec	c_{n1}	8511.5
Phase margin 'PM'	43.8^0	c_{n2}	96.7

*The parameter design criteria is listed in the Appendix.

The implementation of (34) is shown in Fig. 21. A frequency adaptive DSC4 filter is employed as a filter similar to the proposed Type-1c FLL scheme. The performance of Type-1c FLL and Type-2c PLL is evaluated using several grid disturbance tests in comparison with the conventional Type-2 FLL and Type-3 PL. All tests are performed under a frequency ramp from 50 Hz to 48 Hz in 200 ms.

A. Comparative Performance of Type-1c FLL & Type-2c PLL With Type-2 FLL and Type-3 PLL Schemes

For a fair comparison, the test sequence and the parameters are taken from [34] as illustrated in Table II. In addition, comprehensive test cases are carried out as follows:

- Case 1: frequency ramp from 50 Hz to 48 Hz in 200 ms.
- Case 2: frequency ramp with 40% voltage dip.
- Case 3: frequency ramp with 10% 5th harmonics.
- Case 4: frequency step with -2 Hz from 50 Hz to 48 Hz.
- Case 5: Voltage phase angle jump with $+20$ degrees.
- Case 6: switch over between single DSC4 and DDSC4 in case of a frequency ramp with 5% of the 5th order harmonic and 40% phase A voltage dip.

The simulation results demonstrate the superior performance of the proposed Type-1c FLL and Type-2c PLL as well as the effectiveness of the selective filter technique as shown in Figs. 22 to 27. In all test cases, the presented schemes have

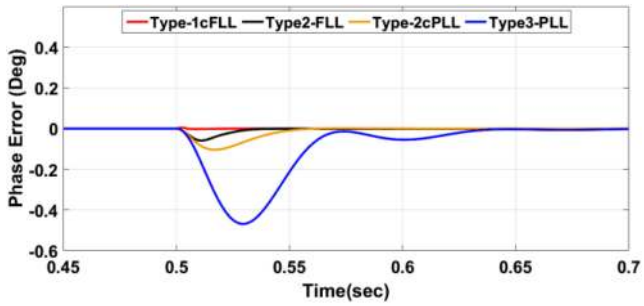

Fig. 22. Simulation results for test case 1.

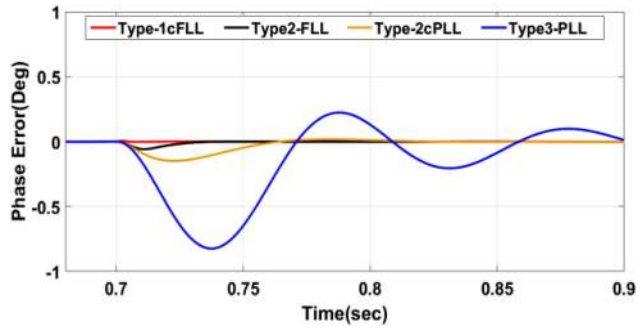

Fig. 23. Simulation results for test case 2.

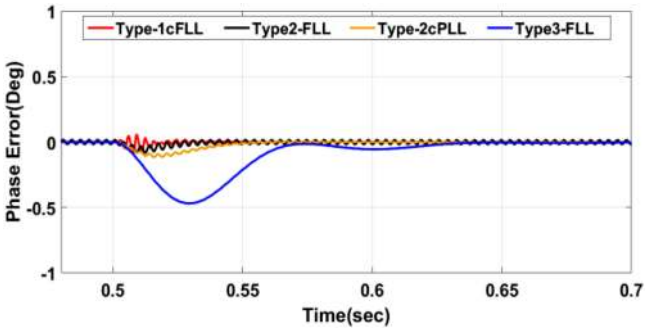

Fig. 24. Simulation results for test case 3.

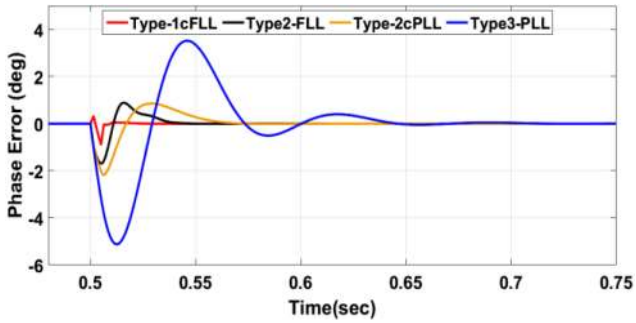

Fig. 25. Simulation results for test case 4.

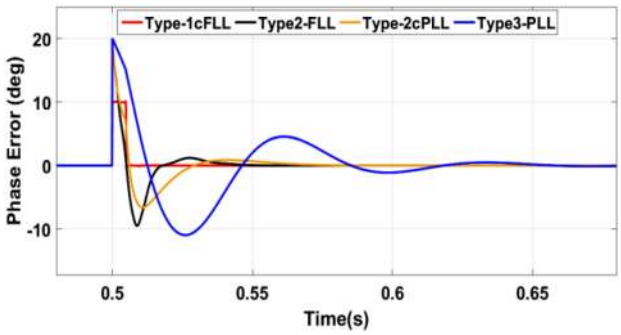

Fig. 26. Simulation results for test case 5.

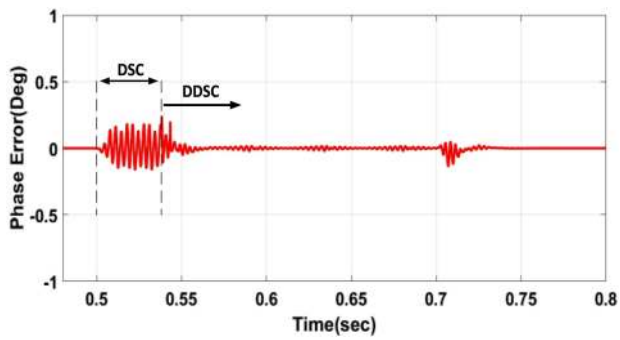

Fig. 27. Simulation results for test case 6.

successfully mitigated the steady-state phase angle error, even at highly distorted grid conditions, with different response times for each synchronization scheme. The proposed Type-1c FLL compensated the phase angle error during the frequency ramp while preserving the order of Type-1. Also, the Type-2c PLL maintains zero steady-state phase-angle error without increasing the order of the control system. Thus, it realizes the same feature of Type-3 PLL while maintaining faster response and higher transient margin.

In addition, the proposed Type-1c FLL shows the best performance compared to other schemes as illustrated in Table III. It can be noticed from Fig. 27 that implementing the DDSC filter reduces significantly the amount of residual distortion due to harmonics content. However, the results demonstrate the effectiveness of the selective scheme in mitigating the phase angle error.

B. Experimental Validation of the Proposed Type-1c FLL and Type-2c PLL

This experimental section introduces a comparison between the proposed out-loop compensation schemes Type-1c FLL and Type-2c PLL with the dominant types of Type-2 FLL and Type-3 PLL presented in the literature. In addition, the design and the performance of the Type-1c FLL including the selective scheme are validated. Therefore, the following test scenarios are carried out to validate the effective performance of Type-1c FLL and Type-2c PLL with respect to Type-2 FLL and Type-3 PLL, respectively:

- Frequency ramp from 50 Hz to 48 Hz in 200 ms.
- Frequency ramp with 40% voltage dip.
- Frequency ramp with 10% 5^{th} harmonics.
- Voltage phase angle jump with $+20$ degrees.

TABLE III
COMPARISON UNDER VARIOUS TEST CONDITIONS

	Proposed Type-1c FLL	Type2-FLL	Proposed Type-2c PLL	Type3-PLL
2 Hz Frequency ramp				
- Peak phase angle deviation	**0.0047**	0.059	0.104	0.468
- Settling time (2% criterion)	≈ 0 s	24 ms	44 ms	125.2 ms
40% voltage dip with -2 Frequency ramp				
- Peak phase angle deviation	**0.0047**	0.059	0.148	0.824
- Settling time (2% criterion)	≈ 0 s	24 ms	57.2 ms	>200 ms
-2 Hz frequency step				
- Peak phase angle deviation	**-0.9**	-1.7	-2.17	-5.11
- Settling time (2% criterion)	≈ 20 ms	44 ms	67.9 ms	206.2 ms
+20° phase angle jump				
- phase angle Settling time	**5 ms**	**51.7 ms**	**80 ms**	**>100 ms**

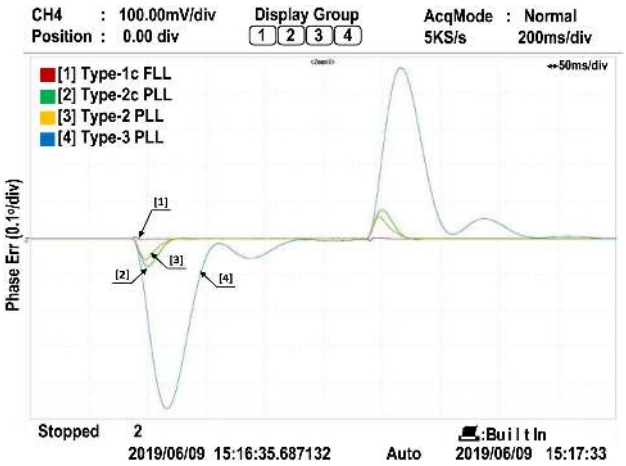

Fig. 28. Frequency ramp test.

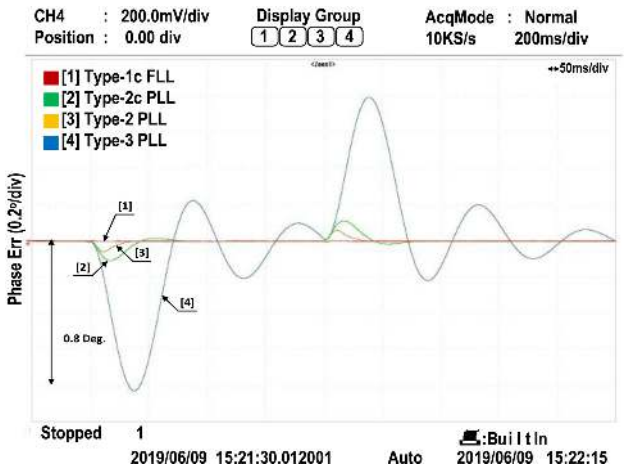

Fig. 29. 40% voltage dip + Frequency ramp test.

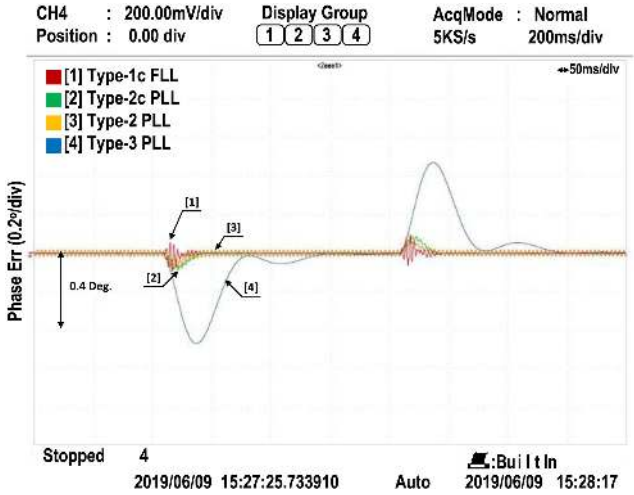

Fig. 30. 10% 5th harmonics + Frequency ramp test.

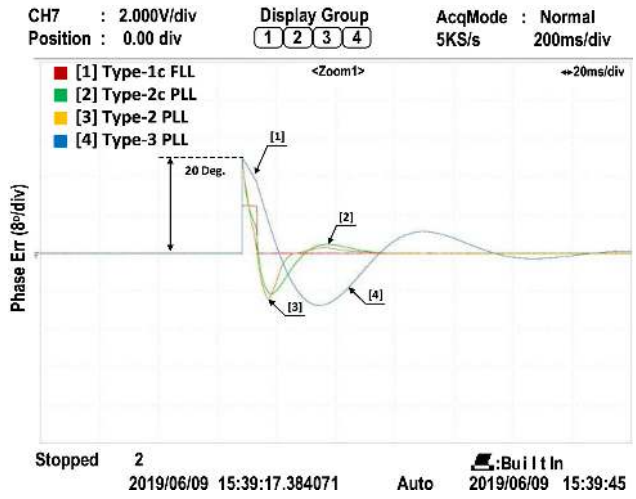

Fig. 31. Phase angle jumps with +20 degrees.

Various experimental results for all schemes are obtained using dSPACE-DS1103 Digital Signal Processor (DSP). The discrete models are sampled at 10 kHz with the same design parameters used for the obtained simulation results. The results shown in Figs. 28 to 31 validate the superior performance of Type-1c FLL and Type-2c PLL compared to Type-2 FLL and Type-3 PLL, respectively. The experimental results demonstrated the effectiveness of the proposed out-loop compensation scheme for eliminating the phase-angle error for both Type-1c FLL and Type-2c PLL with a considerable enhancement of the dynamic response compared with Type-2 FLL and Type-3 PLL, respectively. The experimental results demonstrated the effectiveness

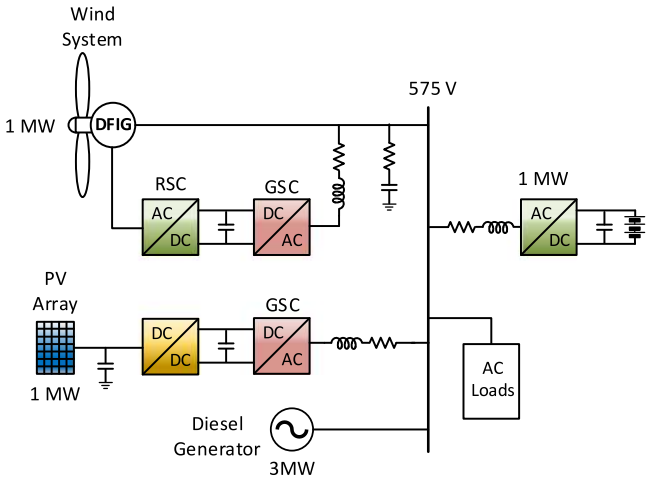

Fig. 32. Islanded microgrid configuration.

of the proposed out-loop compensation scheme for eliminating the phase-angle error for both Type-1c FLL and Type-2c PLL with a considerable enhancement of the dynamic response compared with Type-2 FLL and Type-3 PLL, respectively.

C. Impact of Synchronization Schemes on Islanded Microgrid Operation

In this section, the performance of Type-1c FLL, Type-2 FLL and Type-3 PLL is evaluated for the islanded microgrid shown in Fig. 32. The synchronization schemes are alternatively employed in the microgrid's components (BESS, PV and DFIG-WT) while carrying out comparative analysis for the following two tests: 1) Operation with changes of RES power generation and 2) Islanded Microgrid operation with a sudden voltage phase jump. For a fair comparison, all deployed schemes are equipped with DSC filter, which is designed to eliminate the 5^{th} and 7^{th} harmonics.

1) Operation With Changes of RES Power Generation: In this test, the performance of the islanded microgrid is evaluated under normal operation with solar irradiance, wind speeds, and loads variations. In normal operation, the energy sources were supplying 3.5 MW load such that the PV, DFIG WT, BESS and DZ are supplying 1 MW (1 pu), 0.9 MW (0.9 pu), 0.01 MW (0.01 pu) and 1.5 MW (0.5 pu), respectively as shown in Fig. 33. The over and under-frequency cases are simulated by suddenly decreasing the load by 28.6% of its rated value (3.5 MW to 2.5 MW) at 10 s, 800 w/m^2 irradiance change at t = 20 s and 3 m/s wind speed change at t = 30 s.

It can be observed from Fig. 33 that all the synchronization schemes have almost the same performance, and the islanded microgrid is capable of withstanding the variations of the load, solar irradiance, and wind speed without violating the IEEE Standards 1547-2018.

2) Performance of the Islanded Microgrid in Response to Voltage Phase Jump: The performance of the synchronization schemes is evaluated in response to a phase angle jump of 20° taking place in the microgrid voltage as shown in Fig. 34.

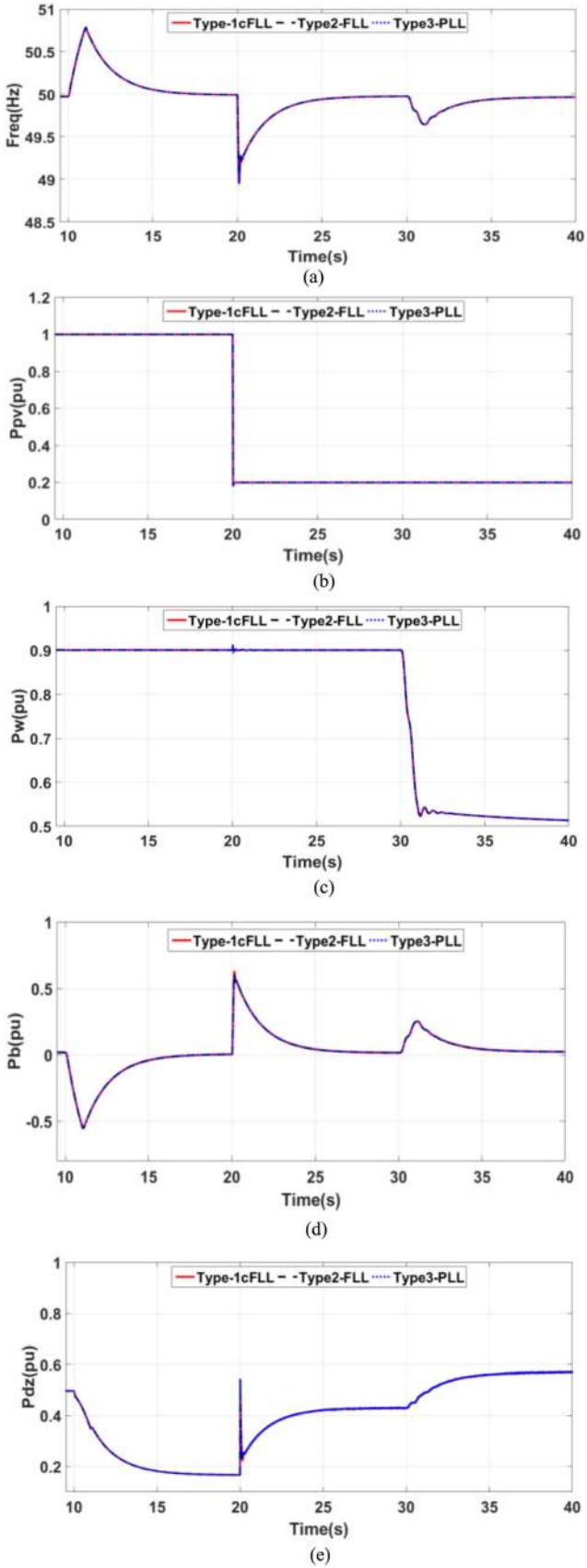

Fig. 33. Islanded Microgrid operation with variation of RES power generation: (a) Frequency. (b) PV active power. (c) DFIG WT active power. (d) BESS active power. (e) Diesel generator active power.

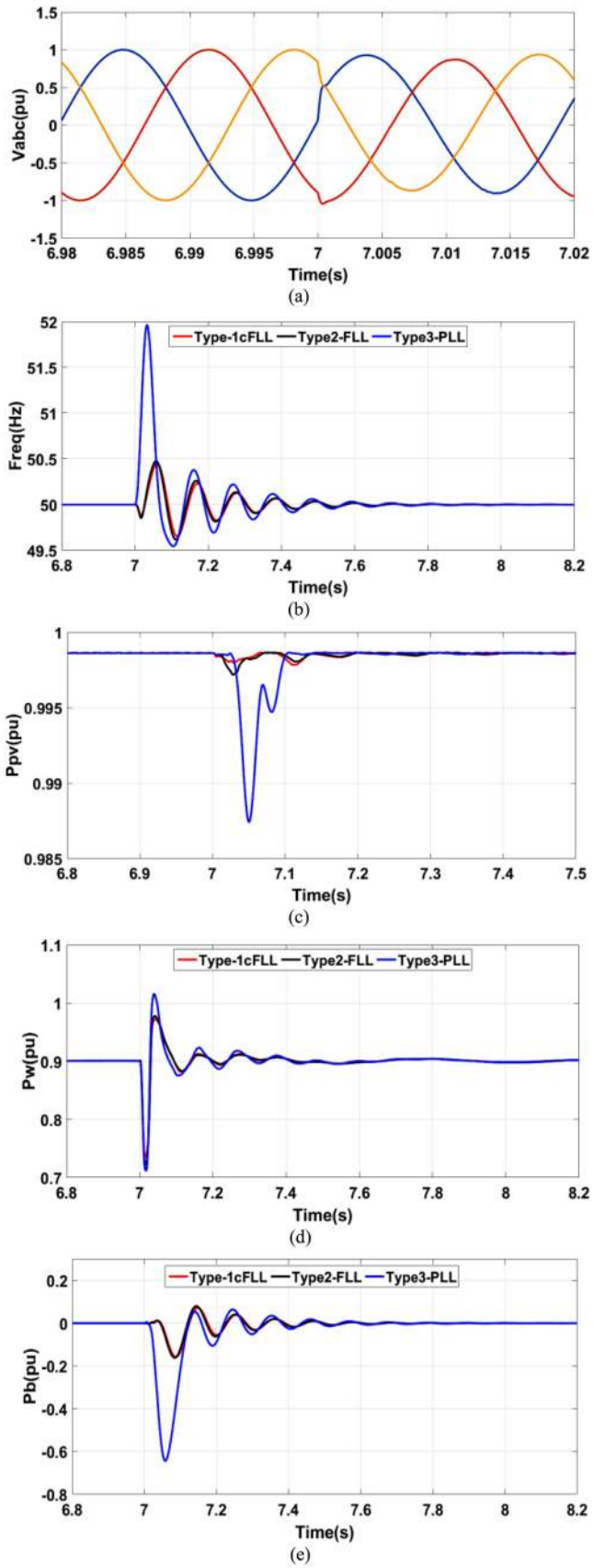

Fig. 34. Study of the phase jump condition on Microgrid operation: (a) Vabc, (b) Frequency (c) PV active power, (d) DFIG WT active power and (e) BESS active power.

The proposed Type-1cFLL and Type 2-FLL show the minimum frequency deviation of 0.45 Hz at the instance of the phase jump. However, Type3-PLL shows the worst response with a deviation of 1.95 Hz resulting in making the battery storage charging 620 KW (0.62 pu) at the instant of the phase jump compared with only 150 KW (0.15 pu) with Type-1c FLL. The DFIG-WT and PV are also affected by such a deviation, and Type-1cFLL is able to ensure the same feature of Type2-FLL with a lower order control system and with enhanced transient response compared to Type3-PLL.

VIII. Conclusion

In this paper, an out-loop phase angle compensation scheme for Type-1 FLL was developed and verified. Different pre-filter schemes were tested for the proposed FLL. Distortion elimination capability of the proposed FLL was improved by introducing an adaptive delayed signal cancelation filter. The proposed selective pre-filter stage based on single DSC or Double DSC (DDSC) was presented to obtain the best performance in response to severe grid disturbances. The effectiveness of the proposed FLL was evaluated based on intensive experimental results. A performance comparison between the proposed scheme and the other mature schemes was also conducted. Results indicated that using the DSC as a pre-filter for Type-1c FLL is the optimum choice in terms of the dynamic response and distortion elimination capability under nominal frequency. For further improvement of Type-1c performance, the double DSC pre-filter is implemented, which significantly improves its distortion elimination capability. The experimental results demonstrated that the proposed Type-1c FLL with the selective pre-filtering stage achieved the best performance in terms of dynamic response and distortion elimination capability with a zero phase angle error during the frequency drift. In conclusion, the proposed Type-1c FLL is able to obtain the features of the higher-order FLLs without increasing its model order.

Appendix

The parameters for Type2-c PLL with DSC4 as a pre-filter are calculated using symmetrical optimum criteria (SO). The symmetrical optimum method ensure the maximum phase margin (PM) for the PLL. In this case, the controller gains are calculated using the following relation, $k_p = \frac{1}{bT_d}$, $k_i = \frac{1}{b^3 T_d^2}$, where T_d is the delay introduced by the DSC4 filter, "b" is a constant value equals to $1+\sqrt{2}$. For DSC4 pre-filter, it introduces a 5 ms delay, this delay is presented simply by a first-order delay function $\frac{1}{1+T_d S}$ and $T_d = \frac{T_{DSC}}{2} = 2.5$ ms

Hence,

$$k_p = \frac{1}{(2.4142) \times \left(2.5 \times 10^{-3}\right)} = 165.6864 \approx 166$$

$$ki = \frac{1}{b^3 T_d^2} = \frac{1}{(2.4142)^2 \times \left(2.5 \times 10^{-3}\right)^3}$$

$$= 11370.85 \approx 11371$$

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