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Research Article

Advances in Evaporated Solid-Phase-Crystallized Poly-Si Thin-Film Solar Cells on Glass (EVA)

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Polycrystalline silicon thin-film solar cells on glass obtained by solid-phase crystallization (SPC) of PECVD-deposited a-Si precursor diodes are capable of producing large-area devices with respectable photovoltaic efficiency. This has not yet been shown for equivalent devices made from evaporated Si precursor diodes ("EVA" solar cells). We demonstrate that there are two main problems for the metallization of EVA solar cells: (i) shunting of the p-n junction when the air-side metal contact is deposited; (ii) formation of the glass-side contact with low contact resistance and without shunting. We present a working metallization scheme and first current-voltage and quantum efficiency results of 2 cm^2 EVA solar cells. The best planar EVA solar cells produced so far achieved fill factors up to 64%, series resistance values in the range of 4-5 Ωcm^2, short-circuit current densities of up to 15.6 mA/cm^2, and efficiencies of up to 4.25%. Using numerical device simulation, a diffusion length of about 4 μm is demonstrated for such devices. These promising results confirm that the device fabrication scheme presented in this paper is well suited for the metallization of EVA solar cells and that the electronic properties of evaporated SPC poly-Si materials are sufficient for PV applications.

1. Introduction

Thin-film silicon photovoltaics has seen increasing interest in its development for the solar cell market over the last decade, based on its immense potential to produce electricity at significantly lower cost per watt compared to bulk Si technologies. This is the case since the combination of large-area deposition onto foreign substrates, more streamlined processing, and monolithic cell interconnection can lead to substantially lower fabrication cost, while at the same time only a fraction of the expensive Si raw material is needed [1–3]. One of the most promising candidates for large-scale production of thin-film solar cells is polycrystalline silicon (poly-Si) on glass since it makes use of an abundant raw material and since it benefits from decades of expertise that has been gained with crystalline Si in the semiconductor industry. Previously, solid-phase crystallized (SPC) poly-Si solar cells have proven to be capable of achieving efficiencies of over 9% on metal substrates [4] and more recently over 10% efficiency has been demonstrated on borosilicate glass superstrates [5, 6].

In order to make poly-Si on glass economically competitive in the rapidly growing PV market, it is desirable or even necessary to further improve its efficiencies and to reduce the associated module production cost [7]. One way of achieving the latter could be the replacement of the currently predominantly used plasma-enhanced chemical vapour deposition (PECVD) method for production of the a-Si precursor diodes with e-beam evaporation which can be deposited in an in-line process and is therefore potentially both faster and cheaper [8, 9]. However, it has yet to be shown that evaporated SPC poly-Si can lead to diodes with similar material quality (i.e., that similar solar cell efficiencies can potentially be achieved with this deposition method). We have recently shown that e-beam evaporated SPC poly-Si on glass solar cells (EVA) have promising diode properties as confirmed by Suns-V_{oc} measurements but we have not been able to efficiently metallise this type of solar cell due to

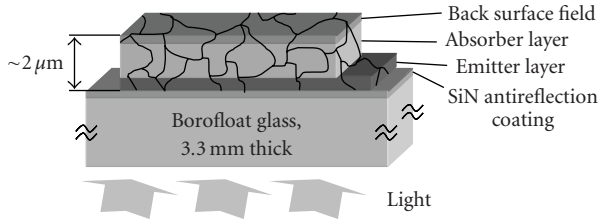


Figure 1: Schematic of an EVA solar cell in superstrate configuration (i.e., with air-side BSF and glass-side emitter). Note that the layer thicknesses are not to scale.

severe shunting problems when either the emitter or the BSF contact is deposited. In this paper, we introduce an approach that enables the successful metallization of EVA solar cells and that demonstrates that these devices are promising candidates for the cost-effective production of PV electricity.

2. Background: EVA Device Structure

The devices investigated in this work are thin-film solar cells obtained from solid phase crystallization (SPC) of evaporated a-Si precursor diodes. The a-Si diodes are deposited via e-beam evaporation under non-ultrahigh vacuum conditions (base pressure $\sim 2\times10^{-8}$ Torr, deposition pressure $\sim$1-2$\times10^{-7}$ Torr) onto planar 5$\times$5-cm^2 SiN-coated borosilicate glass superstrates from Schott AG (Borofloat33, 3.3 mm thick). The SiN layer serves as both antireflection coating and barrier layer for contaminants from the glass and is deposited by PECVD. The dopants (boron and phosphorus) are added in situ during the a-Si deposition process, using high-temperature effusion cells from MBE Komponenten, Germany. Usually the cell structure is intended for the superstrate configuration (i.e., the sunlight enters the solar cells through the glass). In this case, the emitter is located directly on top of the SiN antireflection coating. For reasons of clarity, we restrict ourselves in this work to this configuration and term the highly doped air-side layer the back surface field (BSF) and the highly doped glass-side layer the emitter, respectively. However, it has to be kept in mind that the inverse structure, that is substrate configuration, where the emitter is located on the air-facing side of the device, is also possible. After solid phase crystallization ($\geq$24 hours at 600°C), the poly-Si diodes receive a rapid thermal anneal (RTA) at a temperature of ~900°C for ~4 minutes. This high-temperature treatment activates dopants and anneals point defects in the poly-Si films. The diode fabrication process is terminated with a hydrogen plasma treatment at plateau temperatures in the range 600–650°C for 15–20 minutes, using a low-pressure chemical vapour deposition (LPCVD) system with an inductively coupled remote plasma source (Advanced Energy, USA). Both post-deposition treatments (RTA and hydrogenation) are essential processes for achieving appreciable performance of SPC poly-Si solar cells on glass [10, 11]. The total thickness of the poly-Si films is about 2 μm. The structure of the finished poly-Si diodes is schematically displayed in Figure 1. Typical design parameters of the cells are summarized in Table 1 [8].

Table 1: Typical design parameters of EVA solar cells in superstrate configuration (i.e., with glass-side emitter and air-side BSF).

Parameter	Details
Glass	3.3 mm, borosilicate, planar or textured
AR coating	~70 nm PECVD deposited SiN, $n \approx 2.1$
Emitter	~100 nm, p^+ or n^+, ~200–400 Ω/sq
Base	~1.8 μm, n^- or p^-, $\sim 5\times10^{16}$ cm^{-3}
SPC	$\geq$24 h at 600°C
BSF	~100 nm, n^+ or p^+, ~500–1000 Ω/sq
RTA	4 min at ~900°C
Hydrogenation	15–20 min at ~600–650°C, remote plasma

Prior to this work, EVA solar cells had to be processed into mesa-type structures in order to measure *I-V* characteristics. In this configuration, a transparent conducting oxide (TCO) layer was used as glass-side electrode and the samples were illuminated from the air side (substrate configuration). Energy conversion efficiencies of up to 1.35% on such small-area cells (0.126 cm^2) were demonstrated elsewhere [9, 12].

3. Results

3.1. Air-Side Metallization

We have recently developed a metallization scheme for PECVD-deposited poly-Si thin-film solar cells (PLASMA) of identical structure, whereby an evaporated blanket Al layer is successfully used to contact the highly doped air-side layer of these diodes [13]. In sharp contrast, EVA solar cells get severely shunted when a blanket air-side metal electrode (Al) is deposited [14]. After blanket Al deposition onto the BSF layer of EVA cells, we consistently observe an unacceptable reduction of the solar cell performance when investigated via Suns-V_{oc} measurements [15]. Suns-V_{oc} is used to evaluate our metallization schemes since it has the great advantage that it can be used on partially metallized solar cells or even on the bare poly-Si diodes, provided both highly doped layers are accessible to the measurement probes. The performance drop of EVA cells due to the evaporated Al layer is characterized by a severe reduction in the open-circuit voltage V_{oc}, the pseudofill factor *pFF*, and the shunt resistance R_{sh} (see Table 2, whereby Suns-V_{oc} was measured before and after thermal evaporation of a 640 nm thick blanket Al layer). To determine the shunt resistance in units of Ωcm^2, a two-diode model fit was performed and a light-generated current density of 10 mA/cm^2 was assumed [16].

Another useful parameter for the determination of the diode quality is the effective ideality factor n_{eff} that is calculated from the slope of the Suns-V_{oc} curve between the maximum power point *MPP* and the open-circuit voltage V_{oc} using

$$n_{\text{eff}} = \frac{V_{\text{oc}}(MPP) - V_{\text{oc}}(1\ Sun)}{V_T \times \ln(Suns(MPP))}, \quad (1)$$

where $V_{oc}(MPP)$ and $V_{oc}(1\ Sun)$ are the open-circuit voltages at *MPP* and 1 *Sun* illumination, respectively, V_T

Table 2: Suns-V_{oc} results of an EVA sample measured before and after blanket deposition of Al onto the BSF layer. Note that the determination of R_{sh} stems from a two-diode model fit to the measured data and assumes a light-generated current density of 10 mA/cm^2.

	V_{oc} (mV)	R_{sh} (Ωcm^2)	*pFF* (%)	n_{eff}
Before blanket Al deposition	429	1003	66.4	1.93
After blanket Al deposition	373	174	50.4	3.41

Table 3: Suns-V_{oc} results of an EVA sample measured before and after metallization of the BSF layer using line contacts in combination with an etching step that effectively reduces the shunting between emitter and BSF.

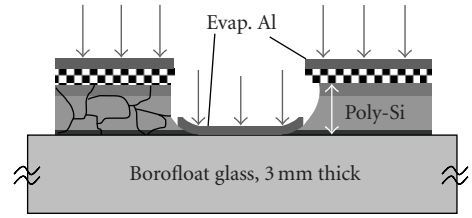
	V_{oc} (mV)	R_{sh} (Ωcm^2)	*pFF* (%)	n_{eff}
Before metalisation	459	Infinity	73.6	1.40
After metalisation	455	Infinity	75.7	1.24

is the thermal voltage ($kT/q \approx 25.8$ mV at 300 K) and *Suns*(*MPP*) the illumination intensity (in *Suns*) at the *MPP* of the pseudo *I-V* curve. Note that n_{eff} is directly obtained from the measured data and does not rely on a fitting procedure. Table 2 shows that n_{eff} is much higher when Al is present on the BSF layer, which is another indication that the *I-V* relationship at the p-n junction is severely distorted.

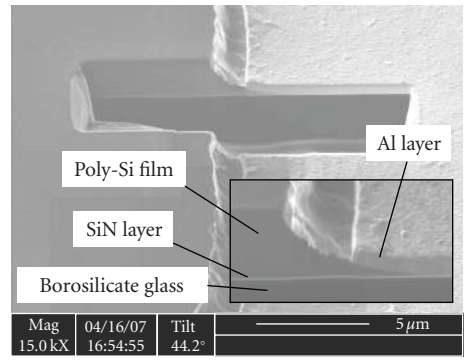
Our investigations of this shunting effect revealed that shunting through submicron-sized pinholes is responsible for this severe performance drop. Two ways of overcoming this problem were found: (i) to contact only a small fraction of the rear Si surface via a point contacting scheme, whereby the metal layer needs to be thin (<1 μm) and the fractional area coverage small (<5%), and (ii) to deposit line contacts in a bifacial interdigitated scheme, whereby a thick layer of metal is deposited followed by a wet-chemical etching step that effectively reduces shunting by preferentially etching away the shunting paths [17].

For obtaining reasonable efficiencies with poly-Si thin-film solar cells, it is vital to have effective light trapping in place [18–20]. For this reason, we decided to pursue the second approach using line contacts as air-side electrode since this offers more flexibility for the incorporation of a suitable back surface reflector (BSR). A BSR can lead to drastic current gains in poly-Si thin-film solar cells [19, 21] and can, in principle, be of specular [19] or diffuse [22] nature, whereby diffuse reflectors seem to be particularly effective for cells that are deposited on planar substrates [21].

In Table 3, we see Suns-V_{oc} results of the line contacted rear-surface metallization developed in our group. Evidentially the open-circuit voltage is nearly unaffected whereas the *pFF* and n_{eff} even improve slightly. We attribute this surprising result to a Schottky barrier that is introduced between the Al line contacts and the poly-Si layer and that causes a small Schottky voltage at light intensities around (and higher than) 1 *Sun*, as also reported elsewhere [23].



(a)



(b)

Figure 2: (a) Schematic of the self-aligned scheme for emitter groove metallization after blanket Al evaporation (the SiN layer is not displayed); (b) FIB image of an emitter groove after completed self-aligned emitter groove metallization. The inset on the bottom right is a close-up of the contact region between the evaporated Al layer and the poly-Si film.

3.2. Self-Aligned Method for Glass-Side Metallization

Since all three Si layers of EVA solar cells are deposited in a single evaporation process, the thin emitter layer is buried beneath the base and BSF layers. One of the challenges when metallizing thin-film solar cells is therefore to find a suitable way of accessing the buried layer and to contact this layer with a metal electrode, obtaining low contact resistance ρ_{cont} and without the introduction of a significant shunt resistance effect. In a first approach, we intended to adopt a metallization scheme that works well on PECVD-deposited poly-Si thin-film solar cells. The method is based on opening up a resist layer via photolithography and to subsequently etch down to the buried emitter layer using an SF_6 plasma etching process. Then Al is evaporated onto the device and the photoresist (with Al on top) is removed using a lift-off procedure [24]. Figure 2(a) displays a schematic of the device just prior to the lift-off process. It can be seen that the slope on the sidewall of the emitter groove resulting from the isotropic plasma etching process enables contacting of the emitter without introduction of a shunting path to the BSF layer. Figure 2(b) shows a cross-sectional focused ion beam (FIB) image taken on an EVA solar cell just after the lift-off procedure. The Si film is ~2.2 μm thick, the Al layer is about

Table 4: Suns-V_{oc} results of the self-aligned emitter contacting scheme for two different cells on the same $4.5 \times 4.5\,cm^2$ sample. The values in the temperature column refer to the measured parameters before metallization ("virgin"), the freshly fabricated emitter contacts ("no bake"), and to measurements performed after successive furnace anneals (20 minutes each) in air at the corresponding temperature.

Cell	Temp (°C)	V_{oc} (mV)	R_{sh} (Ωcm^2)	*pFF* (%)	n_{eff}
virgin	no bake	425	7261	68.0	1.77
a	no bake	415	2242	68.5	1.69
b	no bake	411	16224	68.6	1.68
a	150	397	1880	68.1	1.64
b	150	401	6375	69.2	1.57
a	200	373	3001	62.2	2.07
b	200	393	n/a	65.6	1.86
a	250	214	n/a	47.9	2.19
b	250	297	n/a	50.0	2.76

550 nm thick, and the emitter layer has a thickness in the range 100–200 nm. Two things can be noted: (i) the slope of the plasma etched groove is very well suited to allow contact between the highly doped emitter layer and the evaporated aluminium and (ii) while there is *no* contact to the BSF anywhere in this image, it becomes clear that it is essentially impossible to contact *only* the emitter layer without getting an interface between the edge of the Al layer and the lightly doped base of the cell.

The electrical performance of this self-aligned emitter contacting scheme was, again, evaluated via Suns-V_{oc} measurements. Table 4 shows the Suns-V_{oc} characteristics of two solar cells fabricated according to this scheme (each with dimensions of $1.6 \times 1.25\,cm^2$) on a $4.5 \times 4.5\,cm^2$ poly-Si on glass sample, after different metallization processing steps. The row termed "virgin" corresponds to Suns-V_{oc} of the sample before emitter groove formation, with the measurement done between the BSF and a small region of emitter layer exposed by a silicon etch (CP4). Subsequent rows of Table 4 correspond to the metallized sample after baking at different temperatures. As can be seen, after metallization and before bake, the Suns-V_{oc} measurements indicate only a slight drop in V_{oc} and the cells appear to be intact (i.e., the *pFF* values R_{sh} and n_{eff} are not significantly altered by the metallization procedure). However, successive bakes in ambient air (annealing time of 20 minutes) and at increasingly higher temperatures degrade the cell performance drastically, as evidenced by a reduction of V_{oc} and *pFF* and an increase of n_{eff} (for $T > 150°C$). The hottest bake (at 250°C) is clearly the most detrimental to the cell performance. This can be seen by a cumulative voltage drop of more than 100 mV for both cells and significantly degraded *pFF* and n_{eff} values. In those cases where a two-diode model fit could not be performed (due to the distorted *I-V* relationship of the solar cells), we recorded "n/a" in Table 4. Such a distorted Suns-V_{oc} curve is an indication that we have lateral current flow in the cells to regions of increased recombination ("shunting"). In addition to these Suns-V_{oc} results, we also measured the short-circuit current density J_{sc} of the cells as a function of the flash lamp intensity (using a modified Suns-V_{oc} setup to obtain the so-called "J_{sc}-Suns" measurements [16]) to gain insight into the lumped series resistance of the test structures. This was possible because all cells received BSF line contacts prior to emitter contact formation. In contrast to the Suns-V_{oc} results, the bakes *did not degrade* the J_{sc}-Suns curves at all and good R_s values of around $3.5\,\Omega cm^2$ were determined via curve fitting to a two-diode model, indicating that the contact resistance is not the limiting factor for this metallization scheme.

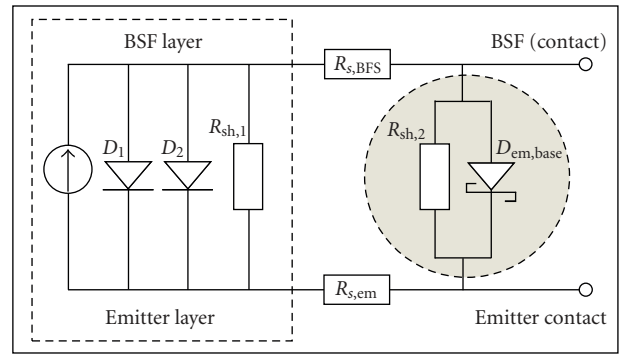


Figure 3: Simplified equivalent circuit diagram of an EVA cell with Schottky barrier between emitter and the base of the solar cell.

We explain the obtained Suns-V_{oc} and J_{sc}-Suns results as a consequence of a Schottky barrier that is formed between the lightly doped base (intended base doping $\sim 5 \times 10^{16}\,cm^{-3}$ for the measured cells) and the edge of the Al layer, in agreement with [25]. This situation is illustrated in the simplified equivalent circuit diagram in Figure 3. In this diagram, the virgin diode is displayed in the dashed rectangle to the left (two-diode representation) and the Al-Si interface is highlighted in the dashed circle to the right. The light-generated current inevitably has to flow laterally through the two highly doped layers (p^+, n^+) in order to reach the edge of the emitter groove. This is represented by the resistors $R_{s,BSF}$ and $R_{s,em}$ corresponding to the BSF and the emitter component, respectively. The metal-semiconductor interface is generally modeled by a resistive (shunting) component $R_{sh,2}$ and a Schottky diode $D_{em,base}$. The latter is similar in its *I-V* characteristics to an ideal diode with an ideality factor slightly above unity (usually in the range 1.02–1.15)

Figure 4: (a) Dark lock-in thermography (DLIT) image of one test structure with self-aligned emitter groove metallization after the baking procedure. The image was taken at a lock-in frequency of 20 Hz, using a forward bias voltage of 250 mV. (b) is the same as (a), but for a reverse bias voltage of 250 mV. (c) Topography image of the same sample region for comparison.

but with much larger reverse saturation current densities leading to "turn-on voltages" of about 200 mV lower as compared to corresponding p-n junctions [26]. The drop in open-circuit voltage as demonstrated in Table 4 is in good agreement with this model. Since the devices are "clamped" to nearly zero voltage at the metal contacts during J_{sc}-Suns measurements, the short-circuit performance of the test structures is unaffected by this Schottky barrier. Trying to retain the performance of the devices via omitting of the contact annealing step is futile since contact aging has the same influence of a barrier increase for the (p-type) Si-Al system as an anneal and thus the devices would therefore degrade over time even without these temperature treatments [25].

To gain further insight into the observed shunting, we employed lock-in thermography (LIT), a highly sensitive technique that allows imaging of tiny temperature differences ($<100\,\mu$K) as they occur at shunting sites in solar cells with resolutions down to $5\,\mu$m [27]. During dark lock-in thermography (DLIT) measurements, a pulsed voltage is applied to the sample and the resulting spatial heating pattern is imaged using an infrared (IR) focal plane array camera in lock-in mode [28]. DLIT images of the test structure "b" from Table 4 are displayed in Figures 4(a), and 4(b). The images were taken at a lock-in frequency of 20 Hz and at two different biasing conditions (at 250 mV forward bias (a) and at 250 mV reverse bias (b)) since this can prove useful for better understanding the nature of the shunts. For comparison, a topography image of the same region is shown in Figure 4(c). In forward bias, a current of 8 mA was measured and it can be seen that essentially only the emitter grooves are shunted (they appear bright in these images). Note that the shunting is distributed along the emitter contact fingers and not distributed over the whole cell area or of point-like nature as is the case for the BSF fingers after contact formation. In contrast, a current of only 1mA was measured in reverse bias and the whole cell area is dark, indicating that no significant linear shunts are present in this cell ($R_{sh,2} \geq 500\,\Omega\text{cm}^2$) and that the shunting paths associated with the emitter grooves have a distinctly nonlinear (diode like) behavior. This finding is in good agreement with the observation of a metal-semiconductor interface formed between the emitter contact metal and the base.

In addition to the method outlined above, we investigated an alternative self-aligned process using photoresist that is exposed through the glass in predefined emitter grooves (SAMPL [29]). These tests showed that we either get severe shunting of the solar cells as a result of the emitter metallization or that the series resistance values are too high for an efficient metallization of EVA solar cells.

In summary, from the results presented in this section we conclude that both self-aligned emitter groove metallization processes are, in their current forms, not suitable for EVA solar cells. We, therefore, investigated an alternative method, as described in the following section.

3.3. Aligned Bifacial Metallization Scheme

Learning from the problems encountered with the self-aligned emitter metallization experiments described above, we investigated a different approach that eliminates the possibility of shunting between the emitter electrode and the base layer entirely. Instead of plasma etching through the entire silicon thickness, we used a time etch stop such that a thinned emitter layer remains at the bottom of the groove. Then, using an *aligned* photolithography step, the glass-side comb-like electrode is centered in the groove, leaving significant space ($>10\,\mu$m) between the edge of the electrode and the groove sidewall as shown in Figure 5. The result is a bifacial solar cell with two interpenetrating comb-like electrodes. The processing steps to realize this structure are as follows:

(i) first photolithography step that defines the emitter grooves and the cell edges;

(ii) plasma etching (SF_6 plasma, ~65 W RF power, ~40 Pa) with time etch stop to expose the highly doped emitter layer;

(iii) removal of the photoresist;

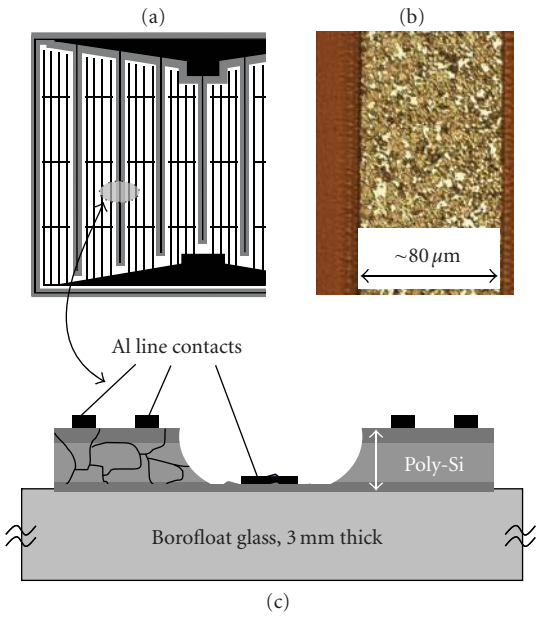


Figure 5: (a) Schematic (top view) of a fully metallized EVA solar cell where the grey areas correspond to plasma-etched regions within which the emitter electrode (black) is located. (b) Transmission microscopic image of an emitter groove after plasma etching. (c) Cross-sectional schematic of the region indicated in (a).

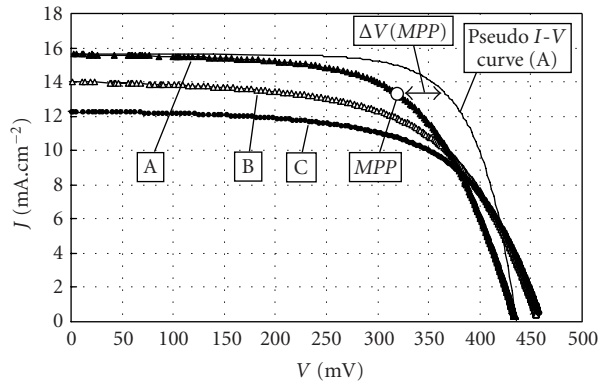


Figure 6: Illuminated *J-V* curves (1 sun) of three different EVA solar cells (open and filled symbols) that were metallized with the aligned bifacial metallization scheme. The cells feature a layer of white paint as back surface reflector. For cell A, the pseudo *J-V* curve (solid line) obtained from Suns-V_{oc} measurements is added for comparison and the method used to determine R_s is indicated.

(iv) piranha clean (96% H_2SO_4: 30% H_2O_2, ratio 1:1; 5 minutes), 5% HF dip, and evaporation of a blanket Al layer (1-2 microns);

(v) second photolithography step to define both comb-like electrodes (BSF, emitter), where the emitter fingers are aligned to the centers of the grooves;

(vi) Al etch back process using diluted phosphoric acid (85% H_3PO_4: H_2O, ratio 1:1; ~65°C for several minutes) to remove exposed Al;

(vii) removal of the photoresist;

(viii) short etching step in diluted phosphoric acid to remove the shunting that is caused by the BSF line contacts.

Figure 5(a) displays a top-view schematic of a metallized EVA cell with interdigitated metal electrodes. The grey areas are the plasma-etched regions within which the comb-like emitter electrode (black) is located. The remaining black areas are the BSF electrode (fingers and busbar), whereby the number of BSF fingers per emitter finger is 4 owing to the higher sheet resistance of the BSF layer compared to the emitter layer and the fact that emitter grooves inevitably lead to a reduction of the active cell area via the groove etching. It is noted that the schematic is not to scale and that in real devices the relative contact areas and groove widths are significantly smaller. A microscopic image of a plasma-etched emitter groove is displayed in Figure 5(b). Due to the grain orientation-dependent etching rate of poly-Si, the plasma-etched Si film exhibits voids in which the Si film has been completely removed and the glass surface becomes exposed. The example shown represents a good tradeoff between obtaining a good series resistance (stemming from the contact resistance between the emitter and its electrode and the lateral resistance of the exposed poly-Si emitter layer) and a good shunt resistance. The latter arises if the etching depth is not large enough and if hence significant parts of base material are still remaining on top of the emitter layer forming conductive lateral paths to the base and BSF region. In contrast, etching too much of the emitter away causes an excessive density of voids and hence a large series resistance. While such cells perform reasonably well at very low light intensities due to their high shunt resistance (allowing, e.g., accurate EQE measurements), they perform poorly at 1 Sun due to the low *FF*. A cross-sectional schematic of the section indicated in Figure 5(a) is displayed in Figure 5(c). Clearly, if the silicon film has been etched to the right depth and the alignment is done properly, there is no shunting between the emitter electrode and the base layer. Currently our alignment accuracy is about +/− 15 microns, limited by the nonflat glass surface that causes nonoptimal photolithography results. It needs to be mentioned that this metallization scheme, despite working well in the lab, is not suited for industry due to the critical alignment step. However, the method is very beneficial in the laboratory as it allows us for the first time to characterize the full performance of EVA solar cells (i.e., their performance with respect to voltage *and* current).

3.4. Current-Voltage and Quantum Efficiency Results

Figure 6 shows the illuminated *I-V* curves (1 sun) of three metallized EVA solar cells (A–C) that were produced with the aligned bifacial metallization scheme. Each cell has an area of 2 cm^2 and features a white paint back surface reflector coating. The cells were measured using a halogen lamp-based system. For each cell, the light intensity was adjusted

such that the measured short-circuit current density agreed with that calculated from the measured external quantum efficiency (EQE). This procedure is necessary because the spectrum of the halogen lamp deviates significantly from the standard AM1.5G spectrum. The lumped series resistance $R_s(MPP)$ was determined by comparison of the illuminated I-V curve with the pseudo I-V curve obtained from Suns-V_{oc} measurements [15]:

$$R_s(MPP) = \frac{\Delta V(MPP)}{J(MPP)}, \tag{2}$$

where $\Delta V(MPP)$ denotes the voltage difference between pseudo I-V and illuminated I-V curve at the maximum power point MPP of the latter and $J(MPP)$ denotes the short-circuit current density at MPP, respectively. The method is indicated in Figure 6 and the 1-sun I-V parameters of the measured cells (A–C) are listed in Table 5. The shunt resistance is >2000 Ωcm^2 for all three cells and hence is not listed since it has negligible effect on their 1-sun performance. It can be noted that we are currently limited by two main factors: (i) the relatively high series resistance (usually 4-5 Ωcm^2 for the best cells) adversely affecting the FF (loss ~10% as compared to pFF), and (ii) the relatively low short-circuit current densities. The latter is related to the short diffusion length in some of the cells (as outlined below) but, more importantly, results from the fact that all of these cells were deposited on *planar* glass superstrates, giving poor light trapping. Significant current (and hence efficiency) gains are expected from a transfer of the EVA technology to textured glass sheets [13]. Figure 7 illustrates the improvement of the EQE of cells A and B due to the deposition of a layer of white paint as back surface reflector. The highest EQE values achieved so far are ~70% with the paint reflector being present and ~65% on nonpainted samples. The strongest influence of the rear reflector is seen in the red and infrared regions, but it can also be noted that the cell with longer diffusion length and enhanced red response (cell A) additionally obtains a shift of the peak EQE wavelength and amplitude, which is not seen for cell C featuring a rather poor diffusion length (as will be discussed below). One of the shortcomings of a pigmented dielectric BSR, such as the one used in this work, is the fact that the low refractive index of such reflectors (n~1.5) leads to scattering of the light into rather shallow angles once crossing the BSR/poly-Si interface (the maximum scattering angle is about 24%). The resulting paths through the poly-Si layer are only marginally larger than the cell thickness and a large fraction of the light will be coupled out once reaching the glass-side of the solar cell since total internal reflection does not occur for light of such small angles. The development of a suitable texture for the air-side of EVA cells will therefore lead to much larger current gains due to a strongly increased pathlength enhancement through multiple bounces of long wavelength light in EVA cells.

Mapping of the voltages across short-circuited EVA cells revealed that the resistance of our contact fingers is the main contributor to the high R_s values of the cells. Efforts are presently underway to minimize this problem. One approach is to use wider metal fingers (this also reduces contact resistance effects) or to simply deposit thicker metal layers. An additional metal plating step to thicken the electrodes after the standard metallization is completed could also achieve this goal.

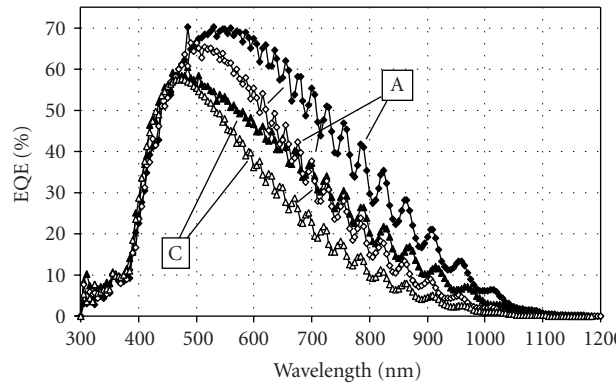


Figure 7: EQE curves of cell A (triangles) and cell C (diamonds) before (open symbols) and after (filled symbols) application of white paint as back surface reflector.

3.5. Computer Modeling Using PC1D

Computer modeling of the above cells was employed in order to gain further insight into the electronic properties of these metallized EVA solar cells. The simulations were performed with the 1-dimensional electronic device simulator PC1D [30]. Relevant device parameters were obtained by fitting of the measured EQE and hemispherical reflectance (R) data with PC1D, whereby the internal quantum efficiency (IQE) was determined via IQE = EQE/(1 − R). All investigated cells could be fitted with good accuracy. Figure 8 shows an example of the measured and modeled QE and reflectance curves of cell B before (Figure 8(a)) and after (Figure 8(b)) deposition of a white paint back reflector. Excellent agreement between the measured and fitted electrical as well as optical data has been obtained in case (a) but it is somewhat difficult to get good agreement between the measured and the fitted data in the long wavelength range (>800 nm, corresponding to ≥10 μm absorption length in Si) for the painted cells. We believe that this phenomenon ("missing reflectance") is caused by light that is obliquely reflected by the diffuse reflector and enters the glass at large angles such that it is totally internally reflected and leaves the sample at locations other than where it can enter the integrating sphere and is collected during the measurement. Such artefacts result from the fact that the light beam used during the measurement is small in its dimensions as compared to the lateral travel distance of the long-wavelength light in the glass. Reduced long-wavelength reflectance of the commercial paint which was used could be an additional contributor to the disagreement between measured and modeled reflectance curves.

The emitter properties influence the QE curves mainly in the wavelength range 300–500 nm, whereby the slope of the

Table 5: Measured light *J-V* results (1 sun) of the three EVA solar cells of Figure 6. The shunt resistance of each cell has a negligible effect on the *J-V* curve. The *pFF* was determined from Suns-V_{oc} measurements.

Cell	V_{oc} (mV)	J_{sc} (mA/cm^2)	*pFF* (%)	*FF* (%)	Efficiency (%)	R_s ($\Omega\cdot$cm^2)
A	436	15.62	72.7	62.5	4.25	3.63
B	458	14.01	72.9	59.6	3.82	5.52
C	462	12.26	71.1	61.8	3.50	4.88

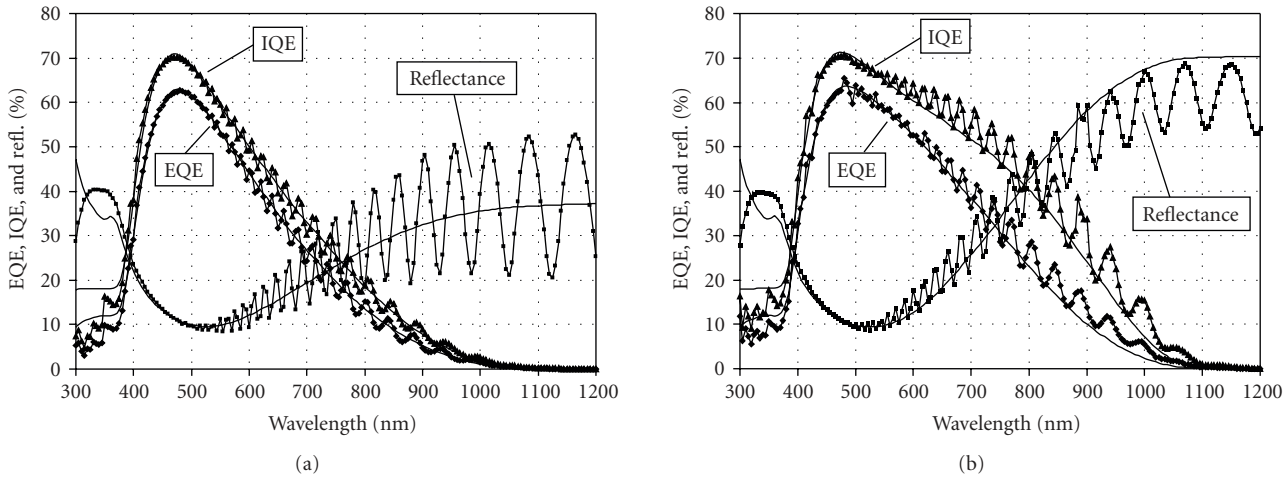


Figure 8: Comparison between measured (filled symbols, thin lines) and PC1D-simulated (thick lines) EQE (diamonds), IQE (triangles), and reflectance (squares) curves of cell B (a) without white paint back surface reflector and (b) with back surface reflector.

QE curve in this section is related to the emitter diffusion length and its location is essentially determined by the emitter thickness. The parameters that were used to obtain the best fits for both cases with and without back reflector are listed in Table 6. From this and Figure 8, it seems evident that the cells have a rather *poor blue response* as a consequence of the thick emitter layer. In all three cases, we find that there is a "dead layer" of at least 120 nm thickness, whereby the best cell (A) is affected most (~180 nm). All cells were deposited with an intended emitter thickness of 100 nm and it therefore has to be concluded that the emitter layers of all cells are too thick. We obtained similar results on equivalent samples that were analyzed via secondary ion mass spectroscopy (SIMS) measurements (here, the measured thickness was twice the intended thickness). The most likely cause for these thick emitter layers is the slow drop-off of the phosphorus background pressure in the deposition chamber after completion of the emitter deposition. Two ways of achieving thinner emitters are conceivable: (i) deposition of cells with opposite polarity since boron is much less volatile in vacuum systems than phosphorus and therefore allows the deposition of thin p^+-type emitters, or (ii) interruption of the deposition after completion of the emitter layer for a sufficiently long time until the partial pressure of phosphorus is low enough to not overcompensate the boron base doping.

The base doping of thin-film solar cells has considerable influence on the electrical performance of the modeled solar cells since it impacts on the depletion region width that accounts for a considerable fraction of the total device in such thin cells. For this reason, we measure the base doping density via impedance analysis [31] prior to PC1D modeling and subsequently use the obtained base doping results in the PC1D model. Generally for our devices, the base (absorber) diffusion length L_n influences the QE curves in the wavelength range above the peak EQE (at around 500 nm) and can be extracted with good accuracy if it is not significantly longer than the base thickness. In the present case, we notice considerable differences in the obtained diffusion lengths ranging from about 1 μm (cell C) to about 4 μm (cell A). Note that in two out of three cases the absorber diffusion length even had to be increased after application of the paint layer in order to get satisfactory fit results. Comparison of the obtained values of L_n with the base doping values obtained from impedance analysis (also listed in Table 6) indicates that the absorber diffusion length is inversely related to the active base doping density and it seems that in order to achieve good diffusion length (longer than the base thickness) it is necessary to achieve a base doping density of below $\sim 1\times10^{16}$ cm^{-3}. The fact that the best of these cells has a diffusion length in the order of 4 microns is very encouraging and proves that SPC poly-Si on glass is a promising candidate for the cost-effective production of thin-film solar cells and may be able to produce similar efficiencies as its PECVD deposited counterparts.

4. Conclusion

In this paper, a metallization scheme for EVA poly-Si solar cells on glass has been introduced and successfully tested.

Table 6: Parameters that were used to model solar cells (A–C) with PC1D before and after deposition of a white paint back reflector. In the latter case, the back surface reflectance was chosen to be diffuse rather than specular as in the nonpainted case.

		Without paint			With paint		
Parameter	Unit	A	B	C	A	B	C
Emitter thickness	(nm)	330	210	230	330	210	230
Emitter doping density	(cm^{-3})	5×10^{19}	5×10^{19}	5×10^{19}	5×10^{19}	5×10^{19}	5×10^{19}
Emitter diffusion length	(nm)	146	90	110	146	90	110
Base thickness	(nm)	1900	2000	2000	1900	2000	2000
Base doping density	(cm^{-3})	5×10^{15}	1.6×10^{16}	3×10^{16}	5×10^{15}	1.6×10^{16}	3×10^{16}
Base diffusion length	(μm)	4	1.55	1.1	5	1.55	1.25
Base minority carrier lifetime	(ns)	5.2	0.9	0.51	8.1	0.9	0.66
BSF thickness	(nm)	100	100	100	100	100	100
BSF doping density	(cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}	1×10^{19}	1×10^{19}	1×10^{19}
BSF diffusion length	(nm)	50	50	50	50	50	50
Ext. reflectance layer 1: thickness; n	(nm)	10^6; 1	10^6; 1	10^6; 1	10^6; 1	10^6; 1	10^6; 1
Ext. reflectance layer 2: thickness, n	(nm)	10^6; 1.48	10^6; 1.48	10^6; 1.48	10^6; 1.48	10^6; 1.48	10^6; 1.48
Ext. reflectance layer 3: thickness, n	(nm)	71; 1.90	68; 1.95	68; 1.93	71; 1.90	68; 1.95	68; 1.93
Int. front surface reflectance	(%)	5	5	5	15	15	15
Int. back surface reflectance	(%)	28 (spec.)	28 (spec.)	30 (spec.)	70 (diff.)	70 (diff.)	70 (diff.)

The new scheme overcomes two problems that have so far plagued our efforts of metallizing this type of device. The first is the formation of the air-side electrode without introduction of shunting paths that are usually present due to submicron-sized pinholes in this silicon material. The second is contacting of the highly doped glass-side layer such that Schottky-type shunting to the lowly doped base layer is avoided. The problem with the air-side electrode has been overcome by metallizing only a small fraction of the rear surface (line contacts) and by a subsequent metal etching step that eliminates the pinhole-related shunting paths. The problem with the glass-side electrode has been solved by an alignment of the emitter electrode fingers to the centers of the emitter grooves. All cells of this work were deposited on planar glass superstrates and featured only minor light trapping via a dielectric back surface reflector. Since efficient light trapping is one of the key requirements for efficient Si thin-film solar cells, we are currently investigating several ways of increased light absorption, namely, back surface texturing, texturing of the glass superstrates, and an increase in cell thickness.

From an analysis of the measured illuminated *I-V* characteristics, it follows that the cell efficiency will also greatly benefit from an improved series resistance which can rather easily be achieved via an increase in metal thickness and/or changes of the metallization pattern.

We are confident that the above measures will lead to substantial efficiency improvements for this solar cell type in the near future.

Through computer modeling, we have demonstrated that the diffusion length in the absorber layer of our best cells is about 4 μm, which is a clear confirmation that evaporated SPC poly-Si diodes are a promising candidate for the cost-effective generation of PV electricity.

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