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AGIPD, a high dynamic range fast detector for the European XFEL

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ABSTRACT: AGIPD — (Adaptive Gain Integrating Pixel Detector) is a hybrid pixel X-ray detector developed by a collaboration between Deutsches Elektronen-Synchrotron (DESY), Paul-Scherrer-Institut (PSI), University of Hamburg and the University of Bonn. The detector is designed to comply with the requirements of the European XFEL. The radiation tolerant Application Specific Integrated Circuit (ASIC) is designed with the following highlights: high dynamic range, spanning from single photon sensitivity up to 10^4 12.5keV photons, achieved by the use of the dynamic gain switching technique using 3 possible gains of the charge sensitive preamplifier. In order to store the image data, the ASIC incorporates 352 analog memory cells per pixel, allowing also to store 3 voltage levels corresponding to the selected gain. It is operated in random-access mode at 4.5MHz frame rate. The data acquisition is done during the 99.4ms between the bunch trains. The AGIPD has a pixel area of 200×200 μm^2 and a 500μm thick silicon sensor is used. The architecture

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principles were proven in different experiments and the ASIC characterization was done with a series of development prototypes. The mechanical concept was developed in the close contact with the XFEL beamline scientists and is now being manufactured. A first single module system was successfully tested at APS.

KEYWORDS: X-ray detectors; Hybrid detectors; Front-end electronics for detector readout; Radiation-hard detectors

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1 Detector challenges

The European X-Ray Free Electron Laser (XFEL) [1] will provide ultra-short, highly coherent X-ray pulses which will revolutionize scientific experiments in a variety of disciplines spanning physics, chemistry, materials science, and biology. It is expected that the source will produce short ($\sim$100 fs), highly coherent pulses with a peak brilliance of 10^{33} ph/(s mm^2 mrad^2 0.1%BW) in the energy range 0.3 — 25keV depending on the experimental station. The pulses will be organized in bunch trains with a frequency of 10Hz. Each train consists of 2700 pulses with more than 10^{12} photons of 12keV each separated by 220ns resulting in a 4.5MHz pulse frequency.

Such characteristics of the source put severe requirements on the detector readout electronics. It should provide high dynamic range: from single photon sensitivity up to 10^4 12.5keV photons, which implies a low noise requirement: less than a 500 e$^-$. At the same time the detector must be XFEL timing compliant, so it should be able to record as many as possible consequent single pulses from the 2700 in a bunch train, which means burst mode operation at 4.5MHz frame rate. The detector should be radiation tolerant enough to operate for more than 3 years at the European XFEL, where it will accumulate more than 10MGy within that time. The mechanical constraints call for the lowest possible dead area, a central hole for the intense direct beam and a vacuum vessel as integral part of the design.

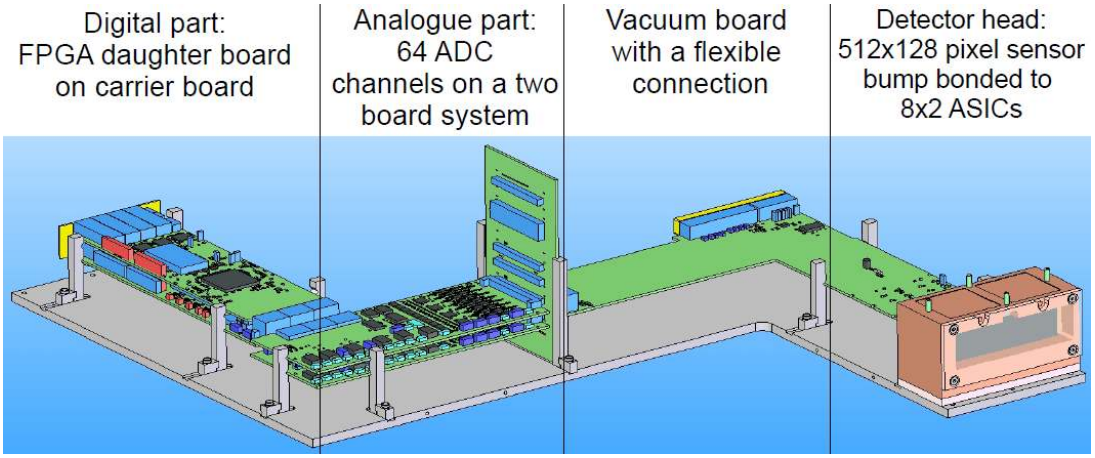

Figure 1. Structure of an AGIPD single module.

2 Detector concepts

2.1 Detector structure

AGIPD is a hybrid detector, composed from 16 modules as basic building blocks, each being in principle an independent detector system itself. The structure of a module consists of 4 main parts (figure 1). The X-Rays are absorbed in the detector head by the 500μm thick silicon sensor bump bonded to 8x2 ASICs resulting in a 512$\times$128 pixel array. The square pixels are arranged with 200μm pitch. A hybrid is formed by an array of ASICs bump bonded to the monolithic pixelated silicon sensor. The hybrid is then glued onto a sensor board made from low temperature co-fired ceramics (LTCC) and electrically connected to it by wire bonding to form the bare modules of the detector head.

Each module is connected to a vacuum board, which provides the connection to the ADC boards for the analogue signals as well as the power of the ASICs and the sensor. The vacuum barrier between the analogue and vacuum boards is formed by another PCB, which also provides a connection to the quadrant controller boards, providing the timing and control signals for the ASICs. The analogue part consists of a 64 ADC channels on a two board system. The analogue signal is digitized with 14-bit resolution and transferred then to the digital part: a carrier board with an FPGA daughter card on top to process the digital data and form packets sends these via one of four standard 10 Gbit/s Ethernet links by means of the standard TCP/UDP protocol.

2.2 Mechanical concept

The mechanical concept was developed in close contact with the XFEL beamline scientists and is now being produced. For operation at the European XFEL it is currently foreseen to have an AGIPD 1M system (figure 2) at the SPB beamline, and a second 1M system for the MID beamline. In order to increase the angular coverage towards the beam axis, the SPB beamline at the European XFEL will additionally employ a 128k pixel downstream detector consisting of 2 modules. Installing a 4M system, and/or single module systems at a later date is currently under discussion.

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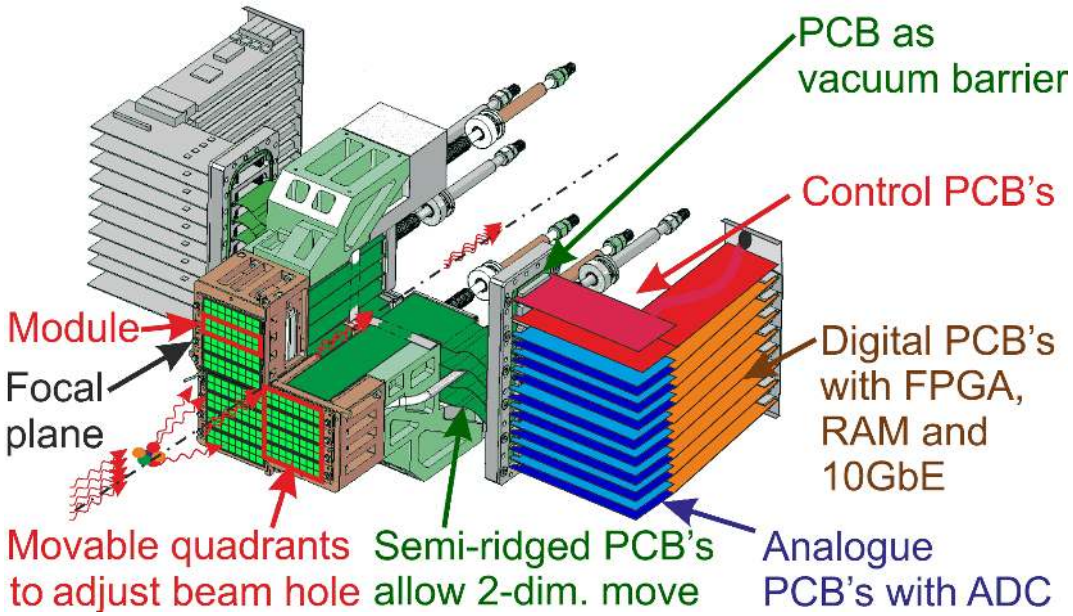

Figure 2. Mechanics of a 1M AGIPD system.

The AGIPD 1M system is subdivided into 4 independently movable quadrants that will allow the user to define an arbitrary hole sizes within the 25mm × 25mm limit of the system. Each individual quadrant carries 4 detector modules, the basic building blocks of the system [2]. In order to reduce the amount of space occupied along the beam axis, the electronics were designed in an angled shape, and form so called wings. Inside the vacuum vessel the wings are elongated along the beam axis, such that the detector plane protrudes from the vessel flange into the experimental chamber. Outside the vessel, each wing will feature a closed loop air stream cooling inside a special housing, employing a water cooled heat exchanger to remove the heat of the interface electronics (about 500W) without dissipation into the experimental area.

3 ASIC

3.1 Structure

The block diagram of the analog readout chain is given in figure 3. When the photon pulses arrive at the sensor, the charge generated in a pixel integrated by the preamplifier. The correlated double sampling (CDS) buffer following the preamplifier removes the reset noise and reduces the low frequency noise [3].

The output of the charge sensitive preamplifier not only connects to the CDS buffer, but also to a discriminator. If an input signal triggers this discriminator, additional feedback capacitors are added to the preamplifier feedback, thus lowering sensitivity and increasing the dynamic range in two steps. Each output of the CDS buffer and an analogue encoding of the selected gain are written to the analogue memory, which can store 352 samples. The signals for the operation of the pixel and the addressing of the memory are generated by a command based serial interface. Between the bunch trains, the stored signals are read out through the pixel buffer, column buffer and off-chip driver [4, 5].

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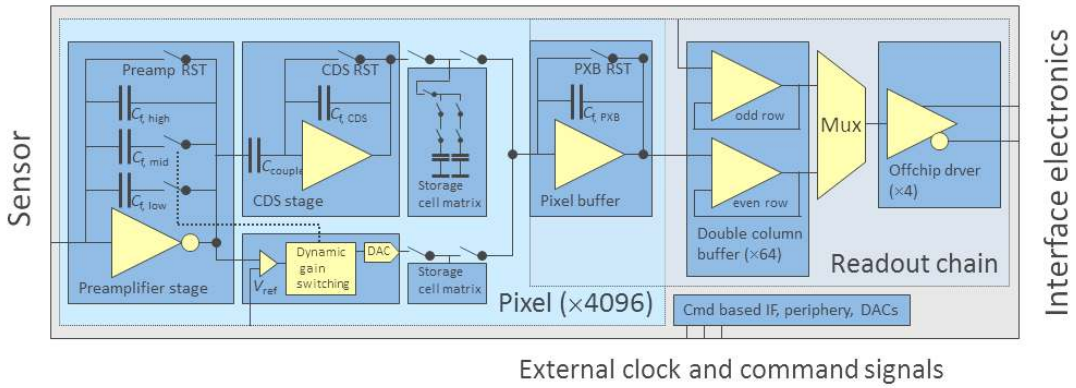

Figure 3. Analog readout channel of the ASIC.

Figure 4. AGIPD runs prototypes and full scale ASIC.

3.2 Development and characterization

In order to prove the adaptive gain concept, to study the characteristics of analogue and digital blocks, and to investigate the radiation hardness during the development of the AGIPD ASIC, 4 multi-project wafer (MPW) run prototypes were designed (figure 4). The technology is IBM 0.13μm 8RF-DM.

AGIPD 0.1 contained no pixels, but only readout blocks: a readout chain consisting of preamp and CDS stage and three different kinds of leakage current compensation circuitry.

AGHIPD 0.2 has 16 by 16 pixels with 100 memory cells each, no leakage current compensation and different combinations of preamp and storage architectures. AGIPD 0.3 incorporated the 16 by 16 pixel array with 200 radiation hard memory cells per pixel, high speed command based control interface, improved discriminator and CDS buffer. The 0.4 version has the same number of pixels, a higher sensitivity preamp (C_f = 60fF), 352 memory cells, double-column readout, an improved analogue multiplexer and off-chip driver but no command line interface. The full scale ASIC AGIPD 1.0 was taped out in April 2013. It has an array of 64 by 64 pixels with 352 memory cells per pixel, high sensitivity preamp, double-column readout, high speed command based control interface and landing pads for through-silicon vias (TSVs), which can be used instead of conventional wire bonds.

All prototype ASICs as well as the full scale one were extensively tested and characterized. The gain and noise measurements as well as linearity in the dynamic range of the AGIPD 1.0 are shown in figures 5 and 6. The non-linearity of the gain for all 3 gain stages was measured to be less than 0.5 % and the noise is below the Poisson limit.

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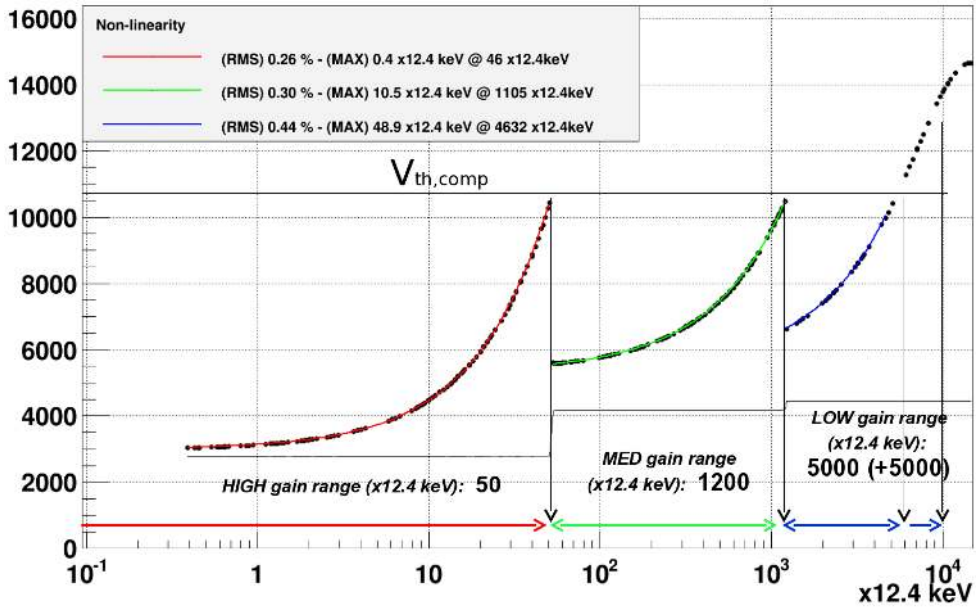

Figure 5. AGIPD 1.0 gain characterization.

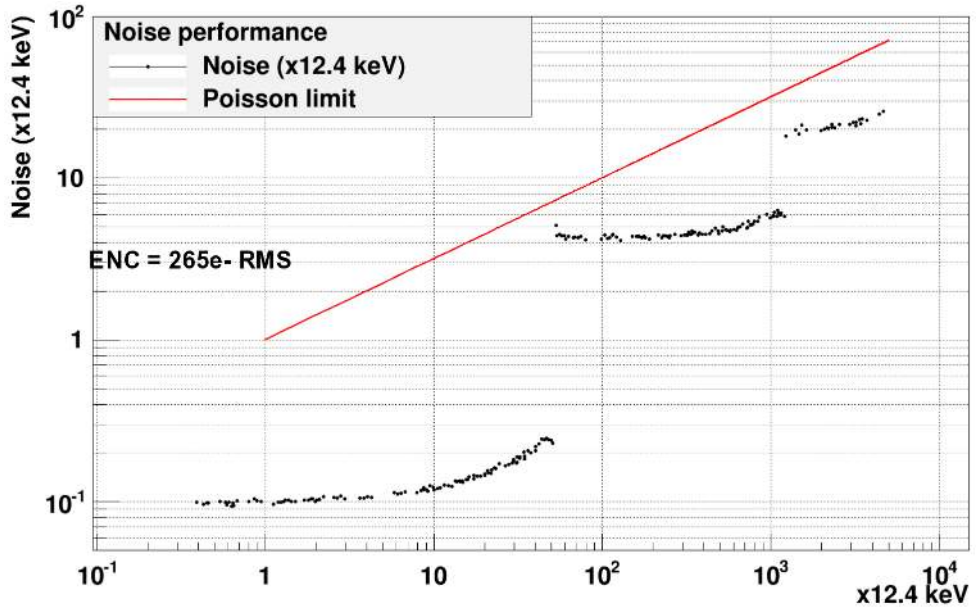

Figure 6. AGIPD 1.0 noise measurements.

3.3 Layout

The AGIPD 1.0 ASIC has dimensions of approximately 13mm by 14.2mm, and apart from the blocks mentioned above also contains DACs to bias the analogue circuits and internal calibration structures, digital buffers between the command based control block and the pixel matrix, and power distribution layers. The interface wire bond pads are subdivided in 7 different groups:

- 4 power groups providing analog, digital, input/output, and protection diode power,
- a digital input group containing three LVDS receivers and one CMOS receiver,

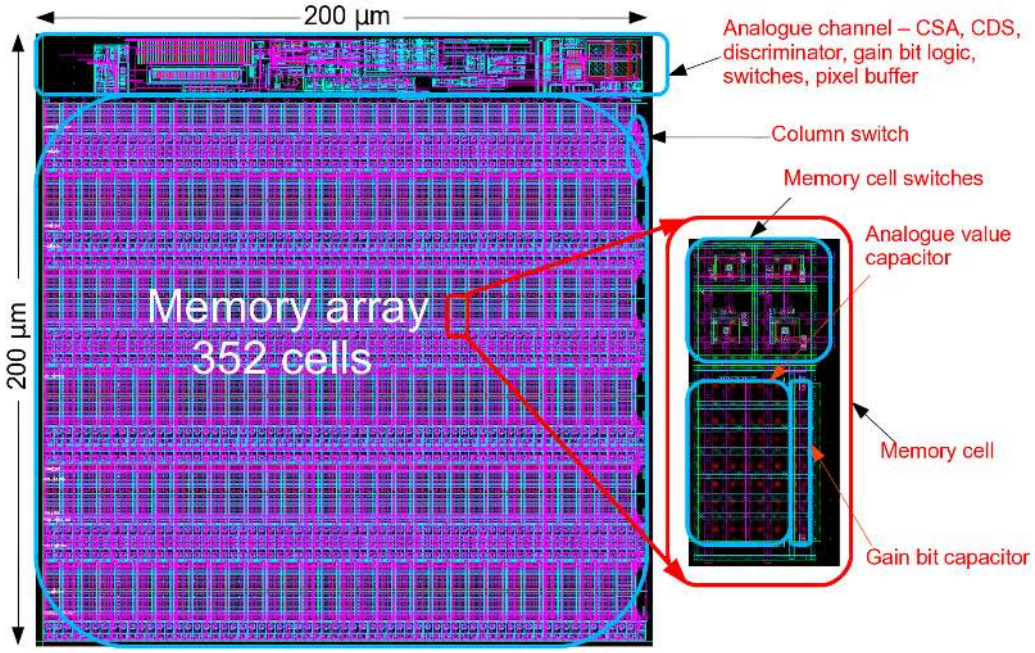

Figure 7. AGIPD 1.0 pixel layout.

- an analogue output group formed by 4 fully-differential off-chip drivers and
- the auxiliary group providing the possibility of external biasing, resetting and calibration injection.

The rectangular wire bond pads are 80μm by 174μm wide with a 200 μm pitch, which allows convenient re-bonding if needed. The ASICs wire bond pads can be cut off in order to reduce the insensitive space between modules in case TSV connections are used.

The pixel layout (figure 7) incorporates the analogue channel and 352 analogue memory cells in a 200 μm by 200 μm area. The "analogue channel" includes the charge-sensitive preamp (CSA), correlated double sampler (CDS), discriminator and gain bit logic circuitry, along with switches, some internal calibration structures and a pixel buffer. For internal calibration a current source and a voltage step over a test capacitor are used. Each memory cell stores charge values on two capacitors. The capacitor for the analogue value is 200fF while the one used to store the gain information is only 30fF. Since the gain data has a discrete nature, signal quality requirements are relaxed and droop is of no big concern. Therefore the approach to use analogue encoding of the gain information and the same readout path for amplitude and gain information on one hand increases the number of memory cells per pixel, while it on the other hand simplifies the readout architecture.

4 Data acquisition

Data from the detector is acquired by sending commands to the ASICs and digitizing its analogue output. The signal from each off-chip driver arrives at one of 64 ADC channels per module. After the conversion the data is acquired by the FPGA on the digital board. The digital board forms

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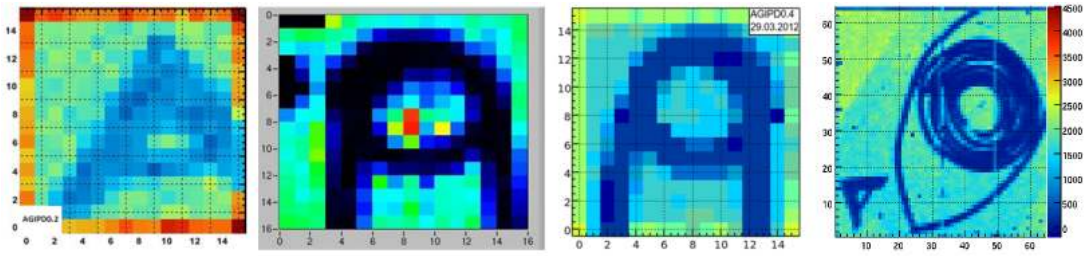

Figure 8. First images from AGIPD prototype chips, illuminated with an X-ray tube.

the TCP/UDP packets of the digitized data and sends them to the DAQ computer cluster via one standard 1/10 Gbit/s link. The software on the DAQ computers has two main functions: it creates an ASIC command lists and downloads it to FPGA of the quadrant board (or the digital board for single-module systems respectively). The software also controls the connection to the detector and data acquisition, performs data sorting and writing to disc, selects individual ASICs in a module and controls the power. On the vacuum board the ASIC power is controlled using an I^2C interface [6].

5 Beamline and imaging tests

An important part of the development was the imaging and beamline testing of different AGIPD prototypes and systems. The imaging tests were performed with an x-ray tube and dedicated laboratory equipment as a data acquisition system. In figure 8 the letter "A" was made from copper. From left to right: AGIPD 0.2, AGIPD 0.3, AGIPD 0.4. The rightmost picture originates from AGIPD 1.0 and shows the first "A" used for the AGIPD 0.2 test in addition to the fragment of an AGIPD logo made of Sn soldering wire.

First beamline tests were performed with the AGIPD 0.4 prototype, most of them at the P10 and P01 beamlines of PETRAIII at Deutsches Elektronen-Synchrotron (DESY). A single module system was tested at the Advanced Photon Source (APS) at Argonne National Laboratory (ANL) on the BM-1 beamline.

In the first test of an AGIPD 0.4 assembly at the P10 beamline the adaptive gain concept was proven. The test chip successfully imaged both the direct synchrotron beam and single 7.05keV photons at the same time, demonstrating the large dynamic range required for XFEL experiments. X-ray scattering measurements from a test sample agreed with calibrated measurements, proving the chip's capability to observe dynamics on a microsecond time scale [7].

In figure 9 the image of the direct beam is shown in logarithmic scale. The line-cuts of the left image show, that it simultaneously contains pixels in all three gain settings, as indicated by the dashed lines. Both images show the data averaged from 3000 individual frames. The right graph shows the histogram of a single pixel: the average intensity is 0.3 photons per 200 ns, corresponding to a count rate of 1.5Mcps/pixel or 37.5Mcps/mm^2. The individual peaks of photons of 7.05keV are clearly distinguishable. The ENC[1] of this pixel is 320 electrons rms.

In order to test the single pulse imaging capabilities of the same system, it was operated synchronous with the PETRA III storage ring running in 40 bunch mode (192ns pulse spacing).

[1] Equivalent Noise Charge.

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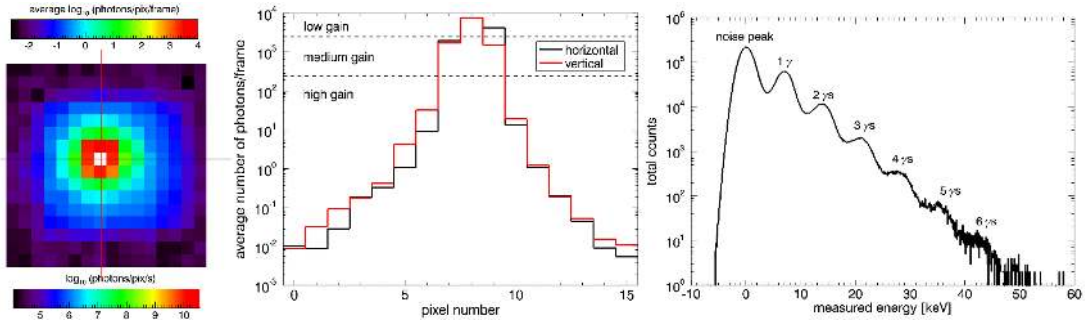

Figure 9. Experimets with AGIPD 0.4 at ETRA III. Left: image of the direct beam, middle: line-cut of the beam image, right: histogram of a single pixel.

As a test an experiment on the coherence properties of single x-ray pulses [8] was performed at the P01 beamline of PETRA III. It was carried out at 14.4keV photon energy, using a high-resolution monochromator and a KB-mirror to redirect to beam onto the detector. AGIPD 0.4 was operated at 5.2 MHz frame rate, i.e. faster than in the final application at the European XFEL.

Moving from prototypes to the full scale chip, in a similar experiment single shot imaging of the direct beam at 5.2 MHz was conducted with AGIPD 1.0. at P10.

Tests of the single module system at APS included burst imaging, dynamic range scans, a pencil beam scan, and imaging of a an object (fish). For characterization also memory cell scans and the recording of a gain map was performed. The data taken during that beamtime is currently processed and evaluated. The detector was able to run in burst mode taking 352 subsequent images synchronized to the source.

6 Summary

The adaptive gain approach was tested and found working on prototypes and a full scale chips. The high dynamic range of the AGIPD detector allows for direct imaging of a synchrotron beam simultaneous with single photon sensitivity. The system shows good linearity in all the dynamic range and noise below the Poisson limit. The system can operate at a frame rates even higher then European XFEL, which was successfully tested during a beamtimes at PETRA and APS synchrotron sources. Its performance and characteristics make AGIPD a useful imaging tool for the European XFEL, complying with all its requirements.

Among different ongoing activities within the AGIPD project, most important are: ASIC wafer testing, edgeless sensor development for use with TSV-compatible cuts of the chip, design of additional boards and mechanics for different AGIPD systems, which could be used at different sources, and the development of an ASIC for the next generation of detectors.

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APS BM-1: R. Bradford, D. M. Kline, S. Stoupin.

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