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We present the fabrication and characterization of an aluminum transmon qubit on a silicon-on-insulator substrate. Key to the qubit fabrication is the use of an anhydrous hydrofluoric vapor process which selectively removes the lossy silicon oxide buried underneath the silicon device layer. For a 5.6 GHz qubit measured dispersively by a 7.1 GHz resonator, we find $T_1 = 3.5$ μs and $T_2^* = 2.2$ μs. This process in principle permits the co-fabrication of silicon photonic and mechanical elements, providing a route towards chip-scale integration of electro-opto-mechanical transducers for quantum networking of superconducting microwave quantum circuits. The additional processing steps are compatible with established fabrication techniques for aluminum transmon qubits on silicon. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4994661]

In recent years, significant developments in experimental quantum information science[1,2] have been realized using microwave superconducting qubits. These devices, consisting of Josephson junctions (JJs) and linear circuit elements, are typically coupled to high-Q superconducting microwave cavities, which realizes the microwave analog of cavity QED—so-called circuit QED.[3–5] The advent of the transmon qubit[6–8] has provided a robust and scalable circuit QED building block. The large vacuum coupling rate attainable between qubit and cavity in the circuit QED architecture has enabled, among other things, realization of the strong dispersive coupling regime,[5,9] creation of quantum gates with state-of-the-art gate fidelities,[10] and most recently, circuits capable of quantum error detection and correction.[11,12]

Interfacing the circuit QED toolbox with other systems of physical or technological interest—cavity optomechanical systems, for example, Refs. 13 and 14—requires scalable fabrication techniques on compatible materials systems. Many works within the circuit QED community have focused on developing fabrication methods that realize long qubit lifetimes and small dephasing rates.[15–17] Two primary approaches have emerged: the so-called planar approach wherein qubits are coupled to on-chip resonators[18] and the 3D cavity approach wherein qubits are coupled to 3D box cavities.[19] Whereas the former affords higher device densities and more integration, the latter yields longer coherence times. In recent years, silicon has become favored as a substrate for its low dielectric loss and for the diversity of available fabrication techniques,[20–22] resulting in transmon qubits that have coherence times and gate fidelities similar to or exceeding their sapphire counterparts.[10,18,23–25]

Here, we present the fabrication and characterization of a planar transmon qubit on silicon-on-insulator (SOI) with a coherence time which is a factor of 20 improvement over prior work in this material system.[26] These SOI qubit fabrication methods not only realize viable qubits but are also compatible with the integration of other photonic, electronic, and MEMS components on the same SOI substrate.[27] Moreover, the processing steps for SOI may be simply added to those required for a silicon qubit process, enabling either Si or SOI qubits to be fabricated without a complete process change.

Our qubit design [pictured in Fig. 1(b) and shown schematically in Fig. 2(c)] is based on the Xmon qubit.[18] A long rectangular capacitor is capacitively coupled to both a readout resonator and an XY-control line; the capacitor is connected to ground through a SQUID loop [Fig. 1(c)] that is inductively coupled to a DC control line, which allows for frequency tuning of the qubit.[18] Our readout resonator, consisting of a $\lambda/4$ coplanar waveguide resonator, is inductively coupled to a transmission line, which allows for dispersive readout of the qubit.[18] We realize the as-measured parameters of: $f_q = \omega_q/2\pi = 5.652$ GHz, $\eta/2\pi = -300$ MHz, $\omega_r/2\pi = 7.143$ GHz, and $\chi/2\pi = 3.5$ MHz, where $\omega_q = \omega_{10}$ is the qubit transition frequency, $\eta = (\omega_{21} - \omega_{10})$ is the anharmonicity, ω_r is the readout resonator frequency, and $2\chi = \omega_{r,|0\rangle} - \omega_{r,|1\rangle}$ is the dispersive shift. These measured values imply a Josephson energy $E_J/h = 14.8$ GHz in the transmon limit ($E_J \gg E_C$), where $\hbar\omega_q \approx \sqrt{8E_JE_C} - E_C$ and the charging energy $E_C \approx -\hbar\eta$, as well as a vacuum qubit-resonator coupling rate $g/2\pi = 177$ MHz where $g \approx \sqrt{-\Delta\chi(1 + \Delta/\eta)}$ and $\Delta = \omega_q - \omega_r$. The readout resonator has intrinsic and extrinsic coupling Qs of $Q_i = 45.8 \times 10^3$ and $Q_e = 6.1 \times 10^3$, measured at single-digit intracavity photon numbers. These values are close to the designed and expected values.

Our fabrication process is a multi-layer process pictured in Fig. 1(a). We begin with a 10 mm × 10 mm chip of SOI [Si device layer: float zone grown, 220 nm, $\gtrsim 3$ kΩ cm; buried oxide (BOX) layer: 3 μm, silicon dioxide; Si handle: Czochralski grown, 750 μm, $\gtrsim 5$ kΩ cm]. We then perform the following main fabrication steps [from left to right in Fig. 1(a)]: (i) C_4F_8/SF_6 inductively coupled plasma reactive

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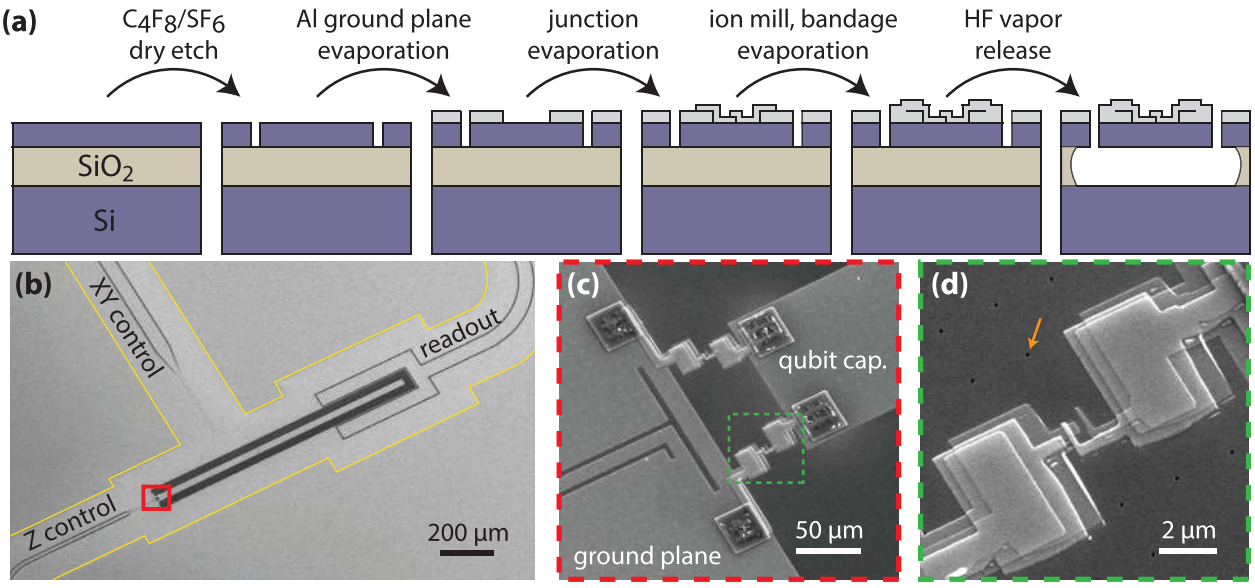

FIG. 1. Qubit fabrication process and SEM images of the SOI device. (a) Five step fabrication process as detailed in the text. (b) SEM image of an SOI qubit. The light (dark) gray regions are Al (exposed Si). The yellow outline demarcates the etch front of the HF vapor release, which extends ≈100 μm under the ground plane so as to isolate the qubit from the lossy Si-SiO_2 interface. The red box denotes the SQUID loop region of the device. (c) Zoom-in image of the SQUID loop, formed by a double angle evaporation process. The green box bounds one junction. "Bandage" regions described in the main text are visible as darker squares on both the qubit capacitor and the ground plane. (d) Zoom-in of an individual Josephson junction. Each junction has an approximate area of $(200\,\text{nm})^2$, corresponding to a zero-bias Josephson inductance of $L_{J,0} = 22$ nH per junction under the conditions described in the main text. The lattice of tiny dark circles faintly visible here are the etched holes that allow for HF vapor release. An orange arrow points to one such hole.

ion etch (ICP-RIE) of 50 nm radius holes through the device layer to allow for release in step (v) below; (ii) electron beam evaporation of 120 nm Al at 1 nm/s to define a ground plane, the qubit capacitor, and the readout resonator; (iii) double-angle electron beam evaporation of 60 nm and 120 nm of Al at 1 nm/s with an intervening 20 min oxidation at 5 mbar and subsequent 2 min oxidation at 10 mbar to forms the JJs; (iv) 5 min argon ion mill and 140 nm Al evaporation to form a "bandage" layer that electrically contacts the Al layers defined in steps (ii) and (iii); and (v) HF vapor etch of the underlying BOX layer. In the supplementary material, we omit steps (i) and (v) to fabricate a qubit on a high-resistivity Si substrate, with characterization confirming that steps (ii)–(iv) alone yield a viable qubit on Si (as opposed to SOI).

After steps (ii)–(iv), a liftoff process was performed in n-methyl-2-pyrrolidone at 80 °C for 2 h. In (i)–(iv), we use electron beam lithography to pattern our resist. The above process is similar to that described elsewhere[28,29] and, for SOI samples, yields a device layer that is partially suspended above the handle wafer. As highlighted by the yellow boundary line in the scanning electron microscope image of Fig. 1(b), we etch 100 μm into the BOX layer such that the circuit is far from the lossy Si/SiO_2 interface.[28]

We characterize the qubit in a ^{3}He/^{4}He dry dilution refrigerator with a base temperature of $T_f \sim 7$ mK using frequency-domain and time-domain spectroscopy. We begin with frequency-domain characterization and measure transmission (S_{21}) through a coplanar waveguide feedline using a two-port vector network analyzer (VNA). The Z control line is used to carry a small current which produces an external flux bias, Φ_{ext}, in the SQUID loop of the qubit, thereby tuning the qubit transition frequency, f_q. For a given Φ_{ext}, we identify f_q and transitions to higher levels (from which we extract η) by sweeping a continuous-wave (CW) microwave tone applied to the XY drive line and monitoring the resonator response.[30]

Having identified device parameters, we switch over to time-domain characterization, using the measurement setup summarized in Fig. 2. We characterize the qubit using dispersive readout[31] (Fig. 3), with Φ_{ext} set so that the qubit is at a first-order flux-insensitive point.[6,18] Excited state population decay [Fig. 3(b)] and Ramsey oscillations [Fig. 3(c)] yield $T_1 = 3.5\,\mu$s and $T_2^* = 2.2\,\mu$s, respectively. Comparative work, involving superconducting phase qubits on much thicker (2 μm device layer) SOI, has previously realized $T_1 = 1.6\,\mu$s and $T_2^* = 110$ ns.[26]

We can estimate the Purcell-limited T_1 by the simplistic single-mode estimate $(\Delta/g)^2/\kappa_r = 8.5\,\mu$s, where $\kappa_r = \omega_r/Q$ and $1/Q = 1/Q_i + 1/Q_e$. This is not much higher than our measured T_1, implying that incorporating an on-chip Purcell filter may improve our qubit lifetime.[32,33] Regarding the measured T_2^* values, since obtaining these measurements, we have identified and resolved some grounding issues in our measurement setup that likely contributed to excess flux noise coming from 60 Hz currents on our flux bias line. We anticipate that these improvements may even be important at the first-order flux insensitive point.

To characterize our gate fidelities, we utilized Clifford group randomized benchmarking,[10,34,35] shown schematically in Figs. 4(a) and 4(b). We measured three gates (X_π, $X_{\pi/2}$, and Y_π). We realize an average gate fidelity of $\bar{f}(C) = 0.9860(2)$ as well as individual gate fidelities of >0.992 for all measured gates. It should be noted that these gates have not yet been optimized to avoid phase errors or leakage outside the computational basis.[36]

In terms of the impact of the SOI device layer properties or various fabrication steps on the resulting qubit decoherence times, further systematic studies are required. In particular, the

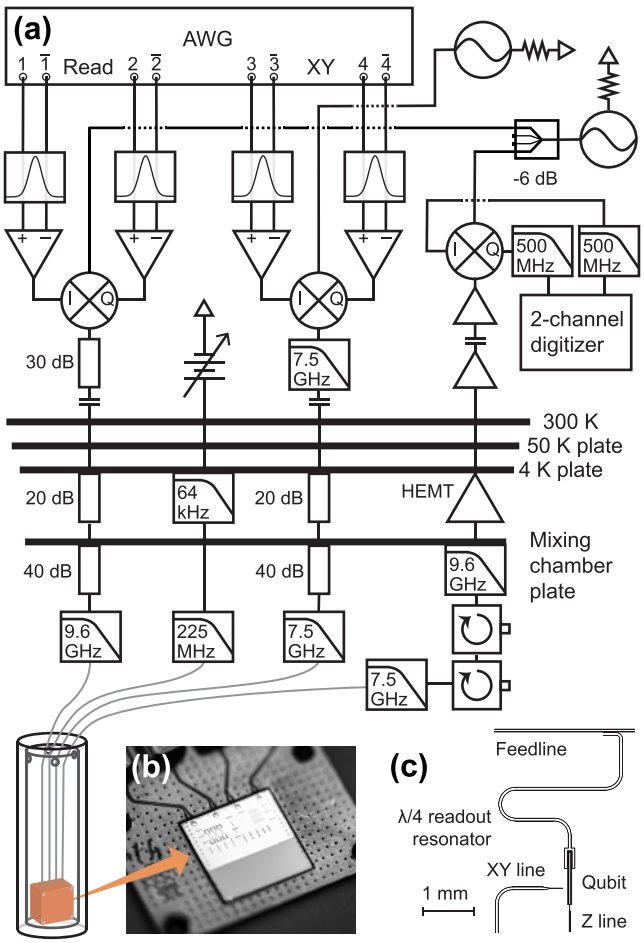

FIG. 2. (a) Time-domain measurement scheme. Near the top, Gaussian filters are indicated by enclosed Gaussian lineshapes (lines i and $\bar{i}$ are filtered individually). CW microwave sources with $Z = 50\ \Omega$ are indicated by the ac voltage symbols. The microwave source used for readout is followed by a power divider (we use just two ports and terminate others with 50 Ω). Attenuators are indicated by rectangles with labeled power attenuation. Capacitor symbols show inner/outer DC blocks. All low pass filters are reflective except for the 64 kHz filter, which is a dissipative RCR filter ($R = 499\ \Omega$, $C = 10$ nF). (b) Photograph of 1 cm^2 chip wire-bonded to printed circuit board. (c) Schematic of the device, including the layout of qubit, readout resonator, control lines, and cavity feedline.

importance of using the vapor HF etch to remove native oxides and (temporarily) passivate the Si surface before every evaporation step of aluminum on the Si layer (including right before the double angle evaporation used to form the JJs) needs to be clarified further. Also, any residual effects of the underlying BOX layer needs to be ruled out through the systematic studies of qubit coherence versus undercut extent, in conjunction with 3D numerical modeling to determine more optimized qubit and membrane geometries. Even while the precise physical and materials limitations of our system are unclear, current coherence times are sufficient for many quantum simulation and quantum optics experiments. Meanwhile, our realization of a highly coherent SOI qubit represents an essential building block for hybrid electro-opto-mechanical systems on SOI. Already, electromechanical and optomechanical coherent transduction bandwidths exceed the bandwidth of our qubit by a factor of two,[14,28,37] a prerequisite for high-fidelity, bi-directional microwave-to-optical quantum state transduction—an interesting and challenging research program in its own right, with many potential realizations.

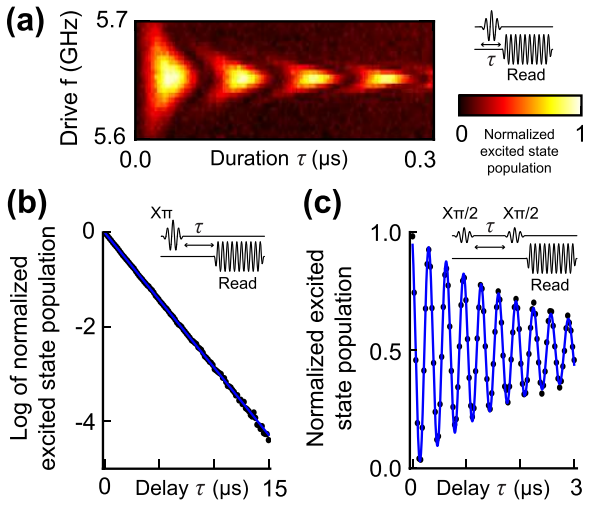

FIG. 3. Qubit characterization. (a) Excited state population (normalized to the unit interval) as a function of XY drive frequency and pulse duration τ exhibits a chevron pattern typical of a qubit undergoing Rabi oscillations. (b) Natural log of the excited state population, normalized to the unit interval, shows exponential decay as a function of waiting time τ with lifetime $T_1 = 3.5\ \mu s$ (points are data, blue trace is fit). (c) By applying two off-resonance $\pi/2$ pulses with a variable intervening delay τ, the excited state population shows Ramsey oscillations (points are data; blue trace is fit). The decay of the envelope yields coherence time and $T^*_{2,SOI} = 2.2\ \mu s$. In (a)–(c), we use a rectangle-windowed 500 ns readout pulse and 30 ns X_π and $X_{\pi/2}$ pulses.

Overall, our fabrication and measurements of Al qubits on SOI represent a modest but important technical stepping stone on the path to a variety of potential quantum information and quantum science goals. Taken together with complementary advances in the fields of cavity opto- and electromechanics,[14,38] and in the context of competing systems,[18,25] we are optimistic about the potential of hybrid quantum systems and circuit QED on silicon-on-insulator.

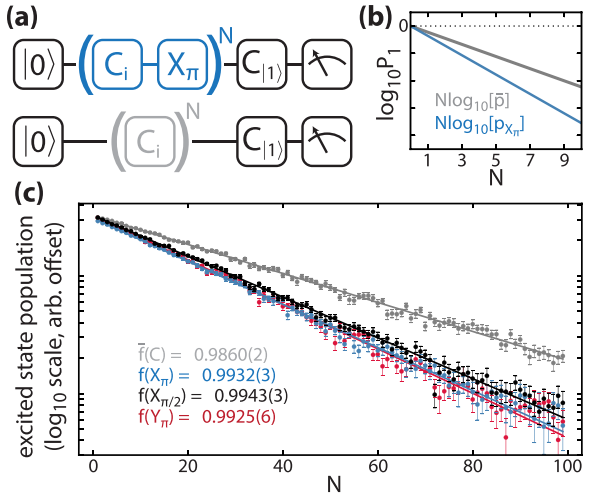

FIG. 4. Randomized benchmarking. (a) A schematic of Clifford group randomized benchmarking, described in the supplementary material. (b) Excited state probability as a function of N reveals the gate fidelity through the slope of the resultant line on a semilog plot and the relations described in the supplementary material. The limit of perfect fidelity is shown as a dashed line. (c) Gate fidelity (with an arbitrary offset given by the readout fidelity) as a function of N using 30 ns pulses. Error bars are 1 standard error in the measurements averaged over 50 random Clifford sequences. Uncertainties in the gate fidelities represent 1 standard deviation of f due to the statistical uncertainty of the parameter p in the exponential fit.

See supplementary material for details concerning the measurement setup and the randomized benchmarking, and for characterization of an Al-on-Si transmon fabricated by omitting the first and last steps of our SOI fabrication process.

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