ECS Transactions, 3 (15) 173-181 (2007)
10.1149/1.2721486, copyright The Electrochemical Society

# ALD Options for Si-integrated Ultrahigh-density Decoupling Capacitors in Pore and Trench Designs

F. Roozeboom[1,*] J.H. Klootwijk[2], J.F.C. Verhoeven[2], F.C. van den Heuvel[2], W. Dekkers[1], S.B.S. Heil[3], J.L. van Hemmen[3], M.C.M. van de Sanden[3], W.M.M. Kessels[3], F. Le Cornec[4], L. Guiraud[4], D. Chevrie[4], C. Bunel[4], F. Murray[4], H.-D. Kim[5] and D. Blin[6]

*[1]NXP Semiconductors Research, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands*
*[2] Philips Research, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands*
*[3]Dept. of Applied Physics, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands*
*[4] NXP Semiconductors, 2, Rue de la Girafe, Caen Cedex, 14096, France*
*[5]Jusung Engineering, 49 Neungpyeong-Ri, Opo-EupGwangju-Si, Gyunggi-Do, Korea 464-890*
*[6] Jusung Engineering Europe, 914 Avenue Ambroise Croizat, 38920 Crolles, France*

This paper reviews the options of using Atomic Layer Deposition (ALD) in passive and heterogeneous integration. The miniaturization intended by both integration schemes aim at Si-based integration for the former and at die stacking in a compact System-in-Package for the latter.

In future Si-based integrated passives a next miniaturization step in trench capacitors requires the use of multiple 'classical' MOS layer stacks and the use of so-called high-k dielectrics (based on $HfO_2$, etc.) and novel conductive layers like TiN, etc. to compose MIS and MIM stacks in 'trench' and 'pore' capacitors with capacitance densities exceeding 200 $nF/mm^2$.

One of the major challenges in realizing ultrahigh-density trench capacitors is to find an attractive pore lining and filling fabrication technology at reasonable cost and reaction rate as well as low temperature (for back-end processing freedom). As the deposition for the dielectric and conductive layers should be highly uniform, step-conformal and low-temperature ($\leq$ 400 °C), ALD is an enabling technology here, by virtue of the self-limiting mechanism of this layer-by-layer deposition technique.

This article discusses first a few examples of LPCVD deposition of conventional MOS layers with ONO-dielectrics and *in situ* doped polycrystalline silicon, both as single layers and multilayer stacks. In addition, a few options for ALD deposition of thin dielectric and conductive layers (e.g. $HfO_2$- and TiN-based) will be discussed. The silicon substrates that were used contained high aspect ratio ($\geq$ 20) features with cross-section and spacing of the order of 1 μm.

[*] Phone +31-40-2742767 ; Email : fred.roozeboom@nxp.com



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

## 1. Introduction

### Challenges in passive and heterogeneous integration

In the past decade the integration of passive components in silicon and the further 3D integration and stacking of individual chips from different technologies (e.g. CMOS, GaAs, MEMS) into one package ('*heterogeneous*' integration) have been developed to such an extent that now the first mass-volume production has started. Today, the International Technology Roadmap for Semiconductors includes the future projections for the next generation Si-based Integrated Passives and *System-in-Package* (SiP) integration (1).

Recently the first highly integrated cellular RF transceiver systems based on the use of these technologies were launched (2). Here, amongst others, Philips (now NXP) Semiconductors utilizes back-end silicon processing to integrate passive components onto a silicon substrate that can act as a carrier for the heterogeneous integration of active component dies, MEMS dies, etc. (3). As an example, a transceiver IC can be flip-chip mounted onto this passive component silicon substrate, thus minimizing interconnect parasitics and footprint area. This sub-assembly is then flipped back into a standard lead frame package (3), see Fig. 1.

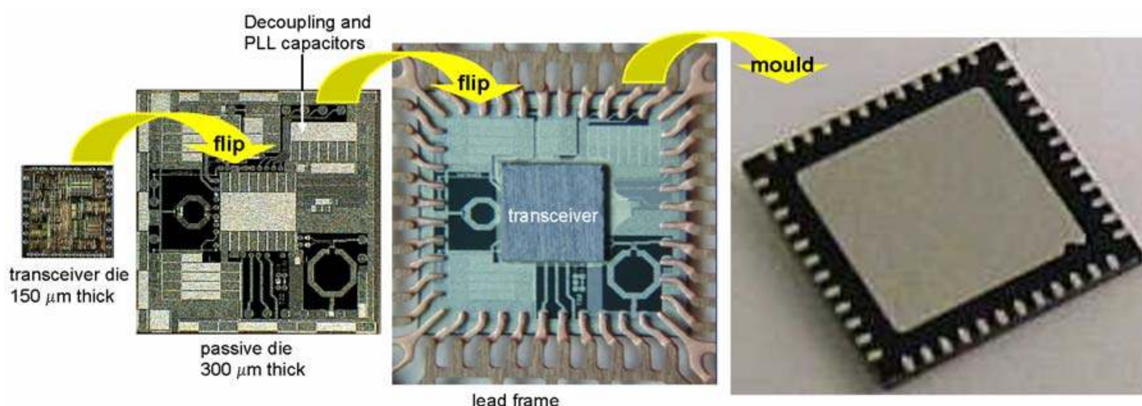


***Figure 1.*** *Passive die with active transceiver die flipped on top, double-flipped on a lead frame and finally moulded into a System-in-Package module. Shown is an example of a Bluetooth 'plug and play' System-in-Package radio module. After ref. 3.*

The passive die is made in the so-called PICS (Passive Integration Connecting Substrate) technology developed to integrate passive components such as high-Q inductors, resistors, accurate MIM capacitors and, in particular, high-density (~30 nF/mm$^2$) MOS 'trench' capacitors for decoupling and filtering. These are fabricated in silicon by dry-etching arrays of high aspect ratio macropores with cross-section and spacing of the order of ~ 1 µm, and up to ~30 µm depth. Trench capacitors filled with ~ 30 nm silicon oxide and nitride ('*ONO*') dielectrics and a poly-Si/ Al top electrode showed superior dielectric breakdown voltage (30 V typical), and very low leakage current and long lifetime (4,5).

A next miniaturization step includes the use of so-called *high-k dielectrics* (based on $HfO_2$, etc.) to compose MIS and MIM trench and pore capacitors with increased capacitance densities of ≥ 200 nF/mm$^2$. Capacitance enhancement techniques are known from CMOS technology (6). Recently, 3D MIM decoupling capacitors integrated in the BiCMOS technology interconnect levels have been reported to have 35 nF/mm$^2$ capacitance density (7).



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

In this paper we address the challenges and opportunities in realizing ultrahigh density macropore and -trench capacitors with sufficient breakdown voltage. One emerging technique to accomplish this on flat substrates, is the growth of MIS layer stacks containing so-called '*high-k'* dielectrics and metallization layers, both grown by Atomic Layer Deposition (ALD). However, the application of ALD onto wafers with high aspect ratio features leads to additional challenges: the roughness on the feature sidewalls may cause undesired lower breakdown voltages. Also the formation of interfacial oxide layers may lead to undesired lower relative dielectric constants.

The second, alternative way to reach ultrahigh capacitance density is to use the conventional techniques (mainly LPCVD) for depositing a double (or multiple) MOS layer stack in the pore and trench arrays with even thinner 'ONO'-based dielectrics. Note, that the temperatures used in conventional processing do not allow their use in back-end processing, whereas ALD temperature budgets do.

**Atomic Layer Deposition, perspectives and limitations**

One of the major challenges in realizing ultrahigh-density trench capacitors is to find an attractive pore lining and filling fabrication technology at reasonable cost and reaction rate as well as low temperature (for back-end processing freedom). The deposition of the dielectric and conductive layers should be highly uniform and step-conformal and low-temperature ($\leq$ 400 °C). Here ALD is an enabling candidate by virtue of the self-limiting mechanism of this layer-by-layer deposition technique. A substrate surface is submitted to alternating exposures to vapors of two reagents, for example, trimethylaluminum (TMA) and water vapor in the case of $Al_2O_3$ deposition. Through its self-limiting surface reactions, ALD enables the uniform lining or filling of high aspect ratio pores with (sub)monolayer control. The self-limiting character provides inherent conformality, as even demonstrated for challenging devices like deep DRAM trench capacitors with ~60:1 aspect ratios at design rules below 100 nm (7). Yet, ALD processing improves the production of many other devices with a large topology, such as via holes in stacked dies, MEMS, planar waveguides, multilayer optical filters, and layers protecting against diffusion, oxidation, corrosion, etc.

## 2. Experimental

Highly conductive silicon (100) substrates were used or high resistivity (> 5 kΩ·cm) substrates that were phosphorus-doped in the macropore regions later in the process. The macropore arrays were dry-etched in wafers with 150 mm diameter. We used Reactive Ion Etching with the so-called *Bosch* process in an inductively coupled plasma reactor, using a 1 μm oxide hard mask and optionally a 1.3 μm pohotoresist on top of the wafers.

Single conventional MOS layer stacks were deposited as described earlier (8). The 30 nm dielectric 'ONO' layer is grown by thermal oxidation, silicon nitride deposition by LPCVD and TEOS oxide deposition, respectively. This is followed by LPCVD of ~ 0.5 μm in situ phosphorus-doped polycrystalline silicon. More details were published elsewhere (8).

Double conventional MOS capacitor stacks (' *MOMOS* ') were designed in such a lay-



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

out that the electrical characterization could be carried out at both the individual single capacitor and at the double capacitor level. Basically the growth sequence is performed twice, with one exception: the second ONO-layer starts with a TEOS deposition instead of thermal oxidation. This is done in order to keep the first polysilicon non-oxidized, preventing additional roughening of this polysilicon layer (9).

The total dielectric layer thickness varied from 16 to 40 nm and the n-type poly-silicon layer thickness remained of the order of ~0.5 μm.

**ALD-grown capacitors**

Macropore array substrates were used for the growth of various structures of which we report on two examples:

1) a stack of ONO (total 30 nm, grown as above), and 10 nm TiN deposited on top with plasma-assisted ALD at 400 $^oC$ using $TiCl_4$ vapor dosing (order $\sim 1\times10^4$ L) in combination with $H_2$-$N_2$ plasma exposure ($p_{N2}$ =1 mtorr, $p_{H2}$ = 10 mtorr). More details are described elsewhere (10).
2) a stack of $Al_2O_3$/$HfO_2$/$Al_2O_3$, grown in $O_3$ plasma with ALD from trimethyl aluminum (TMA) at 380 $^oC$ and from tetrakis (ethylmethylamino)hafnium (TEMAHf), at 400 $^oC$, with a 0.5 μm n-type poly-silicon layer deposited on top, as described previously (11).

**Structural and electrical characterization**

The layer stacks grown were further processed into capacitor test structures as described previously (3, 8) for electrical testing.

## 3. Results and discussion

### 3.1 Classical MOS capacitors

Since we have reported extensively on the growth and the electrical performance of single MOS stack capacitors in pore arrays (3-5, 8, 10), we will focus on the double MOS stacks here. Figure 2 shows a cross-section SEM image of a double MOS stack grown in high aspect ratio (~20) macropores. The thickness uniformity of the individual layers across he pores is ‘ideal’ and equal to that for the single MOS stacks that we have typically published in recent years.

Figure 3 shows images of the stages in the growth of a double MOS stack in a high aspect ratio 3D-trench array. This design contains an open space between the features, which facilitates the transport probability of the gaseous reagents and products, both during etching and layer stack coating of the features. This is illustrated in Fig. 4, which displays the transport probability of particles as a function of aspect ratio and length/width ratio of pores and trenches. The curves are obtained by a Monte Carlo simulation of the molecular flow conductance based on Knudsen transport of particles in the features (12). It is evident that molecular flow conductance limits free diffusion most in pores and the least in more open 2D structures. In our case this limitation is even less because of our 3D trench design.



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

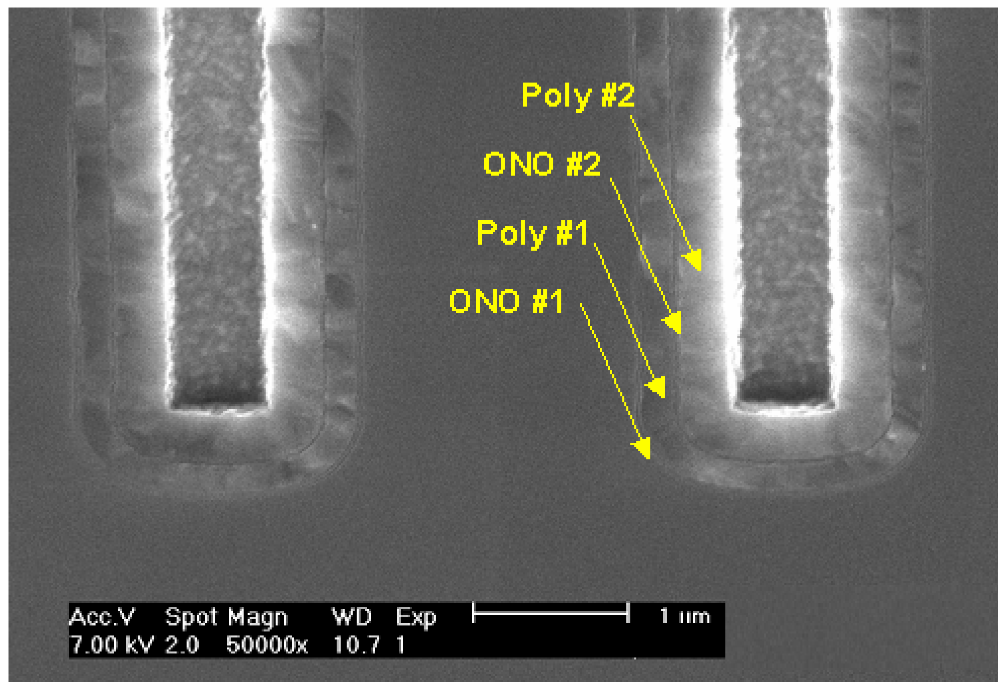


***Figure 2.*** *Double MOS stack with ONO and phosphorus-doped polycrystalline silicon grown in macropores.*

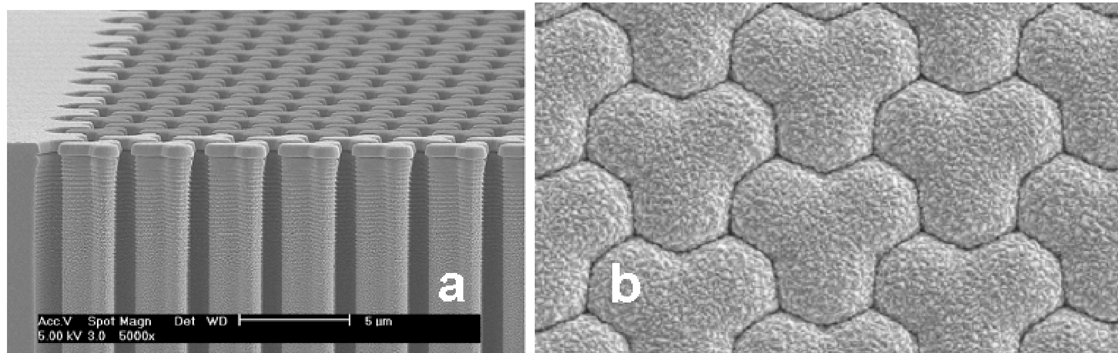


***Figure 3.*** *SEM images of 3D trench-array; (a) side view after RIE-etching and (b) top view after filling with a double MOS capacitor stack.*

The electrical testing of these double stack capacitors revealed capacitance densities as high as 230 nF/mm$^2$ with a breakdown voltage of 11.7 V for the thinnest dielectrics (~16 nm ONO, with maximum nitride) on the highest aspect ratio (~20) features. For comparison, a single stack capacitor on lower aspect ratio (~15) features with ~20 nm ONO revealed 80-90 nF/mm$^2$ with a breakdown at 15.5 V.



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

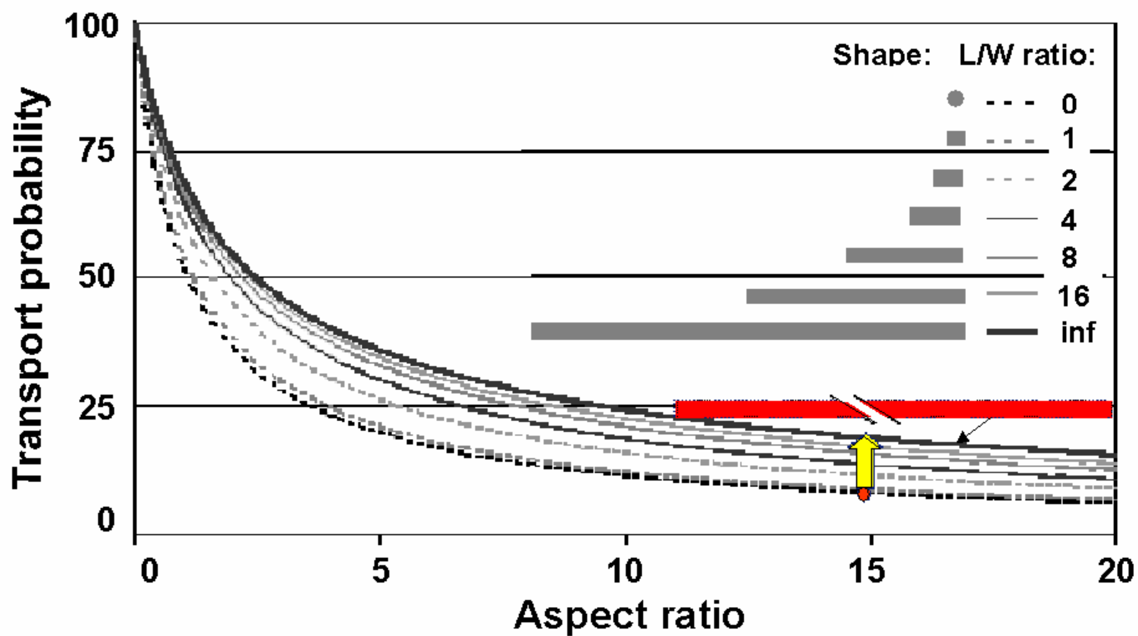


***Figure 4.*** *Transport coefficients obtained by Monte Carlo simulation. After J. Kiihamäki (12). Illustrated is the enhanced transport in features (pores and trenches) with longer 2D cross-section (Length/Width) and lower aspect ratio.*

### 3.2 ALD grown capacitors

The TiN plasma-assisted ALD (PA-ALD) process based on $TiCl_4$ yielded thin TiN films with an excellent resistivity (130 μΩ·cm, compared to ~800 μΩ·cm for poly-Si) and low impurity levels (C, H, Cl, etc.) surpassing the material quality achieved with the usual thermal process employing $NH_3$ dosing (10).

TiN films deposited by plasma-assisted ALD for application as electrode material in trench capacitors have been explored. In terms of acceptable material quality the thermal process is limited to the substrate temperature range of 300-400 °C while the plasma-based process can yield fair material properties down to temperatures as low as 100 °C.

Figure 5 shows TEM images of a MOS stack of 30 nm 'ONO' with PA-ALD TiN and LPCVD poly-Si on top grown in 30 μm deep pores. It appeared that the layer thickness along the pores was very uniform.

The same holds for the $Al_2O_3$ / $HfO_2$ / $Al_2O_3$ stack shown in Fig. 6. This stack is covered by poly-Si and showed 120 nF/mm$^2$ capacitance density. This is lower than one might expect based on the nominal thicknesses (3 nm $Al_2O_3$ / 10 nm $HfO_2$ / 3 nm $Al_2O_3$ in our structure should yield ~ 50 % more) and we ascribe the discrepancy mainly to the interfacial $SiO_2$ layer that is prominently present. We note, that after wafer cleaning by HF-dipping our measures to preclude oxidation of the etched pores were not optimal.



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

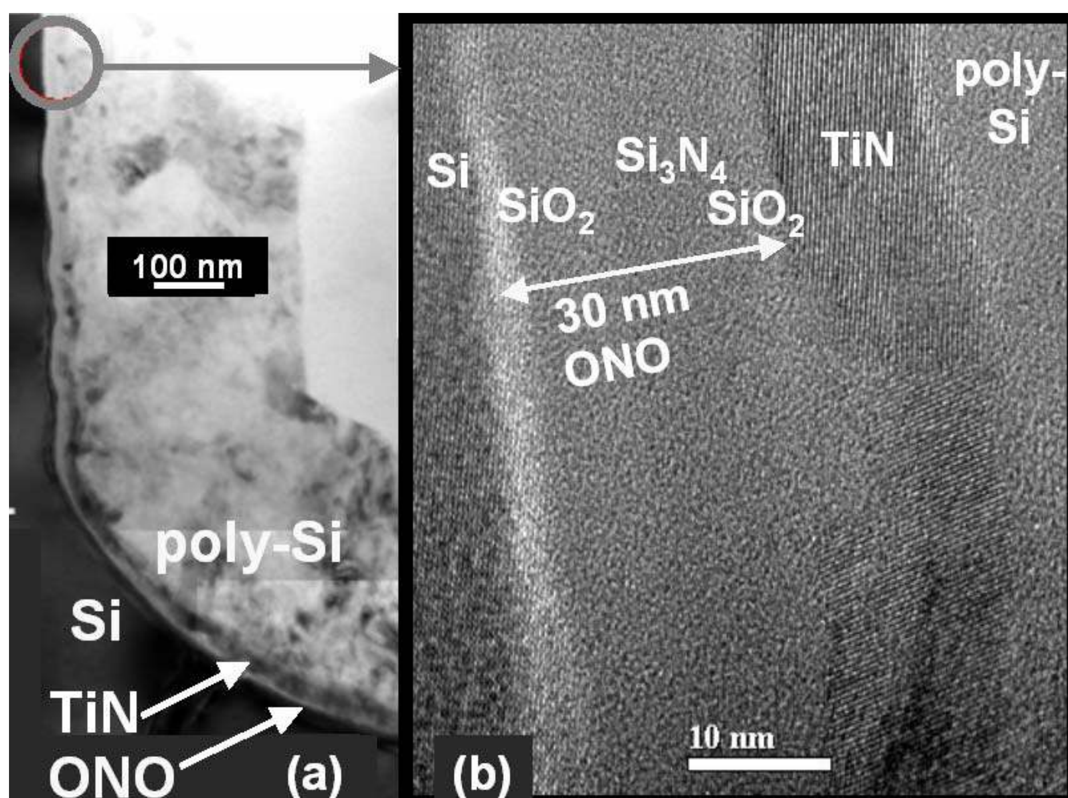


***Figure 5***. *Bright-field (a) and high-resolution (b) TEM images of a MOS stack of 'ONO' dielectric and PA-ALD TiN with LPCVD poly-Si on top.*

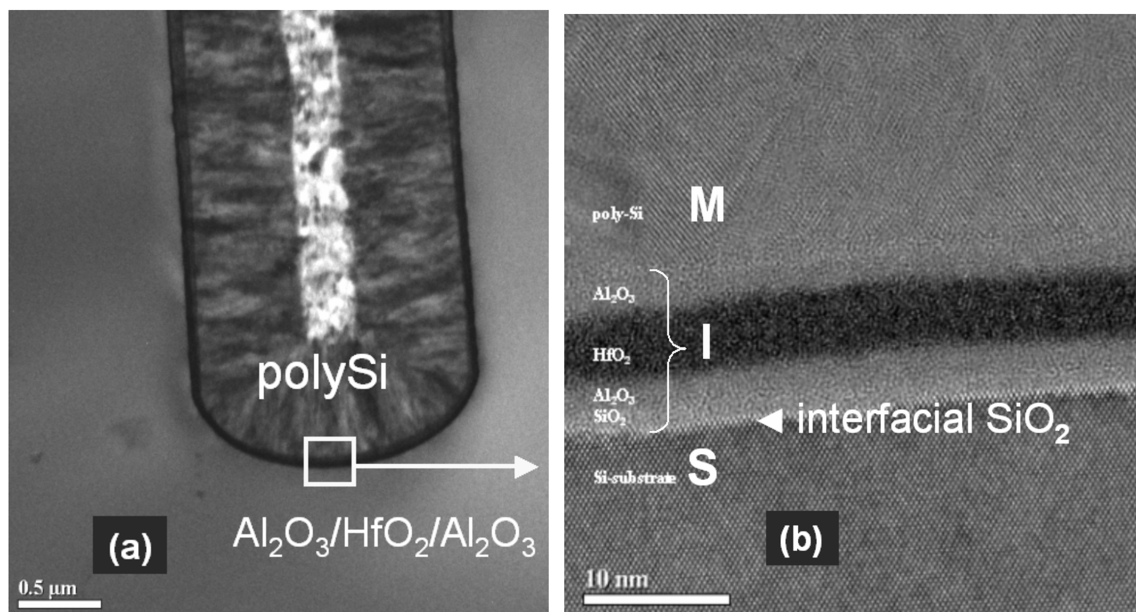


***Figure 6***. *(a) SEM cross-section and (b) high-resolution TEM image of an $Al_2O_3$ / $HfO_2$ / $Al_2O_3$ dielectric layer stack with a poly-Si electrode layer on top.*



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

## 4. Concluding remarks

We have shown that ultrahigh density (> 200 nF/mm$^2$) capacitors can be manufactured by classical layer deposition (LPCVD) of MOS capacitor stacks in high aspect ratio macropore and trench shaped substrates and by Atomic Layer Deposition of MIS layers in macropore arrays. With the former method we have shown :

- ~30 nF/mm$^2$ capacitance density with breakdown voltages ($V_{bd}$) of 30 V for single MOS capacitor stacks grown in macropore arrays.
- higher capacitance densities, up to 80-90 nF/mm$^2$ for single MOS stacks with thinner dielectrics (~20 nm), withstanding up to ~15.5 V.
- over 200 nF/mm$^2$ capacitance densities with breakdown voltages of 11.7 V for double MOS capacitor stacks with ~ 16 nm dielectric layers grown in trenches.
- ~120 nF/mm$^2$ capacitance density for a single $Al_2O_3$ / $HfO_2$ / $Al_2O_3$ MIS capacitor stack; this can be further improved by measures to suppress spontaneous oxidation of the Si-substrate.

The results of our current study on the ALD growth and electrical performance of ALD-grown $Al_2O_3$/TiN multilayer stacks in pore and trench arrays will be published soon (13).

Compared to LPCVD, Atomic Layer Deposition offers more freedom of back-end (low-temperature) processing and combining with other 3D heterogeneous integration schemes e.g. for seed and diffusion barrier layers (14) in via interconnect structures (with)in the same substrate.

In conclusion, there is a bright prospect for ALD in passive and heterogeneous integration. One provision is that ALD be further developed to maturity and cost factors (e.g. the low wafer throughput due to its slow deposition rate) are reduced. Here, the development of ALD at the batch level for mass manufacturing may compensate for the low growth rates in single-wafer ALD.

## Acknowledgments

This work is funded by Senter-Novem, The Netherlands (IS-044041 project '*INNOVia*'), and is performed in collaboration with the Universities of Technology in Eindhoven and Delft. The research of W.M.M. Kessels has been made possible by a fellowship of the Royal Netherlands Academy of Arts and Sciences (KNAW). Finally, the long-term collaboration with Jusung Engineering (Korea) is especially acknowledged here.



Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

## References


1. ITRS Roadmap 2005 edition, '*Assembly and Packaging*', see: http://www.itrs.net/Links/2005ITRS/Home2005.htm.
2. See: http://www.3d-ic.org/literature.html.
3. F. Roozeboom, A.L.A.M. Kemmeren, J.F.C. Verhoeven, F.C. van den Heuvel, J. Klootwijk, H. Kretschman, T. Frič, E.C.E. van Grunsven, S. Bardy, C. Bunel, D. Chevrie, F. LeCornec, S. Ledain, F. Murray and P. Philippe, *Thin Solid Films* **504**, 391 (2006).
4. F. Roozeboom, A. Kemmeren, J. Verhoeven, F. van den Heuvel, H. Kretschman and T. Frič, *Mat. Res. Soc. Symp. Proc.* **783**, 157 (2003).
5. F. Roozeboom, A.L.A.M. Kemmeren, J.F.C. Verhoeven, F.C. van den Heuvel, J. Klootwijk, H. Kretschman, T. Frič, E.C.E. van Grunsven, S. Bardy, C. Bunel, D. Chevrie, F. LeCornec, S. Ledain, F. Murray and P. Philippe, *Electrochem. Soc. Symp. Proc*. **2005-8**, 16 (2005).
6. M. Gutsche, H. Seidl, J. Luetzen, A. Birner, T. Hecht, S. Jakschik, M. Kerber, M. Leonhardt, P. Moll, T. Pompl, H. Reisinger, S. Rongen, A. Saenger, U. Schroeder, B. Sell, A. Wahl and D. Schumann, *Tech. Digest IEDM* **2001**, Washington DC, pp. 18.6.1-18.6.4.
7. A. Bajolet, J.C. Giraudin, C. Rossato, L. Pinzelli, S. Bruyère, S. Cremer, T. Jagueneau, P. Delpech, L. Montes, G. Ghibaudo, *Proc. 35$^{th}$ ESSDERC* **2005**, Grenoble, pp. 121-124.
8. F. Roozeboom, R. Elfrink, T.G.S.M. Rijks, J. Verhoeven, A. Kemmeren and J. van den Meerakker, *Int. J. Microcircuits and Electronic Packaging*, **24** (3) 182 (2001), and refs. therein.
9. J.H. Klootwijk, H. van Kranenburg, P.H. Woerlee and H. Wallinga, *IEEE Trans. Electron Devices*, **46** (7), 1435 (1999).
10. S.B.S. Heil, E. Langereis, F. Roozeboom, M.C.M. van de Sanden and W.M.M. Kessels, *J. Electrochem. Soc*. **153**, G956-G965 (2006).
11. J. Klootwijk, A. Kemmeren, R. Wolters, F. Roozeboom, J. Verhoeven and F. van den Heuvel, in '*Defects in Advanced High-κ Dielectric Nano-Electronic Semiconductor Devices*', (E. Gusev, ed.); Springer: Dordrecht, 2006, p. 17.
12. J. Kiihamäki, 'Fabrication of SOI micromechanical devices,' PhD thesis, Helsinki University of Technology, VTT Publications 559, Espoo 2005.
13. J.H. Klootwijk *et al*., to be published.
14. H. Kim, C. Detavenier, O. van der Straten, S.M. Rossnagel, A.J. Kellock and D.-G. Park, *J. Appl. Phys*. **98**, 014308 (2005).




Downloaded 10 Mar 2009 to 131.155.108.71. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp