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Aliasing Suppression of Multi-sampled Current Controlled LCL-Filtered Inverters

Shan He, *Student Member, IEEE*, Dao Zhou, *Senior Member, IEEE*, Xiongfei Wang, *Senior Member, IEEE* and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Multisampling control provides an attractive way to reduce the control delays in LCL-filtered grid-connected inverters. Thereby, the bandwidth and stability margin will be improved. However, high frequency switching harmonics (SHs) is introduced in the control loop when the inverter-side current is sampled. In order to investigate the effect of multisampled high frequency SHs, the relationship between the double-update pulse width modulation (PWM) and multi-update PWM is deduced through geometric deduction. It is shown that the multi-update PWM is equivalent to double-update PWM with sampling instant shift, and the equivalent Nyquist frequency is equal to the switching frequency. Moreover, the non-averaged value of current is sampled within one switching period and aliased low-order harmonics will appear in the grid-side current. Hence, filtering the multi-sampled SHs is necessary, and an improved repetitive filter is proposed to remove all the sampled SHs and keep the advantage of phase boost by using the multisampling control. The method is evaluated with a single-loop inverter-side current control, and its effectiveness is verified through the simulation and experiment.**

***Index Terms*—Multisampling, aliasing, low-order harmonics, switching harmonics, improved repetitive filter.**

I. Introduction

LCL-filtered grid-connected inverters have been widely used in distributed generation systems based on photovoltaic, wind turbine, and energy storage systems [1-2]. Due to the digital control delays, the control bandwidth and the low frequency gains are limited with the given stability margins [3-4]. Especially in high-power inverters operating at a low switching frequency, the regular sampling methods (i.e., single-sampling or double-sampling in a switching period) impose constraints on the transient dynamics of the system [5-6]. Alternatively, multisampling control is a potential candidate, since the control delay is inversely proportional to the multisampling rate (the ratio between the sampling frequency and the switching frequency) [7-8]. The timing diagrams of two regular sampling methods are shown in Fig. 1(a) and Fig. 1(b), where T_s is the switching period and T_c is the sampling period. In the case of the multisampling (see Fig. 1(c)), the state variables are sampled and modulation signals are updated multiple times in one switching period. Therefore, the multisampling has been widely used to improve the control bandwidth of power converters including grid-connected converters [9-10], dc-dc converters [11-12], and motor drives [13-14]. In addition, some advanced control methods are combined with multisampling to further improve the control performance such as deadbeat controller [15], repetitive controller [16], hysteresis controller [17], sliding mode controller [18] and model predictive controller [19].

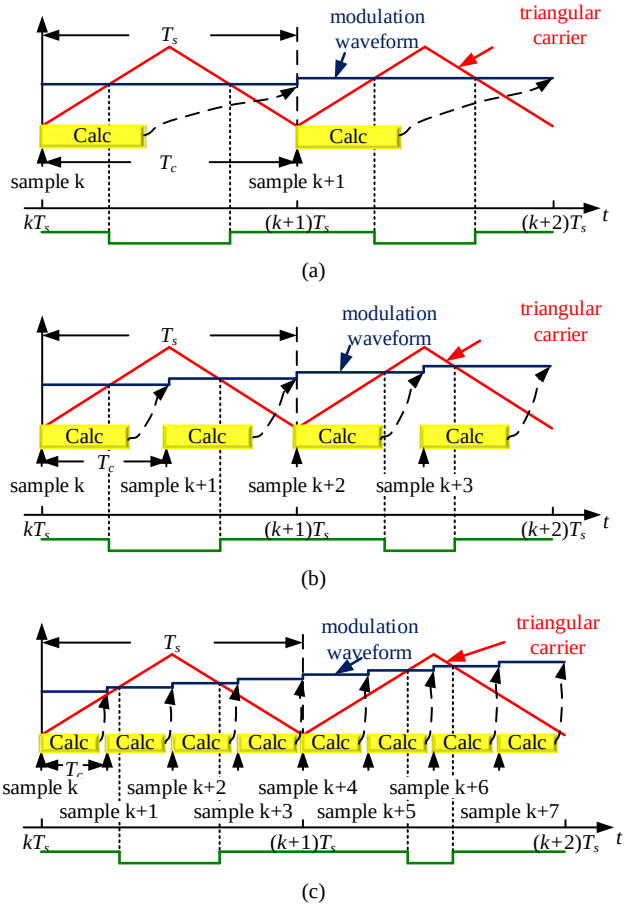

Fig. 1. Schmatic diagram and switching pattern of digital PWM. (a) single-update PWM, (b) double-update PWM, (c) four-update PWM.

Although the dynamic performance can be improved, high frequency switching harmonics (SHs) are also introduced into the control loop by the multisampling technique, which affect the whole system loop gain and cause low-order aliased

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S. He, D. Zhou and X. Wang are with the Department of Energy Technology, Aalborg University, Aalborg, Denmark (e-mail: she@et.aau.dk, zda@et.aau.dk, xwa@et.aau.dk).

F. Blaabjerg is with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. (Corresponding author, e-mail: fbl@et.aau.dk).

harmonics [20]. However, the aliasing effect of multisampled high frequency SHs on the grid-side currents is still not fully analyzed, and most researchers focus on the aliasing analysis of single/double-sampling control. Indeed, the sampling frequency in the digital control is limited, and it is always lower than twice the bandwidth of measured signals. Consequently, the aliasing is inevitable during the sampling process according to Shannon's sampling theorem. In an early stage, some simulation based analysis is presented to illustrate the aliasing phenomenon when sampling at valley/peak of carrier wave within one switching period [21-22]. In [23], based on the natural sampling SPWM, a multi-frequency PWM model is established to analyze the amplitude and phase of aliased low-order harmonics. In terms of digital PWM and sampling instant, a more general PWM model in the time domain is proposed in [24], which analytically explains the reason that sampling at valley/peak of carrier wave within one switching period can suppress aliasing and shifting sampling instant can cause severe aliasing. In order to analyze the stability in terms of aliasing, a modified PWM model in the frequency domain is proposed for a wide range of frequencies, ideally also around and above the Nyquist frequency of the converter system [25].

In this paper, the relationship between the double-update PWM and the multi-update PWM is established through geometric deduction. It is revealed that the multi-update PWM is equivalent to a double-update PWM with sampling instant shift. Then the equivalent Nyquist frequency for the multi-update PWM is equal to switching frequency, and the previous analyzing methods for the single/double-sampling aliasing can be used in the multi-update PWM. Consequently, the low-order aliased harmonics are introduced in the multi-update PWM, because the non-average value is sampled in the modulation process.

In order to suppress the aliasing, five kinds of methods are presented in the past ten years. For the interleaved converters, the equivalent switching frequency is multiple times larger than the switching frequency. If the sampling frequency is twice higher than the equivalent switching frequency, the average value can be acquired and the aliasing effect is little. For example, for the single-phase H-bridge inverter with unipolar modulation, four-sampling control can be used without sampling switching noise [26]. Similarly, the sampling rate can be four times higher than the number of cells for the cascaded H-bridge inverter [5, 27]. Moreover, the sampling rate can be twice higher than the number of cells for the interleaved dc-dc converter and modular multilevel converter [28-29]. If the sampling rate is larger than the allowable maximum sampling rate, the switching noise is also introduced. The noise-free sampling method depends on the topology of converter, and it is not suitable for single three-phase dc-ac or dc-dc converter. Second, by replacing the zero-order hold with first-order hold in the sampling process, the modulation signal is more like a continuous signal using multi-update PWM. The arbitrary sampling rate can be used with improved harmonic performance, linearity and phase delay compared with zero-order hold [30-31]. But first-order hold based sampler is still new, and the small signal stability analysis and controller design need to be further researched. Third, based on the single-edge modulator, the multisampled SHs can be compensated through an offline pre-distorted carrier. Then the aliasing error is reduced to a dc error, which is easily compensated by the feedback control [32-33]. However, the double-edge modulator is more general in grid-connected applications, and the compensation strategy for the single-edge modulator cannot be used directly. Fourth, the state variables with less switching noise are selected in the control. In [3], the capacitor current at one fourth of switching period is selected to damp the resonance. The grid-side current and capacitor voltage are recommended as the multisampled variables [4]. Fifth, the filter-based method is used widely to suppress the aliasing. For the multisampling model predictive control, the multisampled SHs are estimated with a switched model based Kalman filter [19], and the feasibility in the linear control is not reported. A multisampling average method is proposed in [23], but it is only suitable for single-update PWM and the control delay is considerable. In real-time single/double-sampling control, a high-pass filter is added into the damping loop to remove the aliased low-order harmonics and to keep the resonant component only [24, 34]. However, the multisampled SHs still exist if adding a high-pass filter, because the turnover frequency of high-pass filter should be lower than the resonant frequency. The anti-aliasing low-pass filter or moving-average filter are used in [21-22, 35-37], but the introduced delay is large and it will reduce the advantage of multisampling control. Simplified repetitive filter (SRF), among others, provides a competitive approach to filter out SHs, which utilizes the periodic nature of harmonic distortions, and does not affect the phase boost of multisampling control [20].

Unfortunately, the SRF can only remove parts of SHs, while the aliasing effects from the sampled SHs still exist. To address this challenge, an improved repetitive filter (IRF) is proposed in this work to suppress aliasing effect of the sampled SHs. This paper begins with an analysis of the relationship between double-update PWM and multi-update PWM, and the aliasing phenomenon for multi-update PWM is illustrated based on the equivalent sampling instant in Section II. Then the drawback of SRF is analyzed and the IRF is proposed in Section III to remove the sampled high frequency SHs and to suppress the aliasing. The proposed IRF using multisampling control is tested with the single-loop inverter-side current feedback control of an LCL-filtered inverter. Simulation and experimental results are provided to verify the theoretical analysis in Section IV and V, respectively. Finally, Section VI concludes this paper.

II. Aliasing Analysis in Multi-Update PWM Based on Geometric Deduction

In the multi-update PWM, although the duty ratio is updated multiple times within one switching period, not every duty ratio will intersect with the carrier and produce the effective pulse pattern [7]. Hence, it is necessary to reconsider the mechanism of multi-update PWM in order to investigate the effect of sampled SHs.

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A. *Effective Duty Ratio Analysis*

The analysis begins with the four-update PWM, because it is the most basic multi-update PWM, and the duty ratio is only updated four times within one switching period. According to the geometric principle, the amplitude of duty ratio determines the intersection position between the modulation wave and carrier wave. As shown in Fig. 2, D_1 to D_4 are the four duty ratios within one switching period. The critical range for D_1 and D_4 are (0, 0.5), and the critical range for D_2 and D_3 are (0.5, 1). That is to say, the duty ratio will intersect with the carrier if it is within the critical range, which can be defined as the effective duty ratio. For example, as shown in Fig. 2(a), D_1 and D_3 are effective duty ratios since they are in the critical range. Moreover, there are totally 16 intersection cases when considering whether all four duty ratios are in the critical range. All the cases are illustrated in Fig. 2 and Table I.

It is worth noting that there are five cases where more than two intersections happen within one switching period, as shown in Fig. 2(*l*)-(*p*). Consequently, the switch is triggered more than twice for these five cases, and the switching loss will increase compared to the double-sampling control. In order to avoid these undesired cases, the maximum rate of the change of the reference should not equal or exceed that of the carrier signal [38-39], which leads to the constraint

$$K_p \frac{0.5U_{dc}}{L_1} < 2U_{dc} f_s \tag{1}$$

where K_p is proportional coefficient in the current controller, L_1 is the inverter-side inductance, U_{dc} is the dc-link voltage, and f_s is the switching frequency. In addition, it can also be avoided through a ‘‘self-lock’’ logic in the digital signal processor [40].

On the other hand, there is another undesired phenomenon called vertical crossing, as shown in Fig. 2(*e*)-(*k*), i.e., the modulation wave crosses with the carrier wave vertically. In Fig. 2(*e*)-(*i*), the switch cannot be triggered or only be triggered once within one switching period in the real digital implementation. It indicates that there is only one effective duty ratio or no effective ratio under the vertical crossing condition. However, the modulation signal is a sinusoidal wave during the steady-state, the vertical crossing only happens in the zero crossing points of the modulation wave for the four-update PWM. Consequently, the maximum frequency of the vertical crossing occurrence is twice higher than the grid frequency. For the two cases in Fig. 2(*j*)-(*k*), if the interval between two switching is short or using a ‘‘self-lock’’ logic, the switch will be triggered only once. In addition, through the detection of vertical crossing, the vertical crossing can be avoided by forcing the PWM to output pull-up and pull-down [40], hence the above cases cannot represent the whole multi-update PWM behavior.

Although the cases in Fig. 2(*a*) and (*d*) are the normal cases, they still cannot represent the whole multi-update behavior, since both cases only happen in the zero crossing points of the modulation wave. Hence, the cases in Fig. 2(b) and (c) are the main focuses as they represent the negative half cycle and positive half cycle of the modulation wave.

TABLE I
ALL KINDS OF INTERSECTIONS AND EFFECTIVE DUTY RATIO

Case	Duty ratio range	Effective duty ratio
(*a*)	$0<D_1<0.5$, $0<D_2<0.5$, $0.5<D_3<1$, $0.5<D_4<1$	(D_1, D_3)
(*b*)	$0<D_1<0.5$, $0<D_2<0.5$, $0<D_3<0.5$, $0<D_4<0.5$	(D_1, D_4)
(*c*)	$0.5<D_1<1$, $0.5<D_2<1$, $0.5<D_3<1$, $0.5<D_4<1$	(D_2, D_3)
(*d*)	$0.5<D_1<1$, $0.5<D_2<1$, $0<D_3<0.5$, $0<D_4<0.5$	(D_2, D_4)
(*e*)	$0<D_1<0.5$, $0<D_2<0.5$, $0<D_3<0.5$, $0.5<D_4<1$	(D_1)
(*f*)	$0.5<D_1<1$, $0.5<D_2<1$, $0<D_3<0.5$, $0.5<D_4<1$	(D_2)
(*g*)	$0.5<D_1<1$, $0<D_2<0.5$, $0.5<D_3<1$, $0.5<D_4<1$	(D_3)
(*h*)	$0.5<D_1<1$, $0<D_2<0.5$, $0<D_3<0.5$, $0<D_4<0.5$	(D_4)
(*i*)	$0.5<D_1<1$, $0<D_2<0.5$, $0<D_3<0.5$, $0.5<D_4<1$	No
(*j*)	$0<D_1<0.5$, $0.5<D_2<1$, $0<D_3<0.5$, $0.5<D_4<1$	(D_1, D_2)
(*k*)	$0.5<D_1<1$, $0<D_2<0.5$, $0.5<D_3<1$, $0<D_4<0.5$	(D_3, D_4)
(*l*)	$0<D_1<0.5$, $0.5<D_2<1$, $0.5<D_3<1$, $0.5<D_4<1$	(D_1, D_2, D_3)
(*m*)	$0<D_1<0.5$, $0.5<D_2<1$, $0<D_3<0.5$, $0<D_4<0.5$	(D_1, D_2, D_4)
(*n*)	$0<D_1<0.5$, $0<D_2<0.5$, $0.5<D_3<1$, $0<D_4<0.5$	(D_1, D_3, D_4)
(*o*)	$0.5<D_1<1$, $0.5<D_2<1$, $0.5<D_3<1$, $0<D_4<0.5$	(D_2, D_3, D_4)
(*p*)	$0.5<D_1<1$, $0.5<D_2<1$, $0.5<D_3<1$, $0<D_4<0.5$	(D_1, D_2, D_3, D_4)

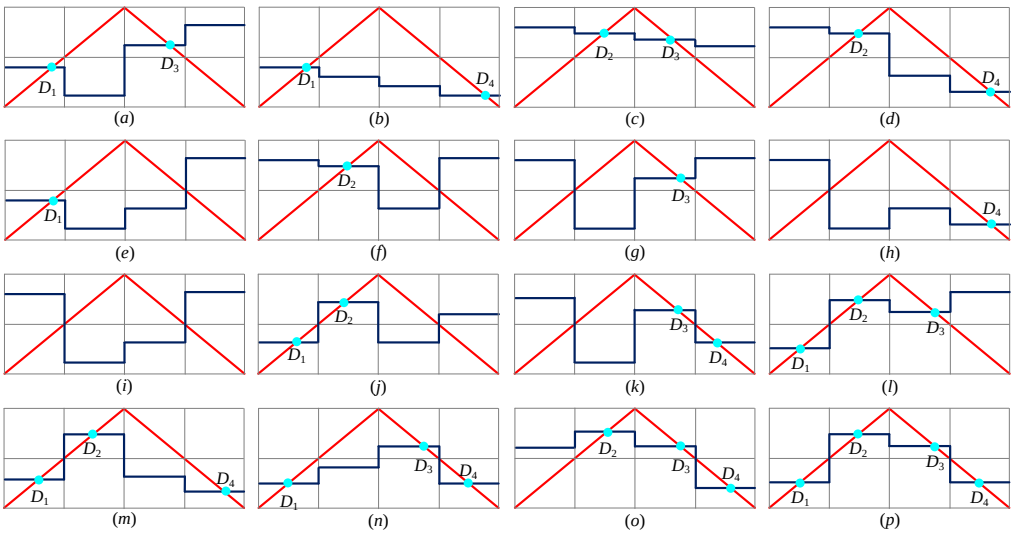

Fig. 2. All possible interseption cases between modulation wave and carrier wave in case of four-update PWM.

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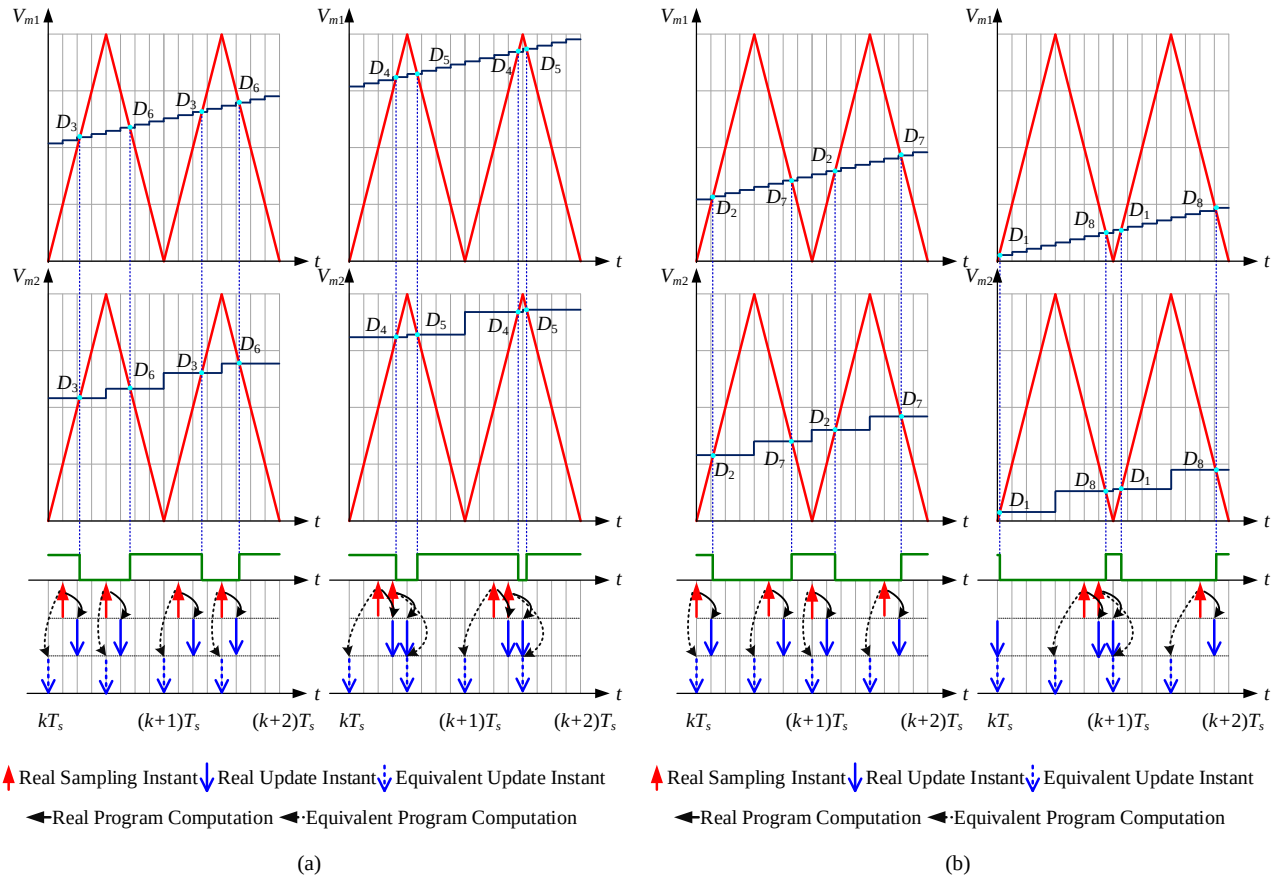

Fig. 3. The relationship between double-update PWM and eight-update PWM. (a) Positive half cycle, (b) Negative half cycle.

In order to fully exploit the advantage of multisampling, the sampling rate can be set from eight to sixteen [38]. Therefore, a more general analysis of multi-update PWM behavior with a higher sampling rate is necessary. Taking an eight-sampling PWM as an example, where the duty ratio is updated eight times within one switching period. As shown in Fig. 3, there are four critical duty ratio ranges which determine the intersection position between the modulation wave and carrier wave. The critical duty ratio ranges are (0, 0.25), (0.25, 0.5), (0.5, 0.75), (0.75, 1), respectively. Hence, there are totally 4^8 intersection cases within one switching period. Similar to the analysis of the four-update PWM, the multiple intersection and vertical crossing are ignored. Moreover, since the step size of low frequency modulation wave within one sampling period is smaller than 0.25 in steady-state, most of intersection cases can be also ignored. Hence, only positive half cycle and negative half cycle are considered. The effective duty ratios in Fig. 3 are (D_3, D_6), (D_4, D_5), (D_2, D_7) and (D_1, D_8), respectively. The behavior of multi-update PWM with a higher sampling rate can also be deduced based on the geometric deduction.

B. *Aliasing Analysis*

According to the geometric deduction of multi-update PWM, there are only two effective duty ratios within one switching period. In order to analyze the aliasing, it is natural to transform the multi-update PWM into a double-update PWM. Based on the voltage-second balance principle, the duration time of the effective duty ratio can be extended to half of one switching period. Considering the positive half cycle of four-update PWM, as shown in Fig. 4(a), there is no computational delay for the duty ratio D_2, and the equivalent update instant is the same as the sampling instant. Besides, there is a $0.25T_s$ equivalent computational delay for the duty ratio D_3. As a result, the four-update PWM can be equivalent to a double-update PWM in respect to voltage-second balance principle, yet, the difference between them lies in the equivalent sampling instant. The duty ratio D_2 is calculated from the sampled value at kT_s, and no aliasing happens since the average value is sampled. However, the duty ratio D_3 is calculated from the sampled value at $(k+0.25)T_s$ instead of the beginning or at the middle of the switching period, so the non-average value is sampled and aliased with the low-order harmonics [24].

Moreover, the average computational delay in one switching period is $(0.25+0)/2=0.125T_s$. Considering the double-sampled PWM delay of $0.25T_s$, the total control delay is $0.375T_s$, which is consistent with the multisampling delay $1.5T_s/4$ [5] and validates the effectiveness of the proposed analytical method. Similarly, the effective duty ratios in the negative half cycle of the four-update PWM are D_1 and D_4, as shown in Fig. 4(b). The equivalent sampling instant is at $(k+0.75)T_s$ and $(k+0.5)T_s$, respectively. Consequently, D_4 is calculated from the average value, and sampling aliasing happens again at $(k+0.75)T_s$ for the calculation of D_1. The total control delay for the negative half cycle is also equal to $1.5T_s/4$. In other words, within a switching period, one average value and another non-average value are sampled when using the four-sampling control. Furthermore, low-order aliased harmonics are introduced in the control loop during the modulation process, leading to grid-side current distortion.

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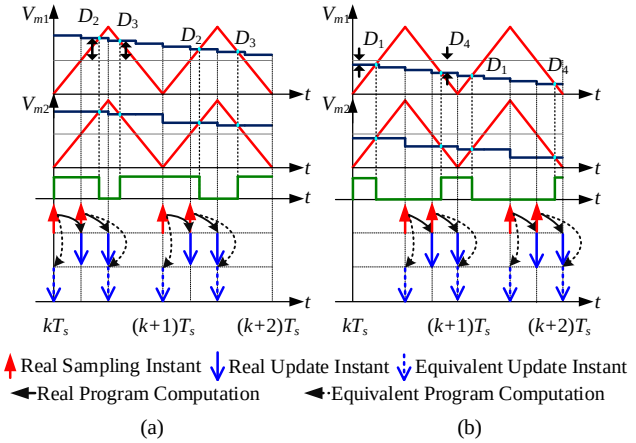

Fig. 4. The relationship between double-update PWM and four-update PWM. (a) Positive half cycle, (b) Negative half cycle.

For the eight-update PWM, the duration time of the effective duty ratios in Fig. 3 can also be extended to half of the switching period, and the eight-sampling control is equivalent to the double-sampling control. Taking Fig. 3(a) as an example, D_3 and D_6 are the effective duty ratios when the amplitude of modulation wave is from 0.5 to 0.75. The duty ratio D_3 is calculated from the sampled value at $(k+0.125)T_s$, which is not the average value and aliased low-order harmonics are introduced. On the other hand, D_6 is calculated from the sampled value at $(k+0.5)T_s$, which is the average value and no aliasing happens. It is worth noting that the equivalent update instant for D_3 is at kT_s. Hence the equivalent computational delay for the duty ratio D_3 is equal to $-0.125T_s/8$, which achieves a phase leading behavior. Similarly, the equivalent computational delay for the duty ratio D_6 is equal to $0T_s$. Hence, the average computation delay within one switching period is $(-0.125+0)/2=-0.0625T_s$. Considering the double-sampling PWM delay $0.25T_s$, the total control delay is $0.1875T_s$, which is consistent with the multisampling delay $1.5T_s/8$ [5] and validates again the effectiveness of the proposed analytical method. Further more, the equivalent sampling instants for effective duty ratios (D_4, D_5), (D_2, D_7) and (D_1, D_8) are at (($k+0.25$)T_s, ($k+0.375$)T_s), (kT_s, ($k+0.625$)T_s) and (($k+0.875$)T_s, ($k+0.75$)T_s), respectively. It can be seen that at least one effective duty ratio of eight-update PWM is calculated from the sampled non-average value, and low frequency aliased harmonics are introduced in the control loop [24]. The control delay for the other three cases is also $1.5T_s/8$.

Therefore, based on the geometrical deduction and effective duty ratio analysis, multi-update PWM is equal to the double-update PWM with a sampling instant shift. The advantage of the multi-update PWM is that it can achieve a phase leading function for some effective duty ratios, which can reduce the control delay effectively. However, the high frequency SHs are sampled in the control loop, and the aliasing happens when the multisampling control is applied, i.e., the double-sampling control with a sampling instant shift. It is thus necessary to remove the sampled SHs in order to suppress the aliasing.

III. Sampled Switching Harmonics Filtering Based Aliasing Suppression

A. Improved Repetitive Filter

In this paper, the single-loop control with inverter-side current feedback is used as a case study, and the overall control diagram is shown in Fig. 5. In terms of current control, there is always a trade-off between the bandwidth and overshoot for the proportional integral (PI) controller, which weakens the advantage of multisampling [41]. The pseudo-derivative-feedback controller is applied to substitute the PI controller in order to suppress the overshoot and improve the response speed [42]. Table II gives the parameters of a down-scale three-phase grid-connected inverter. According to the high power LCL filtered converter design [43], the inverter-side inductance, filter capacitor and grid-side inductance and is 0.11 p.u., 0.16 p.u. and 0.059 p.u. respectively. In this paper, the LCL parameters is 0.08 p.u., 0.26 p.u. and 0.08 p.u., respectively. The value of capacitor is relatively larger than the design standard, and the resonant frequency can be smaller than the one-sixth of double-sampling frequency (4000 Hz) in order to achieve the grid-side currents THD comparison between double-sampling and multisampling control.

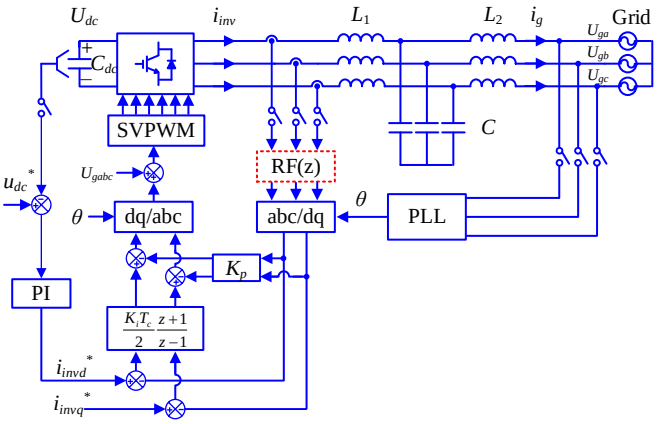

Fig. 5. Diagram of a grid-connected single-loop controlled inverter-side current feedback system (RF: repetitive filter).

TABLE II
MAIN PARAMETERS OF GRID-CONNECTED INVERTER

Symbol	Description	Value	Symbol	Description	Value
U_{grms}	Grid voltage	220 V	P_o	Output power	7 kW
L_1	Inverter-side inductor	5 mH	L_2	Grid-side inductor	5 mH
C	Filter capacitor	40 μF	C_{dc}	DC-link capacitor	297 μF
f_r	Reasonance frequency	503 Hz	U_{dc}	DC-link voltage	600 V
f_s	Switching frequency	2 kHz	T_f	DC-link filter time constant	1 ms
K_{p8}	Proportional coefficient	15.6	K_{i8}	Integral coefficient	5050
K_{p2}	Proportional coefficient	6.6	K_{i2}	Integral coefficient	600
K_{pdc}	Proportional coefficient	0.03	K_{idc}	Integral coefficient	0.4

As shown in Fig. 6, when the reference current is set to 15 A (the rated current), the eight-sampled inverter-side current without filter contains high frequency SHs around odd-order

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and even-order SHs (2 kHz, 4 kHz and 6 kHz). These sampled SHs will cause aliasing, and a simplified repetitive filter (SRF) with low phase lag is used in an active power filter to remove them [20]. The expression of the SRF in the discrete domain is given as

$$SRF(z) = \frac{1}{2}(1 + z^{-N/2}) \tag{2}$$

where N is the multisampling rate. When N is eight, it can be seen from the bode diagram of SRF in Fig. 7 that SRF can remove the SHs around odd-order SHs (2 kHz and 6 kHz), where f_c is the sampling frequency. However, the SHs around even-order SHs (4 kHz) cannot be removed, as shown in Fig. 8, and the aliasing still exists. Hence SRF is only suitable for four-sampling control and only SHs around 2 kHz need to be removed. Moreover, the ability of SRF in removing SHs will be weaker with the increase of multisampling. For example, only the SHs around 2 kHz, 6 kHz and 10 kHz and 14 kHz can be removed when the multisampling rate reaches sixteen.

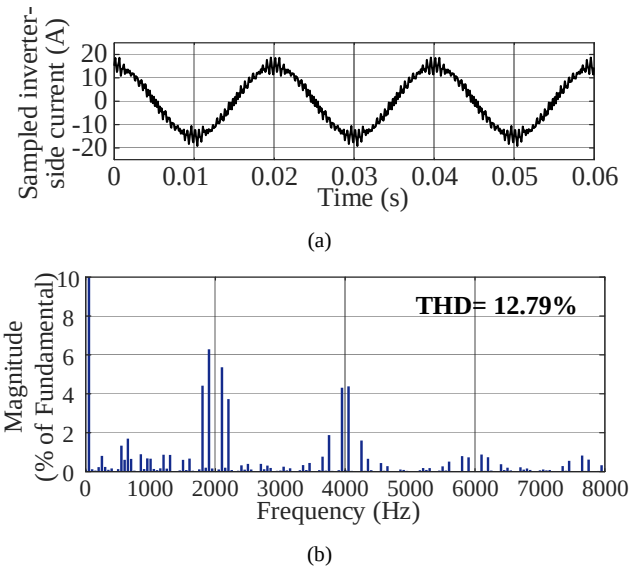


Fig. 6. The eight-sampled inverter-side current without any filter. (a) Sampled inverter-side current waveform, (b) Current spectrum.

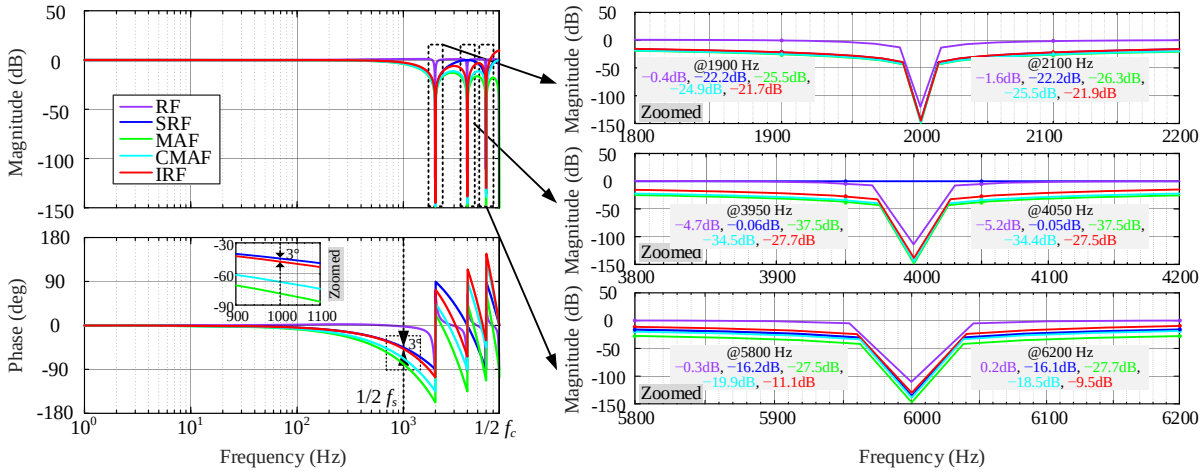


Fig. 7. The bode diagram of the repetitive filters based on eight-sampling (RF: repetitive filter, SRF: simplified repetitive filter, MAF: moving average filter, CMAF: compromised moving averaging filter, IRF: improved repetitive filter).

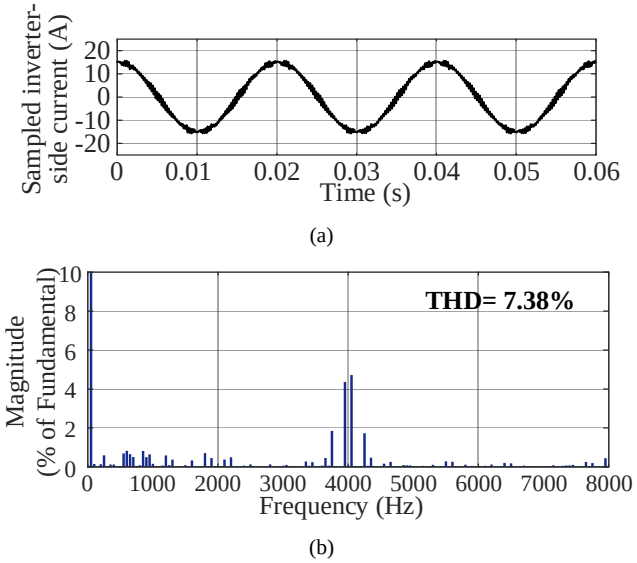


Fig. 8. The eight-sampled inverter-side current with SRF. (a) Sampled inverter-side current waveform, (b) Current spectrum.

The repetitive filter (RF) uses all the sampled data within one switching period based on internal model principle, as shown in (3), and it introduces a low phase lag. But it is only effective at interger switching frequency such as 2 kHz, 4 kHz and 6 kHz, as shown in Fig. 7. Actually, the sampled switching harmonics are side-band harmonics, i.e., 1900 Hz, 2100 Hz, etc, and RF in [20] is not as effective as SRF in AC applications. The most effective repetitive filter is moving average filter (MAF) with a window equal to one switching period, as shown in (4). But moving average filter introduces a delay equal to $T_s/2$, which is fully equivalent to the single-sampling PWM delay, thus loosing any possible advantages of the multisampling solution in terms of phase boost [35]. Therefore, a compromised moving average filter (CMAF) is proposed, and the size of the window reduces from one to half of switching period, as shown in (5). It can be seen from Fig. 7 that there is still a delay from CMAF compared with SRF, hence a linear delay compensation block [44] is inserted after CMAF, i.e., improved repetitive filter (IRF), as shown in (6). Consequently, IRF can not only remove the sampled even order and odd order switching harmonics, but it also has a similar phase lag with SRF.

$$RF(z) = \frac{(1+0.25)(1-(z^{-N}-\frac{1}{N}\sum_{n=1}^{N}z^{-n}))}{1-(z^{-N}-\frac{1}{N}\sum_{n=1}^{N}z^{-n})+0.25} \quad (3)$$

$$MAF(z) = \frac{1}{N}\sum_{k=0}^{N-1}z^{-k} \quad (4)$$

$$CMAF(z) = \frac{2}{N}(1+z^{-2}+z^{-4}+\cdots z^{-(N-2)}) \quad (5)$$

$$IRF(z) = \frac{2}{N}(1+z^{-2}+z^{-4}+\ldots z^{-(N-2)}) \times(3\log_2 N-7-(3\log_2 N-8)z^{-1}) \quad (6)$$

Taking eight-sampling as an example, SRF and CMAF in low frequency range can approximately be

$$CMAF(z)_{N=8} = \frac{1}{4}(1+z^{-2}+z^{-4}+z^{-6}) \approx z^{-3} \quad (7)$$

$$SRF(z)_{N=8} = \frac{1}{2}(1+z^{-4}) \approx z^{-2} \quad (8)$$

The linear delay compensation block is

$$G_{com}(z) = 1+\frac{T_d}{T_c}-\frac{T_d}{T_c}z^{-1} \quad (9)$$

It can be seen that one-step control delay needs to be compensated in the eight-sampling control, and T_d can be set as T_c, and the expression of IRF is given as

$$IRF(z)_{N=8} = \frac{1}{4}(1+z^{-2}+z^{-4}+z^{-6})(2-z^{-1}) \quad (10)$$

Hence, the general IRF can be deduced in terms of control delay and sampling rate, as shown in (6). According to Fig. 7 and Fig. 9, IRF can remove all the SHs around 2 kHz, 4 kHz and 6 kHz. Moreover, IRF shows almost same frequency characteristic with SRF below half of the switching frequency (1000 Hz), which is usually the main frequency range of concern in terms of current control bandwidth [45].

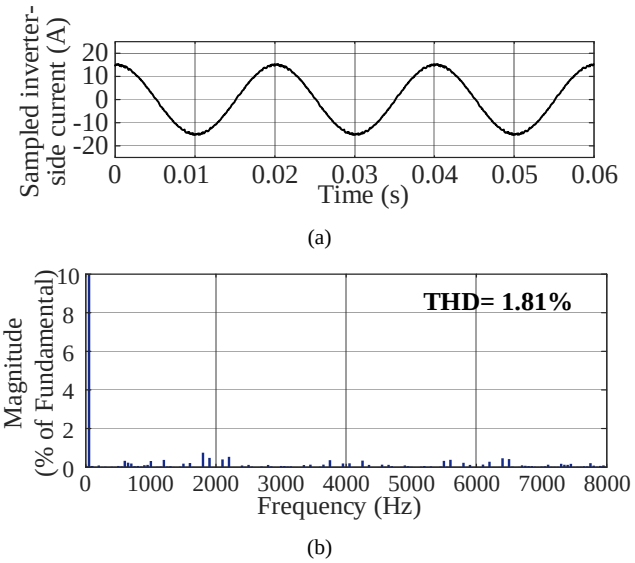


Fig. 9. The eight-sampled inverter-side current with IRF. (a) Sampled inverter-side current waveform, (b) Current spectrum.

B. Current Controller Design

According to Fig. 10, the open-loop transfer function of the inner loop of the current loop is

$$T_{oin}(s) = K_p IRF(s)G_d(s)G_{i1v}(s) \quad (11)$$

where $IRF(s) = \frac{1-e^{-8sT_c}}{1-e^{-2sT_c}}(\frac{1}{2}-\frac{1}{4}e^{-sT_c})$, $G_d(s) = e^{-1.5sT_c}$, $G_{i1v}(s) = \frac{L_2Cs^2+1}{L_1L_2Cs^3+(L_1+L_2)s}$. It is worth noting that the stability of the inner loop is the same as the PI based single-loop control, and the bandwidth of the whole current loop is determined by the inner loop bandwidth and integral coefficient K_i. According to the bandwidth oriented controller design, the open-loop bandwidth of the inner loop can be set as 1/10 of the switching frequency (200 Hz) and the value of eight-sampling proportional control coefficient K_{p8} can be determined [45]. Then the eight-sampling integral control coefficient K_{i8} gradually increases until the overshoot is within 5%. On the other hand, due to the large control delay ($0.75T_s$) in the double-sampling control, the open-loop bandwidth of the inner loop can only be set as 1/20 of the switching frequency (100 Hz). The double-sampling control coefficients K_{p2} and K_{i2} can be seen in Table II: In addition, the first-order low pass filter is added to the voltage control loop and its time constant is set as 1 ms. The bode diagram of the open-loop transfer function of the inner loop is shown in Fig. 11. As a result, the phase margin (PM) for the double-sampling control is 12.8° (PM_1), and the PM for other two controllers are 36.2° (PM_2) and 34.6° (PM_3). Therefore, the eight-sampling controller with IRF not only achieves larger PM and higher bandwidth than the double-sampling controller, but also remove all the SHs compared with SRF. Moreover, there is only 1.6° decrease in PM of the eight-sampling controller with IRF than that with SRF.

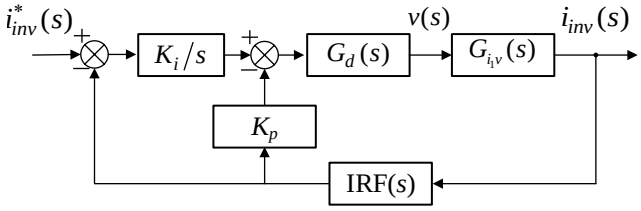


Fig. 10. Block diagram of the single-loop control.

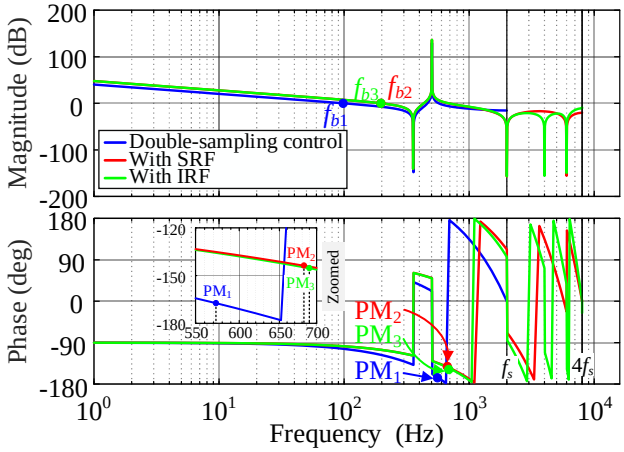


Fig. 11. Bode diagram of the inner loop with different repetitive filters (SRF: simplified repetitive filter, IRF: improved repetitive filter).

IV. Simulation Results

In order to illustrate the effectiveness of aliasing analysis and the advantage of the proposed IRF in aliasing suppression, the reference current steps from 7.5 A to 15 A (rated current), and the multisampling factor is set to eight. The parameters of controller are shown in Table II. As shown in Fig. 12(a) and Fig. 13(a), the eight-sampling controller without filter show better dynamic performance than the double-sampling controller. However, high frequency SHs are introduced in the control loop, as shown in Fig. 12(b) and Fig. 13(b). As a result, the THD of the grid-side current of the eight-sampling controller without a filter is 3.16% (see Fig. 13(c)), and there are some low-order aliased harmonics compared with the double-sampling controller (see Fig. 12(c)).

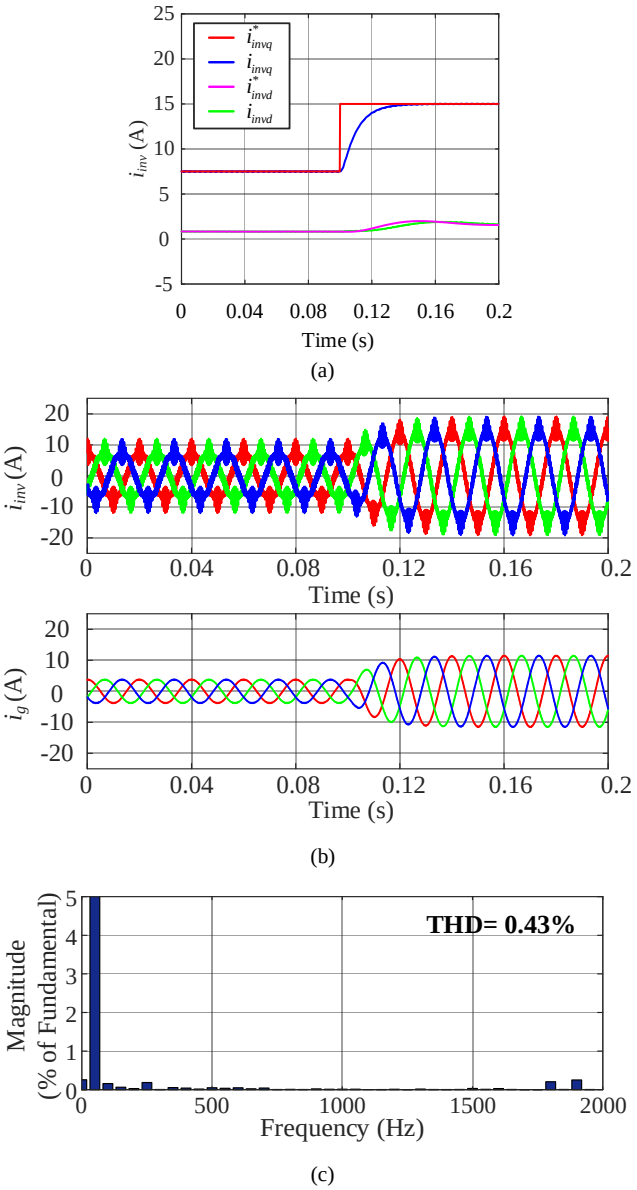


Fig. 12. Double-sampling control. (a) Step response, (b) Real-time inverter-side and grid-side current, (c) THD of grid-side current.

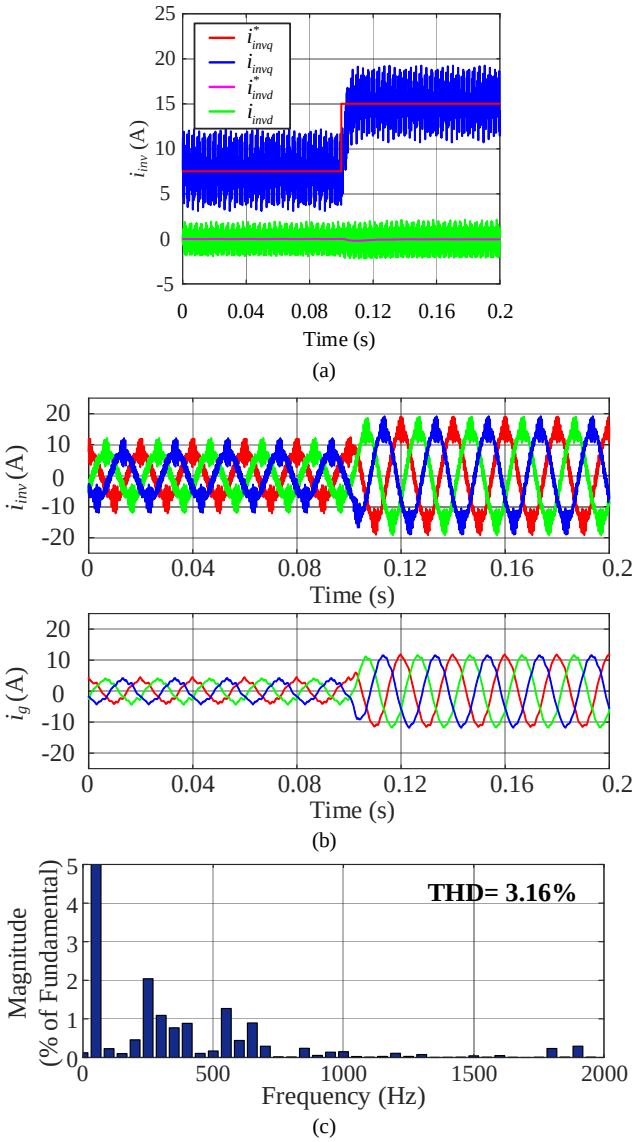


Fig. 13. Eight-sampling control without filter. (a) Step response, (b) Real-time inverter-side and grid-side current, (c) THD of grid-side current.

When using the SRF and the same eight-sampling control parameters, the aliasing still exists because the SHs around 4 kHz cannot be removed, as shown in Fig. 14(a) and Fig. 8. It is worth noting that the aliased low-order harmonics are more severe than the eight-sampling control without filter, and the THD of grid-side current increases from 3.16% to 4.49% (see Fig. 13(c) and Fig. 14(c)). Because IRF can remove all the SHs (see Fig. 15(a)), the low-order aliased harmonics are suppressed. As shown in Fig. 15(c), the THD of grid-side current is 0.78%, which is similar with the double-sampling control (see Fig. 12(c)). Therefore, the eight-sampling control with IRF not only has better dynamic performance compared to the double-sampling control, but also suppresses the aliasing and leads to a good grid-side current quality.

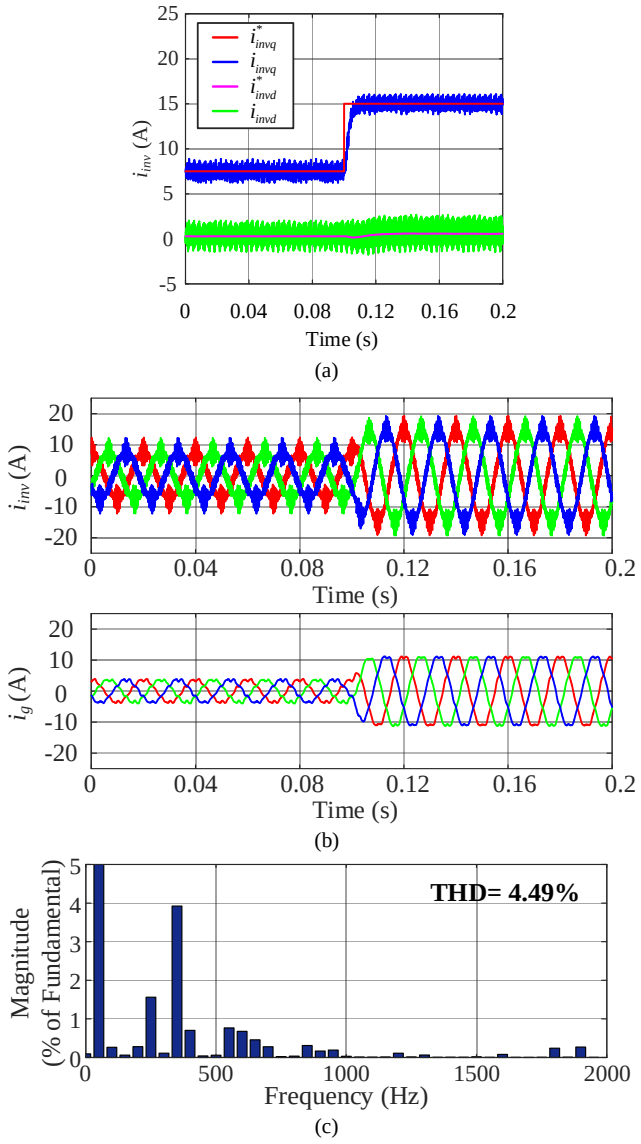
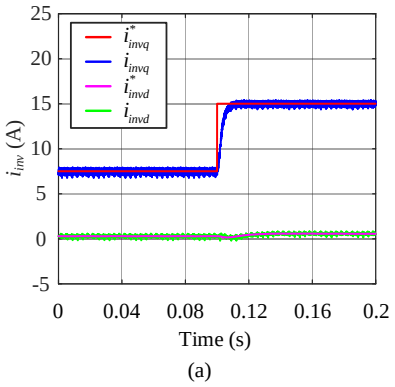


Fig. 14. Eight-sampling control with SRF (SRF: simplifed repetivie filter). (a) Step response, (b) Real-time inverter-side and grid-side current, (c) THD of grid-side current.



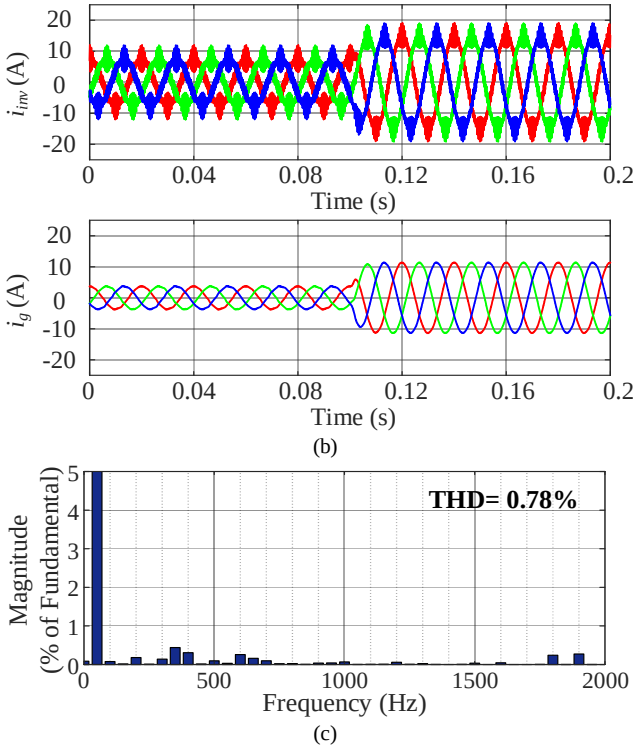


Fig. 15. Eight-sampling control with IRF (IRF: improved repetitive filter). (a) Step response, (b) Real-time inverter-side and grid-side currents, (c) THD of grid-side current.

V. Experimental Validation

To further verify the theoretical analysis, experiments are carried out in a down-scaled three-phase grid-connected inverter with an LCL filter, as shown in Fig. 16. The grid is emulated with a Chroma Grid Simulator Model 61845. The applied half-bridge module and the control platform are a PEB-8024 module and a B-BOX RCP control platform from Imperix, respectively. The used current sensor is LEM CKSR 50-P with a bandwidth of 300 kHz. The THD of grid-side current is measured through the Newtons-4th PPA5530 power analyzer. The experimental parameters for the setup can be seen in Table II.

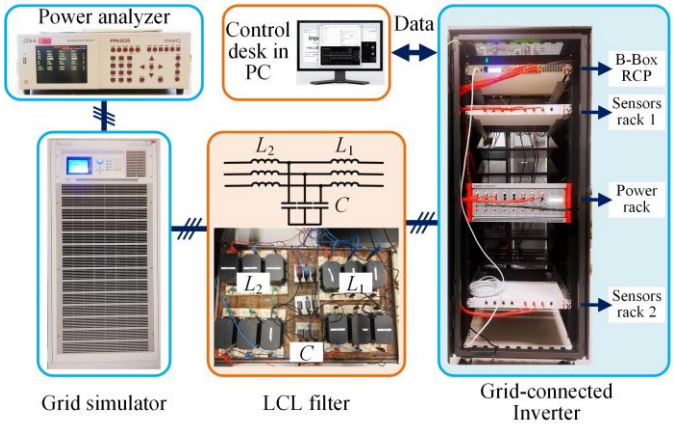
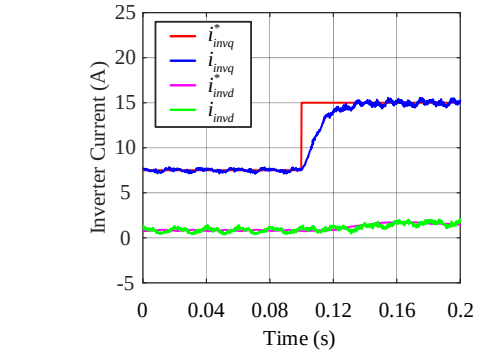


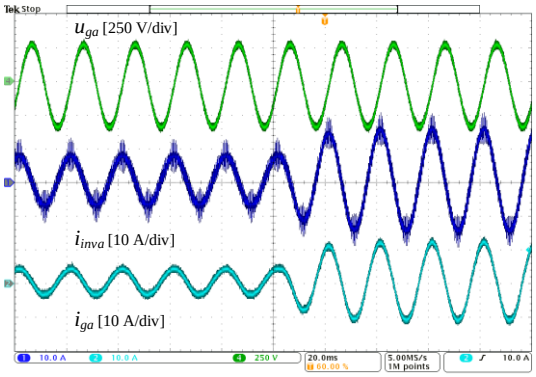
Fig. 16. Down-scaled three-phase grid-connected inverter.

The experimental result from double-sampling control is shown in Fig. 17, and its THD of grid-side current is 1.01%. When using the eight-sampling control without the filter, as shown in Fig. 18(a), the step response is faster than the double-sampling control. However, high frequency SHs are

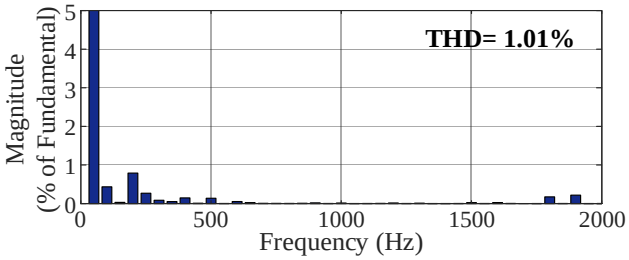
introduced and low-order aliased harmonics are introduced in the grid-side current. It can be seen from Fig. 18(b)-(c) that the THD of grid-side current increases from 1.01% to 2.96%, which is consistent with the theoretical analysis.



(a)

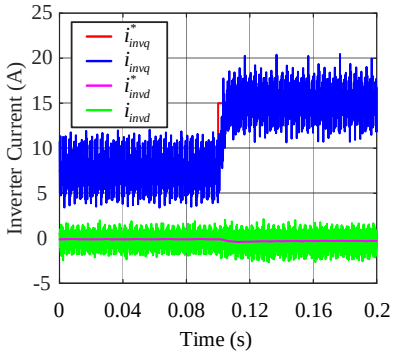


(b)

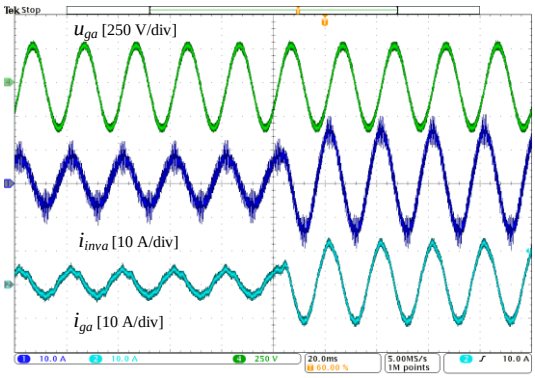


(c)

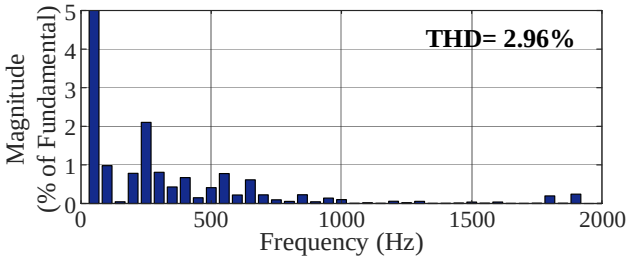
Fig. 17. Experimental results with the double-sampling control. (a) Step response, (b) Inverter-side and grid-side current, (c) THD of grid-side current.



(a)



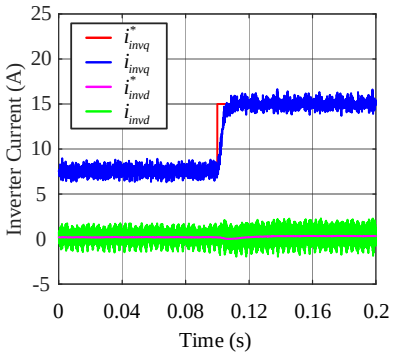
(b)



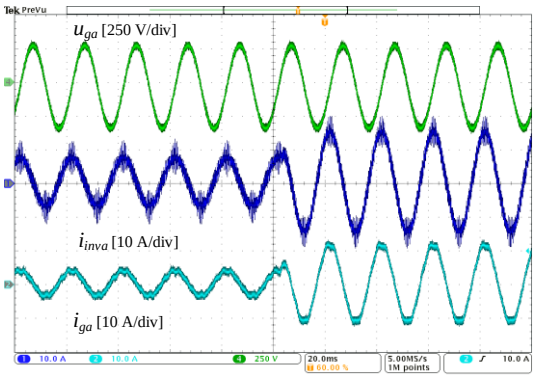
(c)

Fig. 18. Experimental results with the eight-sampling control without the filter. (a) Step response, (b) Inverter-side and grid-side current, (c) THD of grid-side current.

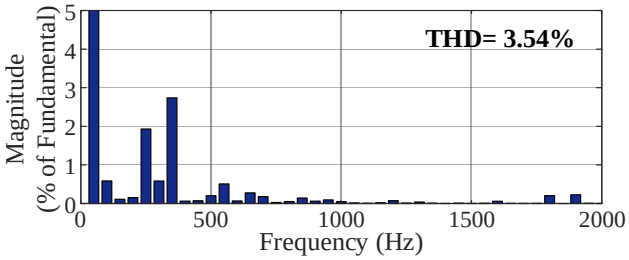
For the eight-sampling control with the SRF, as shown in Fig. 19(a), the switching noise still exists in the control loop. The THD of grid-side current is 3.54% (see Fig. 19(c)), which is larger than the eight-sampling control without the filter (see Fig. 18(c)). Because the proposed IRF can remove all the SHs, the aliased low-order harmonics are suppressed and the THD of grid-side current is 1.10% (see Fig. 20(c)), which is similar with the double-sampling control (see Fig. 17(c)). Moreover, the eight-sampling control with the IRF achieves a faster step response than the double-sampling control (see Fig. 20(a) and Fig. 17(a)). Overall, the eight-sampling controller with IRF can not only suppress the aliasing, but also keep the advantage of fast dynamic performance.



(a)

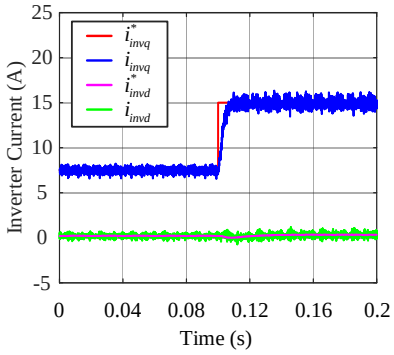


(b)

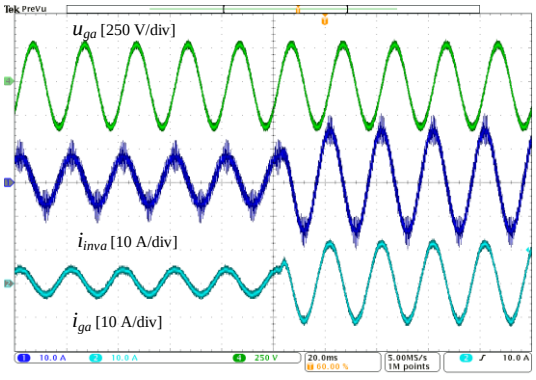


(c)

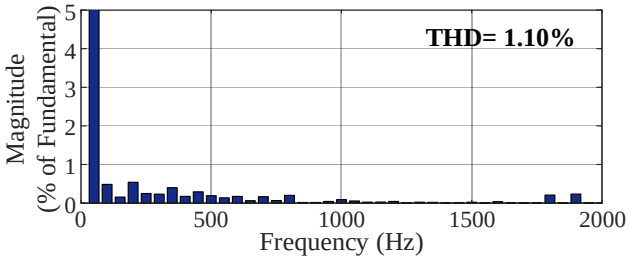
Fig. 19. Experimental results with the eight-sampling control with SRF. (a) Step response, (b) Inverter-side and grid-side current, (c) THD of grid-side current.



(a)



(b)



(c)

Fig. 20. Experimental results under eight-sampling control with the IRF. (a) Step response, (b) Inverter-side and grid-side current, (c) THD of grid-side current.

VI. Conclusion

This paper starts with the investigation of the multi-sampled high frequency SHs effect on the grid-side current distortion. Through the geometric deduction, the multi-update PWM can be transformed into a double-update PWM with the sampling instant shift. As a result, non-average values are used for the calculation of duty ratio within a switching period. Then low-order aliasing happens in the modulation process, which leads to distorted grid-side current. Moreover, an IRF is proposed to remove all the SHs and suppress the aliasing, where the SRF is also used for comparison. Compared with the double-sampling control, the multisampling control with the IRF not only has better dynamic performance and higher bandwidth, but also has low THD for the grid-side current and without aliasing. Finally, the theoretical analysis is verified through the simulation and experiment.

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