IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 17, 2020, accepted February 14, 2020, date of publication March 2, 2020, date of current version March 11, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2977861

All-Digital Mismatched Calibrator and Compensator for SR Latch-Based Variable-Gain Time Amplifier

KUAN-CHIEH CHAO, JUNG-CHIN LAI, AND TERNG-YIN HSU, (Member, IEEE)
Department of Computer Science, National Chiao Tung University, Hsinchu 30010, Taiwan

Corresponding author: Terng-Yin Hsu (tyhsu@cs.nctu.edu.tw)

This work was supported by the Center for Open Intelligent Connectivity from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan.

ABSTRACT Two major mismatches in SR latch-based time amplifiers (TA) include input skew, which causes gain imbalance, and loading mismatch, which reduces gain accuracy. Accordingly, we propose an all-digital mismatched self-calibrator and compensator for an SR latch-based variable-gain TA. Tunable matching cells and variable capacitors are built into TAs to compensate for input skew (gain imbalance) and loading mismatch (gain inaccuracy). To ensure that the proposed calibration works efficiently and accurately, the TA must provide at least high and low gains where the low gain calibrates the most significant bit (MSB) and the high gain calibrates the least significant bit (LSB). This self-calibrator costs 4375 gates, and the power consumption is 2.8 mA for the TA gain with 2 and 3.2 mA for the TA gain with 16 at a sampling rate of 10 MHz.

INDEX TERMS Mismatch calibration, self-calibration, time amplifier.

I. INTRODUCTION

Time amplifiers (TAs) are widely used for time interval measurements in time-to-digital converters (TDCs), time-of-flight (TOF) [1]–[5], analog-to-digital converters [6] [7], and all-digital phase-locked loop (ADPLL) [8]–[11] applications. TAs are used for built-in jitter measurement [12], amplifying the time interval of the jitter and enhancing the resolution. TAs also amplify the measured input interval of the TDC [13], [14]. Several types of TAs have been developed. One is based on differential difference amplifiers in a unity gain buffer configuration [15], which improves input range and gain. 4X TAs [16], [17] use delay cells for different features whose gain is controlled by closed loops. A pulse train time amplifier [18], [19] uses repetitive pulses with a gated delay line to support a programmable gain with quantization. An all-digital time amplifier with interpolation [20] is created using a quantization scheme with an adjustable loading cap, which achieves low gain variation. A CMOS TA [21] achieves dynamic gain, and controls the tail current to yield an output pulse range that spans from a few hundred femtoseconds to a few hundred picoseconds. The architecture of an SR latch-based TA consists of two SR latches [11], input delay T_{OFF}, and an output capacitor. The extending time of the metastable state is used to amplify the time interval. However, that gain is influenced by input skew and loading mismatch where the input skew causes gain imbalance and the loading mismatch induces gain inaccuracy—calibration is important to maintain matching and to minimize gain error. Several calibration methods have been reported to maintain constant gain and reduce gain non-linearity. A lookup table [22] can be established to reduce gain non-linearity in calibrations. To deal with PVT variation, the loading capacitance [23] is changed simultaneously and increased if a higher gain is required.

As illustrated in Fig. 1, the proposed architecture includes a tunable matching cell, a pulse-width arbiter, a tunable capacitor, a calibration controller, a skew calibrator, a load calibrator, a SR-latch based TA, and a TDC. The variable-gain TA is the core of the entire architecture, and the calibrator is used to measure and calibrate the result of time amplification in the calibration process. In the calibration process, both the calibration controller and the skew calibrator are used to calibrate input skew. The pulses are generated by the calibration controller. After these pulses are amplified by the TA, the amplified pulses which indicate the amplification rate are compared using the skew calibrator. Subsequently, the tunable matching cell in the TA compensates for the skew of the input delay. The pulse-width arbiter selects an appropriate gain for each input interval. The loading calibrator and

The associate editor coordinating the review of this manuscript and approving it for publication was Wei Liu.

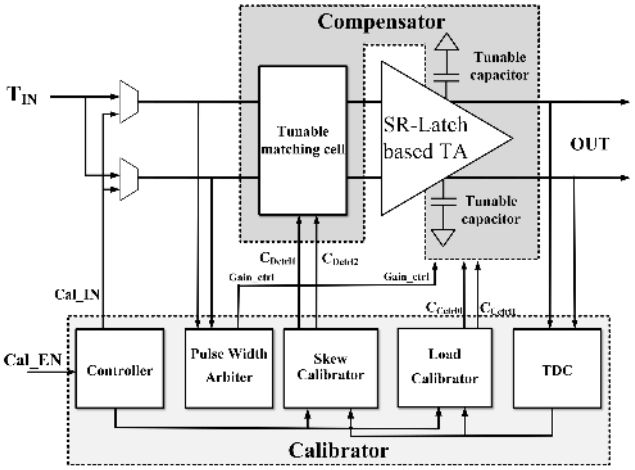


FIGURE 1. Block diagram of proposed architecture.

tunable capacitor are used to adjust the TA gain for the PVT variation. If the gain is less than the target, the load calibrator changes the control code (C_{Cctrl0}) to reduce the capacitance C_0 for a higher gain. In contrast, the capacitance C_1 is reduced for a lower gain by changing the control code (C_{Cctrl1}). The calibration procedure includes skew and gain calibration. The load capacitance calibrator adjusts the capacitance to achieve the proposed target for PVT variation. The calibration design does not require high-resolution TDCs: a simple TDC [31] is used in our circuit.

This paper is organized as follows. In Section II we analyze the input delay skew and capacitance mismatch in previous TAs. We explain in Sections III and IV the proposed self-calibration scheme and its implementation, and in Section V we discuss the simulation results. We conclude in Section VI.

II. TA MISMATCHES

A. IDEAL CHARACTERISTIC

Figures 2(a) and (b) show an SR latch-based TA scheme [11] along with the timing diagram for T_{IN} vs. T_{OUT}, which is obtained by

$$T_{IN} = TA_{IN2} - TA_{IN1} \tag{1}$$

$$T_{OUT} = TA_{OUT2} - TA_{OUT1}. \tag{2}$$

The SR latch-based TA contains two pairs of SR latches, each of which is connected to a T_{OFF} delay chain. The length of the delay chain determines the input range of the pulse. The longer T_{OFF} has a wider input range but a smaller gain as a tradeoff. The output of the NAND gate in an SR latch is connected with an additional capacitor that is related to the TA gain; a larger capacitance gives a larger gain.

When the SR latch starts up [24], [25], TA_{IN1} and TA_{IN2} are in the 0 state; S1 (and S2) and R1 (and R2) are in the 1 state; passing by the XOR gates, the OUTs (TA_{OUT1} and TA_{OUT2}) are in the 0 state. The input pulse T_{IN} is generated when TA_{IN1} and TA_{IN2} sequentially transition from 0 to 1 to make

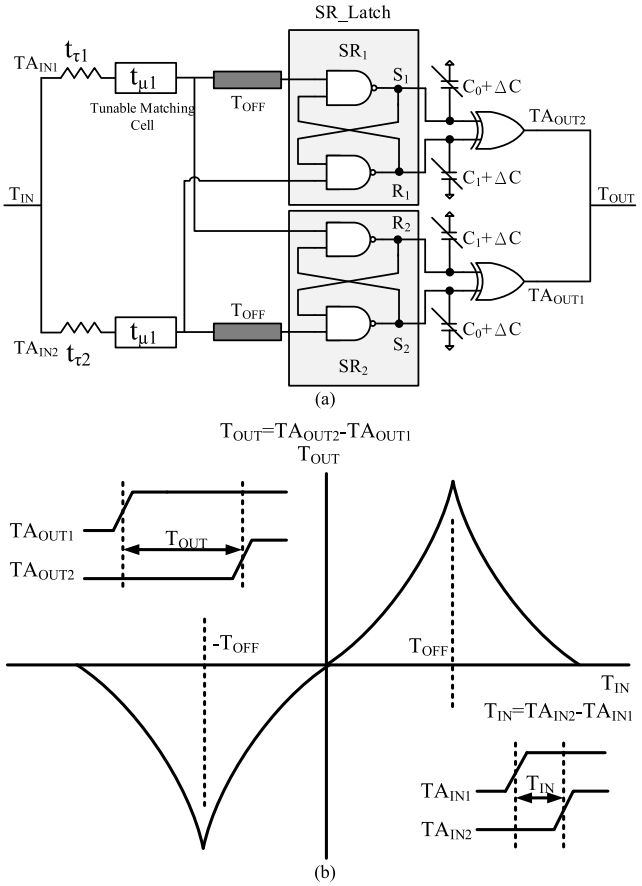


FIGURE 2. SR latch-based TA: (a) schematic and (b) timing characteristic of T_{IN} vs. T_{OUT}.

up the interval of time. During the development, the output of the NAND gate transitions and the SR latch goes into the metastable state. Consequently, the output pulse T_{OUT} is obtained when TA_{OUT1} and TA_{OUT2} both transition from 0 to 1 in the interval of time. If the input pulse T_{IN} is in the range 0–T_{OFF}, the transition of TA_{IN1} is quicker than that of TA_{IN2}, but TA_{IN1} arriving in the component SR_1 is slower than TA_{IN2} owing to the timing delay of T_{OFF}. The longer the interval T_{IN}, the longer the time spent in the metastable state as well as the longer T_{OUT}. If $T_{IN} > T_{OFF}$, the longer T_{IN} increases the interval between TA_{IN1} and TA_{IN2} arriving at SR_1, whereas the metastable time and T_{OUT} are shorter. The timing diagram of T_{IN} vs. T_{OUT} is given in Fig. 2(b).

$$-T_{OFF} < T_{IN} < T_{OFF} \tag{3}$$

The input range of T_{IN} is between $-T_{OFF}$ and T_{OFF}. The TA equation is derived as follows [26], [27]:

$$T_{OUT} = (C/g_m) \cdot [log\,(T_{OFF} + T_{IN}) - log\,(T_{OFF} - T_{IN})] \tag{4}$$

where C is the capacitance of loading at the output side of the NAND gate and g_m is the transconductance of a NAND gate in the metastable state. The larger capacitance C and shorter T_{OFF} result in larger gain. Although we require a larger gain, inserting too many capacitors causes an increase in the area. Similarly, a larger range for the input interval is preferable,

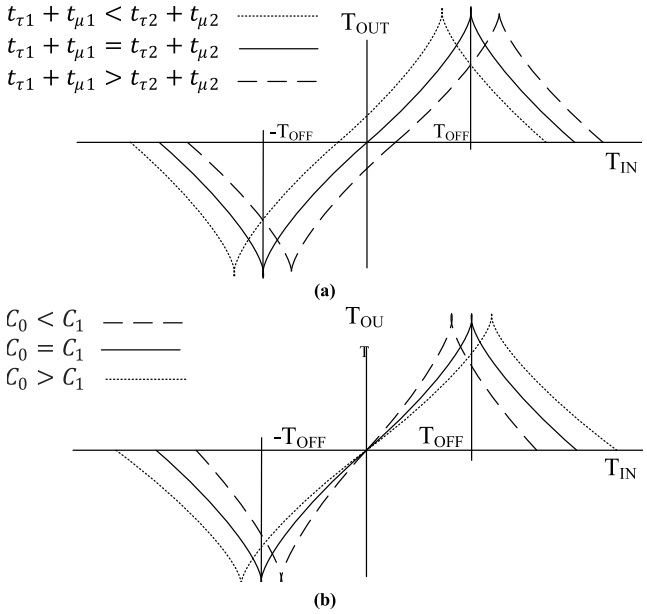


FIGURE 3. T_{IN} vs. T_{OUT} curve: (a) input delay matching on both sides of SR latch and (b) impact of capacitance mismatch of SR latch.

but increasing the delay chain of T_{OFF} to achieve this results in a smaller gain.

B. GAIN IMBALANCE

Fig. 3(a) describes the timing diagram of T_{IN} vs. T_{OUT} when considering input delay matching. The timing $t_{\tau1}$ is the time delay of the routing path for the input signal TA_{IN1}; the timing $t_{\tau2}$ is the time delay of the routing path for the input signal TA_{IN2}. The timing $t_{\mu1}$ is the compensated time by the tunable matching cell of input path TA_{IN1}; the timing $t_{\mu2}$ is the compensated time by the tunable matching cell of input path TA_{IN2}. During PR implementation, if $t_{\tau1}$ and $t_{\tau2}$ are not well-matched, the gains in the input range $T_{IN} > 0$ and $T_{IN} < 0$ are inconsistent. This is a general problem with routing between system-on-a-chip (SoC) IPs. Unmatched routing paths influence the consistency of the TA's gain. Matching cells compensate for and reduce the effect caused by routing skew. After calibration, we achieve a consistent gain in the entire input range, that is, the linearity error of the T_{IN}–T_{OUT} curve is quite small. If the routing matching is not as good as expected, the routing skew before calibration is as follows:

$$t_{\tau1} + t_{\mu1} \neq t_{\tau2} + t_{\mu2} \tag{5}$$

The input routing skew is discussed below:

1. If the total delay of the input path on the TA_{IN1} side is less than that on the TA_{IN2} side, as described by (6), the T_{IN}–T_{OUT} curve shifts left; that is, the gain in the input range $T_{IN} > 0$ is greater than the gain in the input range $T_{IN} < 0$.

$$t_{\tau1} + t_{\mu1} < t_{\tau2} + t_{\mu2} \tag{6}$$

2. If the input delay on the TA_{IN1} side is greater than the input delay on the TA_{IN2} side, as described by (7), the T_{IN}–T_{OUT} curve shifts right; that is, the gain in the input range $T_{IN} > 0$ is less than the gain in the input range $T_{IN} < 0$.

$$t_{\tau1} + t_{\mu1} > t_{\tau2} + t_{\mu2} \tag{7}$$

3. If the input delay on the TA_{IN1} side is equal to the delay on the TA_{IN2} side, as described by (8), the T_{IN}–T_{OUT} curve passes through the origin; that is, T_{OUT} is 0 if $T_{IN} = 0$. The gain in the input range $T_{IN} > 0$ is equal to the gain in the input range $T_{IN} < 0$.

$$t_{\tau1} + t_{\mu1} = t_{\tau2} + t_{\mu2} \tag{8}$$

C. GAIN INACCURACY

The capacitance of loading at the output side of the SR latch (C_0 and C_1) influences the TA gain. The larger value of capacitance increases the gain owing to a longer metastable time [22]. The relation of C_0 and C_1 also decides the gain and input range, as shown in Fig. 3(b).

If $C_0 = C_1$, the gain and input range are as discussed in the previous subsection; the gain is G, and the input ranges from $-T_{OFF}$ to T_{OFF}.

1. If $C_0 < C_1$, the gain is G_1, and the input ranges from $-T_{OFF1}$ to T_{OFF1}. $G_1 > G$, and $T_{OFF1} < T_{OFF}$.
2. If $C_0 > C_1$, the gain is G_2, and the input ranges from $-T_{OFF2}$ to T_{OFF2}. $G_2 < G$, and $T_{OFF2} > T_{OFF}$.

When $C_0 < C_1$, the load capacitance at R_1 is larger than that at S_1. In the valid input range $0 < T_{IN} < T_{OFF}$, the signal TA_{IN2} that arrives at R_1 is faster than the signal TA_{IN1} that arrives at S_1. The closer timing between the transition from R_1 to S_1 results in a longer metastable time and a larger TA_{OUT2} latency. At the other side, the signal TA_{IN1} that arrives at R_2 is much faster than the signal TA_{IN2} that arrives at S_2, and the timing of TA_{OUT1} is only slightly influenced by the load capacitance. Consequently, the output interval T_{OUT} ($TA_{OUT2} - TA_{OUT1}$) increases. The timing diagram of the metastable state is shown in Fig. 4. When $C_0 > C_1$, the load capacitance of R_1 is less than that of S_1. The transition of R_1 is faster due to lighter loading and results in shorter TA_{OUT2} latency. Consequently, the output interval T_{OUT} decreases.

Fig. 5(a) shows the schematic of half of the TA. Fig. 5(b) shows the timing diagram of the input interval T_{IN} and the SR latch transition at R_1 and S_1. A larger value of T_{IN} corresponds to a closer timing between R_1 and S_1 transition. The longer metastable time due to closer transition results in greater TA_{OUT2} latency and a larger T_{OUT}. When $C_0 < C_1$, the retardation of the S_1 transition is less than that of the R_1 transition. This phenomenon causes the closer timing of the transition to be similar to the shorter T_{OFF}. As a result, we have a larger gain and a smaller input range. Inversely, we have a smaller gain and a larger input range when $C_0 > C_1$. The magnitude of the capacitance is proportional to the gain. A larger capacitance results in a larger gain, but also necessitates a larger chip area. We take advantage of this characteristic to design a variable gain TA by reducing the capacitance C_0 of the capacitor at the output side of the SR

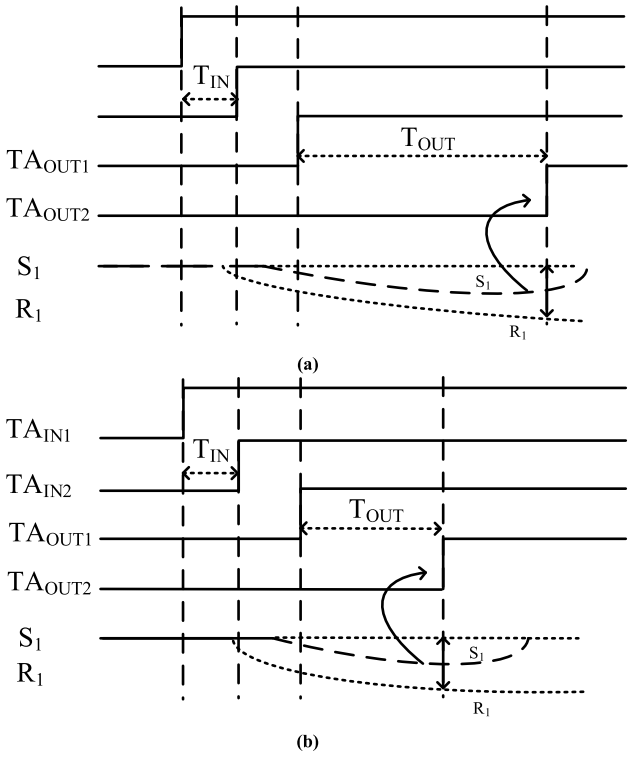


FIGURE 4. SR latch metastable timing diagram: (a) $C_0 < C_1$ and (b) $C_0 > C_1$.

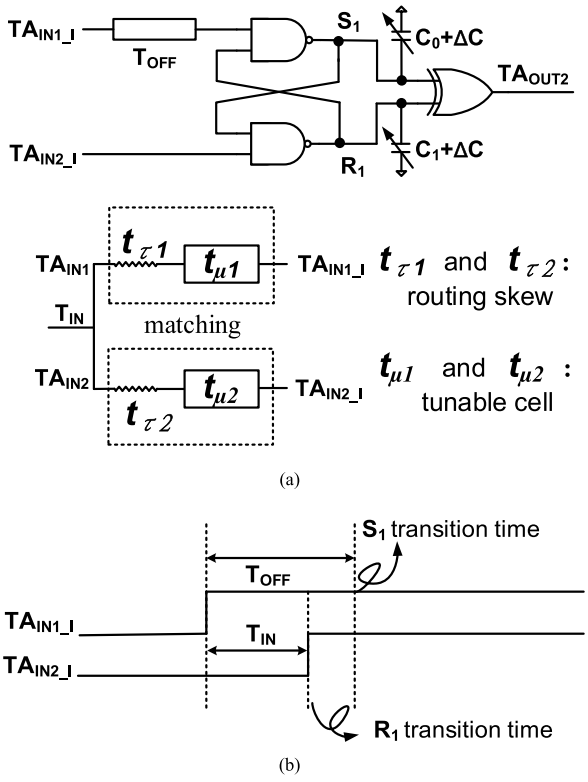
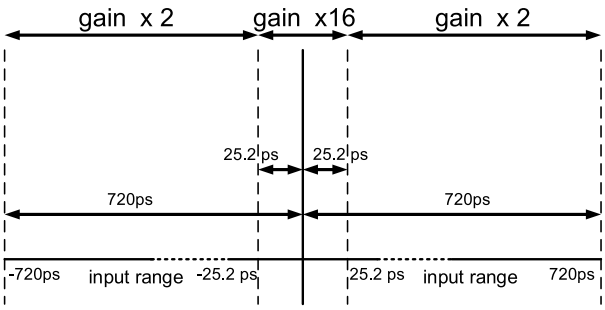


FIGURE 5. Half TA: (a) schematic and (b) timing diagram of input transition.



input range	gain
-25.2 ps<T_{IN}<25.2 ps	x16
-25.2 ps<T_{IN}<720 ps or -720 ps<T_{IN}<-25.2 ps	x 2

FIGURE 6. TA gain vs. input range.

latch for a larger gain requirement. In the proposed method we detect the input pulse and change the TA gain by adjusting the capacitance C_0. For a small input interval T_{IN} of less than 25.2 ps, the circuit is allowed to automatically select the larger TA gain. At the beginning, the default setting is $C_0 = C_1$. The pulse-width arbiter detects the input pulse. If the input pulse is less than the specified range, some C_0 capacitors are switched off for a higher gain. The two-stage gain TA has gains 2 and 16. The gain is controlled by the load capacitance at the output side of the SR latch. The TA input with gain 16 ranges from −25.2 to 25.2 ps. The TA input with gain 2 ranges from −720 to 720 ps. The TA gain and input range is shown in Fig. 6. The default setting of the output capacitance of both C_0 and C_1 is 790 fF. The TA with gain 16 changes the capacitance C_0 from 790 fF to 364.2 fF. In the default setting, the TA with gain 2 has the same load capacitance at both output sides of the SR latch. We propose detecting the interval of the input pulse and determining the TA gain automatically by switching off capacitors. We apply the variable-gain TA to the cyclic-ring Vernier having a resolution of 6.01 ps. If the input interval is −25.2–25.2 ps, the TA gain is 16 and TDC resolution is 0.38 ps. Otherwise, the TA gain is 2 and TDC resolution is 3.01 ps. The calibration of the load capacitance guarantees the consistency of the TA gain during PVT variation.

III. PROPOSED CIRCUITS

As shown in Fig. 7, the major modules of the proposed circuits are the calibrator, the compensator, the TA, and the TDC. The calibration controller generates the input pulse, the TDC converts the amplified interval to a digital code, the skew calibrator decides the method used to compensate for routing skew in the path, and the loading calibrator calibrates the TA gain.

A. VARIABLE-GAIN TA WITH COMPENSATORS

The proposed variable-gain TA with compensators includes a tunable matching cell and a tunable capacitor. The tunable matching cell provides the delay elements used to compensate

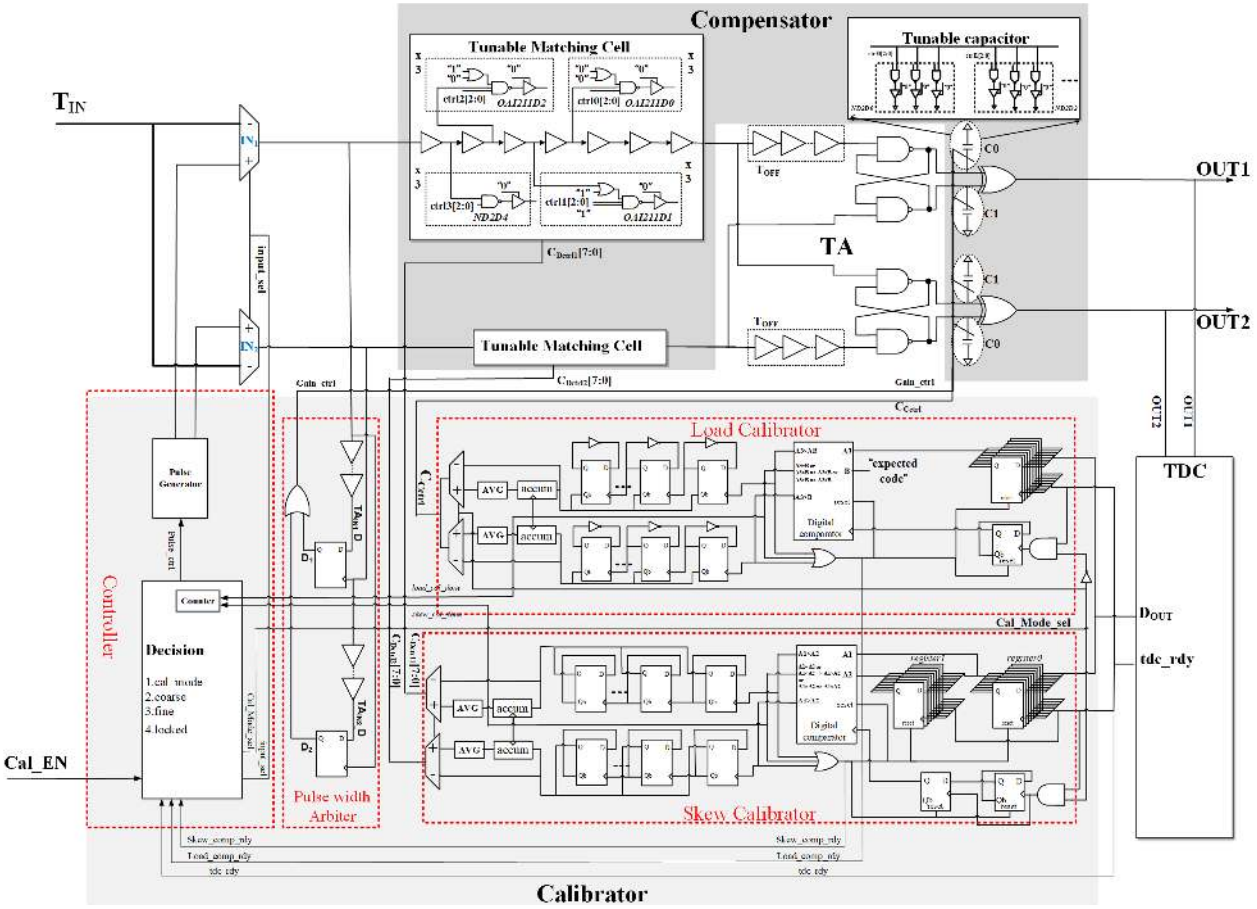


FIGURE 7. Proposed circuits.

for routing skew, and the tunable capacitor provides the precise loading cell to adjust the TA gain. The variable-gain TA has two gain selections derived from the pulse-width arbiter. The TA module works in both normal and calibration modes: in normal mode, the general operation is carried out, and in calibration mode, the timing skew of the input path is compensated for by skew calibration and the TA gain influenced by PVT variation is adjusted by calibrating before normal operation. Skew calibration yields a consistent TA gain in the input range, and loading calibration yields a constant TA gain that is not influenced by PVT variation.

1) TUNABLE MATCHING CELL

Fig. 8 shows a tunable matching cell, which is constructed with OAI and NAND gates as load capacitance in order to delay the input signal. Four types of components are connected to the propagation line as delay cells: OAI211D2, OAI211D1, OAI211D0, and ND2D4. The OAI211D0 cell contributes the finest resolution of 0.12 ps. The time steps of cells OAI211D1 and OAI211D2 are 0.37 ps and 1.2 ps, respectively. Cell ND2D4 contributes the 3.6 ps time step. Thus the design for a tunable matching cell has a resolution of 0.12 ps, and the tunable range is 15.87 ps.

2) TUNABLE CAPACITOR

The tunable capacitor is constructed as shown in Fig. 9. The minimum unit of capacitance is 0.015861 fF, contributed by the cell ND2D0. One input pin of ND2D0 is connected to the loading line, and the other is the control pin. When the control pin switches from 0 to 1, the difference in capacitance at the loading line is 0.015861 fF. The carry bit is contributed by the cell ND2D2. We change its capacitance by switching the control pins of ND2D2, with an amount of change of 0.059153 fF. We use the same concept to construct a five-level tunable capacitor. In this scheme, its small capacitance change is used to achieve precise TA gain.

B. SKEW CALIBRATOR

This circuit compares the TDC results for the input pulses $T_{IN} > 0$ and $T_{IN} < 0$. In the schematic shown in Fig. 10(a), one comparator, two registers, and two counters are present. The registers store the TDC codes from pulses $T_{IN} > 0$ (register_1) and $T_{IN} < 0$ (register_0). When the TDC codes of pulse $T_{IN} > 0$ are higher than that of pulse $T_{IN} < 0$, the timing delay in the IN_2 path is greater than that in the IN_1 path. We compensate for the timing skew by adding the timing delay in the IN_1 path; signal A1 < A2 triggers

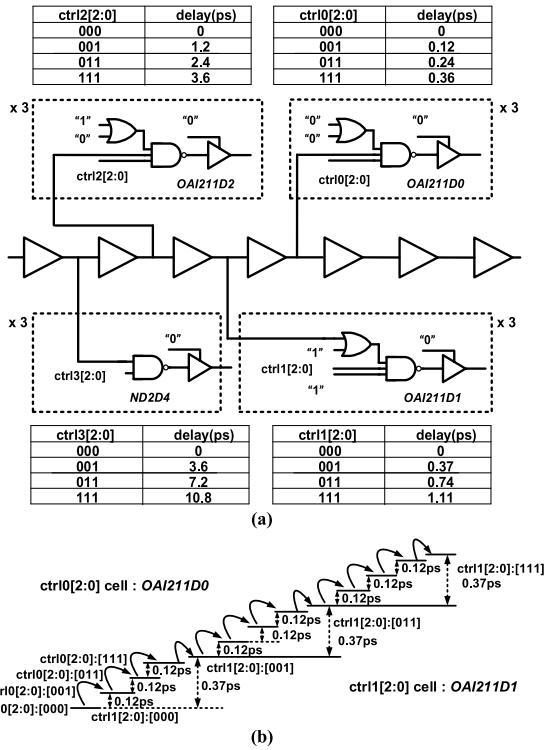


FIGURE 8. Tunable matching cell: (a) schematic and (b) step diagram.

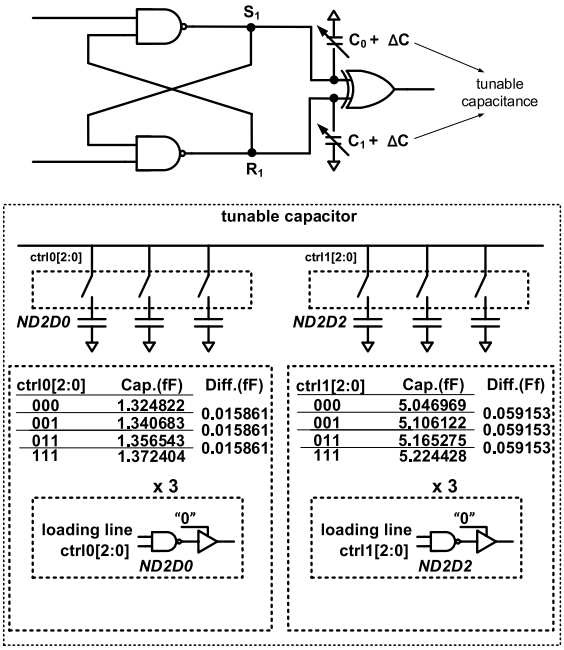


FIGURE 9. Tunable capacitor.

the counter to add the code of C_{Dctrl1}. Likewise, signal A1 > A2 triggers the counter to add the code of C_{Dctrl2}. The timing diagram is shown in Fig. 10(b). The first trigger of the *tdc_rdy* signal latches D_{OUT} ($T_{IN} > 0$) from TDC to *reg_0*. The second *tdc_rdy* trigger transfers D_{OUT} ($T_{IN} > 0$) from *reg_0* to *reg_1* and latches D_{OUT} ($T_{IN} < 0$) from

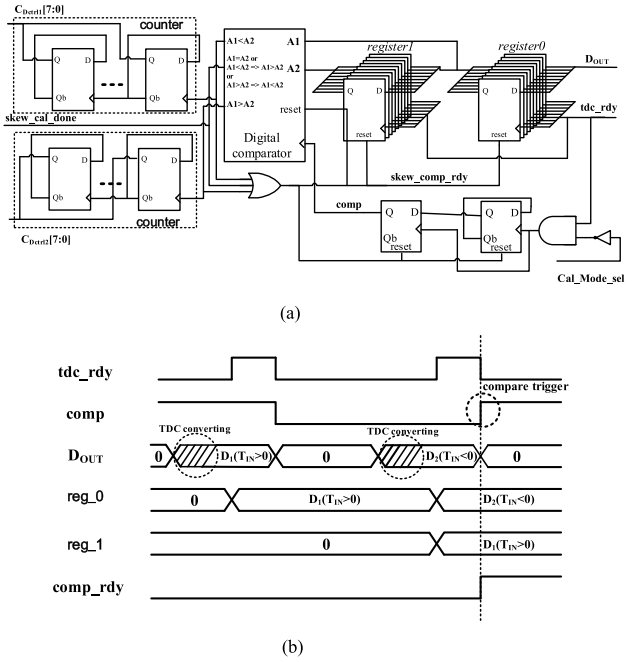


FIGURE 10. Skew calibrator: (a) schematic; and (b) timing diagram.

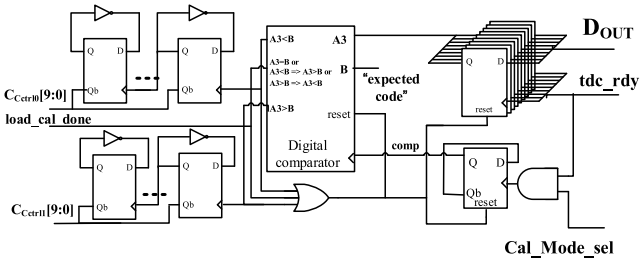


FIGURE 11. Loading calibrator.

TDC to *reg_0*. The *comp* signal triggers the comparator to compare the data stored in *reg_0* and *reg_1*. If the data in both registers are consistent, the *skew_cal_done* signal announces that calibration is complete. In routing the skew calibration mode, we use the low-gain TA for coarse calibration and to compensate for skew with bits $C_{Dctrl}[7:6]$. We use the high-gain TA for fine calibration and to compensate for skew with bits $C_{Dctrl}[5:0]$.

C. LOADING CALIBRATOR

The schematic of the loading calibrator is shown in Fig. 11. This circuit compares the TDC data from the amplified interval and the expected code that maps to the expected amplified pulse. One comparator, one register, and two counters are present. The register saves the TDC code from the amplified interval, and the comparator compares the TDC code and the expected code. The counter bits are the control codes that control the tunable capacitor. The control codes from the down counter decrease capacitance C_0 if the gain is smaller than expected. Otherwise, the control codes from the down counter decrease the capacitance C_1 to reduce the TA gain.

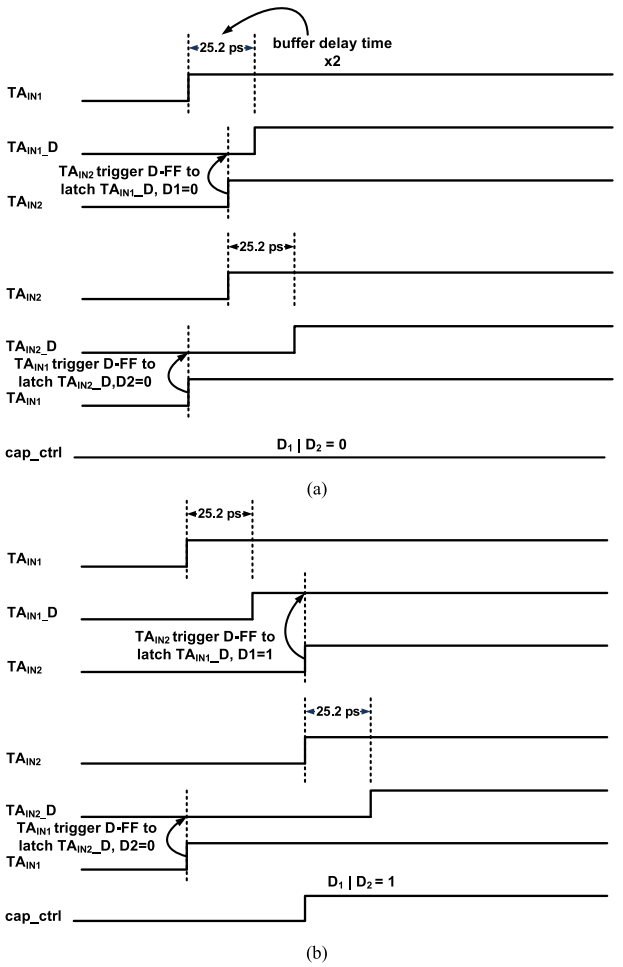


FIGURE 12. Pulse-width arbiter: (a) $T_{IN} < 25.2$ ps and (b) $T_{IN} > 25.2$ ps.

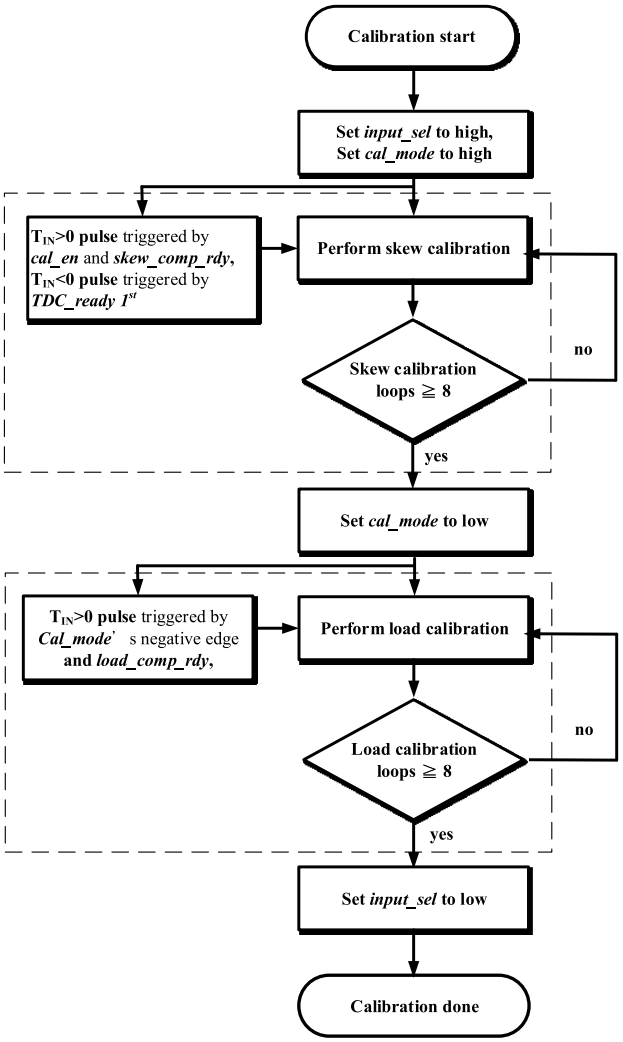


FIGURE 13. Calibration control flowchart.

The operation repeats until the expected gain is met. The loading calibration adjusts the capacitances C_0 and C_1 at the output of the SR latch. There are two loops of calibration for gains 2 and 16. The TA with the specified gain receives and amplifies the pulse from the pulse generator, after which the TDC converts the amplified interval to the codes. The loading calibrator compares the codes with the expected value: if the gain is greater than the expected value, capacitance C_1 is reduced, and if the gain is less than expected, capacitance C_0 is reduced.

D. PULSE-WIDTH ARBITER

The pulse-width arbiter is composed of two D flip-flops and one OR gate. The device detects the width of the input interval with two regions. If the input interval is more than 25.2 ps, the *gain_ctrl* signal is set to 1 and the capacitance C_0 is 790 fF for the TA with gain 2. If the input interval is less than 25.2 ps, *gain_ctrl* changes to 0 and capacitance C_0 is 364.2 fF for the TA with gain 16. In the proposed design, capacitances C_0 and C_1 can change to switch the TA gain. When $T_{IN} > 0$, TA_{IN1} is ahead of TA_{IN2}. If TA_{IN1} is still ahead of TA_{IN2} in the timing after propagating through two buffers, the input interval is greater than 25.2 ps. The TA_{IN2} signal triggers the D flip-flop to latch the TA_{IN1}_D signal, and the result of the latch is the D_1 signal. If the input interval is greater than 25.2 ps, D_1 is 1. Otherwise, D_1 is 0. In the other D flip-flop, TA_{IN1} is always ahead of TA_{IN2}_D, and the latch result stays at 0. If $T_{IN} < 0$, TA_{IN2} is ahead of TA_{IN1}. Signal D_2 is the latch result and D_1 stays at 0; the *gain_ctrl* detection signal is due to the latch result of D_2. The control signal *gain_ctrl* is the combinational result of D_1 and D_2 through the OR gate. Capacitance C_0 is variable and is controlled by *gain_ctrl*, which when switching the capacitors is much faster than the TA_{IN1} signal arriving at S_1; it is also faster than TA_{IN2} arriving at S_2 through theT_{OFF} delay to guarantee that the capacitor switch is ready before the TA develops. The detection timing diagrams for $T_{IN} < 25.2$ ps and $T_{IN} > 25.2$ ps are shown in Figures 12(a) and 12(b).

E. CONTROLLER

Figures 13 and 14 show flowchart and the time diagram of controller. The cal_en signal triggers the calibration mode.

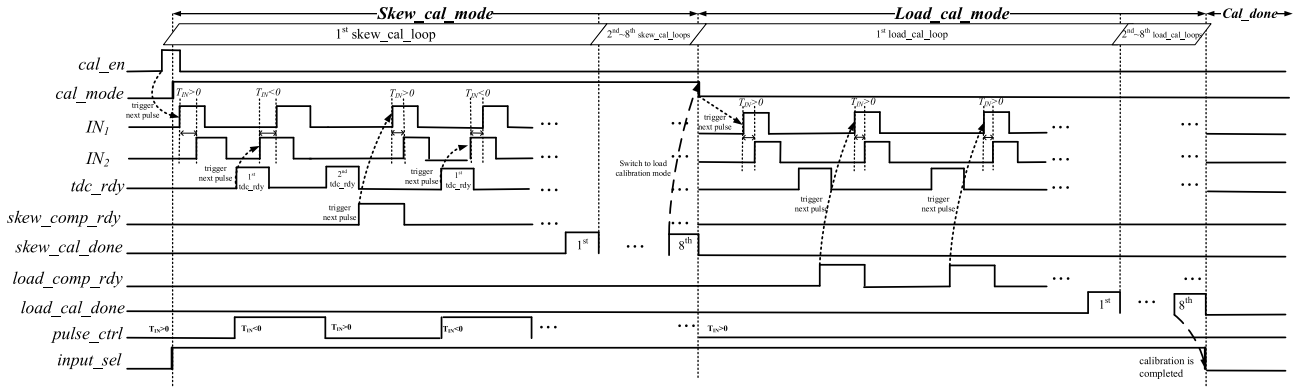


FIGURE 14. Timing diagram for controller.

At the same time, the input_sel signal is set to "high". This means that the IN_1 and IN_2 signals are provided by the pulse generator. Calibration of skew mismatch is processed first in calibration mode. At first, the pluse_ctrl signal is set to "low", meaning that the IN_1 signal is ahead of IN_2. When the first operation of TDC ($T_{IN} > 0$) is complete, the TDC produces the tdc_rdy signal to trigger the counter and the pluse_ctrl signal changes to "high". The negative pulse ($T_{IN} < 0$) is generated by switching the input path of the multiplexer, which is controlled by the pluse_ctrl signal. The comparator compares the TA gain of the input pulses $T_{IN} > 0$ and $T_{IN} < 0$. If the TDC results are the same, the skew_cal_done signal notices that the skew calibration loop is complete. Otherwise, the second run is triggered by the skew_comp_rdy signal and the procedure described previously is repeated. During this phase, the skew calibration loop is performed eight times. When skew calibration mode is completed, the cal_mode signal is set to "low" and load calibration mode is executed. The negative edge of cal_mode triggers the first input interval at the turn of $T_{IN} > 0$ and begins to perform eight load calibration loops. In load calibration mode, the pulse_sel signal is fixed at "low". When the load calibration mode is also completed, the overall calibration work has been finished, and the input_sel signal is set to low.

Here the width of the input interval is 25.2 ps by the propagation delay of the two buffers in the pulse generator to ensure that the direction of the input pulse does not change even in the maximum compensable skew 15.87 ps.

IV. PROPOSED CALIBRATION

Due to gain imbalance, we propose skew calibration. We leverage the characteristics of variable gain to perform two-stage calibration. Coarse calibration with the low-gain TA is used to get the MSB and fine calibration with the high-gain TA is used to get the LSB. Because of gain inaccuracy, we use loading calibration for TA gain adjustment. Loading calibration is performed when skew calibration is completed. The tunable matching cell is implemented at the input side of the SR latch for skew compensation, whereas the tunable capacitor is implemented at the output side of the SR latch for loading calibration.

TABLE 1. 2-to-3 decoder function.

INPUT		*OUTPUT*		
$C_{Dctrl\ 7}$	$C_{Dctrl\ 6}$	$ctrl3_2$	$ctrl3_1$	$ctrl3_0$
$C_{Dctrl\ 5}$	$C_{Dctrl\ 4}$	$ctrl2_2$	$ctrl2_1$	$ctrl2_0$
$C_{Dctrl\ 3}$	$C_{Dctrl\ 2}$	$ctrl1_2$	$ctrl1_1$	$ctrl1_0$
$C_{Dctrl\ 1}$	$C_{Dctrl\ 0}$	$ctrl0_2$	$ctrl0_1$	$ctrl0_0$
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

A. SKEW CALIBRATION

In skew calibration mode, the skew calibrator compares the TDC results for the input pulses $T_{IN} > 0$ and $T_{IN} < 0$ with the same width, and generates code $C_{Dctrl}[7:0]$ to control the tunable matching cell for skew compensation by comparing results. We use a 2-to-3 decoder, the function of which is shown in Table 1, to convert Code C_{Dctrl} [7: 6] to Code ctrl3 [2: 0] which is the control code for cell ND2D4 with a time step of 3.6 ps. $C_{Dctrl}[5:4]$, $C_{Dctrl}[3:2]$, and $C_{Dctrl}[1:0]$ are converted to ctrl2[2:0], ctrl1[2:0], and ctrl0[2:0] for OAI211D2 with a time step of 1.2 ps, OAI211D1 with a time step of 0.37 ps, and OAI211D0 with a time step of 0.12 ps, respectively.

In skew calibration mode we use two-stage calibration, composed of coarse calibration and fine calibration, to reduce the calibration time. Coarse calibration compensates for the considerable routing skew and fine calibration is for improved resolution. When coarse calibration is completed and the remaining routing skew is minimized, fine calibration is used to improve the resolution with fine step compensation. Here we set high gain to 16 and low gain to 2. Calibration with the low- and high-gain TAs contributes 2 bits with a resolution of 3.01 ps and 6 bits with a resolution of 0.38 ps, respectively. In the first stage of skew calibration, we use the low-gain TA for coarse calibration to compensate for skew with bits $C_{Dctrl}[7:6]$. After the first stage is complete, we use the

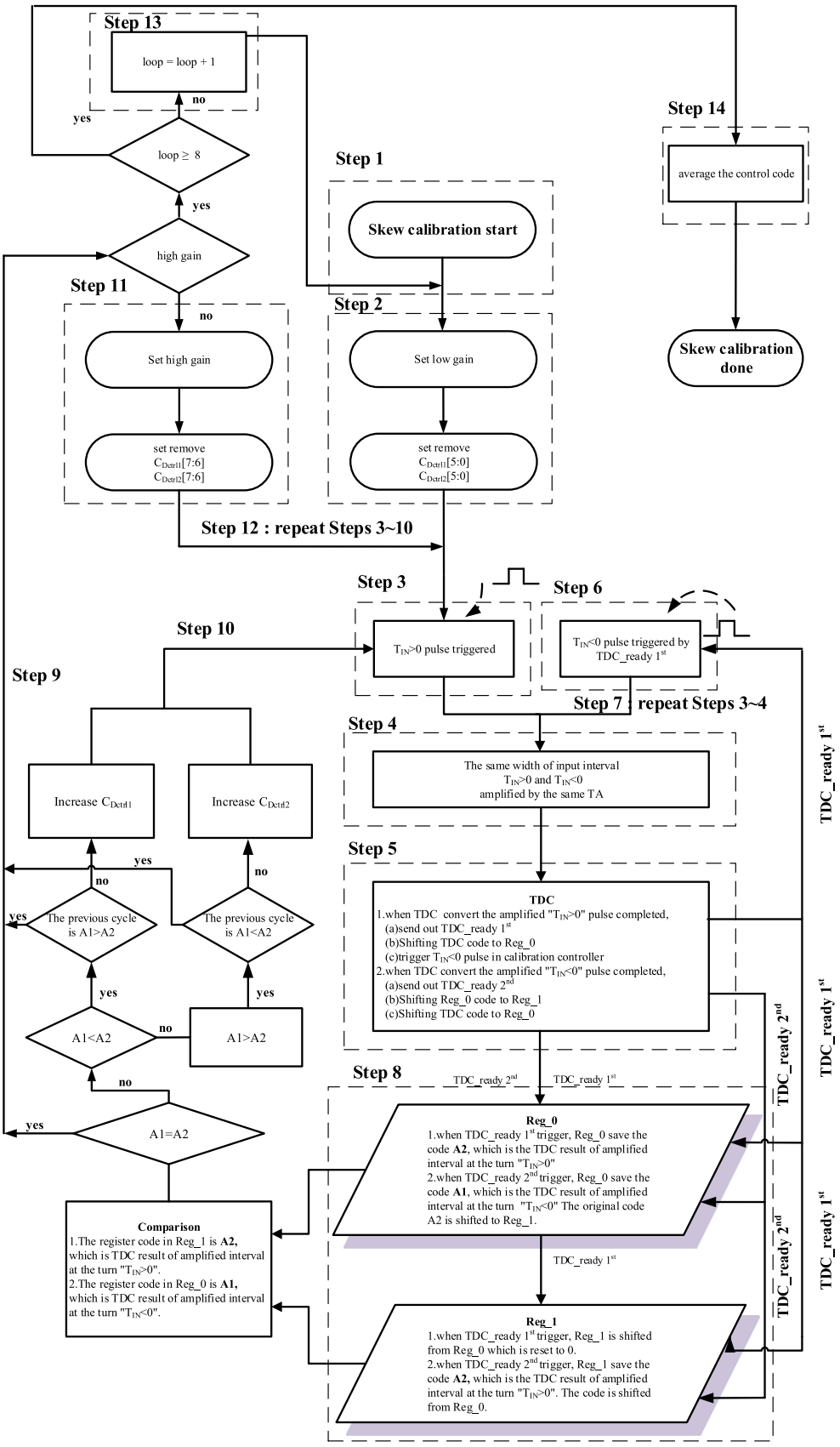


FIGURE 15. Skew calibration flowchart.

high-gain TA for fine calibration and to compensate for skew with bits $C_{Dctrl}[5:0]$.

Fig. 15 shows the flow chart for skew calibration. It consists of the following fourteen steps:

Step 1: Enable skew calibration; set loop = 0.
Step 2: Select low-gain TA for coarse calibration with coarse codes $C_{Dctrl1}[7:6]$ and $C_{Dctrl2}[7:6]$; remove fine codes $C_{Dctrl1}[5:0]$ and $C_{Dctrl2}[5:0]$.
Step 3: Generate pulse with $T_{IN} > 0$.
Step 4: Amplify time interval with low-gain TA.
Step 5: Convert amplified interval to code.
Step 6: Generate pulse with $T_{IN} < 0$.
Step 7: Repeat Steps 4–5.
Step 8: Save conversion result to code A2 for $T_{IN} > 0$ and to code A1 for $T_{IN} < 0$.
Step 9: Compare digital code A1 and A2; if A1 < A2, add code $C_{Dctrl1;}$ if A1 > A2, add code $C_{Dctrl2.}$
Step 10: Repeat Steps 2–8 until comparison result of A1 and A2 is changed. (If previous cycle is A1 > A2, changed result is A1 = A2 or A1 < A2; in contrast, if previous cycle is A1 < A2, changed result is A1 = A2 or A1 > A2)
Step 11: Select high-gain TA for fine calibration with fine codes $C_{Dctrl1}[5:0]$ and $C_{Dctrl2}[5:0]$; remove coarse codes $C_{Dctrl1}[7:6]$ and $C_{Dctrl2}[7:6]$.
Step 12: Repeat Steps 3–10.
Step 13: Loop = loop + 1, repeat Steps 2–12 until loop = 8.
Step 14: Average codes $C_{Dctrl1}[7:0]$ and $C_{Dctrl2}[7:0]$.

These fourteen steps are repeated until the skew has been compensated for.

A detailed description of the flow is as follows. The calibration controller produces the first input interval at the turn of $T_{IN} > 0$. This input interval is amplified by the TA and its value is then converted to a digital code by the TDC and saved as register0, after which it sends out the *tdc_rdy* signal as the trigger signal at the turn of $T_{IN} < 0$. The input interval with the same width but $T_{IN} < 0$ is amplified by the TA. Its value is then converted to a digital code by the TDC and saved as register0. The value in the former register0 is then shifted to register1. When the skew calibrator has completed these actions, the comparator compares the two TDC results. After comparison, if code A1 at the turn of $T_{IN} > 0$ and code A2 at the turn of $T_{IN} < 0$ are consistent, the calibration is complete. If these codes are inconsistent, the routing skew is compensated for by the tunable matching cell. When A1 > A2, the timing delay in IN_1 path is increased. Otherwise, the timing delay in IN_2 path is increased. These procedures are repeated until A1 = A2 or until the comparison result of A1 and A2 is changed, and skew calibration is complete.

Figure 16 is an example of a skew calibration loop. In the example we set the skew to 8ps, meaning that the timing delay of the IN_2 path is 8 ps more than the IN_1 path. In the first stage, we increase the value of $C_{Dctrl1}[7:6]$ according to the comparison result. When the value of $C_{Dctrl1}[7:6]$ is 11, the comparison result is changed compared to the previous cycle. Then skew calibration enters the second stage, at which point the timing delay of the IN_1 path is 2.8 ps more than the IN_2 path. In the second stage, we increase the value of $C_{Dctrl2}[5:0]$ according to the comparison result. When the value of $C_{Dctrl2}[5:0]$ is 10_0101, the comparison result is changed compared to the previous cycle. Eventually the timing delay of the IN_2 path is 0.09 ps more than the IN_1 path, and the value is less than the smallest adjustable time step. In the example, we end up with 1100_0000 and 0010_0101 as the value of $C_{Dctrl1}[7:0]$ and $C_{Dctrl2}[7:0]$, respectively.

B. LOADING CALIBRATION

The loading calibration flow is repeated 8 times, after which the average is taken for TA gain adjustment. The steps of calibration are as following: $C_{Cctrl0}[9:0]$ is the control code of capacitor C_0 and $C_{Cctrl1}[9:0]$ is the control code of capacitor C_1. Shown in Fig. 17, the loading calibration flow comprises the following eight steps:

Step 1: Set initial $C_{Cctrl0}[9:0]$ and $C_{Cctrl1}[9:0]$.
Step 2: Generate pulse T_{IN}.
Step 3: Amplify pulse T_{IN} using TA.
Step 4: Convert amplified interval to digital code A3.
Step 5: Compare digital code A3 to expected code B; if A3 > expected code B, decrease $C_{Cctrl1}[9:0]$; if A3 < expected code B, decrease $C_{Cctrl0}[9:0]$.
Step 6: Repeat Steps 1–5 until B = expected code.
Step 7: Loop = loop + 1, repeat Steps 1–6 until loop = 8.
Step 8: Compute average of codes $C_{Cctrl0}[9:0]$ and $C_{Cctrl1}[9:0]$.

The load calibrator repeats these eight steps until the expected gain is achieved. The proposed low gain is 2x and high gain is 16x; for the former, capacitances C_0 and C_1 are both set to 790 fF; for the latter, C_0 and C_1 are set to 790 fF and 364.2 fF, respectively. We turn off C_0 to increase the TA gain and C_1 to decrease the TA gain.

V. SIMULATION AND DISCUSSION

A. SIMULATIONS

1) INPUT SKEW

Fig. 18 is the result of input path skew simulations. There are three input path skew possibilities. The routing path match is the ideal case: that is, there is no timing skew between IN_1 and IN_2. A skew of 20 ps means that the routing delay of IN_2 is greater than the routing delay of IN_1, and the delay time is 20 ps. In contrast, a skew of −20 ps means that the routing delay of IN_2 is less than the routing delay of IN_1, and the delay is 20 ps.

a: ROUTING OF IN_1 AND IN_2 MATCHED

When the routing of IN_1 and IN_2 is matched, the T_{IN}–T_{OUT} curve passes through the origin; that is, when T_{IN} is 0, T_{OUT} is 0. This is the ideal case achieved by calibration;

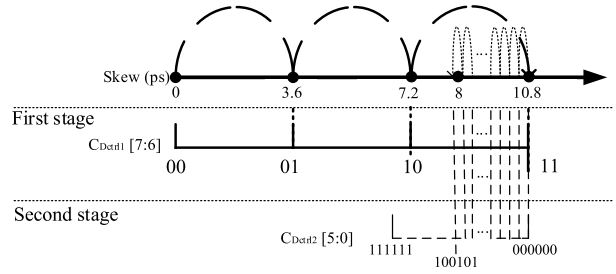


FIGURE 16. An example of a skew calibration loop.

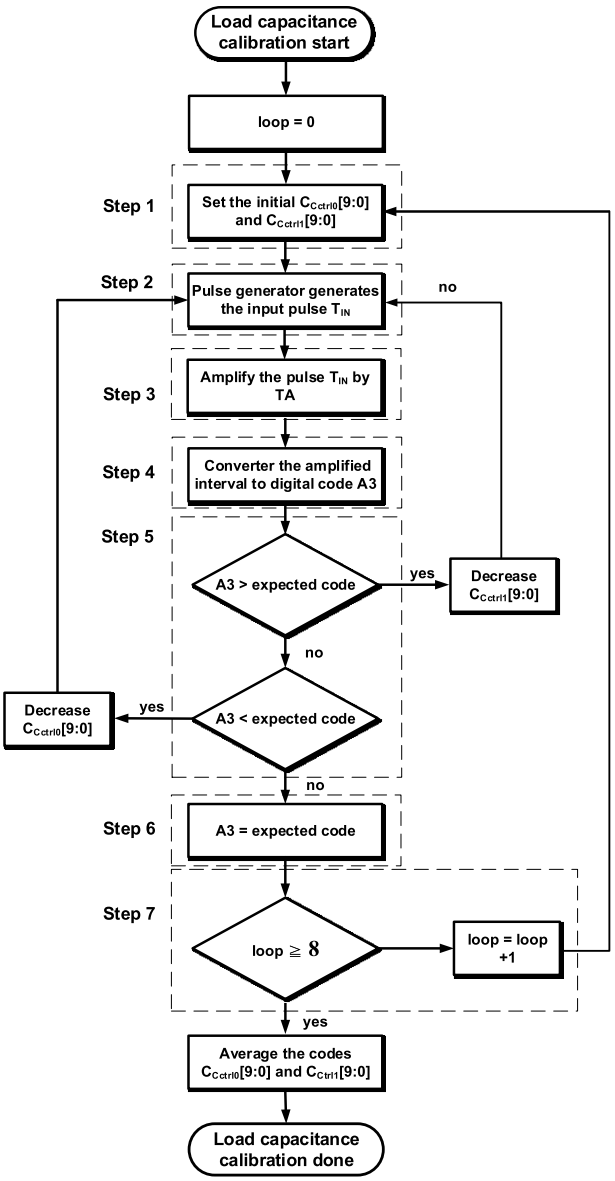


FIGURE 17. Loading calibration flowchart.

we suppose that the routing of IN_1 and IN_2 match after calibration, so the TA gain is consistent in the input range. In Fig. 18, the "matched" curve is the simulation result of matched routing.

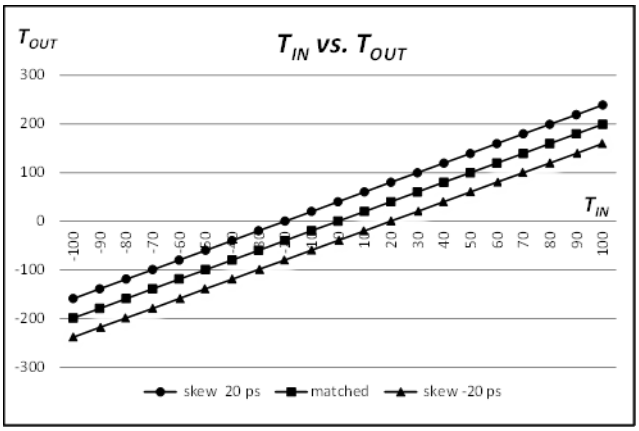


FIGURE 18. Skew simulation result.

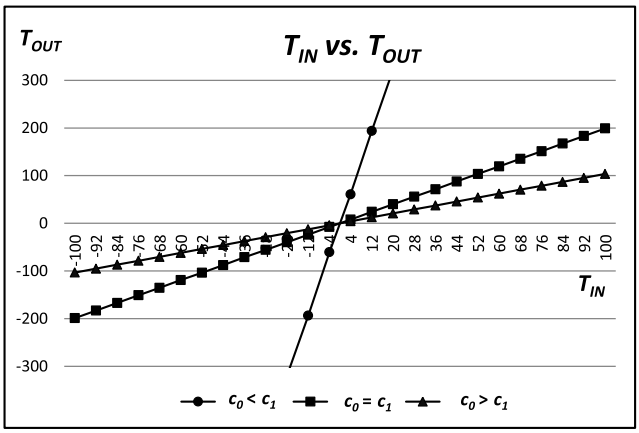


FIGURE 19. TA gain vs. load capacitance simulation result.

b: TIMING DELAY OF IN_1 GREATER THAN IN_2

Here, as the timing delay of IN_1 is greater than IN_2, the resulting T_{IN} is smaller, and the T_{IN}–T_{OUT} curve shifts to the right. When signals IN_1 and IN_2 are transmitted at the same time, that is, $T_{IN} = 0$, the delay of IN_1 is longer, and the signal IN_1 reaches the SR latch later than the signal IN_2; T_{OUT} is less than 0. In Fig. 18, the "skew -20" curve is an example of this.

c: TIMING DELAY OF IN_2 GREATER THAN IN_1

Here, as the timing delay of IN_2 is greater than IN_1, the resulting T_{IN} is larger, and the T_{IN}–T_{OUT} curve shifts to the left. When signals IN_1 and IN_2 are transmitted at the same time, that is, $T_{IN} = 0$, the delay of IN_2 is longer, and the signal IN_2 reaches the SR latch later than the signal IN_1. Therefore, T_{OUT} is greater than 0. In Fig. 18, the "skew 20" curve is an example of this.

2) CAPACITANCE OF C_0 VS. C_1

Fig. 19 is the simulation result of various capacitances at the two ends of the SR latch. The three curves represent the relative values of capacitors C_0 and C_1. By default, C_0 and C_1 are both set to 790 fF; if C_0 is less than C_1, C_0 changes its

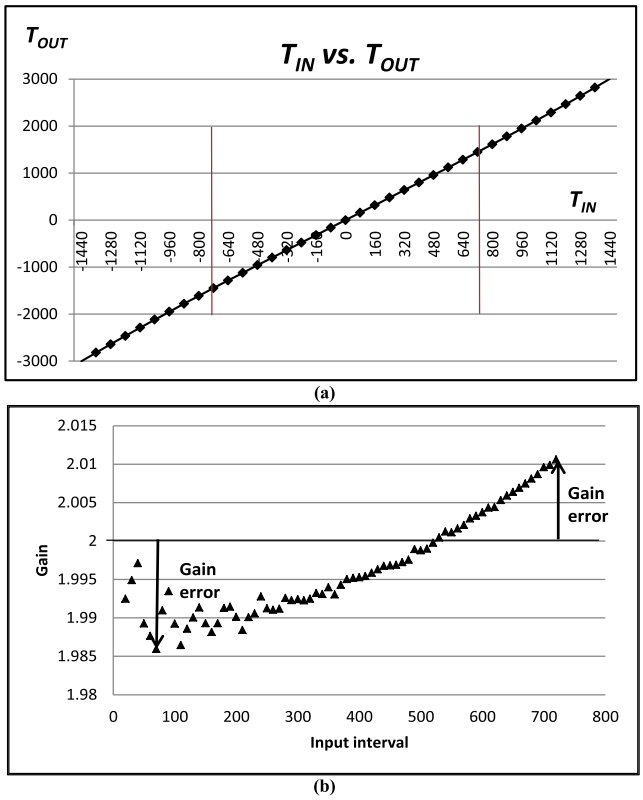


FIGURE 20. TA gain 2: (a) T_{IN} vs. T_{OUT} and (b) gain distribution.

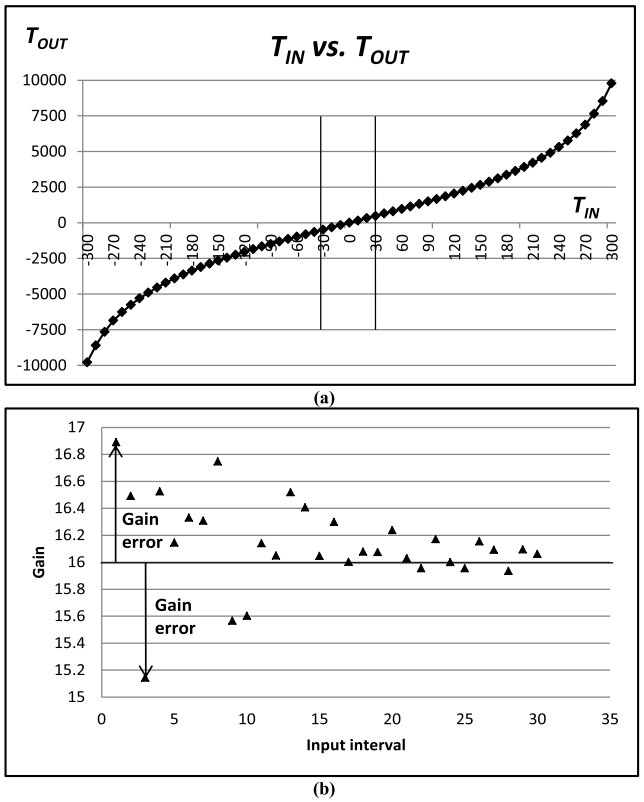


FIGURE 21. TA gain 16: (a) T_{IN} vs. T_{OUT} and (b) gain distribution.

capacitance to 364.2 fF; if C_0 is more than C_1, C_1 changes its capacitance to 364.2 fF.

a: C_0 EQUAL TO C_1

If the capacitances at the two output sides of the SR latches are the same, the propagation time is proportional to the amount of capacitance; that is, the TA gain is proportional to the load capacitance. By default, capacitances C_0 and C_1 are both 790 fF, and the TA gain is 2.

b: C_0 GREATER THAN C_1

If C_0 is greater than C_1, the TA gain is less than if C_0 *were equal to* C_1. In this design, C_1 is reduced, whereas C_0 remains unchanged. Capacitance C_0 is 790 fF, C_1 is 364.2 fF, and the TA gain is 1.054.

c: C_0 LESS THAN C_1

If C_0 is less than C_1, the TA gain is larger than if C_0 *were equal to* C_1. In this design, C_0 is reduced, whereas remains unchanged. Capacitance C_0 is 364.2 fF, C_1 is 790 fF, and the TA gain is 16.

3) TWO-STAGE GAIN TA

The proposed design has two selections of TA gain. The default value of the TA's gain is 2; the other choice is 16. The pulse-width arbiter detects the pulse width and selects the TA gain. If the pulse width is less than 25.2 ps (two buffer propagation time), the TA gain is 16; otherwise, it is 2. The T_{IN}–T_{OUT} curve in the TA gain of 2 is shown in Fig. 20(a). The maximum gain error is 0.014 in the input range from −720 to 720 ps, as shown in Fig. 20(b). The T_{IN}–T_{OUT} curve in the TA gain 16 is shown in Fig. 21(a). The maximum gain error is 0.873 in the input range from −25.2 to 25.2 ps. We use the characteristic of the two-stage gain TA for calibration: the low gain TA is for MSB and the high gain TA is for LSB. This two-stage calibration boasts both a wide input range and high resolution.

According to the simulation results, the mean is 2 and standard deviation (STD) is 0.4% when TA's gain is 2x. For the 16x amplifier case, the mean and STD are 16.14 and 2.1%, respectively. The results indicated that the proposed calibration method makes TA work properly.

B. PERFORMANCE SUMMARY

1) PERFORMANCE

We use a two-stage gain TA to amplify the pulse for skew calibration as shown in Fig. 22. The low-gain TA is for coarse calibration to manage considerable skew, whereas the high-gain TA is for fine calibration. Skew calibration reduces the gain error caused by the timing skew due to routing. If the routing skew is 20 ps (the timing delay of IN_1 is greater than IN_2 and the skew is 20 ps), the gain distribution is shown in Fig. 23(a), and the maximum gain error without calibration is 3.986; if the routing skew is −20 ps (the timing delay of IN_1 is less

TABLE 2. Features and Performance.

Process technology		65-nm CMOS	
TA scheme		SR-latch based TA	
TA gate count		4375	
		TA gain=2	TA gain=16
Power		2.8mA@10MHz	3.2mA@10MHz
Input range		±720 ps	± 25.2 ps
Gain cal. bits		10	10
Skew cal. bits		2	6
Gain error	W/o calibration	3.996	64.51
	W/ calibration	0.014	0.873
Time skew	W/o calibration	19.94 ps	4.3 ps
	W/ calibration	0.95 ps	1.37 ps

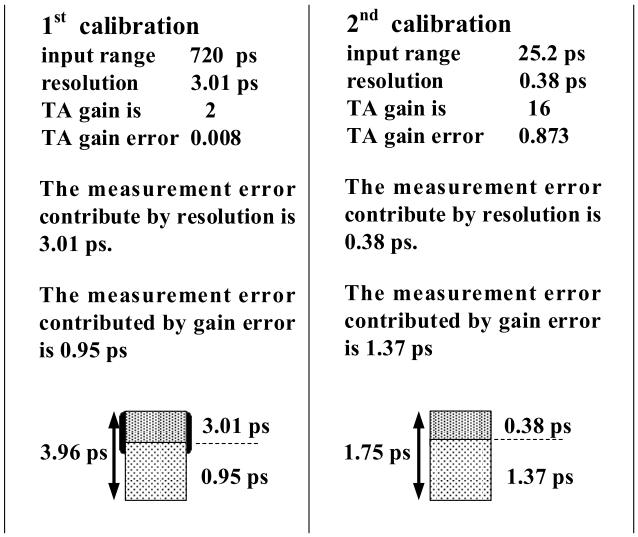


FIGURE 22. Skew calibration with two-stage gain TA.

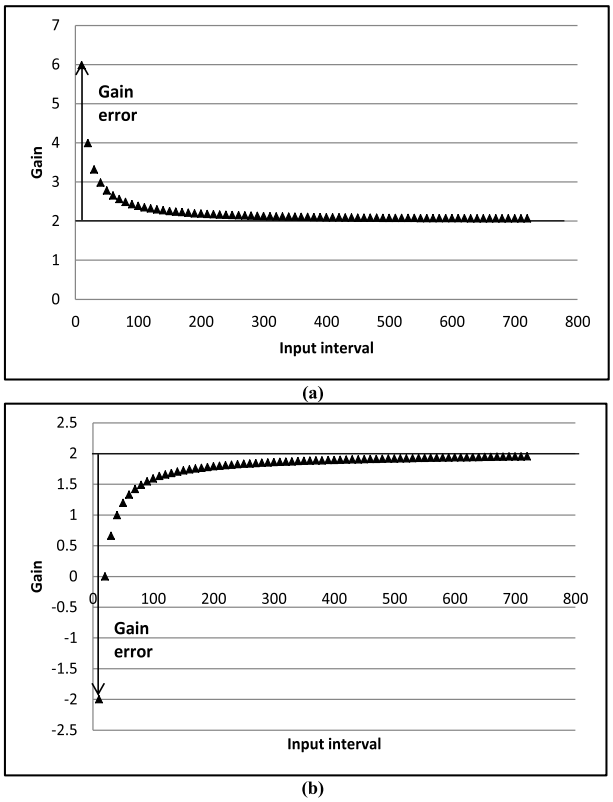


FIGURE 23. Gain error of TA gain 2: (a) 20 ps skew; and (b) −20 ps skew.

than IN_2 and the skew is 20 ps), the gain distribution is shown in Fig. 23(b), and the maximum gain error without calibration is 3.996. The two-stage gain TA selects the gain according to the width of the input pulse. The gain calibration adjusts the load capacitance to achieve the expected gain. If the gain is less than the target, capacitance C_0 is reduced to obtain a higher gain. Otherwise, C_1 is reduced to obtain a lower gain. The resolution of the tunable capacitor is 0.015861 fF, and that of the tunable gain is 0.019 (0.119%) at a TA gain of 16.

Table 2 summarizes the features and performance of the proposed design. The skew calibration with a two-stage TA has 8 bits: the first stage contributes 2 bits and the second stage contributes 6 bits. The resolutions are 3.01 ps and 0.38 ps and time skews caused by gain error are 0.95 ps and 1.37 ps for the TA with gain 2 and with gain 16, respectively. The maximum gain errors are 0.014 and 0.873 for the TA with gain 2 and with gain 16, respectively. The input ranges from −720 to 720 ps for the TA with gain 2 and from −25.2 to 25.2 ps for the TA with gain 16. The pulse-width arbiter checks the width of the input interval to determine the TA gain. There are 10 bits for TA gain calibration. The resolutions of the tunable gain step are 0.0017% and 0.119% at a TA gain of 2 and 16, respectively. This study was designed using a TSMC 65-nm CMOS process with a 1 V power supply, and a power consumption of 2.8 mA (TA gain 2) and 3.2 mA (TA gain 16) at 10 MHz sampling. The total gate count was 4375, and the capacitors occupied an area of 3140 gate counts.

Table 3 compares the key performance of the proposed TA with previous work, compared with which the proposed methods achieve a precise gain for wide-input-range TA.

2) CALIBRATION TIME

In routing the skew calibration mode, we use the low-gain TA for coarse calibration and to compensate for skew with bits $C_{Dctrl}[7:6]$. We use the high-gain TA for fine calibration and to compensate for skew with bits $C_{Dctrl}[5:0]$. Therefore, a skew compensation loop is performed for $2^2 - 1 = 3$ cycles for coarse calibration and $2^6 - 1 = 63$ cycles for fine calibration to achieve the maximum compensated time, and there are 8 loops in skew calibration. Every cycle, input pulses $T_{IN} > 0$ and $T_{IN} < 0$ are amplified by TA and the amplified pulses are converted into code A1 and code A2 by TDC. Similarly, a maximum load compensation loop is performed $2^{10} - 1 = 1023$ cycles with input pulses $T_{IN} > 0$ for TA gains 2x and 16x, and there are 8 loops in load calibration. In addition, as most of the runtime of TDC overlaps with the runtime of TA, we need only consider the TA runtime and the data comparison time in each cycle. Therefore, if the system clock rate is 250MHz and the input pulse is 25.2ps, the maximum calibration time is 71.7 μs. Since calibration is performed only at power-on, restart, and sleep recovery,

TABLE 3. Performance summary and comparison with previous TAs.

	[8]'10	[13]'12	[32]'17	[33]'19	Proposed method	
Process	180nm	130nm	65nm	180nm	65nm	
Gain	2x	2x	2x	2x,4x,8x,16x,32x	2x	16x
Calibration	YES	YES	YES	YES	YES	
PVT-tolerant	-	YES	YES	YES	YES	
Input range	±100 ps	0–40 ps	±150 ps	100 ps	±720 ps	± 25.2 ps
Gain error	max error<8%	-0.5%~+0.5%	-0.5% ~+1.0%	-	-0.7%~+0.6%	-5.3%~+5.4%
Standard deviation	-	-	-	STD=5%@16x	STD=0.4%@2x	STD=2.1%@16.14x

the system can tolerate such latency. The calibration time could be reduced by increasing the clock rate, which however would increase the chip cost and current.

VI. CONCLUSION

In the proposed design, the TA is based on the SR latch. The skew calibration reduces the skew of the two input paths. After calibration, the TA gain is consistent in the input range. In skew calibration, two-stage gain TAs are adopted to achieve a wide input range and precise resolution. The first stage has a smaller gain in comparison to the second stage; thus, when using the second-stage gain, the input interval must be sufficiently small. The pulse-width arbiter determines whether the input interval is within the input range of the second stage; if it is within this range, the capacitor is adjusted and the gain changes to the larger gain. The first-stage gain is 2 for the input range from −720 to 720 ps. The second-stage gain is 16 for the input range from −25.2 to 25.2 ps. The gains are also adjusted by calibration against PVT deviation. The proposed TDC achieves a 0.38 ps resolution. The accuracy influenced by measurement error and resolution is 1.75 ps. Hence, this work carries out calibration not only on the skew of the input path and TA gain but also on two gain selections along with the input interval to enhance TDC performance.

REFERENCES

[1] P. Palojarvi, K. Maatta, and J. Kostamovaara, "Integrated time-of-flight laser radar," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 4, pp. 996–999, Aug. 1997.

[2] J.-H. Yu, M.-K. Park, and S.-W. Kim, "A 2 ps minimum-resolution, wide-input-range time-to-digital converter for the time-of-flight measurement using cyclic technique and time amplifier," in *Proc. IEEE Int. Conf. Consum. Electron. (ICCE)*, Las Vegas, NV, USA, Jan. 2016, pp. 151–152.

[3] Z. Cheng, M. J. Deen, and H. Peng, "A low-power gateable Vernier ring oscillator Time-to-Digital converter for biomedical imaging applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 445–454, Apr. 2016.

[4] Y. Kim and T. W. Kim, "An 11 b 7 ps resolution two-step time-to-digital converter with 3-D vernier space," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2326–2336, Aug. 2014.

[5] S. Kurtti and J. Kostamovaara, "An integrated laser radar receiver channel utilizing a time-domain walk error compensation scheme," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 1, pp. 146–157, Jan. 2011.

[6] H.-J. Kwon, J.-S. Lee, J.-Y. Sim, and H.-J. Park, "A high-gain wide-input-range time amplifier with an open-loop architecture and a gain equal to current bias ratio," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Jeju-do, South Korea, Nov. 2011, pp. 325–328.

[7] S. Ok, J. Kim, G. Yoon, H. Chu, J. Oh, S. Wook Kim, and C. Kim, "A DC-DC converter with a dual VCDL-based ADC and a self-calibrated DLL-based clock generator for an energy-aware EISC processor," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2008, pp. 551–554.

[8] S.-K. Lee, Y.-H. Seo, H.-J. Park, and J.-Y. Sim, "A 1 GHz ADPLL with a 1.25 ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 482–483.

[9] S. Kim, S. Hong, K. Chang, H. Ju, J. Shin, B. Kim, H.-J. Park, and J.-Y. Sim, "A 2 GHz synthesized fractional-N ADPLL with dual-referenced interpolating TDC," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 391–400, Feb. 2016.

[10] D. Zhang, H.-G. Yang, Z. Chen, W. Li, Z. Huang, L. Gao, and W. Zhu, "A fast-locking digital DLL with a high resolution time-to-digital converter," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2013, pp. 22–25.

[11] A. Hamza, S. Ibrahim, M. El-Nozahi, and M. Dessouky, "A wideband 5 GHz digital PLL using a low-power two-step time-to-digital converter," in *Proc. IEEE Int. Conf. Electron., Circuits, Syst. (ICECS)*, Cairo, Egypt, Dec. 2015, pp. 328–331.

[12] K.-H. Cheng, J.-C. Liu, C.-Y. Chang, S.-Y. Jiang, and K.-W. Hong, "Built-in jitter measurement circuit with calibration techniques for a 3-GHz clock generator," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 8, pp. 1325–1335, Aug. 2011.

[13] Y.-H. Seo, J.-S. Kim, H.-J. Park, and J.-Y. Sim, "A 1.25 ps resolution 8b cyclic TDC in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 736–743, Mar. 2012.

[14] S.-J. Kim, T. Kim, and H. Park, "A 0.63 ps, 12 b, synchronous cyclic TDC using a time adder for on-chip jitter measurement of a SoC in 28 nm CMOS technology," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, Jun. 2014, pp. 1–2.

[15] M. H. Chung, W. S. Liu, and H. P. Chou, "Time amplification using closed-loop differential amplifier," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. Rec. (NSS/MIC)*, Anaheim, CA, USA, Oct. 2012, pp. 789–792.

[16] T. Nakura, S. Mandai, M. Ikeda, and K. Asada, "Time difference amplifier using closed-loop gain control," in *Proc. Symp. VLSI Circuit (VLSIC)*, Jun. 2009, pp. 208–209.

[17] S. Mandai, T. Nakura, M. Ikeda, and K. Asada, "Cascaded time difference amplifier using differential logic delay cell," in *Proc. Int. SoC Des. Conf. (ISOCC)*, Busan, South Korea, Nov. 2009, pp. 355–356.

[18] K. Kim, Y.-H. Kim, W. Yu, and S. Cho, "A 7 bit, 3.75 ps resolution two-step time-to-digital converter in 65 nm CMOS using pulse-train time amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1009–1017, Apr. 2013.

[19] K. Kim, Y. Kim, W. Yu, and S. Cho, "A 7 b, 3.75 ps resolution two-step time-to-digital converter in 65 nm CMOS using pulse-train time amplifier," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 192–193.

[20] D. Dhar, Y.-H. Kwak, I. Jung, and C. Kim, "An all digital time amplifier with interpolation scheme for low gain variation," in *Proc. IEEE ISOCC*, San Francisco, CA, USA, Nov. 2010, pp. 276–278.

[21] M. Oulmane and G. W. Roberts, "A CMOS time amplifier for femto-second resolution timing measurement," in *Proc. IEEE Int. Symp. Circuits Syst.*, Vancouver, BC, Canada, vol. 1, May 2004, p. I-509.

[22] S. Mandai, T. Iizuka, T. Nakura, M. Ikeda, and K. Asada, "Time-to-digital converter based on time difference amplifier with non-linearity calibration," in *Proc. Proc. ESSCIRC*, Saarbrücken, Germany, Sep. 2010, pp. 266–269.

[23] B. Tong, W. Yan, and X. Zhou, "A constant-gain time-amplifier with digital self-calibration," in *Proc. IEEE 8th Int. Conf. ASIC*, Changsha, China, Oct. 2009, pp. 1133–1136.

[24] J.-C. Lai and T.-Y. Hsu, "Mismatch-tolerant time amplifier with embedded self-calibration," in *Proc. IEEE 5th Int. Conf. Consum. Electron.–Berlin (ICCE-Berlin)*, Berlin, Germany, Sep. 2015, pp. 393–396.

[25] V. Milovanovic and H. Zimmermann, "Complementary edge alignment and digital output signal speed-up CMOS positive feedback latches," in *IEEE 15th Int. Symp. Design Diagnostics Electron. Circuits Syst. (DDECS)*, Tallinn, Estonia, Apr. 2012, pp. 360–365.

[26] M. Lee and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr. 2008.
[27] A. M. Abas, A. Bystrov, D. J. Kinniment, O. V. Maevsky, G. Russell, and A. V. Yakovlev, "Time difference amplifier," *Electron. Lett.*, vol. 38, no. 23, pp. 1437–1438, Nov. 2002.
[28] W. Chaivipas, T. Ito, T. Kurashina, K. Okada, and A. Matsuzawa, "Fine and wide frequency tuning digital controlled oscillators utilizing capacitance position sensitivity in distributed resonators," in *IEEE ISSCC Dig. Tech. Papers*, Jeju-do, South Korea, Nov. 2007, pp. 424–427.
[29] D.-C. Lee, K.-Y. Kim, Y.-J. Min, K.-M. Kim, A. Abdullah, J. Park, and S.-W. Kim, "A low power all-digital PLL with power optimized digitally controlled oscillator," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Hong Kong, Dec. 2010, pp. 1–4.
[30] I. Vaisband, M. Azhar, E. G. Friedman, and S. Köse, "Digitally controlled pulse width modulator for on-chip power management," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 12, pp. 2527–2534, Dec. 2014.
[31] J.-C. Lai and T.-Y. Hsu, "Cost-effective time-to-digital converter using time-residue feedback," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4690–4700, Jun. 2017.
[32] Y. Lyu, J. Feng, H. Ye, and D. Yu, "All-digital synchronous 2 × time-difference amplifier based on time register," *Electron. Lett.*, vol. 53, no. 16, pp. 1102–1104, Aug. 2017.
[33] H. Molaei and K. Hajsadeghi, "A 5.3-ps, 8-b time to digital converter using a new gain-reconfigurable time amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 3, pp. 352–356, Mar. 2019.

KUAN-CHIEH CHAO received the B.E. degree in electronic engineering from Ming Chuan University, Taoyuan, Taiwan, in 2007, and the M.Eng. degree in electrical engineering from Chung Hua University, Hsinchu, Taiwan, in 2009. He is currently pursuing the Ph.D. degree in computer science and engineering with National Chiao Tung University. His research interests include wireless communications systems and VLSI design.

JUNG-CHIN LAI was born in Taichung, Taiwan. He received the Ph.D. degree from the Institute of Computer Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2017.

He worked as a DDR2/3 DRAM Designer with Nanya Technology Corporation, Taiwan, from 2006 to 2009, and as a DDRIO and DDR-PHY Designer with Global Unichip, Taiwan, from 2010 to 2015. He joined the National Chip Implementation Center, Hsinchu, from 2015 to 2017. He has extensive experience in the field of DDR DRAM. He is also skilled in system-on-a-chip implementation, and has rich experience in system analysis, in particular, for noise inhibition.

TERNG-YIN HSU (Member, IEEE) received the B.S. and M.S. degrees from Feng Chia University, Taichung, Taiwan, in 1993 and 1995, respectively, and the Ph.D. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1999, all in electronics engineering.

In 2003, he joined the Department of Computer Science, National Chiao Tung University, where he is currently a Professor. His current research interests include VLSI architectures, wireless communications, multispec transmissions, high-speed networking, analog-like digital circuits, system-on-a-chip design technology, and related application-specific integrated circuit design.