All-Digital PLL and Transmitter for Mobile Phones

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***Abstract*—We present the first all-digital PLL and polar transmitter for mobile phones. They are part of a single-chip GSM/EDGE transceiver SoC fabricated in a 90 nm digital CMOS process. The circuits are architectured from the ground up to be compatible with digital deep-submicron CMOS processes and be readily integrateable with a digital baseband and application processor. To achieve this, we exploit the new paradigm of a deep-submicron CMOS process environment by leveraging on the fast switching times of MOS transistors, the fine lithography and the precise device matching, while avoiding problems related to the limited voltage headroom. The transmitter architecture is fully digital and utilizes the wideband direct frequency modulation capability of the all-digital PLL. The amplitude modulation is realized digitally by regulating the number of active NMOS transistor switches in accordance with the instantaneous amplitude. The conventional RF frequency synthesizer architecture, based on a voltage-controlled oscillator and phase/frequency detector and charge-pump combination, has been replaced with a digitally controlled oscillator and a time-to-digital converter. The transmitter performs GMSK modulation with less than 0.5° rms phase error, −165 dBc/Hz phase noise at 20 MHz offset, and 10 μs settling time. The 8-PSK EDGE spectral mask is met with 1.2% EVM. The transmitter occupies 1.5 mm^2 and consumes 42 mA at 1.2 V supply while producing 6 dBm RF output power.**

***Index Terms*—All-digital, cellular, deep-submicron CMOS, digital control, digitally controlled oscillator (DCO), frequency synthesizer, GSM, mobile phones, MOS varactor, sigma-delta modulator, voltage-controlled oscillators (VCOs).**

I. Introduction

THE cellular phone industry continues to thrive by providing support for Bluetooth wireless personal area networking (WPAN), positioning technology based on a Global Positioning System (GPS) receiver, and wireless local area networking (WLAN) for high-speed local-area data access. Sophisticated applications, such as MP3 audio playback, camera functions, MPEG video and digital TV further entice a new wave of handset replacements. Such application support dictates high level of memory integration [1] together with large digital signal processing horse-power and information flow management, all requiring sophisticated DSP and microprocessor cores. To maintain low cost and power dissipation, as well as to minimize the printed circuit board (PCB) real estate, the entire radio, including memory, *application processor* (AP), *digital baseband* (DBB) processor, analog baseband and RF circuits, would ideally be all integrated onto a single silicon die with a minimal count of external components.

Nowadays, the DBB and AP designs constantly migrate to the most advanced deep-submicron digital CMOS process available, which usually does not offer any analog extensions and has very limited voltage headroom [2]. Design flow and circuit techniques of contemporary transceivers for multi-GHz cellular applications are typically analog intensive and utilize process technologies that are incompatible with DBB and AP processors. The use of low-voltage deep-submicron CMOS processes allows for an unprecedented degree of scaling and integration in digital circuitry, but complicates implementation of traditional RF circuits. Furthermore, any mask adders for RF/analog circuits are not acceptable from a fabrication cost standpoint. Consequently, a strong incentive has arisen to find digital architectural solutions to the RF functions. Our primary approach to reduce the cost, area and power consumption of the complete mobile handset solutions is through integration of the conventional RF functions with the DBB and AP.

The first demonstration of a fully digital frequency synthesizer and transmitter for RF wireless applications was presented at ISSCC in 2004 [3]. The all-digital PLL (ADPLL) is a foundation of the first-generation Digital Radio Frequency Processor (DRP™) implementing a single-chip fully compliant Bluetooth radio. It was realized in a 130-nm digital CMOS technology without any analog process enhancements.

In this paper, we present details of a local oscillator and transmitter part of the second generation DRP, which was presented at ISSCC in 2005 [4]. It is implemented in 90-nm CMOS and targets single-chip Global System for Mobile Communications (GSM) cellular radios, which are widely considered most challenging from the RF circuit performance perspective. The ADPLL phase noise performance is significantly improved in comparison with [3] through architectural and circuit enhancements, and its wideband frequency modulation capability is extended to accommodate the wider frequency deviations required for the 8-PSK modulation of Enhanced Data for GPRS Evolution (EDGE). To complete the polar TX modulation path, a fully digital amplitude modulation circuit is added. (For a good overview of polar transmitters, see [5] and [6].)

The organization of this paper is as follows: Section II presents on overview of the single-chip GSM/EDGE transceiver based on the second generation of DRP. Section III applies the new paradigm of the deep-submicron CMOS environment to the RF transmitter and local oscillator design. The digitally controlled oscillator and digitally controlled power

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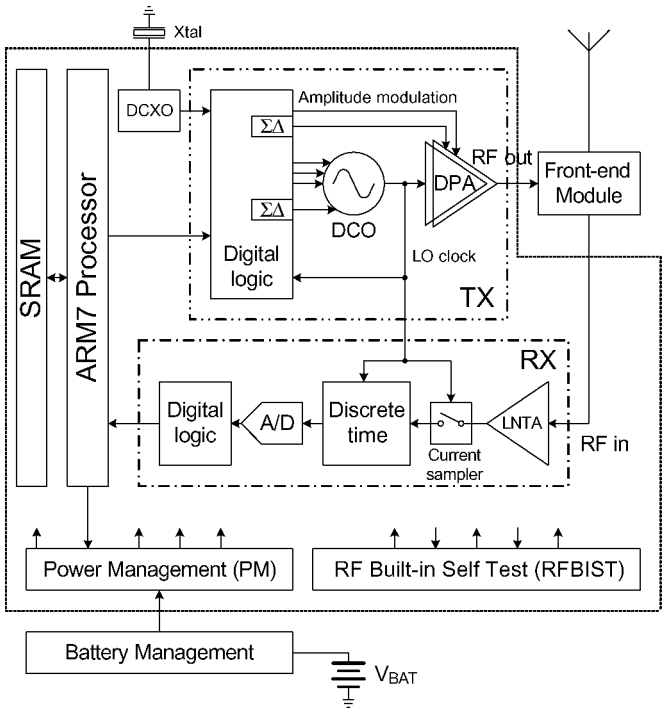

Fig. 1. Single-chip GSM/EDGE transceiver with an all-digital local oscillator and transmitter, and a discrete-time receiver. The TX block is the focus of this paper.

amplifier are described in Section IV and Section V, respectively. Section VI presents the all-digital PLL with wideband direct frequency modulation capability, while Section VII describes the amplitude modulation circuitry. The experimental results are given in Section VIII.

II. Digital RF Processor Overview

Fig. 1 gives an overview of key circuits of the single-chip GSM/EDGE transceiver, with the local oscillator and transmitter being the focus of this paper. At the heart lies a *digitally controlled oscillator* (DCO) [7], which deliberately avoids any analog tuning controls. Fine frequency resolution is achieved through high-speed $\Sigma\Delta$ dithering of its varactors. As first suggested in [8], a digital logic built around the DCO realizes an all-digital PLL that is used as a local oscillator for both the transmitter and receiver. The polar transmitter architecture utilizes the wideband direct frequency modulation capability of the ADPLL [9] and a *digitally controlled power amplifier* (DPA) [10] for the power ramp and amplitude modulation. The DPA operates in near-class-E mode and uses an array of NMOS transistor switches to regulate the RF amplitude. It is followed by a matching network and an external front-end module, which comprises a power amplifier (PA) and a transmit/receive switch for the common antenna. Fine amplitude resolution is achieved through high-speed $\Sigma\Delta$ dithering of the DPA NMOS transistors. The receiver employs a discrete-time architecture [11] in which the RF signal is directly sampled at Nyquist rate of the RF carrier and processed using analog and digital signal processing techniques. The transceiver is integrated with a dedicated ARM7 processor and SRAM memory. The frequency reference (FREF) is generated on-chip by a 26 MHz digitally controlled crystal oscillator (DCXO). The integrated power management (PM) is connected to an external battery management circuit that conditions and stabilizes the supply voltage. The PM consists of multiple low-dropout (LDO) voltage regulators that provide internal supply voltages and also isolate supply noise between circuits, especially protecting the DCO. The RF built-in self-test (RFBIST) performs autonomous phase noise and modulation distortion testing as well as various loopback configurations for bit-error-rate measurements. Almost all the clocks on this SoC are derived from and are synchronous to the RF oscillator clock. This helps to reduce susceptibility to the noise generated through clocking of the massive digital logic.

III. RF Transmitter in Deep-Submicron CMOS

A new paradigm facing analog and RF designers of deep-submicron CMOS circuits was formulated in [12] and is repeated below:

> In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals.

A successful design approach in this environment would exploit the paradigm by emphasizing the following:

- fast switching characteristics or high f_T (40 ps and 100 GHz in this process, respectively) of MOS transistors: high-speed clocks and/or fine control of timing transitions;
- high density of digital logic (250 kgates/mm^2 in this process) makes digital functions extremely inexpensive;
- small device geometries and precise device matching made possible by the fine lithography;

while avoiding the following:

- biasing currents that are commonly used in analog designs;
- reliance on voltage resolution;
- nonstandard devices that are not needed for memory and digital circuits.

Fig. 2 illustrates an application of the new paradigm to an RF wireless transmitter performing an arbitrary quadrature amplitude modulation (QAM). The low cost of digital logic allows for a sophisticated digital signal processing. The tiny and well matched devices allow for precise and high-resolution conversions from digital to analog domains. The use of ultra high-speed clocks, i.e., high oversampling ratios, can eliminate the need for subsequent dedicated reconstruction filtering of spectral replicas and switching transients, so that only the natural filtering of an oscillator ($1/s$ due to the frequency-to-phase conversion), matching network of power amplifier and antenna filter are relied upon. Since the converters utilize DCO clocks that are of high spectral purity, the sampling jitter is very small. The sampling jitter is not significantly affected by modulation, since, as shown in [13], the jitter due to modulation is not greater than the oscillator thermal jitter. The conversion functions covered in this paper are phase/frequency and amplitude modulations of an RF carrier realized using a DCO and a digitally controlled power amplifier (DPA) circuits, respectively. They are

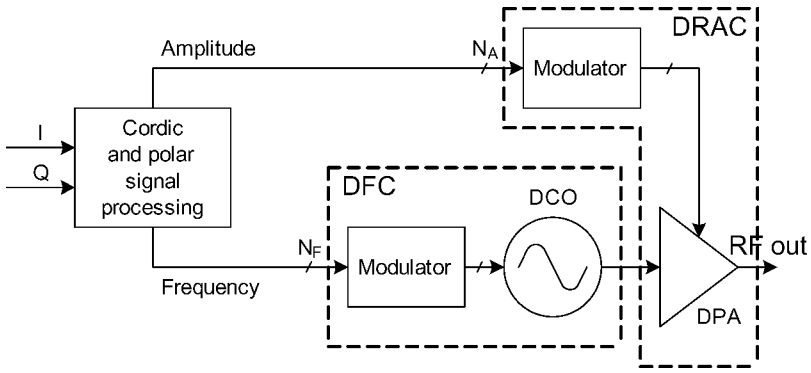

Fig. 2. Polar transmitter based on a DCO and DPA circuits. For simplicity, the all-digital PLL around the DCO is not shown.

digitally intensive equivalents of the conventional voltage-controlled oscillator (VCO) and power amplifier driver circuits. Due to the fine feature size and high switching speed of the modern CMOS technology, the respective *digital-to-frequency conversion* (DFC) and *digital-to-RF-amplitude conversion* (DRAC) transfer functions could be made very linear and of high dynamic range.

The chosen architecture is polar, as it implements the amplitude and phase modulations in separate paths. The I and Q samples of the Cartesian coordinate system generated in the digital baseband (DBB) processor are converted through a CORDIC algorithm into amplitude and phase samples of the polar coordinate system. The phase is then differentiated to obtain frequency deviation. The polar signals are subsequently conditioned through signal processing to sufficiently increase the sampling rate in order to reduce the quantization noise density and lessen the effects of the modulating spectrum replicas. The frequency deviation output signal is fed into the DCO-based N_F-bit DFC, which produces the *phase modulated* (PM) digital carrier:

$$y_{PM}(t) = sgn\left(cos\left(\omega_0 t + \theta[k]\right)\right) \tag{1}$$

where $sgn(x) = 1$ for $x \geq 0$ and $sgn(x) = -1$ for $x < 0$, $\omega_0 = 2\pi f_0$ is the angular RF carrier frequency, and $\theta[k]$ is the modulating baseband phase of the kth sample. The phase $\theta(t) = \int_{-\infty}^{t} f(t)dt$ is an integral of frequency deviation, where $t = k \cdot T_0$ with T_0 being the sampling period.

The *amplitude modulation* (AM) signal controls the envelope of the phase-modulated carrier by means of the DPA-based N_A-bit DRAC. Higher-order harmonics of the digital carrier are filtered out by a matching network so that the $sgn()$ operator is dropped. The composite DPA output contains the desired RF output spectrum.

$$y_{RF}(t) = a[k] \cdot cos\left(\omega_0 t + \theta[k]\right) \tag{2}$$

where $a[k]$ is the modulating baseband amplitude of the kth sample.

Despite their commonalities there are important differences between the two conversion functions. Due to the narrowband nature of the communication system, the DFC operating range is small but with a fine resolution. The DRAC operating range, on the other hand, is almost full scale, but not as precise. In addition, the phase modulating path features an additional $1/s$ filtering caused by the frequency-to-phase conversion of the oscillator. Of course, the signal processing and delay between the AM and PM paths should be matched, otherwise the recombined composite signal will be distorted. Fortunately, the matching invariability to the process, voltage and temperature changes is guaranteed by the clock-cycle accurate characteristics of digital circuits. The group delay of DCO and DPA circuits is relatively small (tens of picoseconds due to the high f_T of the deep-submicron CMOS devices) in comparison with the tolerable range (tens of nano-seconds).

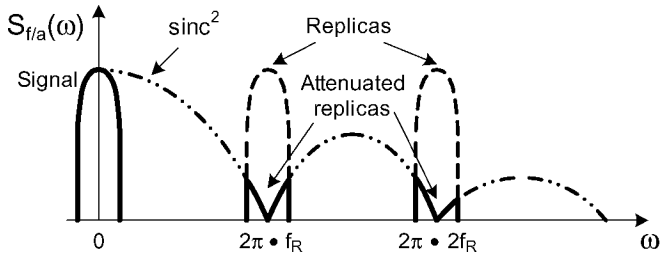

Fig. 3. Spectral replicas of the modulating signal and their filtering through zeroth-order hold. Additional 6 dB/octave filtering from $S_f(\omega)$ to $S_\phi(\omega)$ is inherently provided by the DCO.

The DFC and DRAC are key functions of the all-digital transmitter that does not use any current biasing or dedicated analog continuous-time filtering in the signal path. In order to improve matching, linearity, switching noise and operational speed, the operating conversion cells (bit to frequency or RF carrier amplitude) are mainly realized as unit weighted. Due to the excellent device matching characteristics in a deep-submicron CMOS process, it is relatively easy to guarantee 7-bit conversion resolution in one iteration cycle without resorting to elaborate layout schemes. The DFC and DRAC architectures are presented below. It should be noted that there appear to be no other reports of all-digital wireless RF transmitters in the literature.

Spectral replicas of the discrete-time modulating signal appear at the DCO and DPA inputs at integer multiplies of the sampling rate frequency f_R, as shown in Fig. 3. They are attenuated through multiplication of the sinc^2 function due to the zero-order hold of the DCO/DPA input. The frequency spectrum $S_f(\omega)$ replicas are further attenuated by 6 dB/octave through the $1/s$ operation of the oscillator to finally appear at the RF output

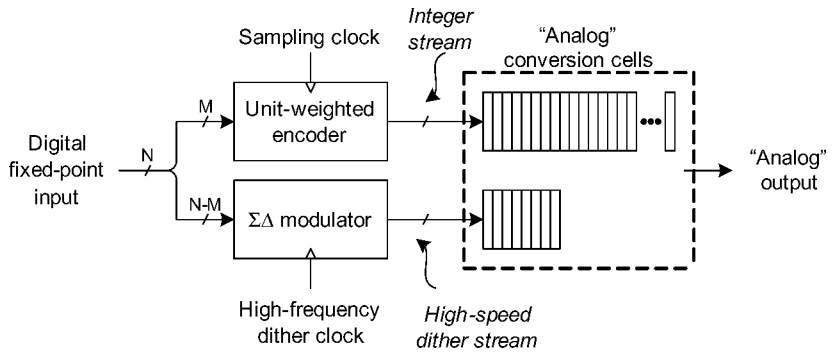

Fig. 4. Digital modulator as part of a generic DAC.

phase spectrum $S_\phi(\omega)$. The sampling rate of $f_R = 26$ MHz is high enough for the replicas to be sufficiently attenuated, thus making the RF signal undistinguishable from that created by the conventional transmitters with continuous-time filtering at baseband.

A. Generic Modulator

The two modulators in Fig. 2 could be considered a digital front-end of a generic *digital-to-analog converter* (DAC), where "analog" stands here either for the frequency or RF carrier amplitude. For the reasons stated above, the cell elements of the physical converters are unit weighted. Consequently, the simplest realization of the modulator would be a binary-to-unit-weighted converter.

Unfortunately, the above arrangement would not be practical due to the limited resolution of the conversion process. For example, the 12 kHz frequency step of the DFC is not adequate for a GSM modulation where the peak frequency deviation is 67.7 kHz. Likewise for the amplitude modulation, the 6-bit amplitude resolution is also too coarse.

In this design, finer conversion resolution is achieved through high-speed dithering of the finest conversion cell elements, as shown in Fig. 4. The N-bit digital fixed-point input is split into M integer (higher-order) bits and $N - M$ fractional (lower-order) bits. The integer word sets the number of activated conversion elements. The fractional word is fed to a $\Sigma\Delta$ modulator that produces a high-speed dithering stream whose average value is equal to the fractional part of the fixed-point input word.

It should be noted that this DAC architecture is similar to [14] but with significant differences to allow higher-frequency operation at reduced power consumption. The lower-rate wide-buswidth integer stream is never merged in digital domain with the higher-rate dithering stream. The final stream addition is done in the device cell domain: In the DCO, the varactor capacitances are added, and in the DPA, the transistor resistances and driving strengths are added. This way, the high-speed operation is constrained to a small portion of the circuit, thus saving the current consumption. A detailed description of the DCO modulator for Bluetooth was given in [8].

IV. Digitally Controlled Oscillator

A DCO is used to perform the digital-to-frequency conversion (DFC). The DCO, which was first reported in [7] for RF wireless applications, lies at the heart of the ADPLL-based frequency synthesizer that acts as a local oscillator for the transmitter and receiver. The DCO deliberately avoids any analog tuning controls.

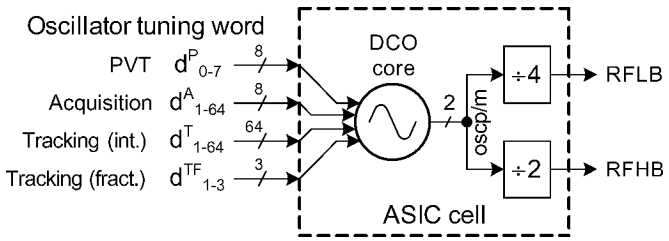

Fig. 5. DCO and high-band and low-band dividers built as an ASIC cell.

The 3.6 GHz oscillator core, low-band (LB) and high-band (HB) dividers are built as a single ASIC cell (Fig. 5) with digital I/Os, even at the HB RF output frequency of 1.8 GHz since the rise and fall times are designed to be less than 50 ps. The single DCO is shared between the transmitter and receiver. The oscillator core nature is analog, but the analog nature does not propagate beyond the ASIC boundaries. Consequently, the circuitry built around it for the purpose of phase/frequency locking can be fully digital.

Frequency planning of the four TX and four RX bands of the GSM specification, which are supported by this design with a single oscillator, is graphically shown in Fig. 6. The DCO core operates in the 3.2–4.0 GHz region with 100 MHz tuning margin. The high and low bands are obtained by dividing the DCO core frequency by two and four, respectively. The full 3.2–4.0 GHz range constitutes a relative extent of 22.2%. The individual TX and RX bands constitute narrower relative frequency ranges, the widest of which is the DCS-1800 TX band of 2.1%. The most stringent phase noise requirement of a GSM oscillator is derived based on the emission specification from the 880–915 MHz TX band into the original 935–960 MHz RX band. Hence, if TX SAW filters are to be avoided, the low-band oscillator phase noise at 20–80 MHz frequency offset shall be < -162 dBc/Hz.

The new varactors and the DCO core structure result in better phase noise than in [16], which is needed to meet the stricter GSM requirements. Fig. 7 shows a simplified schematic of the DCO core whose topology is similar to [15]. L_{1A} and L_{1B} comprise the center-tapped inductor of the resonant tank. The total metal thickness of all inductor layers is lower than 2 μm. NMOS

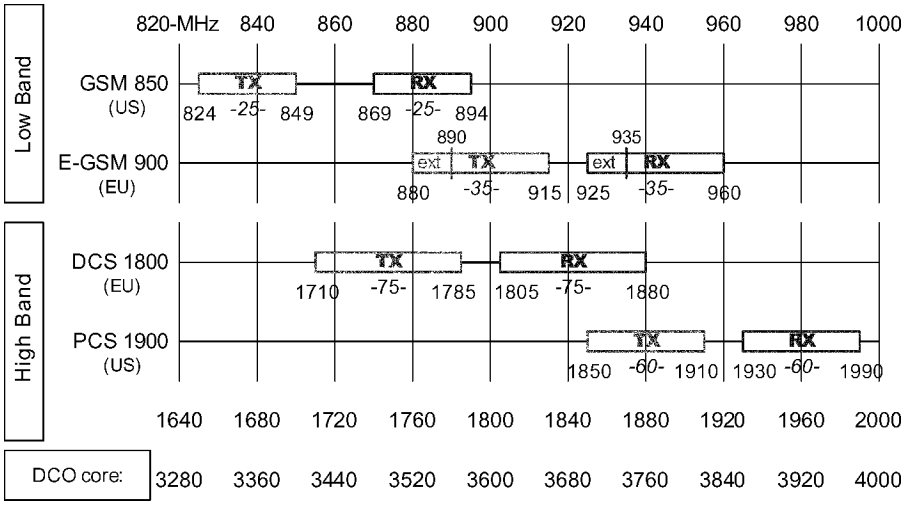

Fig. 6. GSM frequency bands.

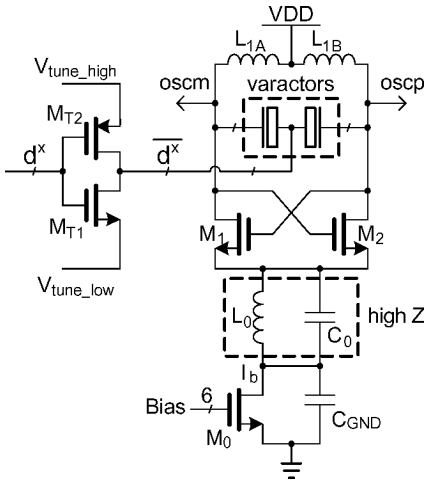

Fig. 7. Oscillator core and the varactor state driver array.

is used for the cross-coupled pair, M_1 and M_2, because in this process it has a lower 1/f noise than that of PMOS. When M_0 is operated in the saturation region, it can contribute as much as 15% to the total phase noise, hence it was biased in the linear region. Although functionally M_0 may be eliminated, it was kept to reduce the phase noise sensitivity to supply noise. M_0 resistance is established through the calibrated 6-bit digital word to yield adequate DCO phase noise performance at minimum current. The second resonator operating at $2\times$ of the main resonant frequency providing high-Z [15] improves effective/loaded tank Q. C_{GND} is a 40 pF NMOS capacitor to bring bottom node of the high-Z tank to an ac ground and to reduce up-conversion of high-frequency noise from the bias circuit. For phase noise performance reasons, the internal sinusoidal differential DCO output, oscp/m, directly drives the NMOS and PMOS gates of the dividers. This is acceptable, since the peak-to-peak single-ended voltage swing is greater than V_{DD}. All the varactors are realized as n-poly/n-well MOSCAP devices that operate in the flat regions of their *C–V* curves (see [7] for an example of the measured *C–V* curve). There will be, however, a certain amount of frequency pushing (20 MHz/V) due to the voltage-dependent parasitic capacitances of the transistor junctions as well as the *C–V* curve operating point shift. Generally, the two *C–V* curve operating points, `V_tune_high` and `V_tune_low`, will depend on the specific process. Here, they are conveniently set to 1.4 V and ground, respectively.

The four DCO input buses comprise the raw *oscillator tuning word* (OTW) that is analogous to the tuning voltage of a VCO. Their bits individually control capacitative states of the LC-tank varactors, thus establishing the LC-tank resonating frequency. The d^P and d^A inputs correspond to the process-voltage-temperature (PVT) and acquisition banks, respectively, and are activated sequentially during frequency locking and are frozen afterwards [16]. The d^T and d^{TF} inputs comprise the integer tracking and fractional tracking bits, respectively, and are used during the actual RF transmission and reception. The integer tracking bus is unit-weighted and is clocked at the 26 MHz reference frequency of the phase comparison. The fractional tracking inputs serve to enhance the DCO frequency resolution through high-speed $\Sigma\Delta$ dithering. Table I summarizes the varactor banks arrangement. The DCO interface logic is described in [8] for the previous generation of DRP.

V. Digitally-Controlled Power Amplifier

The DPA circuit, which acts as a digital-to-RF-amplitude converter (DRAC) is used for the power ramp and amplitude modulation. It operates as a near-class-E RF power amplifier and is driven by the square wave output of the DCO dividers. There are two DPAs, each covering either GSM-850/EGSM-900 or DCS-1800/PCS-1900 bands. The basic structure has been originally reported in [3] to regulate RF power of the Bluetooth transmitter. In Fig. 8, the core NMOS transistors M1X, where $x = a, b, \ldots n$, are used as on/off switches. A radio-frequency choke (RFC) acts as a bi-directional current source, connecting the switch to the on-chip supply voltage regulator. C1 represents the on-chip capacitor connected in parallel to the switch and includes, for analysis purposes, the equivalent capacitance over one cycle given by the nonlinear C_{DD} of M1X. The residual second harmonic of the transmit frequency is filtered by C2 and L1, allowing the

TABLE I
DCO VARACTOR BANKS. Δf IS AT THE HIGH-BAND OUTPUT

Varactor bank	Input	Weighting	Step size Δf
PVT	d^P	8-bit binary	Δf^P = 4 MHz
Acquisition	d^A	64-bit unit	Δf^A = 200 kHz
Tracking int.	d^T	64-bit unit	Δf^T = 12 kHz
Tracking fract.	d^{TF}	3-bit unit	Δf^T = 12 kHz

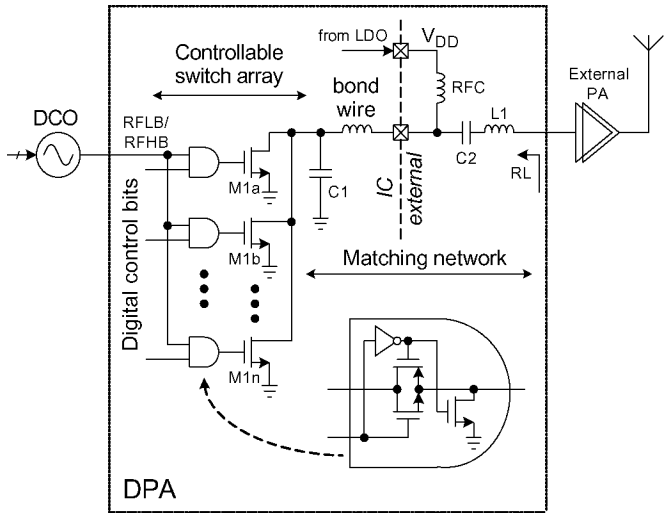

Fig. 8. Digitally controlled PA structure. The quad-band transmitter consists of two such units.

DRAC itself to remain a single-ended circuit, reducing needed matching network components and pin count. The matching network components are chosen to approach the condition where the switch output is critically damped, such that the drain voltage is low when the output current is high and vice versa.

The control logic for each M1X switch comprises an AND gate whose inputs are the phase-modulated output of the DCO and the amplitude control word from the digital modulator block. It is the on-resistance of the switch that is exploited in the DRAC concept to introduce power control of the transmitted waveform and allows the fully digital method of controlling the output power.

In this deep-submicron CMOS technology, the ratio between the maximum output power that can be provided from a maximum supply of 1.4 V to the minimum output power of a single transistor dictates the maximum number of transistors that can be implemented in the DPA. In this design, 64 parallel-connected transistors that result in 6 bits of basic amplitude resolution were selected to simplify the layout.

VI. ALL-DIGITAL PLL

Per PLL classification in R. E. Best's reference [17], the proposed frequency synthesizer is not a classical *digital PLL* (DPLL), which actually is considered a semi-analog circuit, but an *all-digital PLL* (ADPLL) with all building blocks defined as digital at the input/output level. It uses digital design and circuit techniques from the ground up. At the heart lies a DCO, which deliberately avoids any analog tuning voltage controls. This allows for its loop control circuitry to be implemented in a fully digital manner. The DCO is analogous to a flip-flop—the cornerstone of digital circuits—whose internals are analog, but the analog nature does not propagate beyond its boundaries. So far, except for the previous generation of DRP, there are no other similar architectures reported in the literature.

Fig. 9 shows the proposed RF transmitter based on an all-digital PLL frequency synthesizer with a digital direct frequency modulation capability. The expected *variable frequency* (f_V) is related to the *reference frequency* (f_R) by the *frequency command word* (FCW).

$$FCW[k] \equiv \frac{\mathcal{E}\left(f_V[k]\right)}{f_R}. \tag{3}$$

The FCW is time variant and is allowed to change with every cycle $T_R = 1/f_R$ of the frequency reference clock. With $W_F = 24$ fractional part wordlength of FCW, the ADPLL provides fine frequency control with 1.5 Hz accuracy, according to:

$$\Delta f_{\text{res}} = \frac{f_R}{2^{W_F}}. \tag{4}$$

The number of integer bits $W_I = 8$ was chosen to fully cover the GSM band frequency range of $f_V = 1600$–2000 MHz with an arbitrary reference frequency $f_R \geq 8$ MHz.

The ADPLL sequencer traverses through the PVT calibration and acquisition modes during channel selection and frequency locking and stays in the tracking mode during the transmission or reception of a burst. To extend the DCO range to accommodate for voltage and temperature drifts, and to allow wide frequency modulation, the coarser-step acquisition bits are engaged by subtracting an equivalent number (generally fractional) of the tracking bank varactors. The varactor frequency step calibration is conveniently performed just before each burst [9] with minimal overhead using dedicated hardware.

A. Phase-Domain Operation

The phase domain operation is motivated by an observation [18], that, since the reference phase and oscillator phase are in a linear form, their difference produced by the phase detector is also linear with no spurs and the loop filter would not be needed. This is in contrast with conventional charge-pump-based PLLs, whose phase detection operation is correlational and generates significant amount of spurs that require a strong loop filter that degrades the transients and limits the switching time.

The ADPLL operates in a digitally synchronous fixed-point phase domain [19] as follows: The variable phase $R_V[i]$ is determined by counting the number of rising clock transitions of the DCO oscillator clock CKV

$$R_V[i] = \sum_{l=0}^{i} 1. \tag{5}$$

The index i indicates the DCO edge activity. The FREF-sampled variable phase $R_V[k]$, where k is the index of the FREF edge activity, is fixed-point concatenated with the normalized time-to-digital converter (TDC) output $\varepsilon[k]$. The TDC measures and quantizes the time differences between the FREF and DCO edges. The sampled differentiated variable phase is subtracted

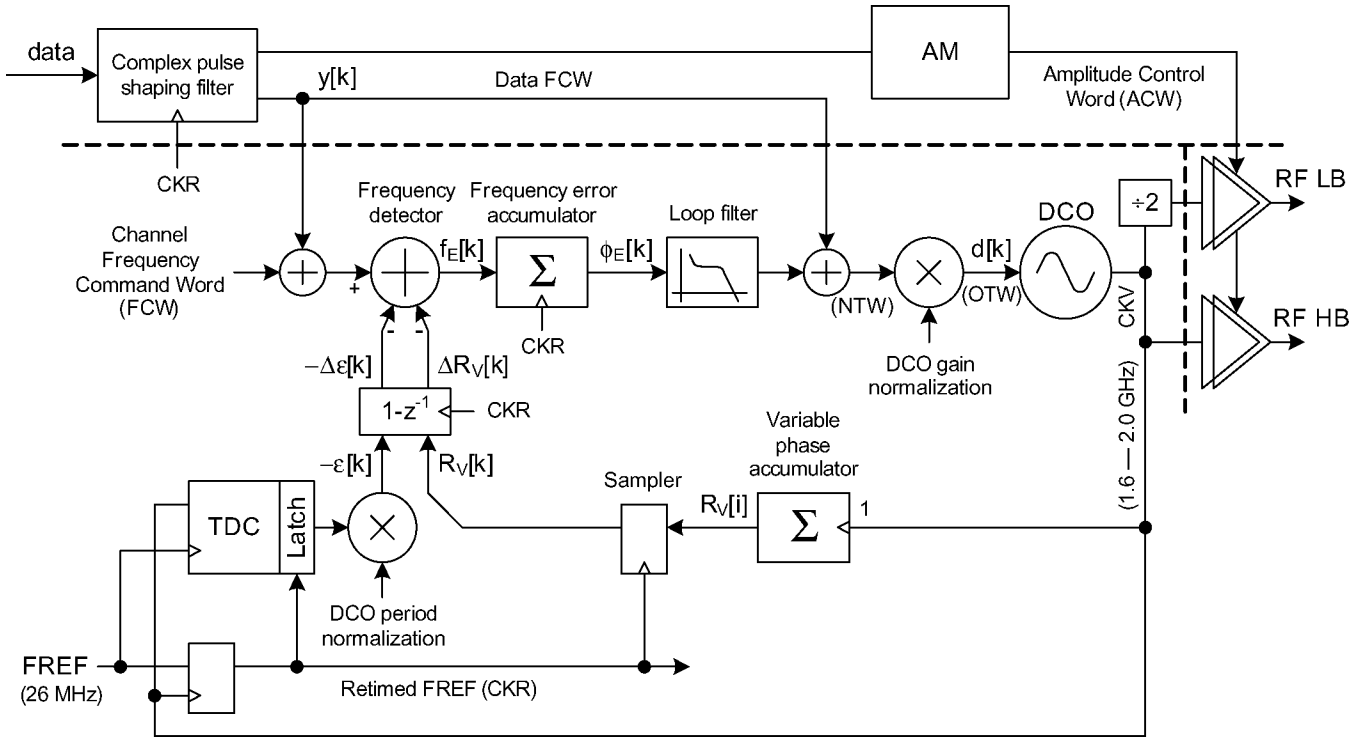

Fig. 9. Polar transmitter based on an all-digital PLL.

from FCW by the digital frequency detector. The frequency error $f_E[k]$ samples

$$f_E[k] = FCW - [(R_V[k] - \varepsilon[k]) - (R_V[k-1]) - \varepsilon[k-1])] \tag{6}$$

are accumulated to create the phase error $\phi_E[k]$ samples

$$\phi_E[k] = \sum_{l=0}^{k} f_E[k] \tag{7}$$

which are then filtered by a fourth-order IIR filter and scaled by a proportional loop attenuator α. A parallel feed with coefficient ρ adds an integrated term to create type-II loop characteristics, which suppresses the DCO flicker noise.

The IIR filter is a cascade of four single stage filters, each satisfying the following equation:

$$y[k] = (1-\lambda)\cdot y[k-1] + \lambda \cdot x[k] \tag{8}$$

where $x[k]$ is the current input, $y[k]$ is the current output, and λ is the configurable coefficient. The 4-pole IIR filter attenuates the reference and TDC quantization noise at the 80 dB/dec slope, primarily to meet the GSM spectral mask requirements at 400 kHz offset. The filtered and scaled phase error samples are then multiplied by the DCO gain K_{DCO} normalization factor $f_R/\widehat{K}_{DCO}$, where f_R is the reference frequency and $\widehat{K}_{DCO}$ is the DCO gain estimate, to make the loop characteristics and modulation independent from K_{DCO}. The modulating data is injected into two points of the ADPLL for the direct frequency modulation [9]. A hitless gear-shifting mechanism for the dynamic loop bandwidth control serves to reduce the settling time. It changes the loop attenuator α several times during the frequency locking while adding the $(\alpha_1/\alpha_2 - 1)\phi_1$ dc offset to the phase error, where indices 1 and 2 stand for before and after the event, respectively. Of course, $\phi_1 = \phi_2$, since the phase is to be continuous.

The FREF input is resampled by the RF oscillator clock, and the resulting *retimed clock* (CKR) is used throughout the system. This ensures that the massive digital logic is clocked after the quiet interval of the phase error detection by the TDC.

B. Direct Frequency Modulation

The frequency modulation uses a hybrid of a predictive/closed-loop modulation method [9]. Referring to Fig. 10, which contains only necessary details of Fig. 9, the fixed-point FCW modulating data $y[k]$, with the sampling rate of f_R, directly affects the oscillating frequency. The PLL loop will try to correct this perceived frequency perturbation integrated over the update period of $1/f_R$. This corrective action is compensated by the other (compensating) $y[k]$ feed that is integrated by the reference phase accumulator. The loop response to $y[k]$ is wideband and $y[k]$ directly modulates the DCO frequency in a feed-forward manner such that it effectively removes the loop dynamics from the modulating transmit path. However, the rest of the loop, including all error sources, operates under the normal closed-loop regime.

C. DCO Gain Normalization

At a higher level of abstraction, the DCO oscillator, together with the DCO gain normalization $f_R/\widehat{K}_{DCO}$ multiplier, logically comprise the *normalized DCO* (nDCO), as illustrated in Fig. 11. The DCO gain normalization conveniently decouples the phase and frequency information throughout the system from the process, voltage and temperature variations that normally affect the K_{DCO}. The frequency information is

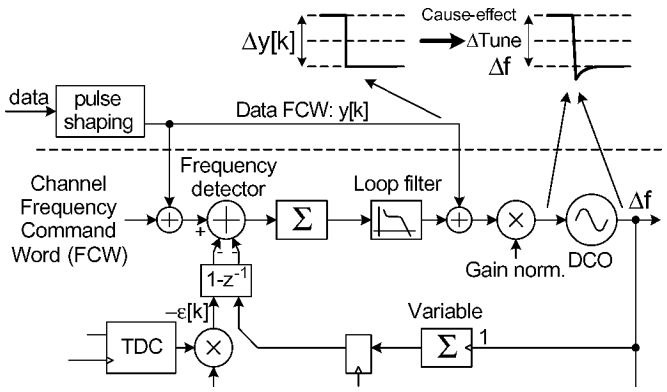

Fig. 10. Wideband frequency modulation of ADPLL.

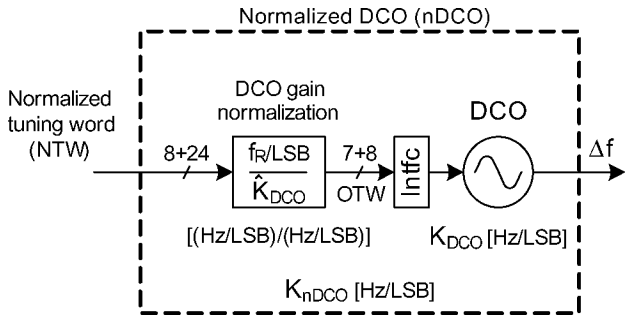

Fig. 11. Hardware abstraction layer of the normalized DCO.

normalized to the value of the external reference frequency f_R. The digital input to the nDCO is a fixed-point *normalized tuning word* (NTW), whose integer part LSB bit corresponds to f_R. The reference frequency is chosen as the normalization factor because it is the master basis for the frequency synthesis. In addition, the clock rate and update operation of this discrete-time system are established by the reference frequency.

The quantity K_{DCO} should be contrasted with the process-temperature-voltage-independent oscillator gain K_{nDCO} which is defined as the frequency deviation (in Hz units) of the DCO in response to the 1 LSB change of the integer part of the NTW input. If the DCO gain estimate is exact, then $K_{nDCO} = f_R/LSB$, otherwise

$$K_{nDCO} = \frac{f_R}{LSB} \cdot \frac{K_{DCO}}{\widehat{K}_{DCO}} = \frac{f_R}{LSB} \cdot r. \tag{9}$$

Dimensionless ratio $r = K_{DCO}/\widehat{K}_{DCO}$ is a measure of the DCO gain estimation accuracy.

D. Time-to-Digital Converter

Due to the DCO edge counting nature, the phase quantization resolution as described above is limited to $\pm(1/2)$ of the variable or DCO clock cycle, T_V. For wireless applications, a finer phase resolution is required, which may be achieved *without* forsaking the digitally intensive approach. The whole-clock-domain quantization error ε is corrected by means of a fractional error correction circuit which is based on a TDC. The TDC measures the fractional delay difference between the reference clock and the next rising edge of the DCO clock, as shown in Fig. 12. Its resolution is a single inverter delay, Δt_{inv}, which

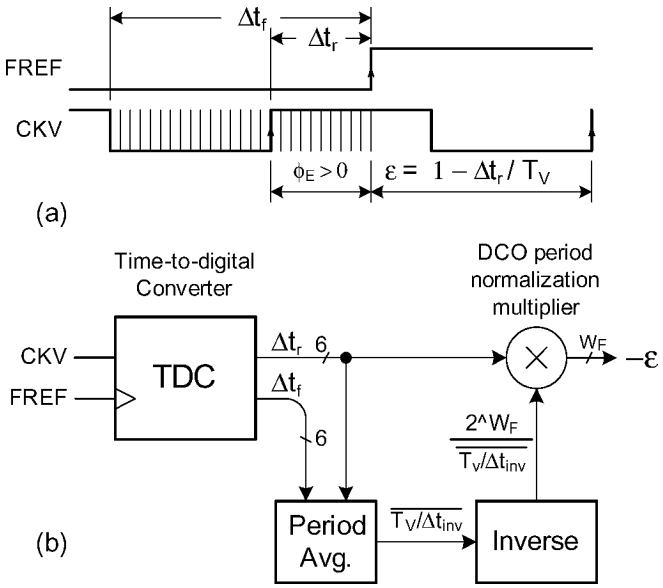

Fig. 12. Fractional phase error estimation based on a TDC.

in this deep-submicron CMOS process is considered the most stable logic-level regenerative delay and is shorter than 20 ps. This allows the implementation of a GSM-quality phase detection mechanism, as evidenced by the excellent close-in and rms phase noise measurement results presented in Section VIII. The TDC is an example of another application of the new paradigm of Section III. It utilizes the fine resolution of digital edge timing transitions.

The TDC used in this design has almost identical structure as that used in the first generation of DRP for Bluetooth and described in detail in [10]. The key differences are: better time resolution due to the process technology advancement (20 ps vs. 30 ps), and higher number of inverter/flip-flop cells (48 vs. 24) due to faster inverters and longer operational DCO clock periods.

1) TDC Resolution Effect on Phase Noise: The TDC quantization of timing estimation Δt_{inv} affects the in-band RF output phase noise of the ADPLL of Fig. 9 according to [21]:

$$\mathcal{L} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{\text{inv}}}{T_V}\right)^2 \cdot \frac{1}{f_R} \tag{10}$$

where T_V is the DCO clock period and f_R is the reference or sampling frequency. Substituting $\Delta t_{\text{inv}} = 20$ ps, $f_R = 26$ MHz, $f_0 = 1.8$ GHz, $T_V = 556$ ps, we obtain $\mathcal{L} = -97.8$ dBc/Hz. Equation (10) was validated experimentally within 1 dB of measurement error for Δt_{inv} spanning 16–34 ps through varying the TDC supply voltage. The in-band phase noise performance provides ample margin for the GSM operation: measured 0.5° of the modulated rms phase noise [4] versus the spec of 5°. The next generations of deep-submicron CMOS processes can only bring reductions in Δt_{inv}, so the phase noise performance will further improve.

E. Frequency Response of Type-II Sixth-Order PLL

The ADPLL is a discrete-time sampled system implemented with all digital components connected with all digital signals.

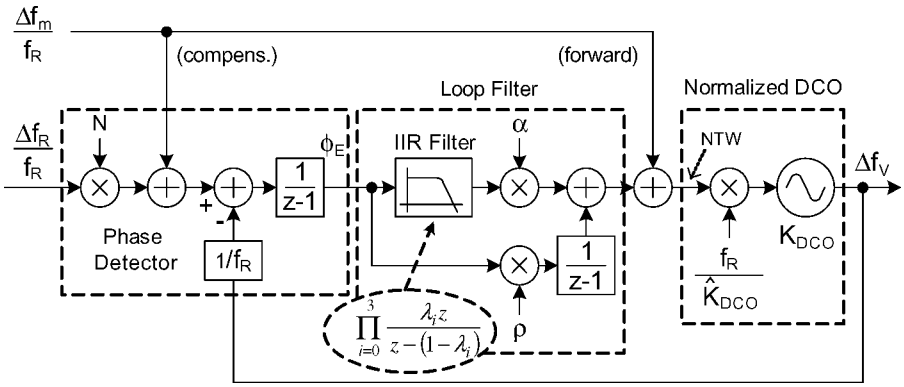

Fig. 13. z-domain model of the ADPLL with wideband frequency modulation.

Consequently, the z-domain representation is not only the most natural fit but it is also the most accurate with no necessity for those approximations that would result, for example, with an impulse response transformation due to the use of analog loop filter components [20]. Fig. 13 shows the z-domain model. It is based on the description and analysis in [19] for the first generation DRP, but with the following changes here: the phase detection is realized as integration of the frequency detector output; the loop filter contains additional filtering stages; and the direct modulation feeds are included.

The ADPLL implemented in this design uses four independently controlled IIR stages. Equation (11) is a linearized s-domain (based on $z \approx 1 + s/f_R$ conversion formula) open-loop model that includes the four cascaded single-stage IIR filters, each with an attenuation factor λ_i, where $i = 0 \ldots 3$

$$H_{ol}(s) = \frac{\varrho \cdot f_R^2}{s} \cdot \frac{1 + \frac{s}{\varrho \cdot \frac{f_R}{\alpha}}}{s} \cdot \prod_{i=0}^{3} \frac{1 + \frac{s}{f_R}}{1 + \frac{s}{\lambda_i \cdot f_R}}. \qquad (11)$$

The type-II sixth-order loop shows two poles at origin $\omega_{p1} = \omega_{p2} = 0$, four poles at $\omega_{p,3+i} = j\lambda_i f_R$, for $i = 0 \ldots 3$, one zero at $\omega_{z1} = j(\varrho f_R/\alpha)$, and four zeros at $\omega_{z,2+i} = jf_R$, for $i = 0 \ldots 3$.

Since the TDC-based phase detection mechanism of the proposed architecture measures the oscillator timing excursion normalized to the DCO clock cycle, the frequency multiplier $N \equiv FCW$ is not part of the open-loop transfer function and, hence, does not affect the loop bandwidth. This is in contrast to conventional PLLs that use frequency division in the feedback path, but is similar, however, to the PLL architectures with frequency down-conversion (heterodyning) in the feedback path. Phase deviation of the frequency reference, on the other hand, needs to be multiplied by N since it is measured by the same phase detection mechanism normalized to the DCO clock cycle. The same amount of timing excursion on the FREF input translates into a larger phase by a factor of N when viewed by the phase detector.

The closed loop transfer function for the reference is low-pass with the gain multiplier $N \equiv FCW$

$$H_{cl}(s) = N \cdot \frac{H_{ol}(s)}{1 + H_{ol}(s)}. \qquad (12)$$

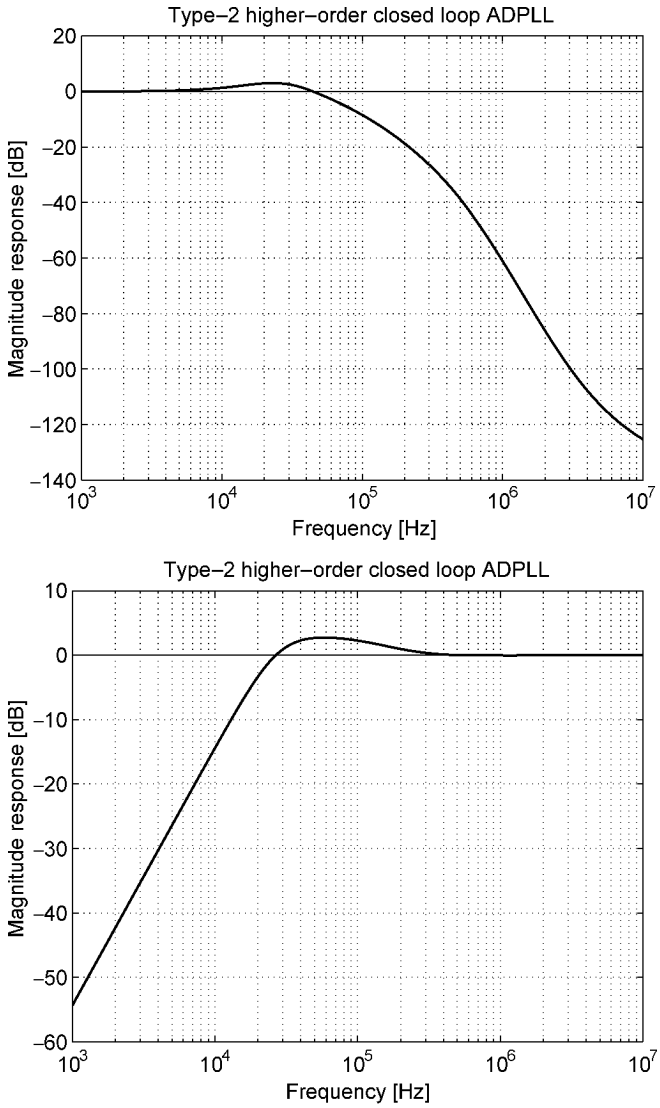

Fig. 14. ADPLL close-loop transfer function for the reference (top) and variable (bottom) with the following loop setting: $\alpha = 2^{-7}$, $\rho = 2^{-15}$ and $\lambda = [2^{-3}, 2^{-3}, 2^{-3}, 2^{-4}]$.

The closed loop transfer function for the TDC is low-pass

$$H_{cl,T}(s) = \frac{H_{ol}(s)}{1 + H_{ol}(s)}. \qquad (13)$$

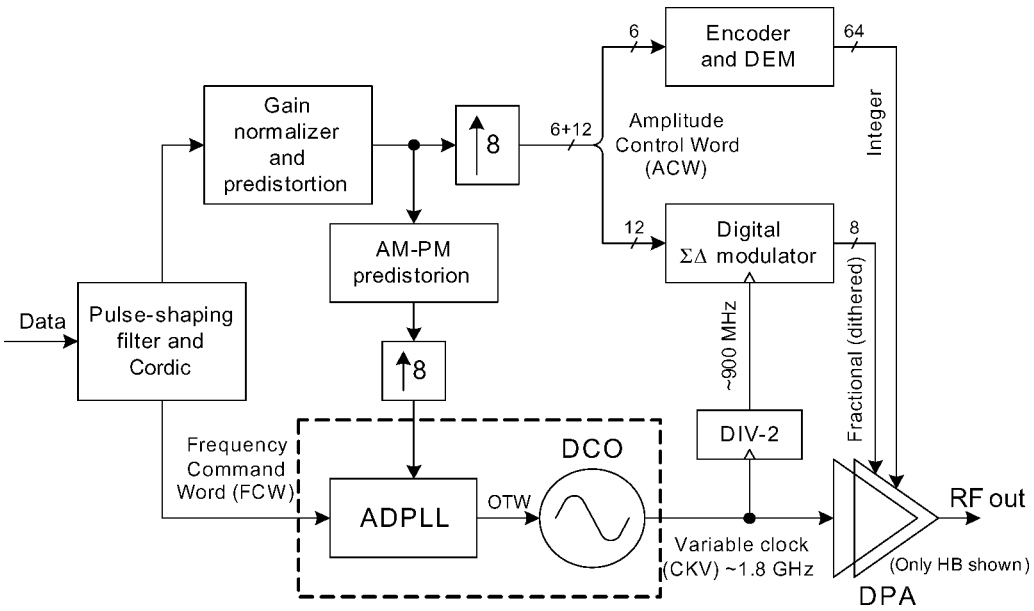

Fig. 15. Amplitude modulation path of the polar transmitter.

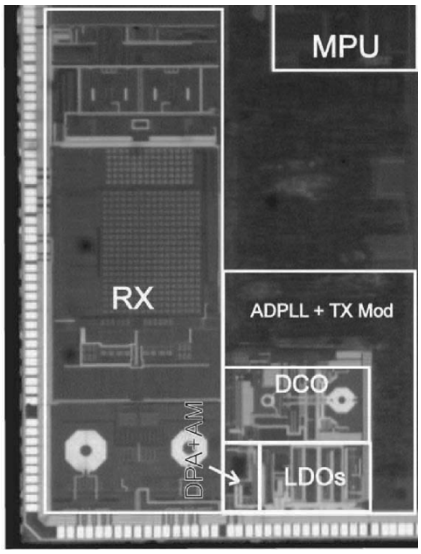

Fig. 16. Die microphotograph.

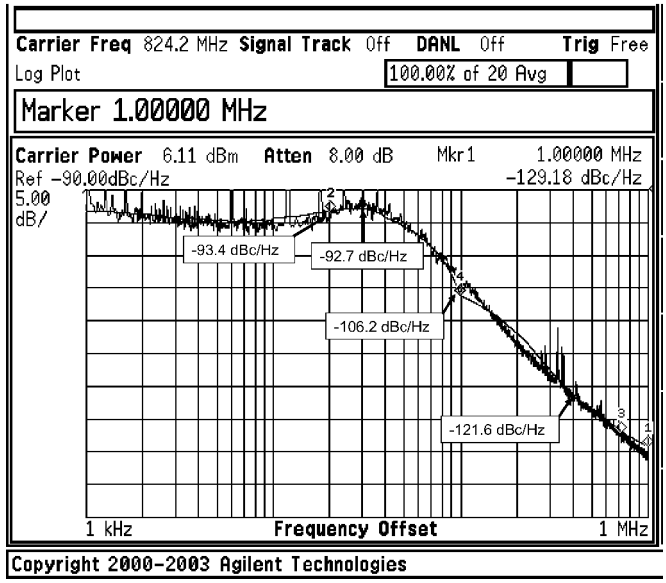

Fig. 17. Measured phase noise of an unmodulated carrier.

The closed loop transfer function for the DCO is high-pass

$$H_{cl,V}(s) = \frac{1}{1 + H_{ol}(s)}. \tag{14}$$

The following loop filter settings: $\alpha = 2^{-7}$, $\rho = 2^{-15}$ and $\lambda = [2^{-3}, 2^{-3}, 2^{-3}, 2^{-4}]$ establish the closed-loop bandwidth of 40 kHz and provide 33 dB of attenuation of the FREF phase noise and TDC quantization noise. The type-II setting provides 40 dB/dec filtering of the DCO 1/f noise. Fig. 14 plots the ADPLL close-loop transfer function for the reference and variable feeds.

VII. Amplitude Modulation

The pulse-shaping filter of Fig. 15 contains separate I and Q filters followed by a CORDIC algorithm to convert to polar-domain phase and amplitude outputs. The sampling rate is 3.25 MHz and is interpolated up to 26 MHz to further smoothen the modulating signals. The phase is differentiated to fit the FCW frequency format of the ADPLL input. The amplitude output is multiplied by the step size of the digitally controlled power amplifier (DPA) and is then AM-AM predistorted. The amplitude control word (ACW) is then converted to the 64-bit unit-weighted format of the DPA. A dedicated bank of 8 DPA transistors undergoes a 900 MHz third-order $\Sigma\Delta$ modulation to enhance the amplitude resolution and to achieve noise spectral shaping. As in the DCO controller, the DPA controller also performs dynamic element matching (DEM) to enhance the time-averaged linearity. In the GSM mode, a single Gaussian pulse shaping filter is used and the CORDIC circuit is bypassed. The AM path is temporarily engaged to ramp the output power to a desired level to remain fixed throughout the payload.

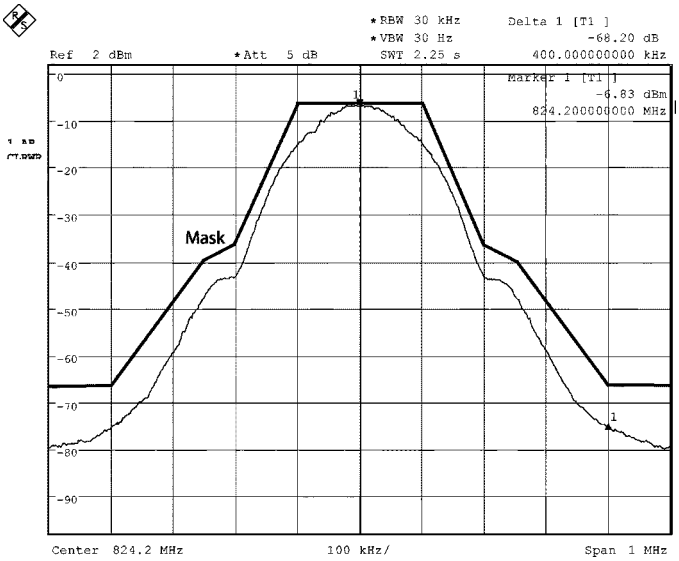

Fig. 18. Measured GSM output spectrum.

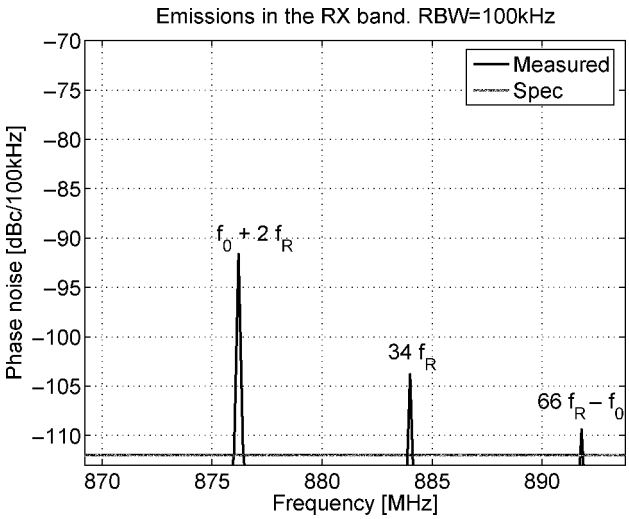

Fig. 19. Measured TX emissions in the RX band. The GSM specification allows for five exceptions. $f_0 = 824.2$ MHz, $f_R = 26$ MHz.

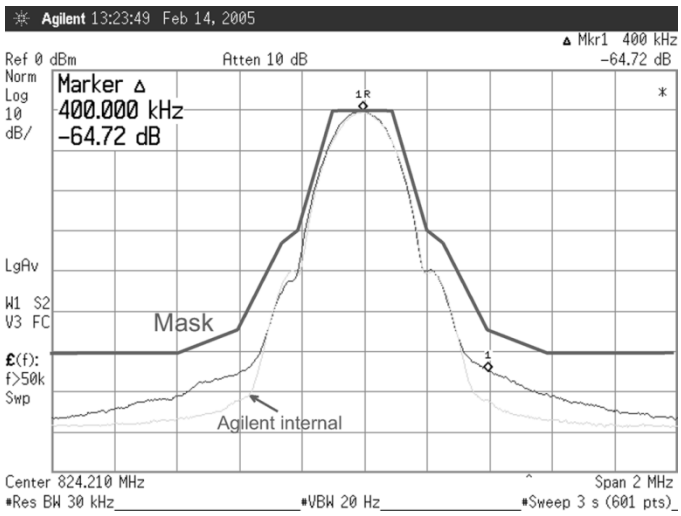

Fig. 20. Measured EDGE output spectrum.

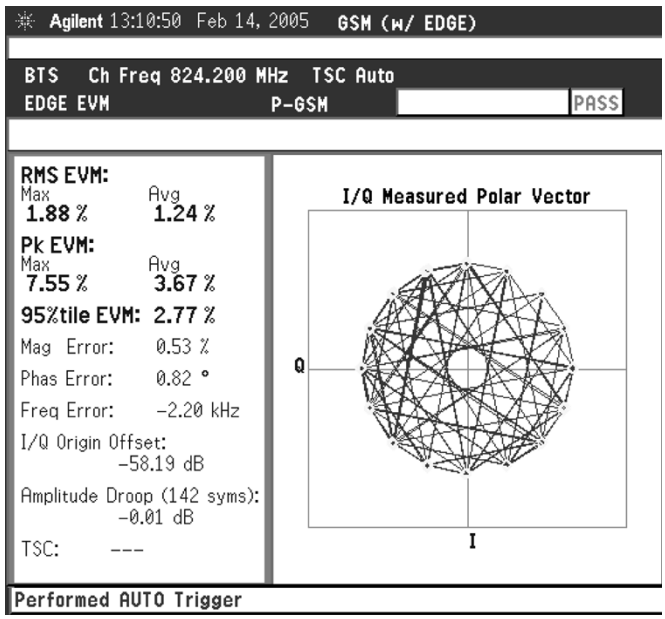

Fig. 21. EDGE constellation and EVM measurements.

VIII. Experimental Results

Fig. 16 shows a microphotograph of the transceiver [4]. The transmitter occupies 1.5 mm^2, which is much smaller than what is found in prior reports. The IC is fabricated in a 90 nm digital CMOS process with no analog extensions. The following parameters characterize the process: minimum metal pitch of 0.27 μm, five levels of copper metal, nominal transistor voltage of 1.2 V, gate oxide thickness of 2.6 nm, logic gate density of 250 kgates/mm^2, SRAM cell density of 1.0 μm^2/bit.

The ICs based on the presented ideas meet all the GSM transmitter specifications. The in-band synthesizer phase noise is measured below -93 dBc/Hz for the loop bandwidth of 40 kHz (Fig. 17). The phase noise at 400 kHz frequency offset from the carrier, which is the most critical point, is -122 dBc/Hz. Fig. 18 shows the modulated spectrum at 2 dBm output power with the resolution bandwidth of 30 kHz against the GSM mask. The 400 kHz frequency offset point has an 8 dB margin against the specification of -60 dB. The measured modulated rms phase error is 0.5° versus the allowed limit of 5°. The far-out reference spurs are below -92 dBc and the far-out phase noise at 20 MHz offset is -165 dBc/Hz, thus eliminating the need for a SAW filter in the TX path. Fig. 19 shows that the TX emissions in the RX band meet the GSM specification, which allows for up to five exceptions (five channels in which the level of spurs or noise within a 100-kHz bandwidth may exceed the -79 dBm/ -71 dBm limits for low and high bands respectively). The spurs are clearly identified: the absolute FREF harmonic at $34f_R$, the second FREF harmonic modulating the DCO at $f_0 + 2f_R$, and their mixing product at $66f_R - f_0$.

The frequency settling time to within the 20 Hz GSM phase-slope error is 10 μs. At 6 dBm output power, the transmitter draws 42 mA from a 1.2 V supply: DCO consumes 18 mA, DPA 6 mA and TDC 1.4 mA. The maximum DPA power was measured at 10 dBm at 50 Ω output load. These measurements

are not significantly affected by digital activity of the processor. The transceiver is fully functional and properly interfaces with layer-1 GSM software, which was demonstrated by a successful phone call over the GSM public network.

The EDGE spectral mask is also met (Fig. 20) with a 10-dB margin at 400- and 600-kHz frequency offsets. As shown in Fig. 21, the rms error vector magnitude (EVM) is 1.2% versus the allowed limit of 9%. The peak EVM is 3.7% versus the 30% limit of the specification.

IX. Conclusion

We have presented a novel architecture of a frequency synthesizer and transmitter for a single-chip fully compliant GSM/EDGE transceiver fabricated in a digital 90 nm CMOS process. The architecture is built from the ground up using digital techniques that exploit the high speed, high density and excellent device matching of a deep-submicron CMOS process while avoiding its weaker handling of voltage resolution. The presented polar transmitter is architectured as two "D/A converters": digital-to-frequency and digital-to-RF-amplitude that are supported by voluminous but inexpensive digital logic. The transmitter architecture is fully digital and takes advantage of the wideband direct frequency modulation capability of the all-digital PLL and a digital control of RF amplitude. The conventional phase/frequency detector and charge-pump combination is replaced by a time-to-digital converter (TDC) and is followed by a digital loop filter that controls a DCO. The presented techniques and principles are extendible to other standards and modulation schemes.

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Sameh Rezeq, photograph and biography not available at the time of publication.

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From 1991 to 1995, he was with the Paul Scherrer Institute, Zurich, Switzerland, where he was involved with Smart pixel optoelectronics. He joined Texas Instruments in Germany in 1995, where he worked on RF process integration, device characterization and modeling, particular the development of RF-CMOS technologies on high resistivity substrates. From 1998 to 1999, he represented Texas Instruments on the ETSI Hiperlan2 committee, where he was editor for the PHY layer technical specification. In 1999, he joined Texas Instruments Incorporated, Dallas, TX, where he is currently a Design Manager of the Digital RF Processor (DRP) group. His research interests include advanced RF architectures, nanometer-scale CMOS processes, and quantum electronics.