All Digital Transistors High Gain Operational Amplifier Using Positive Feedback Technique

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Abstract

New all digital-transistor CMOS very high DC-gain amplifiers that use internal positive-feedback technique are presented. These structures don't require perfect matching of transistors to achieve the very high DC gain, and have a very low gain sensitivity to output swing. An implementation of a sample and hold circuit constructed using one of the proposed amplifiers is described. Special layout pattern is used to cut the parasitic capacitance.

1. Introduction

High gain, accuracy, and high speed are the two most important properties of analog circuits. A variety of analog and mixed signal systems have performance that is limited by the settling behavior of a CMOS amplifier. These include switched capacitor filters, Algorithmic A/D converters, sigma-delta converters, and sample and hold circuits, pipeline A/D converters [1], [2], [3]. The settling behavior of the Op-Amp determines the accuracy and the speed that can be reached. Fast settling requires single pole settling behavior, and a high gain-bandwidth-product [1], [2]. High accuracy requires high DC gain. The task of building fast Op-Amp with very high DC-gain is a very difficult problem. The high unity gain frequency, high speed, calls for single stage design with short channel devices biased with high current levels [2], [4], [5]. The high DC-gain Op-amp can be implemented using one or more of the following techniques. Those techniques are cascading of gain stages, applying dynamic biasing technique, or using output impedance enhancement technique. Cascading two stages or more will result in a very high DC-gain. However, proper compensation for stable operation will seriously limit the high frequency performance [1], [2]. The second method, dynamic biasing technique, was reported to combine high DC gain and fast settling speed [4]. However, in dynamically biased amplifiers, and during the last settling period the DC gain will be very high which slows the settling. Dynamically biased amplifiers have limited acceptance because of this disadvantage [1], [2]. Moreover a single stage dynamically biased amplifier may not provide sufficient gain, and cascading them is very difficult [4]. Moreover, their speed is limited by the fact that the clock period must be long enough to ensure the transfer of charge to be adequately completed in one cycle. The Third method of enhancing amplifier DC-gain is to increase its output impedance. This task was performed either by cascoding, stacking, of transistors at the output node, using gain-boosting technique or by using the negative conductance, positive feedback method. Cascoding is a well-known method to enhance amplifier output impedance, where the amplifier output impedance, gain, becomes proportional to the square, or the cube of the intrinsic transistor gain, gm/go. One level of cascoding doesn't provide sufficient DC-gain. Triple cascoded amplifier has a very limited output swing, and is not applicable to low-voltage circuits. Moreover as we go deep in sub-micron processes, the intrinsic transistor resistance becomes smaller and smaller which limits the advantage of cascoding. Enhancing amplifier gain by gain-boosting technique is one of the most successful ways of boosting amplifier gain without limiting the high frequency performance [2]. However, boosting amplifiers add their own poles, and zeros to the final amplifier, which in general will exhibit zero-pole doublets that affect amplifier settling making it slow. As the industry moves toward using the new digital CMOS processes Cascading, Cascoding, and Gain-boosting techniques do loose their ability to provide very high DC gain amplifiers because digital transistors have a high output conductance. Expensive solutions like using the special analog friendly devices are used most of the time. The final method to boost the gain is using the positive feedback technique, negative conductance. Positive feedback offers the ability of obtaining a very high DC gain, ideally infinite gain, without affecting high frequency performance. However most of the positive feedback implementations have suffered from two problems. First is a strong dependence of amplifier gain on transistor matching [1], [2], [3]. Second, the amplifier transfer function will have a denominator of the form of (Σgx-gy), where gy is the transconductance, or the conductance of a transistor that has it's gate, input, directly connected to the output node. Since we are looking for wide swing operation, this connection will make gy to be a strong function of the output signal. Therefore, the DC gain of the amplifier will drop sharply as the output node swings up or down, this problem is not mentioned in the literature. However positive feedback method still holds potential to build fast amplifiers with high DC gain.

2. Introduction to positive feedback schemes.

The concept of applying a positive feedback, also known as negative conductance, to enhance amplifier gain was proposed in several publications. Most of the proposed structures share the common characteristic of generating a negative resistance by feedback from the output node that is used to compensate some positive resistance at the output to achieve the very high DC gain. To illustrate the idea a simple example is what proposed by Allstot [3]. Cross-coupled active-load PMOS transistors are applied to a simple differential pair as shown in Figure.1.a. The negative conductance, -gm3, generated by the cross coupling used to boost the DC gain. The small signal model is shown in Fig1.b and simplified in Fig1.c. A small signal analysis shows that the DC gain of the amplifier can be written as

$$A_v = \frac{-g_{m1}}{g_{o1} + g_{o2} + g_{o3} + g_{m2} - g_{m3}} \qquad (1)$$

If gm3=go1+go2+go3+gm2 then the amplifier will exhibit an infinite DC gain. Note that no additional nodes, poles, are added. However to get the very high DC gain we need almost perfect matching mainly between gm2 and gm3, since gm>>go. Perfect matching requirement can be relaxed by two methods. First, make one of the important parameters programmable. Second, use some kind of cascoding such that the amplifier DC gain is not completely dependent on the perfect matching issue. Therefore, the existence of cascoding will allow more room for the parameters to move in. A major problem that still exists is that gm2,3 and go1,2,3 3 are output level dependent. If this amplifier is used in a sample and hold circuit that requires an output swing of 1Vp-p. If the amplifier is fully differential, then the output-node voltage level will

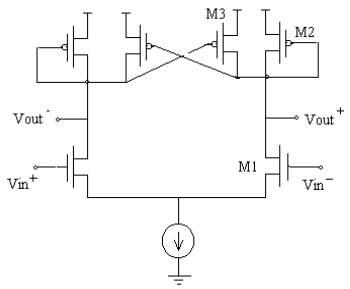
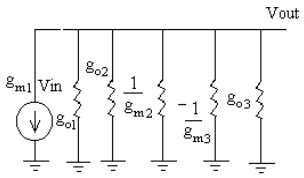


Figure 1.a Regular Differential pair with positive feedback.



Figures 2.b Small signal model, simplified model.

exhibit a change in value by ±250mV. The change of the gate to source voltage of transistors M2 and M3 by ±250mV will completely kill the amplifier gain while settling. This gain variation will introduce nonlinear distortion. Almost all the previously proposed architectures have this property. New architectures have been presented in the literature [M] show low gain sensitivity to output swing, but those architectures require a replica biasing circuitry to maintain the high DC gain. To avoid most of the disadvantages accompanied with implementing the positive feedback technique, we will implement the positive feedback to second and third order amplifiers. Proposed amplifiers will show very high DC gain with stable operation, without the requirement of extra circuitry to control the gain.

3. Conceptual Description of the proposed positive feedback scheme.

We propose constructing new amplifiers by applying positive-feedback to several standard cascoded amplifiers. By applying a self-adjusting feedback in combination with cascoding the transistor matching requirements are relaxed. The positive feedback signal used to enhance the DC-gain is derived from the extra nodes created by cascoding. This will considerably reduce the effect of the output voltage level on the amplifier gain. Figures 2.a, and 2.b show the application of the proposed positive feedback to traditional telescopic, and folded cascode amplifiers. Amplifiers presented here are fully differential. Common mode feed back circuits, and biasing circuits are not shown for simplicity. We will concentrate on the amplifier shown in figure 2.a. The other amplifiers shown exhibit the similar gain properties, amplifiers shown in Fig2.c, and Fig.2.d show faster response, but they need more careful designing procedure. The first stage of the amplifier shown in Fig.2.a, ignoring the bulk effect for simplicity of expressions, has an open-loop gain, Av, of the form.

$$A_v \approx \frac{g_{m1}\cdot(g_{o2}-g_{m2})}{g_{o1}\left[\frac{g_{m2}g_{o3}}{g_{m3}}\right]\left(\frac{g_{o4}}{g_{o1}}+1\right)-g_{o1}g_{o2}} \qquad (2)$$

Assuming that go1=go4, and go1<<gm1 the voltage gain can be written as in equation (3).

$$A_v \approx \frac{-g_{m1}\cdot g_{m2}}{g_{o1}\left(\frac{g_{m2}}{g_{m3}}g_{o3}-g_{o2}\right)} \qquad (3)$$

Equation (3) shows that the DC-gain of the amplifier can be infinite as go3 approaches (gm2/gm3)go3. Looking back to Figure 2.a we see that as go3, or gm3 becomes larger than what expected, then both vgs and vds to the digital transistor M2 become larger, because Vx± move up toward the supply voltage pulling Vout± nodes too. Since transistors M2, M1, M3, and M4 forms an inverting common source amplifier with source degeneration, this amplifier's output will pull Vout± and Vx± nodes down back. This loop of transistors M2, and M3 has a very high gain and its operation is consistent with the operation of the common mode feedback circuit that tries to keep the common mode voltage of nodes Vout± constant. So for limited conditions, variations, the Op-Amp will automatically adjust its biasing condition, and maintain the high DC gain. In a real design we have added small transistors in parallel with M2 that have a gate biased relative to source of transistor M1, this connection helps more the proposed amplifier to be able to maintain the high DC gain across the process and temperature corners with high and almost constant DC gain. Observing voltages Vx+ and Vx- we notice that they experience very small swings compared to Vout+ and Vout- since Vx=Vout/(gm3/go3)/Gs, Where Gs is the gain of the common source output stage, for example in our design, (gm3/go3* Gs)>200. So if the output voltage have a swing of one volt, Vout=Vcm± 250mV, then voltage Vx will experience a swing that can be written as Vx<Vcm±1.25mV. Therefore, the feedback is almost unaffected by the output voltage signal level. Finally the amplifier shown in Figure 2.a is applied to a sample and hold circuit with sampling frequency of 165MHz. Simulation shows high speed slewing and settling as will be shown in the next section.

4. Simulation Results

The telescopic amplifier with the internal positive feedback was simulated using TI, Texas Instruments, digital CMOS 0.21u process. The amplifier consumes a total current of 8.0mA, two stage, and two common mode feedback circuits, using a supply voltage of 1.8V, and deriving a capacitive load of 1.0pF. Simulation shows that the amplifier has a DC gain of 84dB with a unity gain frequency of 1.2GHz. A comparison between the modified and the traditional telescopic cascode is shown in Table 1 where both amplifiers have approximately the same power dissipation, the same excess bias on the similar transistors, and the same load capacitance. The table shows that for approximately the same conditions we where able to enhance the DC-gain from 68dB to 84dB, for the same load, and phase margin. Results are shown in Figures 4.a, 4.b, and 5. Moreover, the same amplifier architecture was applied to a switched capacitor sample and hold circuit with two non over-lapping clocks at frequency of 165MHz loaded by similar stages. One stage is shown in Figure 6. The amplifier implemented consumes a total current of 8.0mA, and drives a load capacitance of 1pF. The sampling unit capacitor has a size of C1=125fF, S&H circuit has a gain of 4. Post layout simulation results are shown in Figure 7.a, and b. Simulation shows that the amplifier was able to slew and settle to an error less than 0.2mV for a 1V peak-to-peak

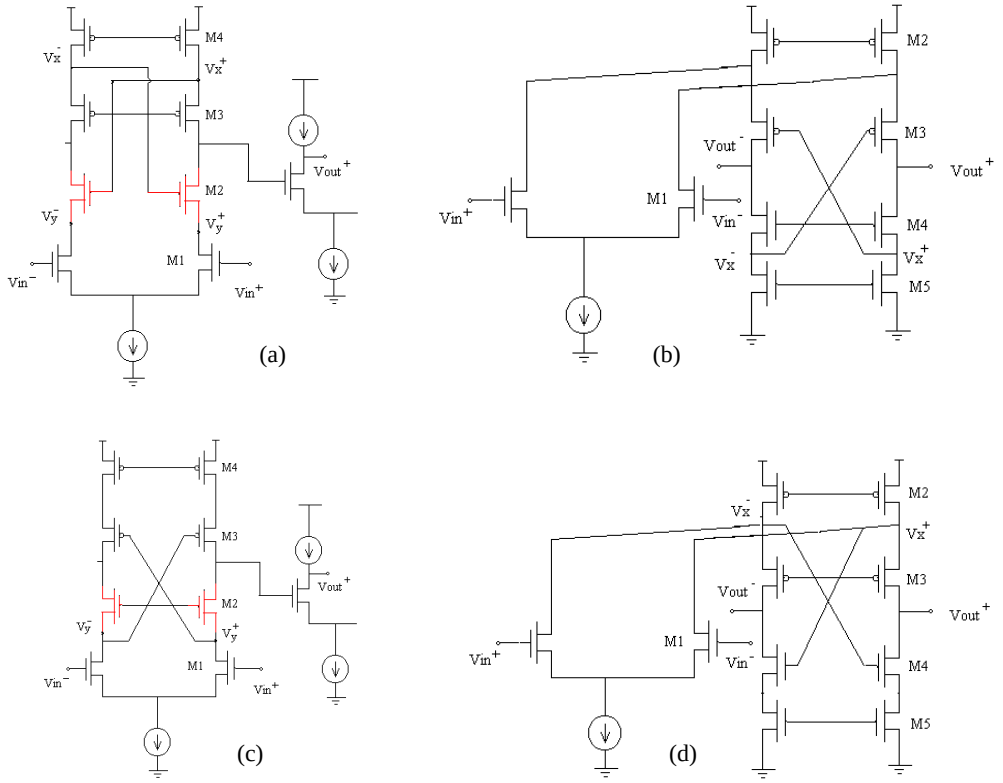


Figure 2.a, b, c, and d different implementations of the positive feedback tech. for different output resistance.

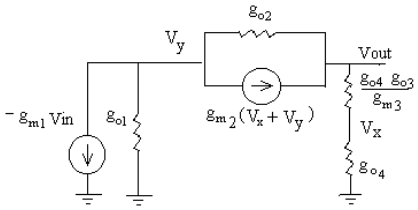


Figure 3 small signal model of one side of Amp. of Fig.2.a

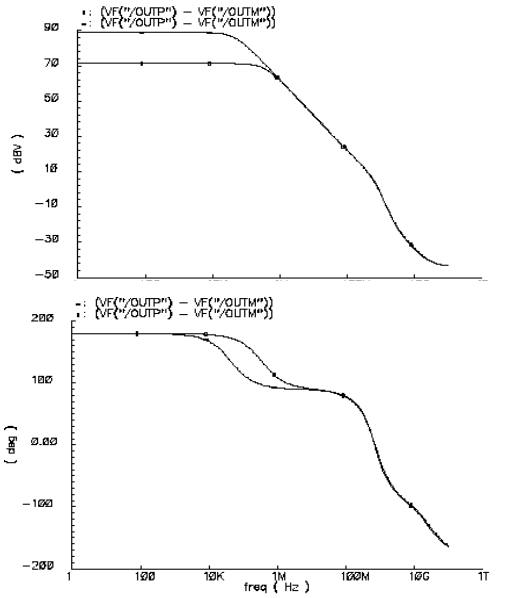


Figure 4.a, b AC char's of Telescopic cascoded, w/wo positive feedback

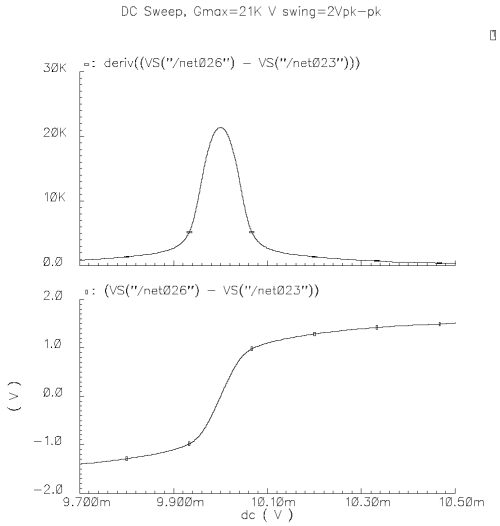


Fig.5 DC sweep of Fig2.a, Output swing is 1.3Vpk-pk

output swing within 2.1nsec for nominal and strong process corners where clock speed is not a problem. Chopped diffusion transistor layout pattern is shown in Figure 8. Using this pattern we reduce the diffusion parasitic capacitance on the expense of increasing the side-wall-capacitance. Layout extraction shows that we can save 15% to 20% of the parasitic capacitance value using this technique, which helps slewing speed. We were able to reduce the parasitic capacitance simply because the sidewall capacitance has much lower density than the diffusion capacitance. Only transistors

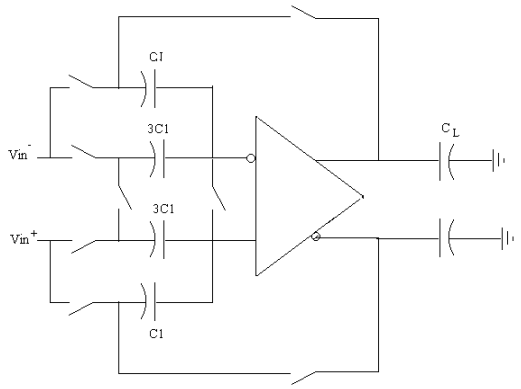


Figure 6. Amplifier of Figure 2.a in an S&H circuit.

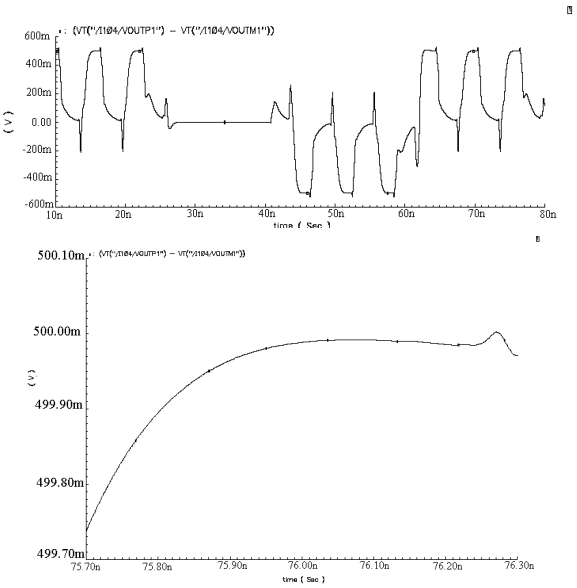


Figure 7.a, b S&H differential output.

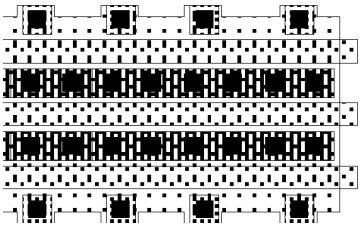


Figure 8. Chopped-diffusion transistor-layout-pattern.

connected across the output nodes, and in the cascode have their diffusion chopped. Finally even though we have a positive feedback active in the differential mode, it is a negative feedback in the common mode. Since the gain is dependent on the biasing parameters, this negative feedback helps the amplifier to maintain the high DC gain condition once it was in that state, this describes why the DC sweep and transient analysis shows higher gain than the AC analysis. Transient simulation parameters are shown in Table 2.

Table 1
Comparison of Amp Characteristics w/wo positive feedback

Telescopic Amp	Positive feedback	Traditional
DC-gain	84 dB	68dB
Unity gain freq.	1.218GHz	1.234GHz
Load cap.	1.0pF	1.0pF
Phase margin	59 degrees	60 degrees
Total current	8mA	8mA
Supply voltage	1.8V	1.8V

Table 2
Transient simulation parameters

Total current	8.0mA
C1	125fF
C_L	1.0pF
Error @ 2.1nsec	0.02%
Output swing	$1V_{pk\text{-}pk}$

5. Conclusion

Positive-feedback technique was used to enhance the DC-gain of popular cascoded amplifiers using all digital transistors. Gain enhancement didn't affect the Bandwidth, speed, of the amplifiers. The gain is automatically adjustable, and not affected by the output voltage swing. Special chopped diffusion transistor layout pattern was used to cut the parasitic capacitance.

6. References

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