Research article

Hailong Zhou[a], Yuhe Zhao[a], Yanxian Wei[a], Feng Li, Jianji Dong* and Xinliang Zhang

All-in-one silicon photonic polarization processor

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Abstract: With the great developments in optical communication technology and large-scale optical integration technology, it is imperative to realize the traditional functions of polarization processing on an integration platform. Most of the existing polarization devices, such as polarization multiplexers/demultiplexers, polarization controllers, polarization analyzers, etc., perform only a single function. Definitely, integrating all these polarization functions on a chip will increase function flexibility and integration density and also cut the cost. In this article, we demonstrate an all-in-one chip-scale polarization processor based on a linear optical network. The polarization functions can be configured by tuning the array of phase shifters on the chip. We demonstrate multiple polarization processing functions, including those of a multiple-input-multiple-output polarization descrambler, polarization controller, and polarization analyzer, which are the basic building blocks of polarization processing. More functions can be realized by using an additional two-dimensional output grating. A numerical gradient descent algorithm is employed to self-configure and self-optimize these functions. Our demonstration suggests great potential for chip-scale, reconfigurable, and fully programmable photonic polarization processors with the artificial intelligence algorithm.

Keywords: silicon photonics; polarization processor; multiple-input-multiple-output.

1 Introduction

Polarization, as one of the fundamental physical characteristics of light, has a great impact on many fields of photonics, including optical communication [1–3], optical imaging [4], and quantum optics [5]. Manipulation of the state of polarization (SOP) of light is fundamental for these applications. With the rapid development of large-scale optical integration technology, numerous on-chip polarization processing devices have been proposed, such as the polarization beam splitter (PBS) [6–9], polarization splitter-rotator (PSR) [10], polarization rotator (PR) [11, 12], polarization controller [13–16], and polarization analyzer [17–21], since an integrated photonic polarization device usually has a much smaller footprint and higher power efficiency. These functions are the basic building blocks for polarization signal processing and show important applications. For example, the PSR, PBS, and PR can be combined to multiplex and demultiplex two orthogonally polarized beams, acting as a polarization multiplexer/demultiplexer [2, 22, 23]. Moreover, a multiple-input-multiple-output (MIMO) algorithm is further needed to descramble the two channels when the SOPs are changed or even become non-orthogonal, caused by crosstalk and unbalanced loss [24]. Unfortunately, the MIMO algorithms suffer from heavy computation requirements for high-bandwidth electronic hardware. Alternatively, all-optical MIMO descramblers were developed to descramble the modes with the inherent speed of light [25–27]; however, all-optical MIMO descramblers are rarely reported in the realm of polarization. A polarization controller is an optical device that allows arbitrary modification of the SOP of light. Polarization controllers can be implemented with free-space optics, through a fiber pigtailed U-bench, or with integrated optical devices [13–16, 28]. An integrated polarization controller is usually composed of PRs and phase shifters. Integrated polarization controllers based

[a]**Hailong Zhou, Yuhe Zhao and Yanxian Wei:** These authors contributed equally to this work.
***Corresponding author: Jianji Dong,** Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China, e-mail: jjdong@hust.edu.cn. https://orcid.org/0000-0002-1852-8650
Hailong Zhou: Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China; and Photonics Research Centre, Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong. https://orcid.org/0000-0002-1878-4291
Yuhe Zhao, Yanxian Wei and Xinliang Zhang: Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China
Feng Li: Photonics Research Centre, Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong

on different materials such as polymer [16] and silicon [13–15] have been developed. The SOP of light can be measured by a polarization analyzer. Typically, the issue of SOP measurement has been addressed by dividing the signal spatially or temporally [4]. Division-of-space polarization analyzers divide the input beam into multiple optical paths, with each path aiming to get different polarization information. Some integrated schemes based on plasmonic nanostructures and metasurfaces have been reported [29–31]. Also, silicon-based schemes have been suggested [18, 19, 21]. For division-of-time methods, different polarization information is measured at different times [32, 33]. For example, two Mach-Zehnder interferometers (MZIs) with a two-dimensional (2D) grating could be combined to form an integrated division-of-time polarization analyzer based on the polarization-frequency mapping technique [17]. In view of both the advantages of silicon-on-isolator (SOI) devices and the necessity of on-chip polarization management, SOI-based polarization analyzers and polarization controllers are highly desirable. Although various integrated functional devices for polarization processing have been developed, most of them show limited reconfigurability, resulting in poor robustness and high cost. An effective solution is to implement multipurpose polarization processing in an optical network with a reconfigurable and integrated polarization processor.

In recent years, some programmable optical devices have been developed. For example, a universal linear optical network was rapidly reprogrammed to implement various quantum applications [34]. Other devices for radio frequency applications [35] and photonics signal processing [36–39] have also been reported. These programmable optical processors show great advantages in reconfigurability and self-configuration capability. They are reconfigurable for multiple functions, self-configurable with some learning ability, and field-programmable with strong fabrication tolerance. Inspired by programmable optics, it is possible to implement a reconfigurable and programmable polarization processor with a linear optical network.

In this article, we propose an all-in-one chip-scale polarization processor based on a linear optical network. The chip contains a 2D grating and four MZIs, which can complete an arbitrary linear transformation by thermal tuning of the phase shifters. By tuning the transmission matrix of the network, the chip can be configured as a polarization MIMO descrambler, a polarization controller, and two kinds of polarization analyzers. A numerical gradient descent algorithm is employed to self-configure and self-optimize these functions. Our demonstration suggests great potential for chip-scale reconfigurable and fully programmable photonic polarization processing with the artificial intelligence (AI) algorithm.

2 Principle

The photonic polarization processor is composed of a 2D grating and four MZIs, as shown in Figure 1A. The 2D grating splits the two orthogonal components (defined as x and y polarizations) of the input light into different waveguide branches with the same TE mode. Both MZI 1 and MZI 4 can perform any arbitrary 2×2 unitary matrix transformation [40–45]. The combination of MZIs 2 and 3 can perform an arbitrary 2×2 diagonal matrix transformation. The four MZIs constitute a complete network that can implement an arbitrary transformation matrix based on singular value decomposition [45, 46]. The light is coupled to the fiber array from the chip with TE gratings. By designing the transmission matrix, the chip is reconfigured to achieve three different functions.

Usually, the SOPs of two polarization channels are orthogonal and set as x and y polarizations. While crosstalk between different channels will be introduced both in the optical transmission link and in the mode multiplexer/demultiplexer, the SOPs of two channels will be changed or even become non-orthogonal. Assume that the Jones matrices of two channels in the receiving end are P and Q, respectively, given by

$$P=[p_x, p_y]^{\mathrm{T}},\ Q=[q_x, q_y]^{\mathrm{T}}. \tag{1}$$

In order to separate the two channels, a transformation matrix is needed to meet

$$M[P, Q]=\Lambda. \tag{2}$$

Here, $\Lambda=[A_1, A_2]$ is a diagonal matrix, representing the optical field distribution in the output ports (Ports 2 and 3) for two channels. The transformation matrix is then given by

$$M=[P, Q]^{-1}\Lambda. \tag{3}$$

From the above analysis, the P-polarized component (Channel 1) of the input light will emerge from Port 2 and the Q-polarized one (Channel 2) will emerge from Port 3. Similarly, the output ports can be switched by rotating the diagonal matrix by 90°. It proves that our chip is able to separate two arbitrary polarization-based channels in theory, which can be used to descramble the polarization-based channels.

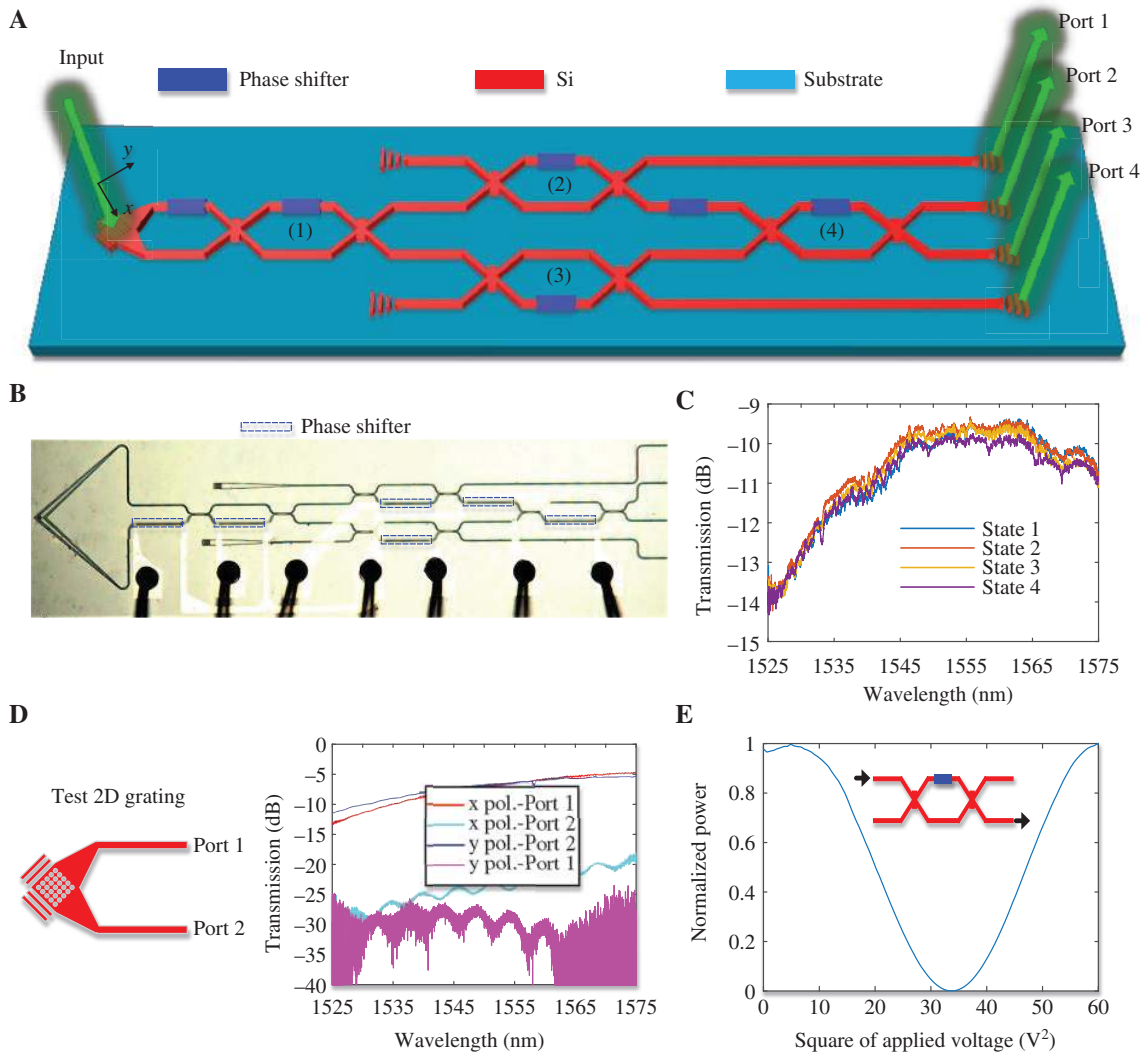

Figure 1: Photonic polarization processing circuits.
(A) Detailed structure of the polarization processor chip. (B) Micrograph of fabricated chip. (C) Transmission spectra of the chip for random input SOPs and applied voltages. (D) Transmission spectra of the 2D grating. (E) Imparted phase depending on the applied voltage for the tested MZI structure.

Meanwhile, our chip can also transform an arbitrary polarization into a fixed known one and transform a fixed known polarization into an arbitrary one in reverse, acting as a polarization controller. The transformation matrix is given by

$$M = \left[P, P_{\perp}\right]^{-1} \text{ or } [P_{\perp}, P]^{-1}. \tag{4}$$

Here, $P_{\perp}$ is the cross-polarization of P. When P-polarized light is incident on the 2D grating, only one output port will excite the light. And in the reverse, arbitrarily polarized light can be generated and emerge from the 2D grating when the light is incident on one of the output ports.

Furthermore, the four ports can output different polarization information, which can be used to measure the SOP of light, making the chip as a division-of-space polarization analyzer. The Stokes parameters $S = [S_0, S_1, S_2, S_3]$ can be obtained by [30]

$$S = TI, \tag{5}$$

where $I = [I_1, I_2, I_3, I_4]$ is the measured optical power in the four output ports. T is a 4×4 matrix dependent on the internal parameters of chip. The four intensities of the different polarized components can be equivalently obtained at different times by applying four sets of direct current (DC) voltage signals on the phase shifters, making the chip as a division-of-time polarization analyzer.

The key point to configure these polarization functions is how to load a targeted transformation matrix on the chip. Here we employ a numerical gradient descent algorithm modified from deep learning [46, 47] to optimize this issue. According to the different purposes of our processor, a suitable and special cost function (CF) should be first defined. Then the only training target is to make the defined CF maximum using the numerical gradient descent algorithm. Theoretically, training needs to combine forward and backward propagation methods, similar to deep learning. Forward propagation is used to calculate the output as the data for the next iteration, and then backward propagation aims to estimate the errors and find the gradient descent. This training algorithm is also called the gradient descent algorithm, which is a common method for training artificial neural networks (ANNs). In our design, the optical chip can output automatically and timely provided the input is set. And the gradient descent can be alternatively measured by fine-tuning each parameter. So in our design, no backward propagation is needed and forward propagation can be implemented by the chip itself at the speed of light. Furthermore, the chip can be regarded as a "black box". That means the internal structure of the chip is transparent to the users. The full training process is as follows:

1. Initialization: all the adjustable parameters $\theta(i=1, 2, \ldots)$ are set randomly. Here, θ_i is the carried phase on the corresponding phase shifter.
2. Tuning each parameter: set θ_1 to $\theta_1+\Delta\theta$ temporarily. If $\mathrm{CF}(\theta_1+\Delta\theta)\geq\mathrm{CF}(\theta_1)$, replace θ_1 with $\theta_1+\Delta\theta$; else, replace θ_1 with $\theta_1-\Delta\theta$.
3. Repeat Step 2 for all adjustable parameters one by one.
4. Repeat Steps 2 and 3 until the CF is converged or reach the target value.

For the polarization MIMO descrambler, the CF is defined independently of the channel by

$$\mathrm{CF}=\frac{\left|A_1\bullet A_{\mathrm{exp1}}\right|}{\left|A_1\right|\left|A_{\mathrm{exp1}}\right|}\frac{\left|A_2\bullet A_{\mathrm{exp2}}\right|}{\left|A_2\right|\left|A_{\mathrm{exp2}}\right|}. \tag{6}$$

The operation "•" means the scalar product of two vectors. $A_{\mathrm{exp}n}$ (n = 1, 2) is the measured output power distribution in Ports 2 and 3 when only Channel n is open.

Similarly, the CF of the polarization controller is defined by

$$\mathrm{CF}=\frac{\left|\mathrm{Pow}\bullet\mathrm{Pow}_{\mathrm{exp}}\right|}{\left|\mathrm{Pow}\right|\left|\mathrm{Pow}_{\mathrm{exp}}\right|}. \tag{7}$$

Here, Pow is the desired output power distribution in four ports and $\mathrm{Pow}_{\mathrm{exp}}$ is the measured one. For example, Pow can be set as [0, 1, 0, 0] if we want to make all the light output from Port 2.

CF ranges from 0 to 1, where CF = 0 means that the experimental results are completely inconsistent with the targeted results and CF = 1 means that they are completely consistent. Our training target is to make CF as close to 1 as possible. To guarantee power efficiency, the first eigenvalue of the transmission matrix is fixed to 1; namely the phase difference of two inner arms of the second MZI in Figure 1A is always equal to π and there is no light output from Port 1. In the following, the chip is reconfigured to achieve three different functions.

3 Results

3.1 Experimental setup

The chip is fabricated on a commercial silicon-on-insulator (SOI) wafer. A passive process is employed to fabricate the structure on the SOI wafer with a 220-nm top silicon layer, a 2-μm silica cladding layer, and a 2-μm-thick buried oxide (BOX) substrate. The size of chip is about 2.0 mm × 0.5 mm. The micrograph of the fabricated chip is shown in Figure 1B. The transmission spectra of the chip are shown in Figure 1C, which are measured by summing the output power of four ports when the input SOP and the applied voltages are both random. The transmission at 1550 nm is about –10 dB (excluding the output TE gratings), and the 3-dB bandwidth is about 40 nm (1535–1575 nm). The 2D grating coupler consists 17 rows and columns of holes of diameter 360 nm and shallow etch of 70 nm. The holes are arranged in the circular lattice with the average period of 635 nm. The transmission spectra of the 2D grating are shown in Figure 1D. The insertion loss at 1550 nm for two polarizations is about 6.5 dB, and the polarization extinction ratios are larger than 15 dB for both polarizations in the entire C-band. The imparted phase, which depends on the applied voltage (V), may be expressed as $\theta=2\pi V^2/T$ [46]. MZIs with internal phase shifters are used to convert the phase change into output power. The measured power distribution, which depends on the square of the applied voltage, is presented in Figure 1E. The measured average period of T is about $55V^2$. The phase tuning efficiency is measured to be 27 mW per π phase shift, and the electrical resistance is about 1000 Ω. The response speed of thermo-optic phase shifters is larger than 10 kHz [17]. The network training (typically <1000 iterations) can be completed within 100 ms provided the external driver is

fast enough. Figure 2 presents the experimental setup. The setup for polarization multiplexing is depicted in Figure 2A. The two channels (SOP1 and SOP2) are independently configured with lasers, single-mode fibers (SMFs), and polarization controllers (PCs). Then they are combined with an optical coupler (OC). Two optical switches (OSs) powered by electricity are inserted in the paths to open or close the corresponding channel. Figure 2B presents the setup for polarization preparation. Any arbitrary or known SOP can be generated by rotating the wave plates (WPs), which contain a half-WP and a quarter-WP. The combined light in Figure 2A or the generated polarized light in Figure 2B is injected to the chip with a 2D grating for subsequent processing. Figure 2C presents the setup for polarization processing. A V-groove fiber array (VGA) and a four-channel photodetector array (PDA) are used to receive the output light from the chip. All the phase shifters in the chip and the OSs are driven by a voltage source array (VSA). All the monitoring instruments and voltage sources are connected and controlled by the same computer.

3.2 Polarization MIMO descrambler

Crosstalk between different channels always exists both in the optical transmission link and in the polarization multiplexer/demultiplexer. Here, all-optical MIMO demultiplexing can be accomplished with our chip. The experimental devices in Figure 2A,C are used to configure the polarization MIMO descrambler. The SOPs of two channels are randomly set by tuning the PCs in Figure 2A, to emulate the optical transmission link and polarization multiplexing with crosstalk accumulation. The two channels can be separated using the self-configuring method, and the CFs in Eq. (6) are used to optimize the problem. Figure 3A presents the training process as a function of the number of iterations (Video S1). The CF is near 0.63 before the training, indicating the two channels are strongly mixed and the crosstalk is quite large. Then the CF is gradually increased with the training algorithm and finally reaches near 1 (0.9999). Figure 3B presents the light power distributions when the number of iterations equals 1, 10, and 40. One can see that the crosstalk can be eliminated using the optimization algorithm, which finally is below –20 dB at 1550 nm. We tested six random states (Cases 1–6), where the SOPs of two channels are randomly set by tuning the PCs in Figure 2A. The normalized transmission spectra for the two channels are measured and presented in Figure 4A,B for the routing states SOP 1-Port 2 and SOP 2-Port 3. The crosstalk is less than –10 dB in a bandwidth of ~9 nm. The routing state can be also switched, and the measured transmission spectra (routing state: SOP1-Port3, SOP2-Port2) for Case 6 are shown in Figure 4C,D. The crosstalk is less than –20 dB at 1550 nm and less than –10 dB in a bandwidth of ~7 nm. It proves that our chip can function as a polarization MIMO descrambler and a polarization switch.

3.3 Polarization controller

The chip can also be configured as a polarization controller. A polarization controller can transform an arbitrary

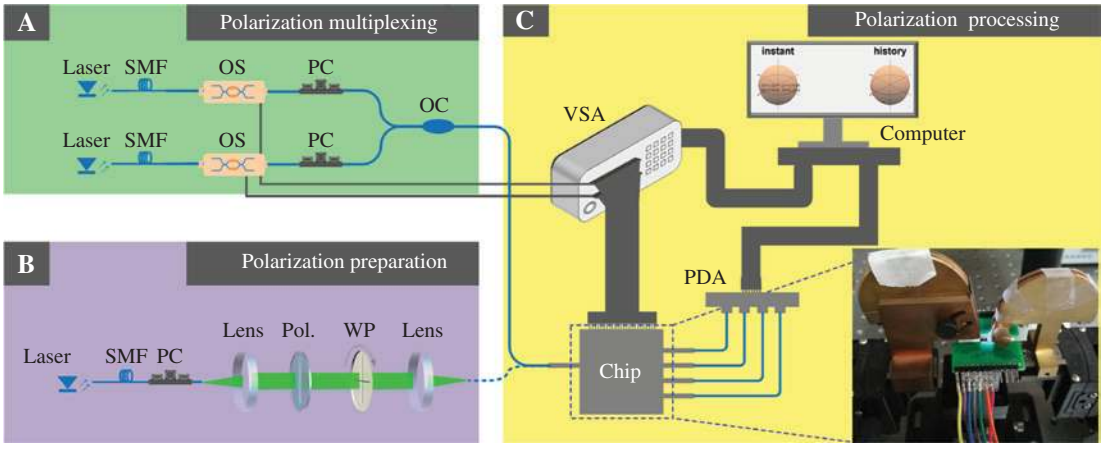

Figure 2: Experimental setup.
(A) Polarization multiplexing: two polarization channels are independently configured and then combined. (B) Polarization preparation: an arbitrary and known SOP can be generated by rotating the wave plates (WPs), which contain a half-WP and a quarter-WP. (C) Polarization processing: all the phase shifters in the chip are driven by a voltage source array (VSA), and the output light is collected by a photodetector array (PDA). The PDA and VSA are connected and controlled by the same computer. The inset shows the details of chip packaging.

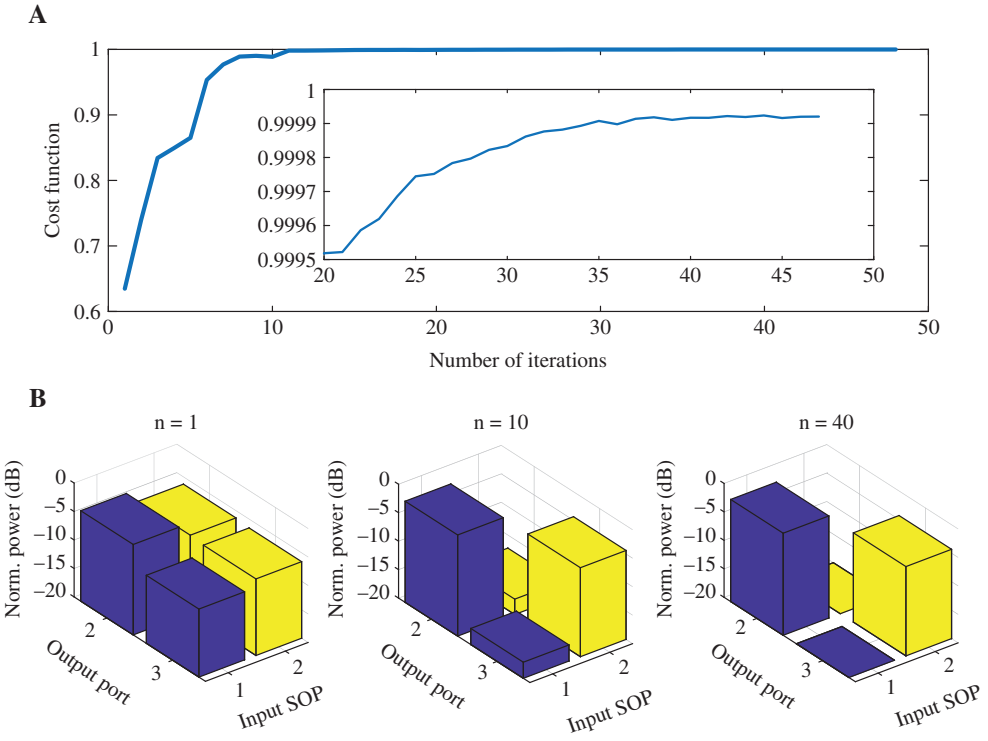

Figure 3: Training process for polarization MIMO descrambler.
(A) Cost function dependent on the number of iterations (Video S1). (B) Light power distributions when the number of iterations equals 1, 10, and 40.

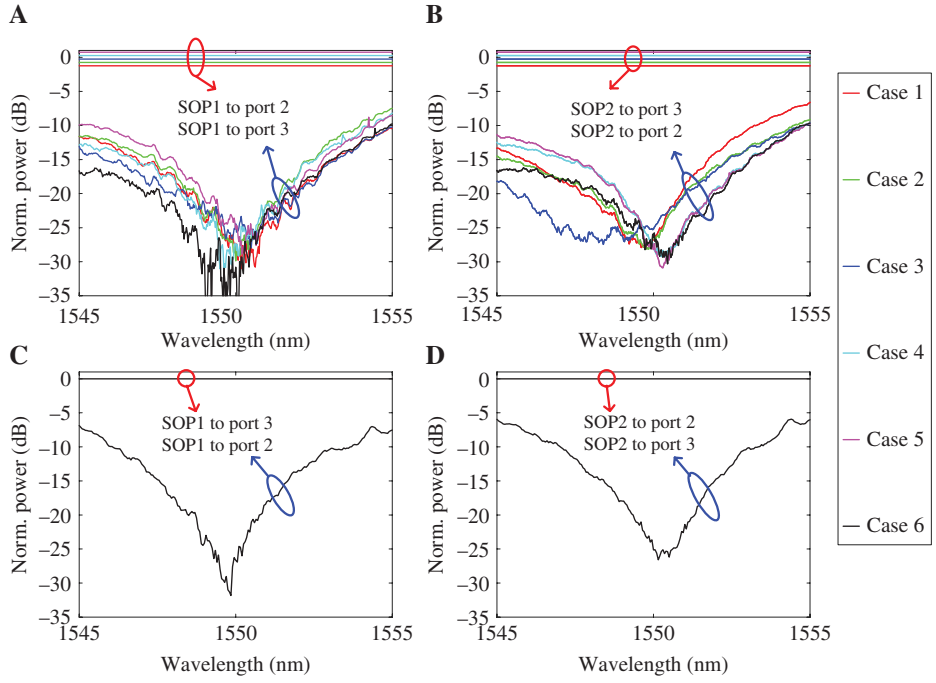

Figure 4: Transmission spectra for polarization MIMO descrambler and polarization switch.
Six random states are tested. (A, B) Routing state: SOP 1–Port 2, SOP 2–Port 3. (C, D) Routing state: SOP 1–Port 3, SOP 2–Port 2.

polarization into a fixed, known one. In our experiment, one of the channels in Figure 2A is used to generate light with random and unknown SOP. And an arbitrary output port can be set as the targeted port to make all the light output from this port. Figure 5A shows an example where Port 4 is the targeted output port (Video S2). The CF in Eq. (7) is used to optimize this kind of problem and train the network. The CF can reach up to 0.999 after 174 rounds of iterations. Figure 5B presents the light power distributions when the number of iterations equals 1, 25, 50 and 174. We can see that the light gradually accumulates at Port 4 and recedes from the other ports correspondingly. Finally, the extinction ratio can be less than –20 dB at 1550 nm. In further experiments, we tested 10 samples of different random SOPs as the initial SOPs. The targeted ports were randomly assigned. The goal was to make light emerge at the assigned port. The measured transmission spectra (including the TE grating couplers) are shown in Figure 5C. The extinction ratio can be less than –18 dB at 1550 nm for all cases.

In the reverse, the polarization controller can transform a fixed, known polarization into an arbitrary one. In this case, we can inject light into the chip from any arbitrary output port, and the light with a specified SOP can emerge from the 2D grating. Both forward and backward trainings can be used to implement polarization control.

3.4 Polarization analyzer

In our chip, the MZIs are asymmetrically designed, thus introducing phase differences in both the internal and external arms. As a result, four output ports can

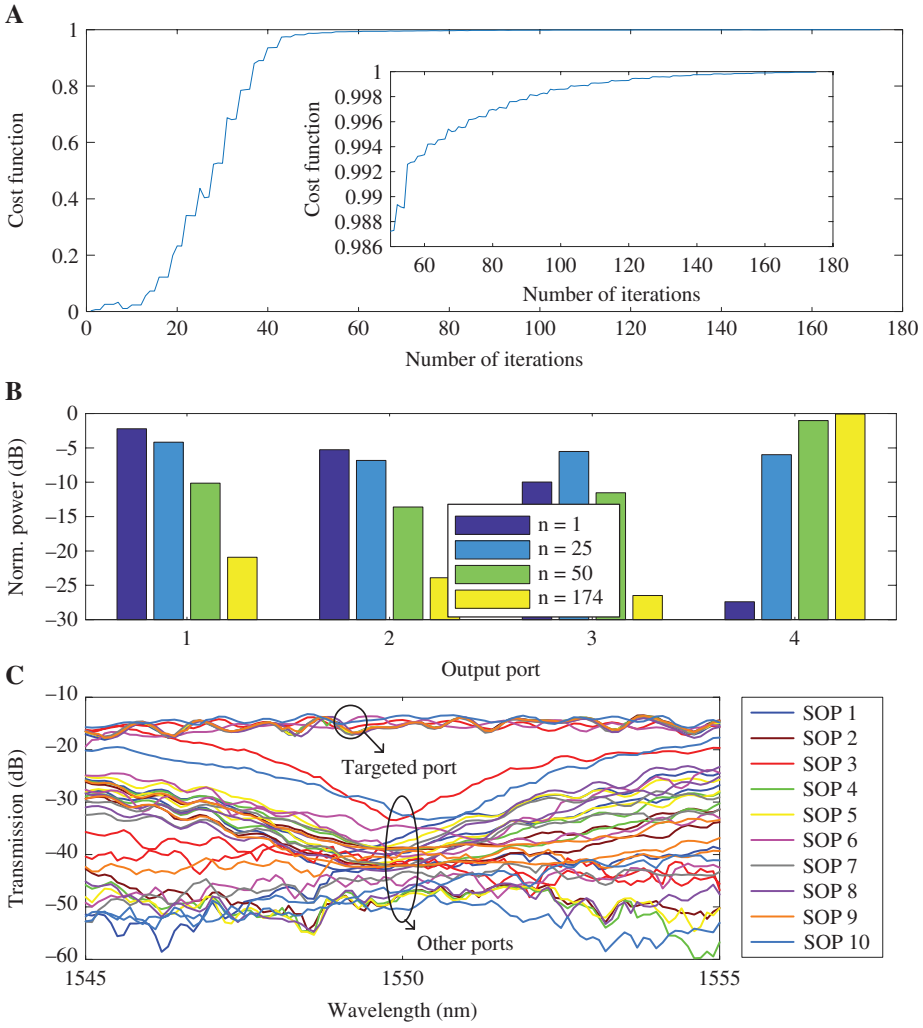

Figure 5: Experimental results for polarization controller.
(A) Cost function dependent on the number of iterations (Video S2). (B) Light power distributions when the number of iterations equals 1, 25, 50, and 174. (C) Transmission spectra (including the TE grating couplers) for 10 cases with random SOPs and random targeted ports.

represent different polarization information, acting as a division-of-space polarization analyzer. The systematic structure is shown in Figure 6A. Here, all phase shifters do not work during the experiment. Namely, we do not apply any voltage on the phase shifters. The input SOPs are prepared with the setup in Figure 2B. A half-WP and a quarter-WP are used to generate an arbitrary and known SOP. Then the output power of different polarized components is received by the PDA. First, the transmission matrix T in Eq. (5) is calibrated by using the four known SOPs in advance. The theoretical SOPs can be calculated according to the readings of WPs. Then the chip can be used to measure the Stokes parameters of unknown input light according to Eq. (5). The Stokes parameters are measured and marked on the Poincaré sphere, as shown in Figure 6B. One can see that the experimental results are well consistent with the theoretical results. A live demo is recorded (Video S3), where the half-WP is rotated continuously, whereupon the measured SOPs should rotate by a circle around the center of the sphere. The ellipticity angle of SOP (labeled by χ) and the orientation angle of SOP (labeled by φ) are defined by

$$\sin(2\chi)=\frac{S_3}{S_0},\ \tan(2\varphi)=\frac{S_2}{S_1}. \tag{8}$$

The deviations of the ellipticity angle (DEAs) and the deviations of the orientation angle (DOAs) are further analyzed, as shown in Figure 6C,D. The DEAs are changed from –2.7° to 5.1° and the DOAs are varied from –0.77° to 2.16°. The root-mean-squared errors (RMSEs) of DEAs and DOAs are 1.38° and 0.45°, respectively.

This chip can also implement a polarization analyzer with the division-of-time method. In this case, only the first MZI and Port 1 are utilized, as shown in Figure 7A. Four sets of random DC voltages are applied on the two phase shifters, and the output power of different polarized components is received at different times. The final experimental Stokes parameters are presented on the Poincaré sphere of Figure 7B, which are consistent with the theoretical results. The DEAs shown in Figure 7C are changed from –3.2° to 7.3°, and the DOAs shown in Figure 7D are varied from –2.1° to 2.2°. The RMSEs of DEAs and DOAs are 1.11° and 0.84°, respectively.

3.5 Potentials for more polarization processing

The proposed photonic polarization processor can perform multiple functions, including as a polarization MIMO

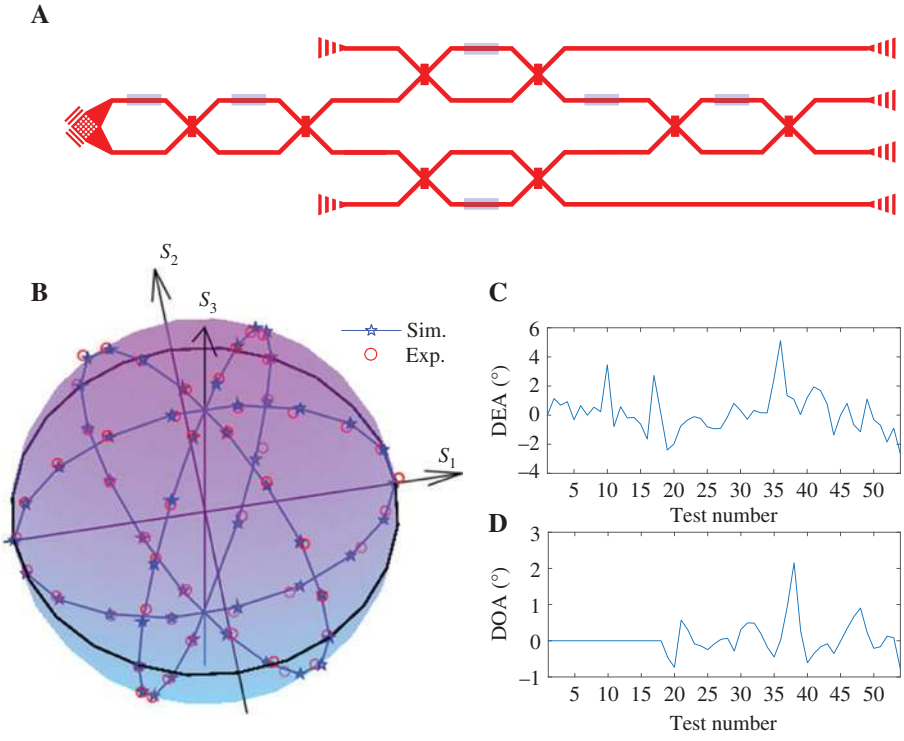

Figure 6: Experimental results for a division-of-space polarization analyzer.
(A) Used structure. (B) Experimental Stokes parameters compared with the theoretical results. (C) Deviations of the ellipticity angle. (D) Deviations of the orientation angle.

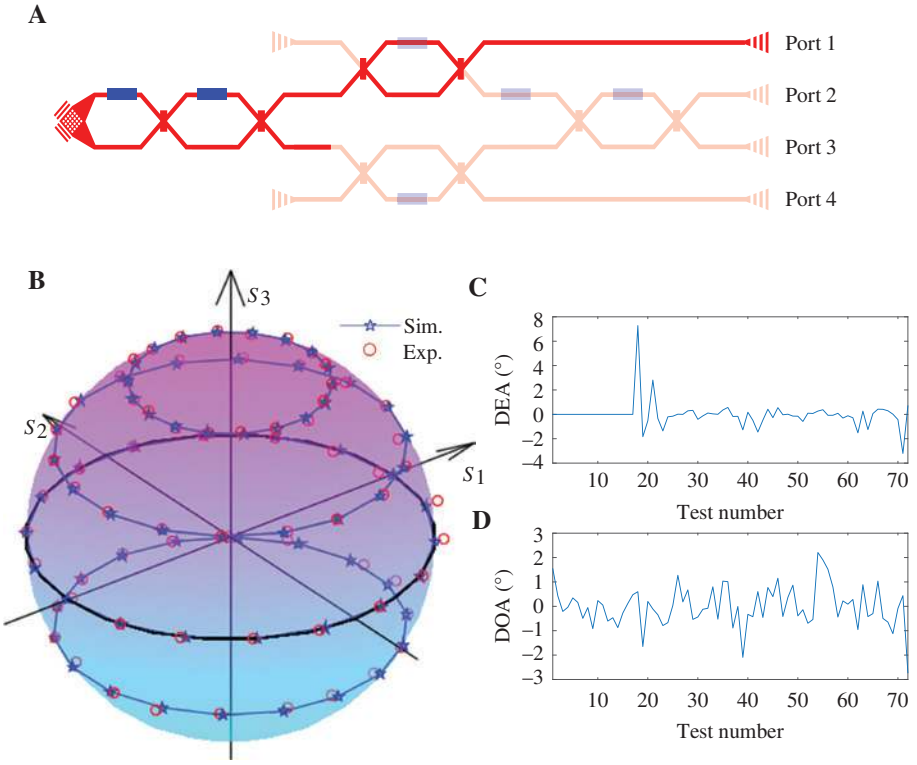

Figure 7: Experimental results for a division-of-time polarization analyzer.
(A) Used structure. (B) Experimental Stokes parameters compared with the theoretical results. (C) Deviations of the ellipticity angle. (D) Deviations of the orientation angle.

descrambler, polarization controller, and polarization analyzer, which are basic building blocks in polarization processing. In fact, the polarization MIMO descrambler can cover the functions of polarization splitting, polarization multiplexing/demultiplexing, and polarization switching. Furthermore, arbitrary polarization-based coordinate conversion can be further performed if another symmetrical 2D grating is used to couple the light out from the chip, as shown in Figure 8. In the case, the polarization transformation can be expressed as

$$[P_{out}, Q_{out}] = M[P_{in}, Q_{in}]. \quad (9)$$

Here, P_{in}, Q_{in} are the input SOPs of two channels and P_{out}, Q_{out} are the output SOPs. A WP or a PR can be realized when the transmission matrix is a unitary matrix (i.e., orthogonal coordinate conversion). And an arbitrary WP or PR can be designed by tuning the transmission matrix. Non-orthogonal coordinate conversion can be also performed if the transmission matrix is reversible but not unitary. It can be used to correct the SOPs of two channels provided the two channels degrade and become non-orthogonal. Finally, an arbitrary polarizer can be implemented when the transmission matrix is irreversible. For example, the light with SOP $P_{\perp}$ is blocked by the chip and the light with SOP P can pass through the chip when $M = [P, P]^*$; here the operation "*" means conjugate transposition. Up to now, we have demonstrated a variety of polarization processing functions with our chip, which cover almost all the basic building blocks of polarization processing, revealing the potential for an all-in-one photonic polarization processor.

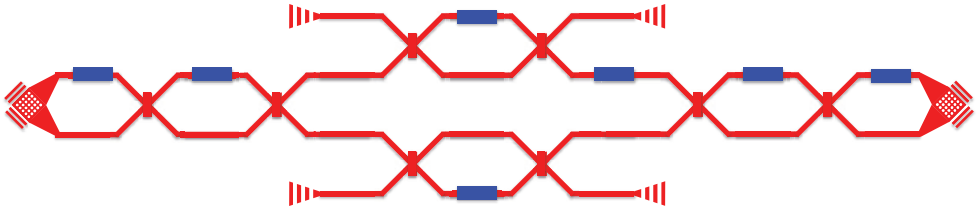

Figure 8: Photonic polarization processing circuits for polarization-based coordinate conversion.

4 Summary

In conclusion, we have designed, fabricated, and demonstrated an all-in-one, chip-scale polarization processor based on a linear optical network. By tuning the transmission matrix of the network, the chip can be configured as a polarization MIMO descrambler, a polarization controller, a division-of-space polarization analyzer, and a division-of-time polarization analyzer. A numerical gradient descent algorithm was employed to self-configure and self-optimize these functions. More functions can be configured, such as an arbitrary wave plate, PR, and polarizer, if another 2D grating is used to couple the light out from the chip. Our chip can achieve almost all the basic building blocks of polarization processing, suggesting great potential for chip-scale, reconfigurable, and fully programmable photonic polarization processing with the AI algorithm.

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