All-inversion region g_m/I_D methodology for RF circuits in FinFET technologies

Rafaella Fiorelli*, Juan Núñez* and Fernando Silveira *Senior Member, IEEE*†
*Instituto de Microelectrónica de Sevilla, IMSE-CNM, (CSIC/Universidad de Sevilla)
{fiorelli, jnunez}@imse-cnm.csic.es
†Instituto de Ingeniería Eléctrica, Universidad de la República, Uruguay
silveira@fing.edu.uy

***Abstract*—In the context of IoT applications, together with the use of deep-submicron technologies as FinFET, this paper presents a revision of the g_m/I_D methodology for radio-frequency analog front-end circuits. Particularly, this methodology is applied for the design of LC-VCOs in the 5.8-GHz band using 20-nm FinFET transistors. To incorporate the FinFET model into the design flow, a semi-empirical model is extracted from electrical simulations. To show the good performance of the methodology, an LC-VCO design, picked from the calculated design maps, is electrically simulated, achieving good match regarding oscillation frequency and phase noise.**

I. Introduction

The advent of Internet of Things (IoT) has led to the proliferation of infinity of applications where analog RF front-ends are required. Since these IoT devices are generally autonomous, the RF blocks have very strong design commitments as it is the case of power consumption. This, in turn, should be linked to the fact that more and more devices are migrated from conventional CMOS to nanometer technologies, such as FinFET and FDSOI. These emerging devices allow aggressive scaling of supply voltages to achieve ultra-low power operation and, thus, overcoming power density and energy efficiency challenges exhibited by CMOS technologies.

From the aforementioned, it is especially important to spotlight those design methodologies of analog RF circuits that allow the fast attainment of accurate designs. This is clearly the case of the g_m/I_D methodology [1], whose potentiality to design analog circuits is more than proven throughout these years in the form of uncountable circuits since its proposal. This methodology has been validated in radio-frequency (RF) analog circuits such as low-noise amplifiers (LNA) [2][3], mixers [4] or voltage-controlled oscillators (VCO) [5].

This paper is intended to revisit the use of the g_m/I_D methodology in the LC voltage controlled oscillator (LC-VCO) implemented in 20-nm FinFET technology at the 5.8-GHz ISM band.

This revision is done utilizing FinFET transistors due to their great potential from the perspective of sub- and near-threshold logic operation, which translate into improved performance, voltage scalability and reduced energy [6][7]. Furthermore, it is shown how the methodology can adapt to a different device. Predictive Technology Model (PTM) for a high-performance (HP) 20-nm multigate FinFET transistor, with nominal supply source V_{DD}=0.9V, has been considered [8].

To incorporate the information of the FinFET model (implemented in electrical simulator using BSIM-CMG FinFET model) into the design methodology of each circuit, a g_m/I_D-semi-empirical model is extracted for these devices. This modeling allows us to condense the most important electrical characteristics of the device in look-up tables (LUT) as current, transconductance and output resistance, and intrinsic capacitances. As far as RF is concerned, the last ones are of paramount importance and its good modeling is essential.

This paper is structured as follows. Section II develops the FinFET semi-empirical model as function of g_m/I_D. Section III describes the VCO design methodology, exemplified with adequate design maps. Section IV presents an 5.8-GHz LC-VCO whose analytical results are compared against those electrically simulated. Finally, Section V concludes the paper.

II. FinFET semi-empirical model

This section presents the FinFET semi-empirical model utilized throughout the paper. The model is obtained with .dc electrical simulations by sweeping the gate-source voltage V_{GS} (fully explained in [5]). Then, it is possible to extract the FinFET characteristics of drain current I_D, transconductance g_m, output conductance g_{ds}, intrinsic capacitances C_{ij} (with $ij = \{gs, gd, gb, bs, bd\}$) and extrinsic capacitance C_{ds} against the equivalent FinFET transistor width W and V_{GS}. With these characteristics it is possible to build a look-up table, LUT_{FinFET}, that includes : i) the normalized current $i_d = I_D/W$, (ii) g_m/I_D, iii) the ratio g_{ds}/I_D, and iv) the normalized capacitances $c_{ij} = C_{ij}/W$. The FinFET width is $W = (2h_{fin} + t_{fin})n_{fin}$, where h_{fin} and t_{fin} are the fin height and width, respectively, and n_{fin} is the number of fins of the FinFET [9].

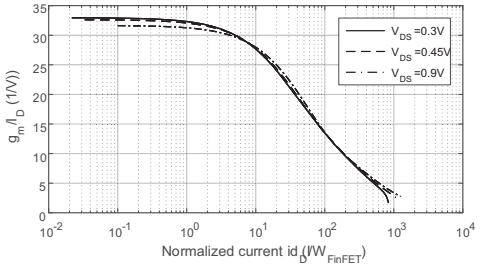

Figure 1. FinFET g_m/I_D curves versus normalized current.

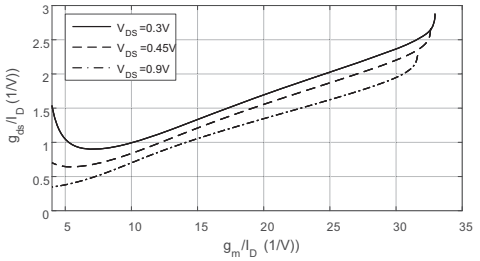

Figure 2. FinFET g_{ds}/I_D curves versus normalized current.

The normalization of I_D and C_{ij} against W makes the LUT$_{FinFET}$ independent of FinFET transistor width on which these characteristics have been extracted. Since h_{fin} and t_{fin} are fixed as well as the length of the transistor, here n_{fin} is varied. This semi-empirical modeling is very appealing as its extraction is performed only once for only a transistor with only one fin ($n_{fin} = 1$) and medium-range drain-source voltage V_{ds}, sweeping its gate voltage V_G. For the PTM BSIM-CMG FinFET model used, the validity range of W and V_{DS} is wide. All these facts are proven onwards.

To extract the LUT characteristics, and to check the independence of them against W, three transistor widths $n_{fin} = \{1, 10, 100\}$, and three drain-source voltages $V_{DS} = \{0.3, 0.45, 0.9\}$V have been used. The extracted g_m/I_D it is presented against the normalized current $i_d = I_D/W$ in Fig. 1. It is observed that the g_m/I_D characteristic has negligible variations over V_{DS}. In turn, the characteristic g_{ds}/I_D is plotted against g_m/I_D in Fig. 2. For identical set of W and V_{DS}, only a slight variation of g_{ds}/I_D for different V_{DS} is appreciated. Finally, $c_{ij} = C_{ij}/W$ is presented versus g_m/I_D in Fig. 3. The c_{ij} normalized capacitances have negligible variations over V_{DS}. Besides, no change is observed when n_{fin} changes in any of the named features. Therefore, contrary to what happens in conventional CMOS, where there is a slight change over W, the listed characteristics are fixed against W. This is expected since the FinFET is built based on parallel connection of unit elements (the fins), so the characteristics of the whole device is intrinsically suited to be described in terms of the characteristics of each unit element, thus to depend

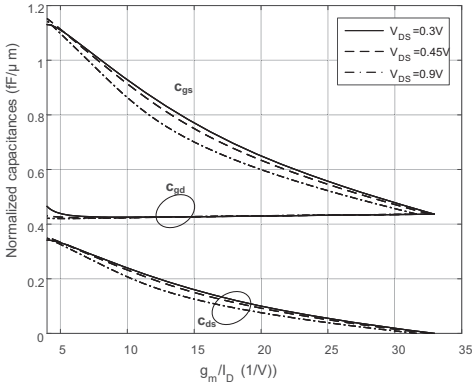

Figure 3. FinFET Normalized capacitances vs g_m/I_D.

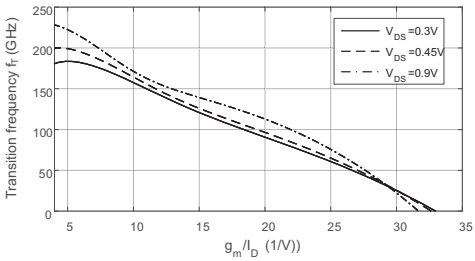

Figure 4. FinFET transition frequency f_T g_m/I_D .

on the current through (or capacitance of) each element, i.e the normalized current or capacitance. These graphs validate the creation of the mentioned semi-empirical model as function of g_m/I_D. Its accuracy is good enough considering the ease of extracting this LUT.

It is important to emphasize that having well-modeled FinFET transistor intrinsic capacitances as function of g_m/I_D makes it possible to achieve good analog RF designs.

Also, by observing the curves of Fig. 1 and Fig. 3, it is immediate to note the advantages of the FinFET respect to conventional CMOS transistors, due to the larger values of g_m/I_D and smaller intrinsic capacitances of the former ones when compared to those of conventional CMOS [5] [3], deriving in higher transition frequency (f_T) figures, as observed in Fig 4.

III. 5.8-GHz LC-VCO design

This section resumes the design methodology of the cross-coupled differential LC-VCO architecture of Fig. 5. This design methodology has been fully presented in [5], whilst here it is proven that it can be applied to a 20-nm FinFET technology and for an oscillation frequency of 5.8 GHz, extracting the design maps of the phase noise, PN, and current consumption I_D under these conditions. The LC-VCO design flow, based on the g_m/I_D methodology, sizes the LC-VCO components to achieve a required oscillation central frequency, f_0,

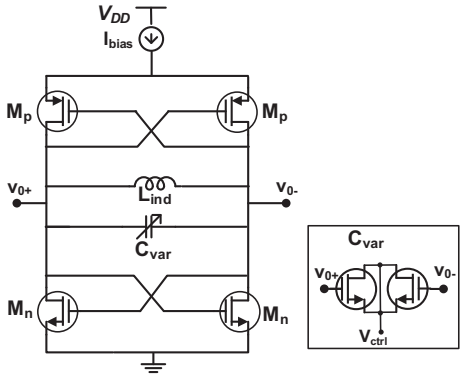

Figure 5. Schematic of the LC-VCO and the FinFET varactor (inset).

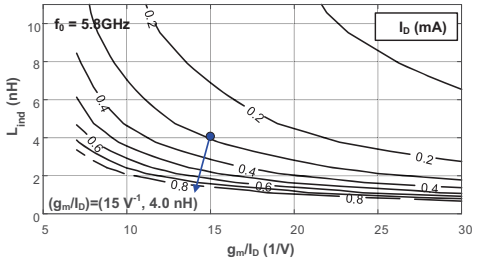

Figure 6. 5.8-GHz LC-VCO current consumption map.

and PN for a range of power consumption and a group of inductor values.

The design flow makes use of the following set of equations which model the frequency, oscillation amplitude, and phase noise of the LC-VCO against g_m/I_D [5]. The f_0 equation is

$$f_0 = \frac{1}{2\pi\sqrt{L_{ind}C_{tank}}} \tag{1}$$

with $C_{tank} = C_{var} + (C_{pFin} + C_{nFin})/2$, and C_{pFin} and C_{nFin} are the equivalent capacitances seen between V_{o1} and V_{o2} of n-FinFET and p-FinFET transistor blocks.

The oscillation condition is

$$g_{tank} = g_{ind} + \frac{g_{ds,p}}{2} + \frac{g_{ds,n}}{2} \leq \frac{g_{m,p}}{2} + \frac{g_{m,n}}{2} \tag{2}$$

where g_{ind} is the parasitic conductance of the inductor, and $g_{ds,n}$ and $g_{ds,p}$ are the n-FinFET and p-FinFET output conductances. The last inequality is transformed to an equality by multiplying g_{tank} by a factor k_{osc}:

$$\begin{aligned} g_m &= k'_{osc} g_{ind} \\ &= \left(\frac{1}{k_{osc}} - \frac{g_{ds,p}/I_D}{g_{m,p}/I_D} - \frac{g_{ds,n}/I_D}{g_{m,n}/I_D}\right)^{-1} g_{ind} \end{aligned} \tag{3}$$

All equations have been explicitly written as function of the g_m/I_D ratio to note the strong dependence of these characteristics with g_m/I_D.

The amplitude oscillation is

$$V_o = \frac{8}{\pi}\frac{k'_{osc}}{g_m/I_D} \tag{4}$$

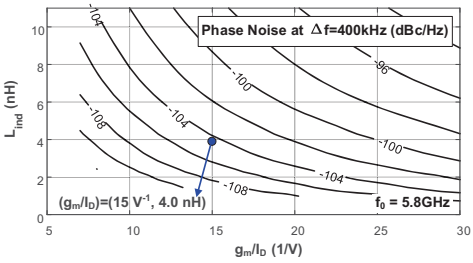

Figure 7. 5.8-GHz LC-VCO phase noise map.

The phase noise expression is

$$PN(\Delta f) = 10log\left(\frac{k_B T\pi^2}{64Q^2}\frac{g_m}{I_D}\frac{1}{I_D}\frac{f_0^2}{(\Delta f)^2}\lambda\right) \tag{5}$$

where k_B is the Boltzmann constant, T is the absolute temperature, the quality factor is $Q = g_{tank}/(2\pi f_0)L_{ind})$, Δf is the PN frequency offset. The noise parameter is $\lambda = \gamma + \frac{1}{k_{osc}}$.

From the above equations, it is clearly stated that they are all function of g_m/I_D.

Since the LC-VCO contains monolithic inductors, a realistic inductor model is necessary. For that, it was considered a set of real on-chip inductors belonging to a commercial nanometer conventional CMOS technology. It is a simple model which includes the equivalent inductor and its associated equivalent parallel resistance at the working frequency [5][3].

An exhaustive process is applied [5] to find the design maps of the LC-VCO characteristics. In this process, the LUTs of the FinFETs, LUT$_{FinFET}$, and that of the inductors, LUT$_{ind}$, are known. Then, initially setting f_0, Δf and k_{osc}, each inductor of the LUT_{ind} is picked, and for each g_m/I_D of a predefined set, and applying equations (1), (3), (4), it is easy to find the transistors, inductor and varactor values as well as PN, oscillation amplitude and the current consumption. Following this design methodology, the design maps of power consumption and phase noise against the inductor L_{ind} and g_m/I_D are generated as displayed in Fig. 6 and Fig. 7. They permit not only to extract specific design point, but also to observe the design trade-offs if working in weak or moderate inversion instead of in strong inversion. A clear trade-off arises between I_D and PN, since low power values imply high phase noise figures and vice-versa. As well, working with small inductors provide lower PN figures at the expense of increasing I_D. From this design flow, it is also easy to find Pareto fronts for PN-I_D requirements.

IV. Application Example: 5.8-GHz LC-VCO

From the design flow, we have picked the design corresponding to the pair $(g_m/I_D, L_{ind})$=(15V^{-1},4nH) (marked in Figures

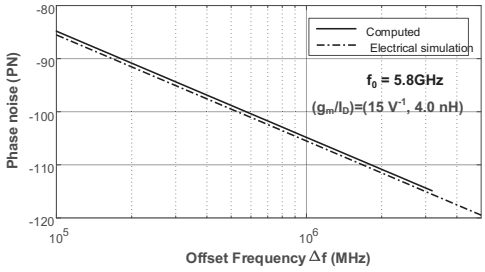

Figure 8. 5.8-GHz LC-VCO comparison between calculate and simulated values.

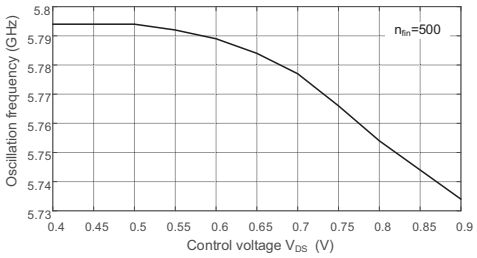

Figure 9. Oscillation frequency versus varactor voltage control.

6 and 7). The resulting n-FinFet and p-Finfet widths are $W_p = 4.1\mu$m and $W_n = 3.8\mu$m and the varactor is C_{var} =180fF. For the calculated value of $I_D = 0.3mA$, the computed $PN_{@400kHz}$ =-97dBc/Hz. Under the Spectre environment, the simulated value of $PN^{sim}_{@400kHz}$=-97.6dBc/Hz was obtained, working with an oscillation frequency of $f_0^{sim} = 5.76$GHz (first harmonic). The simulated PN is compared against the calculated one in the offset frequency range $\{100k, 1M\}$Hz in Fig. 8. As it is observed, for this LC-VCO designed in 20-nm FinFET transistor the g_m/I_D methodology is extremely useful since it attains a good match between theoretical and electrically simulated results and allows to visualize the trade-offs in the circuit design.

To work in the 5.8-GHz ISM unlicensed band, 16 channel with bandwidth of 5 MHz can be utilized for short-range devices. To cover all the channels, coarse and fine tunning is necessary. The former is implemented with an array of capacitors that approximately choose the channel, whereas the latter is made with a varactor that precisely adjust the frequency. The LC-VCO varactor is built with two n-FinFET transistors biased in inversion mode [7], whose drain and source terminals are self-connected and act as the tuning voltage; and their gates are connected to the VCO output voltages. In the implemented VCO, after incorporating the varactor and activating a sub-set of the capacitors of the array, the frequency tuning range covers from 5.79 GHz to 5.74 GHz, as observed in Fig. 9.

V. Conclusions

This paper presented a review of the design of radio-frequency blocks using the g_m/I_D methodology, as well as the usage of semi-empirical models based on look-up tables for 20-nm FinFET transistors. These models described their most significant small-signal characteristics -like current, transconductance, output resistance and capacities- normalized to the transistor size, which were used in design flow of the LC-VCO block. Finally, as a design example, an LC-VCO of the extracted design map is implemented in the Spectre environment, achieving very good matching between results provided by the g_m/I_D methodology and electrical simulation.

VI. Acknowledgment

The authors would link to thanks the ONR under grant ONR N00014141355, TEC2017-87052-P, TEC2013-45638-C3-3-R for financial support.

References

[1] F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep 1996.

[2] A. Shameli and P. Heydari, "A Novel Power Optimization Technique for Ultra-Low Power RFICs," in *ISLPED'06 Proceedings of the 2006 International Symposium on Low Power Electronics and Design*, Oct 2006, pp. 274–279.

[3] R. Fiorelli, F. Silveira, and E. Peralías, "MOST Moderate-Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 3, pp. 556–566, March 2014.

[4] F. P. Cortes and S. Bampi, "A 1.4GHz Up conversion Mixer Design Using the gm/ID Method Suitable for a Multi-Band Analog Interface," in *2007 14th IEEE International Conference on Electronics, Circuits and Systems*, Dec 2007, pp. 1400–1403.

[5] R. Fiorelli, E. Peralias, and F. Silveira, "LC-VCO design optimization methodology based on the gm/ID ratio for nanometer cmos technologies," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 7, pp. 1822–1831, July 2011.

[6] F. Crupi, M. Alioto, J. Franco, P. Magnone, M. Togo, N. Horiguchi, and G. Groeseneken, "Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 7, pp. 439–442, July 2012.

[7] P. Wambacq *et al.*, "The potential of finfets for analog and rf circuit applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 11, pp. 2541–2551, Nov 2007.

[8] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao, "Exploring sub-20nm FinFET design with Predictive Technology Models," in *DAC Design Automation Conference 2012*, June 2012, pp. 283–288.

[9] A. Kranti and G. A. Armstrong, "Design and optimization of finfets for ultra-low-voltage analog applications," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3308–3316, Dec 2007.