All-Optical 3R Burst-Mode Reception at 40 Gb/s Using Four Integrated MZI Switches

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***Abstract*—We demonstrate an all-optical retime, reshape, reamplify (3R) burst-mode receiver (BMR) operating error-free with a 40-Gb/s variable-length asynchronous optical data packets that exhibit up to 9-dB packet-to-packet power variation. The circuit is completely based upon hybrid integrated Mach–Zehnder interferometric (MZI) switches as it employs four cascaded MZIs, each one performing a different functionality. The 3R burst-mode reception is achieved with the combination of two discrete all-optical subsystems. A reshape, reamplify BMR employing a single MZI is used first to perform power equalization of the incoming bursts and provide error-free data reception. This novel approach is experimentally demonstrated to operate error-free, even for a 9-dB dynamic range of power variation between bursty data packets and for a wide range of average input power. The obtained power-equalized data packets are then fed into a 3R regenerator to improve the signal quality by reducing the phase and amplitude jitter of the incoming data. This packet-mode 3R regenerator employs three MZIs that perform wavelength conversion, clock extraction, and data regeneration for every packet separately and operates at 40 Gb/s, exhibiting rms timing jitter reduction from 4 ps at the input to 1 ps at the output and a power penalty improvement of 2.5 dB.**

***Index Terms*—Burst-mode receiver (BMR), dynamic range, integrated Mach–Zehnder interferometer (MZI), optical burst switching, optical packet switching, optical signal processing.**

I. Introduction

OPTICAL packet and burst switching have been introduced as the most competent technologies for third-generation optical networks to enhance bandwidth utilization of the network processing nodes and terminals [1]. The concept of packet and burst switching involves designated time-slots assigned to each user in order to send data to any other user or node, highlighting the multiaccess nature of this scheme. The fundamental feature of multiaccess networks is that successive packets on a single link may vary in terms of phase and amplitude depending on the transmitter characteristics and the optical path traveled by each packet. Key elements for the realization of burst and packet switched networks [2] are the burst-mode receivers (BMRs), since they undertake to handle asynchronous and unequal power level data packet streams to ensure an error-free reception at the intermediate network nodes and end-user terminals.

So far, mainly electronic implementations of BMRs have been demonstrated, operating at 10 Gb/s and requiring a few preamble bits for achieving power equalization and phase recovery [3], [4]. Differential phase shift keying coding schemes also have been utilized in optoelectronic implementations [5] to provide BMRs with enhanced dynamic range. However, increasing demand for a more efficient bandwidth utilization and higher quality of broadband services have set the requirement for all-optical BMR circuits with which increased speed, transmission efficiency, and network granularity can be achieved. All-optical reshape, reamplify (2R) burst-mode reception [6] and retime, reshape, reamplify (3R) regenerators at 40 Gb/s [7] have been demonstrated. Although these circuits have proved the potential of all-optical technology to perform highly functional circuits, they have not been combined to demonstrate a full 3R BMR circuit, revealing in this way the increased scale and complexity of these circuits.

Burst-mode reception is completed in a three-stage process: power equalization of the incoming bursts, clock extraction, and data regeneration for every burst separately [2]. In order to assemble the subsystems required for every stage and realize a larger scale all-optical system, generic small-footprint integrated devices with multifunctional capabilities should be used to simplify a circuit design. Moreover, this would facilitate the integration of larger scale optical subsystems on single platforms. Mach–Zehnder interferometer (MZI) is the best candidate for this role since it has already been integrated as a stand-alone device [8] and has been demonstrated to perform a broad range of functionalities such as bitwise Boolean logic [9], wavelength conversion [10]–[12], demultiplexing [13], and data processing [14].

In this paper, we demonstrate an all-optical 3R BMR circuit operating with 40-Gb/s asynchronous variable-length bursts of data packets with intense power variation. The circuit is completely based upon commercially available hybrid integrated semiconductor optical amplifier (SOA)-based MZI (SOA-MZI) switches [8]. It employs four cascaded SOA-MZIs, each one performing a different functionality. The first SOA-MZI is

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configured to operate as a self-switch and performs 2R burst-mode reception. Three more SOA-MZIs, each realizing a different functionality, are assembled to form a 3R regenerator. In particular, the first SOA-MZI operates as a wavelength converter (WC), while the remaining two SOA-MZIs, with the aid of a Fabry–Pérot (FP) filter, perform clock recovery (CR) and data regeneration [15]. The proposed 3R BMR circuit exhibits an input power dynamic range of 9 dB, has a lock-in time of only 125 ps, and requires a guard band of 350 ps between packets. It requires no optical-electrical-optical converter stages and high-speed electronic processing, and it could be employed as the receiver-end in high-speed optical burst/packet switched networks.

The rest of this paper is organized as follows. Section II presents the experimental demonstration of a novel 2R BMR using a single SOA-MZI. Section III presents the assembly of three SOA-MZIs, each performing a different functionality, to demonstrate an all-optical packet-mode 3R regenerator at 40 Gb/s. Finally, in Section IV, we demonstrate a larger scale optical system by combining the 2R BMR and the 3R regenerator to deliver a complete 3R BMR circuit.

II. Single SOA-MZI 2R Burst-Mode Regenerator

A. Introduction

Large power variations between asynchronous data packets induce an error floor during the data reception process. The role of the 2R BMR is to eliminate this error floor by performing power equalization of the different power levels data packets, with simultaneous 2R regeneration by means of suppressing the signal degradations induced by the accumulation of noise. In this way, an error-free signal is obtained at the output that falls within the operational dynamic range of the 3R regenerator that follows, rendering data regeneration of the bursty packets feasible.

So far, power equalization has been reported utilizing optical limiting amplifier configurations [16], [17]. The first is an optoelectronic approach that makes use of electrical feedback circuit and thus operates at low rates, while the second employs an additional WC and has been shown to operate at 10 Gb/s. Wavelength conversion using a SOA-based delayed interferometer has also been demonstrated to perform power equalization [18] with continuous data streams at 10 Gb/s, but without providing experimental proof of 2R burst-mode reception for asynchronous data packets. The 2R regeneration with noise suppression capabilities of unbalanced MZI has been shown in [19]. However, 2R burst-mode reception performing both power equalization and 2R regeneration has been reported so far only by the study in [6] and has been shown to operate successfully at 40 Gb/s, with an 8-dB dynamic range. Nevertheless, this approach is based on the combination of two discrete optical subsystems, the first exploiting two SOAs to perform power equalization and the second comprising an integrated WC to provide 2R regeneration of the power-equalized optical data bursts.

In this paper, we demonstrate a simple 40-Gb/s all-optical 2R BMR built with only a single hybrid integrated SOA-MZI which has unequal splitting ratio couplers. This unbalanced SOA-MZI exploits the nonlinear transfer function of the interferometer to suppress the "0" noise level and the gain dynamics of the SOAs to achieve packet power equalization. We experimentally demonstrate that it can receive error-free asynchronous and variable-length data packets with up to 9-dB power variation.

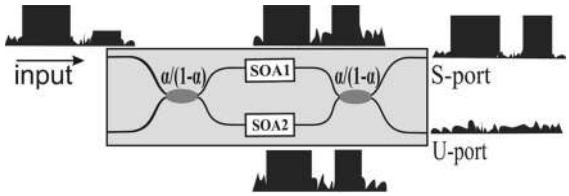

Fig. 1. Configuration of unequal splitting ratio MZI.

The principle of operation of the unequal-coupling-ratio SOA-MZI switch configured as a 2R BMR is shown in Fig. 1. It consists of two couplers with splitting ratio a and of two optical branches, each one employing a SOA as the nonlinear active element. The burst-mode data packets are inserted as the input signal into the SOA-MZI and split into two spatial components of unequal powers aP and $(1-a)P$. The signal component with a power level of aP is injected into the SOA1, and the second component is launched into the SOA2. For a successful burst-mode reception, the two SOAs have to operate at different current conditions I_1 and I_2, respectively, with each driving current determined by the corresponding SOA input signal power. For a higher input power, a higher current value is required, indicating that SOA1 is driven by $I_1 > I_2$, since $aP > (1-a)P$ (a denotes the higher splitting ratio). In this way, each amplifier is forced to operate in its saturated regime for the high-level packets and in its small-signal gain regime for the low-level packets. To this end, a high gain is perceived by the low power level packets, whereas a low gain is experienced by the higher power level packets, resulting in a nearly power-equalized packet stream at the output of each SOA. In addition, the different driving conditions of the two SOAs in combination with the unbalanced nature of SOA-MZI provide a differential phase shift between the two spatial components, since the packet stream traveling through SOA1 experiences a higher gain value and, as a result, a greater phase shift than the corresponding signal traveling through SOA2. By appropriately adjusting the two driving current values, an approximately π differential phase shift between the two power-equalized packet streams at the two branches can be obtained. In this respect, self-switching operation is achieved, and the interference of the two spatial components at the output coupler of the SOA-MZI yields a nearly noise released power-equalized packet stream at the switched port (S-port) of the SOA-MZI. From the above discussion, we can conclude that the equalization properties of the unbalanced SOA-MZI depend on the splitting ratio parameter α, the input signal power level, the SOA driving currents, and the linewidth enhancement factor parameter of the SOAs.

B. Experimental Setup

Fig. 2 shows the experimental setup used to evaluate the 2R burst-mode reception capabilities of the proposed scheme.

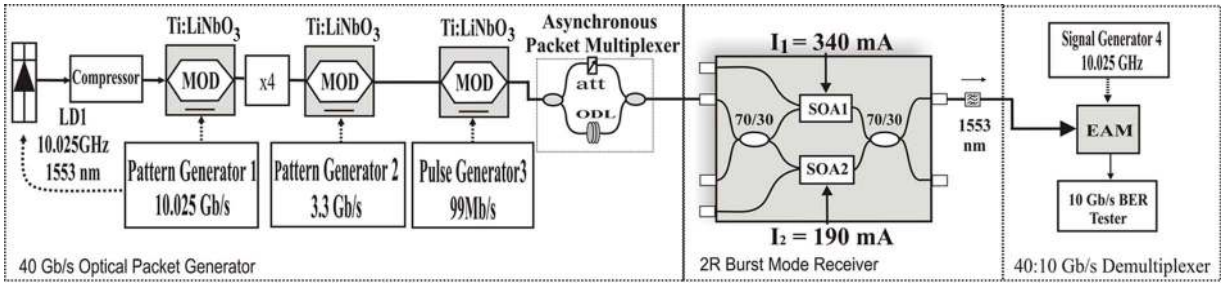

Fig. 2. 2R BMR experimental setup.

It consists of the 40-Gb/s optical packet generator, a hybrid integrated SOA-MZI with unequal splitting ratio couplers that comprises the 2R BMR, and an electroabsorption modulator (EAM) used as a 40–10-Gb/s demultiplexer. The packet generator was designed to produce a stream of variable-length asynchronous data packets exhibiting arbitrary and controllable power levels to simulate bursty traffic. A 1553-nm distributed feedback laser was gain-switched at 10.025 Gb/s to produce 3-ps pulses after both linear and nonlinear compressions. A Ti : $LiNbO_3$ electrooptic modulator and a fiber bit-interleaver were used to form a $2^7 - 1$ pseudo random bit sequence (PRBS) data pattern at 40.1 Gb/s. A second Ti : $LiNbO_3$ electrooptic modulator driven by a 3.3-Gb/s pattern generator was used to produce a sequence of two different data packets of unequal length. This packet stream was then launched into a third Ti : $LiNbO_3$ modulator driven with a low rate signal to partially modulate only one of the two consecutive packets and to allow the second packet through unaffected. As a result, a sequence of two data packets with unequal power levels was obtained at the modulator output. This signal was then introduced into a split-and-delay multiplexer in order to form asynchronous data packets. The asynchronous multiplexer consisted of a 3-dB coupler with fiber lengths of 250-ns differential delay at its outputs and a second 3-dB coupler to recombine the relatively delayed signals. A variable optical delay line and an optical attenuator were employed in the two branches so as to be able to control the phase alignment and the power level of the interleaved packet streams. The resulting signal was then inserted as the input signal into the 2R BMR, which consisted of a hybrid integrated SOA-based MZI with 70/30 input and output coupling ratios. The SOAs provided small signal gain of 23 dB at 200 mA and 30 dB at 300 mA.

C. Results and Discussion

In order to evaluate the performance of this BMR concept, streams of packets with different power level characteristics were constructed and launched into the unequal-coupling-ratio SOA-MZI, whose two SOAs were driven with different current values. Fig. 3(a) shows the input signal trace and eye diagram of 48- and 75-bit-long consecutive packets exhibiting a 9-dB packet-to-packet power variation, defined as the ratio of higher to lower levels. In the eye diagram, the low power level packet cannot be identified since it is hidden under the response of the 40-GHz photodiode. Fig. 3(b) shows the corresponding power-equalized packet stream and eye diagram obtained at the output of the SOA-MZI. The initial 9-dB power variation

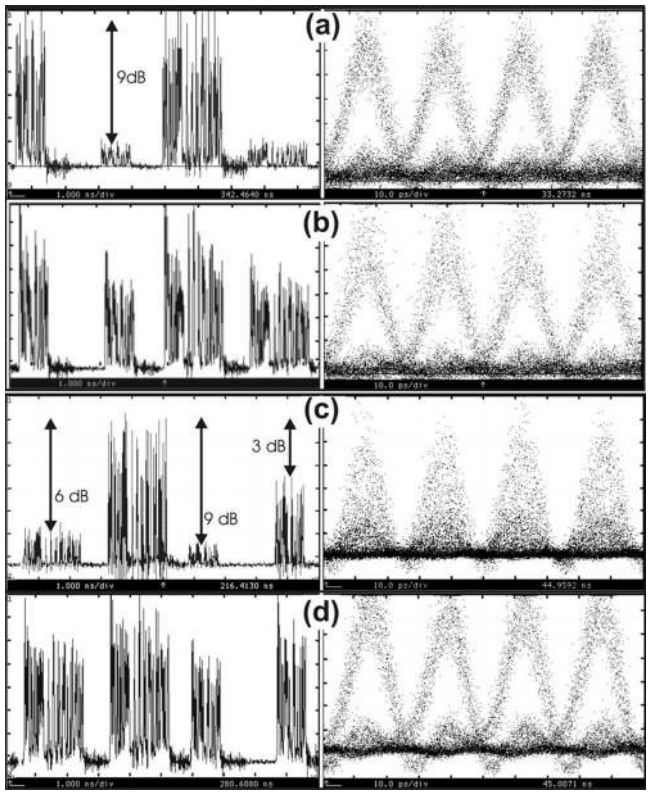

Fig. 3. Pulse traces and eye diagrams for (a) two power levels input, (b) two power levels output, (c) four power levels input, and (d) four power levels output. The time scale is 1 ns/div for the traces and 10 ps/div for the eye diagrams.

between the incoming packets has been reduced into 2-dB amplitude modulation between the power-equalized packets. This amplitude modulation can be reduced using an additional holding beam at the expense of decreasing the input packet power variation dynamic range.

In order to determine the dynamic range of average input power levels within which this 2R BMR scheme can operate, the output packet power variation was recorded for a broad range of average input signal pulse energies and for input packet-to-packet power variations of 3, 6, and 9 dB. Results from these measurements are shown in Fig. 4 and indicate that, for average input pulse energies between 80 and 360 fJ, the power difference is reduced from 3, 6, and 9 dB at the input to 0.5, 1, and 2 dB at the output, respectively. These results essentially imply that, besides being capable of suppressing a large power variation at its input, this 2R BMR scheme can maintain this performance over a broad range of average input powers.

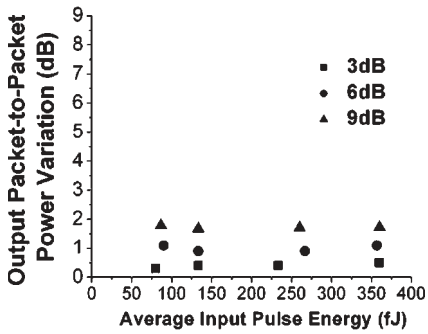

Fig. 4. Experimentally obtained output packet-to-packet power variation for input packet-to-packet power variations of 3, 6, and 9 dB versus average input pulse energy.

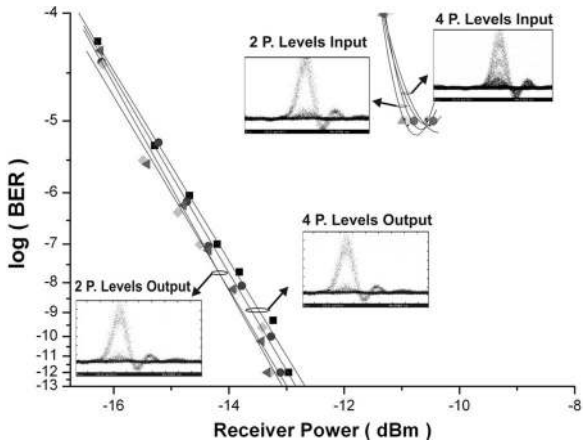

Fig. 5. BER curves for two demuxed channels for 2P. level input, 4P. level input, 2P. level output, and 4P. level output.

The power equalization process was also investigated for simultaneous packet power variations by creating a sequence of four input packets, each having a different power level with a deviation of 3, 6, and 9 dB with respect to the highest power packet. Fig. 3(c) shows the pulse trace and the eye diagram of this signal, revealing full eye closure. Fig. 3(d) shows the corresponding pulse trace and eye diagram at the output of SOA-MZI, where packets were power-equalized within 2 dB and a clear open eye was obtained. The extinction ratio of the low power packet at the input was measured as 4 dB, and a successful operation indicates the highly nonlinear behavior of the packet equalizer. It should be noted that the current driving values of the SOAs were fixed to 340 and 190 mA, respectively, for both cases of input signals. This indicates that the unequal-coupling-ratio SOA-MZI successfully operates for true bursty traffic since it can handle simultaneously packets of arbitrary power levels without altering the SOA driving conditions.

Bit error rate (BER) measurements were carried out to reveal error-free reception of the BMR after the equalization and regeneration processes. An EAM was used in demultiplexing the 40-Gb/s packets into 10-Gb/s data streams, and Fig. 5 shows the BER measurements obtained for two of the four demultiplexed 10-Gb/s channels. The sensitivity of the receiver used was -13 dBm. The BER curves for both input signals, i.e., with two power levels and four power levels between the packets, respectively, indicated an error floor of 10^{-5}. However, the corresponding curves at the output of the receiver show that the error floor was eliminated and that power equalization within 2 dB provided error-free data reception.

III. 40-Gb/s All-Optical 3R Regenerator

A. Operation and Experiment

Following the packet power equalization operation, the 3R regenerator has to be employed to improve the signal quality by reducing the phase and amplitude jitter of the incoming data. An optical 3R regeneration at 40 Gb/s has been reported by employing EAMs and highly nonlinear fiber [20] or a SOA with an MZI [21]. Yet in these cases, a high-frequency electrical circuit has been employed for the clock acquisition, in which case an optoelectronic conversion becomes inevitable. An optically clocked 40-Gb/s 3R regenerator has been proposed in [22], where the regeneration was accomplished through a self-pulsating laser and an MZI switch.

In this section, we report an all-optical 3R regenerator for different length packets at 40 Gb/s, which is demonstrated by using three integrated SOA-MZI switches and a fiber FP (FFP) filter. The experimental setup consists of the 40-Gb/s optical packet generator, the WC implemented with a hybrid integrated SOA-MZI and operated as an adaptation interface stage, and the 3R regenerator circuit employing a FFP filter and two hybrid integrated SOA-MZIs, as shown in Fig. 6. A 40 : 10 demultiplexing circuit (EAM) was also employed in order to obtain the BER measurements. The first stage is included as an adaptation interface which assigns to the incoming signal local physical conditions by wavelength converting it, such as polarization and phase [23]. The original pulse train was produced through a semiconductor mode-locked laser operating at a repetition rate of 10.025 GHz and at a wavelength of 1556 nm. An electrical circuitry was built in order to introduce phase jitter at the generated 4-ps optical pulses. In particular, a sinusoidal variation was imposed on the electrical signal through a variable phase shifter driven by a 10-MHz function generator. The jittery signal was then fed onto the semiconductor laser for mode locking, as well as to the demultiplexing circuit for 10-Gb/s channel demultiplexing, as will be described later. PRBS $2^7 - 1$ was imposed on the pulse train by means of a $LiNbO_3$ (MOD) electrooptic modulator, while that was multiplied to 40 Gb/s with the aid of a fiber bit-interleaver $(\times 4)$. The packets were then generated by modulating the continuous code word through an EAM. The 40-Gb/s test signal was then split and fed to the WC section as well as to the decision gate of the regenerator.

The signal has been wavelength converted to 1548 nm through the first SOA-MZI (MZI 1) operating with a push–pull control scheme for high-speed operation. The differential delay of the control signals has been optimized by means of an optical delay line in order to minimize the switching window of the device, and 7-ps pulses were obtained at its output. The wavelength-converted signal was then amplified and injected into the CR circuit to achieve an all-optical timing extraction. The CR employed a low-Q fiber FFP filter with a free spectral range (FSR) equal to the line rate (40.1 GHz) and finesse of 27, as well as an integrated SOA-MZI (MZI 2) powered by a

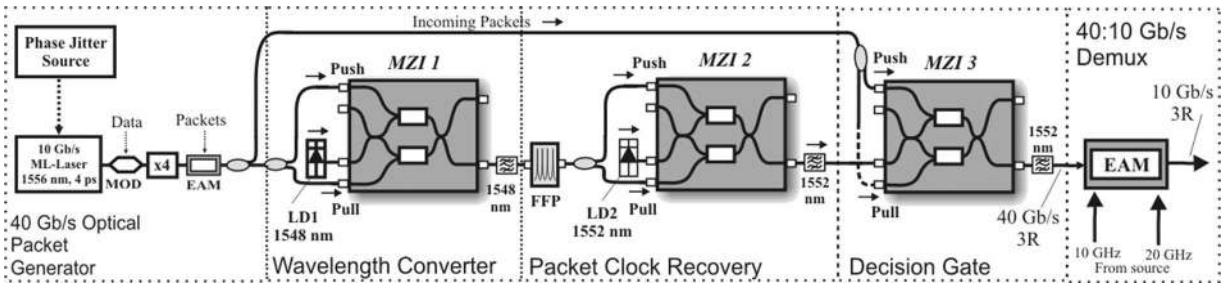

Fig. 6. Experimental setup used to demonstrate the 3R regenerator subsystem.

continuous wave (CW) signal at 1552 nm (LD 2), operating as a holding beam. The FFP filter acts as a passive optical resonator that extracts the line rate spectral component of the input signal, transforming the data packets into clock packets with intense amplitude modulation and duration similar to the corresponding input, as a result of the exponentially decaying impulse response of the filter. This clock-resembling signal entered the nonlinear switch which acted as a power limiter saturated by the CW light. A push–pull configuration was adopted in order to reduce the switching window, thus obtaining 9-ps clock pulses. The recovered clock was then used as the input signal to the third SOA-MZI (MZI 3), where the incoming data served as the two differential controls. In particular, the incoming data packet has been delayed before the third MZI, appropriately, in order to be temporally synchronized with the corresponding recovered clock packet in the MZI. Through a simple logical AND operation, the incoming information was imprinted on the low phase and amplitude jitter clock pulses at the output of the switch. Finally, in order to measure the BER for each multiplexed 10-Gb/s channel, an EAM setup was built for demultiplexing each channel. The switching window of the demultiplexer was achieved by imposing on the EAM the jittery 10-GHz sinusoidal signal superpositioned to a 20-GHz component obtained through a frequency doubler and a 20-GHz microwave filter.

B. Results and Discussion

The 3R regenerator performance was tested with short data packets of different durations, and the results obtained are summarized in Fig. 7. In particular, the oscilloscope traces of the incoming degraded 40-Gb/s packets are illustrated in parallel to the respective eye diagrams. The incoming packet lengths are 3.6 and 1.6 ns for the left-hand side and right-hand side packets, respectively. Each of the incoming data packets accommodated a series of two successive pulses (preamble bits) in their front-end to assist the clock acquisition process that follows in MZI 2. The recovered clock packets are obtained at the output of the CR stage, ensuring clock persistence for a duration equal to the corresponding data packet length, in addition to 100 ps of rise time and 350 ps of fall time. The former value indicates the time taken by the CR to lock to the line-rate of the incoming data packet, while the latter value determines the time required by the CR to lose synchronization after each packet. The same values were measured for the small packet. The incoming data packet is synchronized with the corresponding duration of the recovered clock packet in the decision gate (MZI 3),

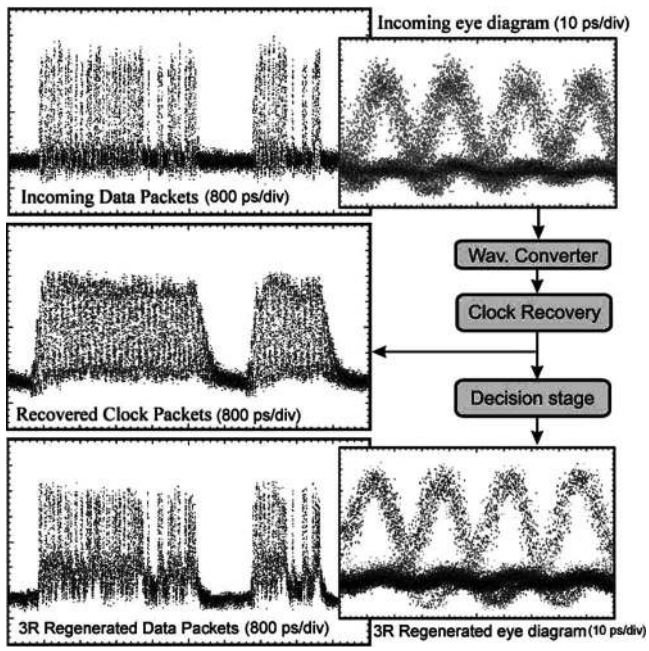

Fig. 7. Results obtained with the 3R regenerator subsystem.

TABLE I
POWER/ENERGY REQUIREMENTS OF MZI SWITCHES

MZI	Input	Control (Push-Pull)
1^{st} MZI (WC)	6.5 dBm (CW)	200 fJ - 100 fJ (pulsed)
2^{nd} MZI (CR)	6.0 dBm (CW)	300 fJ - 250 fJ (pulsed)
3^{rd} MZI (AND)	100 fJ (pulsed)	90 fJ - 20 fJ (pulsed)

while the rise and fall times of the recovered clock packet are not used. The pulses during the rise and fall times of the recovered clock packet are residual and should be accounted for as the necessary interpacket guardbands to avoid overlapping of successive clock packets. The regenerated data packets are obtained at the output of the MZI 3, as shown in Fig. 7 with the respective eye diagrams. The switching energy requirements of each SOA-MZI are summarized in Table I, showing the low (femtosecond range) operational requirements (power is quoted for CW signals). The eye opening of the regenerated signal demonstrates phase jitter, as well as amplitude jitter reduction when compared to the eyes of the incoming data. Phase jitter reduction was confirmed after conducting jitter measurements on the second microwave harmonic of the demultiplexed 10-Gb/s channel at each stage of the regenerator. The single side band (SSB) noise spectra of the input, recovered clock, and regenerated signals were integrated from an offset frequency of

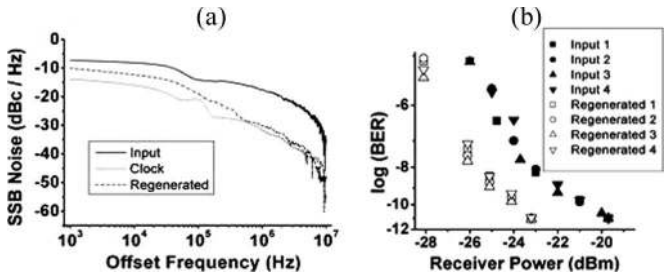

Fig. 8. (a) SSB integration for phase jitter measurements and (b) BER measurements obtained for the 3R regenerator subsystem. Integration range: from 1 kHz to 10 MHz.

1 kHz to 10 MHz from the 20-GHz component, as depicted in Fig. 8(a). The root-mean-square (rms) values were 4 ps for the input, 900 fs for the recovered clock, and 1 ps for the regenerated signal. The phase jitter reduction originates from the FFP filter transfer function, which is centered to the carrier, suppressing the data harmonics, thus reducing the phase jitter of the recovered clock. The amplitude noise reduction is achieved by operating MZI 2 in the deep saturation regime, forcing the switch to operate as a hard limiter and thus smoothing out pulse amplitude fluctuations.

By using an EAM, BER measurements were carried out after demultiplexing each degraded incoming 10-Gb/s channel and the regenerated counterparts. A different receiver was used for this experiment, with a sensitivity of -20 dBm. Fig. 8(b) shows the BER curves for each demultiplexed 10-Gb/s channel at the input and output (regenerated) of the circuit. A negative power penalty of more than 2.5 dB is demonstrated for all four data channels. The SOAs of the SOA-MZI switches were insensitive to control signal polarization state, as observed experimentally.

IV. 3R BMR

A. Experimental Setup

So far, we have demonstrated a 2R burst-mode reception circuit and a 3R regenerator at 40 Gb/s. The former subsystem can be employed to reduce large packet power variations within a range of 2 dB and ensure error-free burst-mode data reception. The latter subsystem improves highly degraded data packets in terms of timing and amplitude jitter, resulting in a power penalty improvement of 2.5 dB. In this section, we combine the functionalities of a 2R BMR and a 3R regenerator to demonstrate for the first time a complete all-optical 3R BMR system at 40 Gb/s by using an array of four hybrid integrated SOA-MZIs.

The experimental setup is shown in Fig. 9, consisting of the 40-Gb/s optical packet generator, the BMR, and an additional SOA-MZI used as a 40–10-Gb/s demultiplexer. The asynchronous packet traffic was generated in the same way that is described in Section II. However, in this paper, the third modulator was set to transparency and is not depicted in Fig. 9. Thus, the optical packet generator provided a stream of packets carrying 40.1-Gb/s $2^7 - 1$ PRBS data. The asynchronous packet multiplexer was used to induce a variable differential delay between the packets, altering the phase alignment of the asynchronous packets. The attenuator in one of the branches controlled the power variation between the data packets that were set to exhibit two different power levels. This packet stream entered as input signal to the power equalizing state.

The SOA-MZI1 of Section II was used for the equalization process of the 3R BMR. In order to operate successfully, SOA-MZI1 required 129 fJ/pulse of the input signal. The 3R regenerator was implemented following the concept described in Section III, employing three SOA-MZIs to perform wavelength conversion, CR, and data reception, respectively. As such, SOA-MZI2 provided at its output a wavelength converted at 1556-nm 40-Gb/s data signal, with a pulsewidth of 7 ps. This signal entered the CR module that employed a FFP filter with an FSR of 40.1 GHz and a finesse of 39, followed by SOA-MZI3 that was powered by a CW signal at 1559 nm (LD2). Data reception was completed in SOA-MZI4 by using the power-equalized packets provided by SOA-MZI1 as input and their corresponding recovered clock packets as the triggering signal. Table II summarizes the power/energy requirements of the SOA-MZI switches. The differences with Table I are due to the different driving currents and gain characteristics of the SOAs of the MZIs used in each experiment. Erbium-doped fiber amplifiers (EDFAs) were employed between the SOA-MZI stages in order to compensate for the losses and properly adjust the required power levels. Table II also shows the power requirements for a fifth SOA-MZI that was used as the demultiplexer of the 40-Gb/s packets into 10-Gb/s data streams to perform the BER measurements. SOA-MZI5 operated in a push–pull control configuration, and a 3-ps clock pulse stream at 1553 nm was used as the control signal.

B. Results and Discussion

The performance of the 3R BMR circuit was evaluated for asynchronous data packets of various length, period, and contents that exhibited two different power levels. Fig. 10 illustrates the evolution of the burst-mode reception process through trace and eye diagrams obtained at each stage of the circuit. Fig. 10(a) shows a typical sequence of four asynchronous incoming data packets at 40 Gb/s having a size of 48 and 75 bits, respectively, exhibiting power variation of 9 dB. In the eye diagram, the small power packet cannot be identified since it is masked under the response of the 40-GHz photodiode used. Fig. 10(b) shows the respective power-equalized packet stream obtained at the output of SOA-MZI1. The 9-dB power variation between the incoming packets has been reduced to roughly 2 dB, providing in this way a signal that is within the operational dynamic range of the 3R regenerator. Fig. 10(c) depicts the output of the first stage of the 3R regenerator implementing the adaptation interface. We note that the wavelength-converted data signal exhibits a moderate improvement regarding the amplitude modulation. Fig. 10(d) shows the recovered clock packets obtained at the output of the CR stage. They persist for a time duration that equals that of the corresponding input data packet, extended on its leading edge by a 5-bit rising time and on its trailing edge by a 14-bit decay time. The former value indicates the time required by the CR to lock to the line-rate of the incoming data packet, while the latter determines the time required by the CR signal to decay

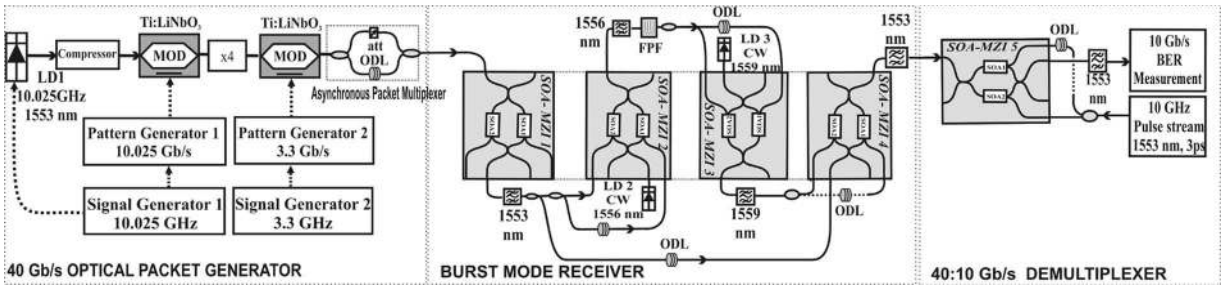

Fig. 9. Experimental setup to demonstrate 3R burst-mode reception.

TABLE II
POWER/ENERGY REQUIREMENTS OF MZI SWITCHES

MZI	Input	Control	
		Push (pulsed)	Pull (pulsed)
MZI1 (PE)	129 fJ		
MZI2 (WC)	7.6 dBm (CW)	107 fJ	49 fJ
MZI3 (CR)	0 dBm (CW)	100 fJ	65 fJ
MZI4 (AND)	47 fJ (pulsed)	359 fJ	143 fJ
MZI5 (DEMUX)	4 fJ (pulsed)	100 fJ	10 fJ

to $1/e$ after each packet. The hits inside the eye diagram of this clock signal are due to the bits of the rising and trailing edge of the packets. Fig. 10(e) illustrates the received equalized data packets at the output of the BMR, indicating clearly that timing jitter and amplitude modulation reduction with respect to the corresponding signal at the output of the power equalization unit (SOA-MZI1) are obtained.

Fig. 11 shows the BER measurements for two of the four 10-Gb/s channels. The receiver used in this paper exhibited a sensitivity of -13 dBm. As shown by the curve identified as "BtB 9 dB," it was not possible to obtain error-free measurements of the input packets with the 9-dB power variation, and an error floor was obtained at 10^{-5}. The error floor was eliminated after the power equalization stage, as shown by the curve "PE o/p," and an error-free operation could be obtained. This effectively indicates that even a single optical gate with unequal coupling ratios and SOA driving currents can perform as a 2R burst-mode reception device. Error-free operation was also obtained at the output of the BMR ("BMRx o/p"), with a negative power penalty of 1.95 dB with respect to the power equalization stage output. Error rate measurements were also taken for the input packet signal with no power fluctuation, and this is shown by the curve "BtB 0 dB." This BER curve lays between the two previous curves and has a 1.3-dB positive power penalty offset with respect to the "BMRx o/p" curve, revealing the overall 3R regeneration capability of the complete BMR circuit. Similar results were obtained for the other two demultiplexed channels.

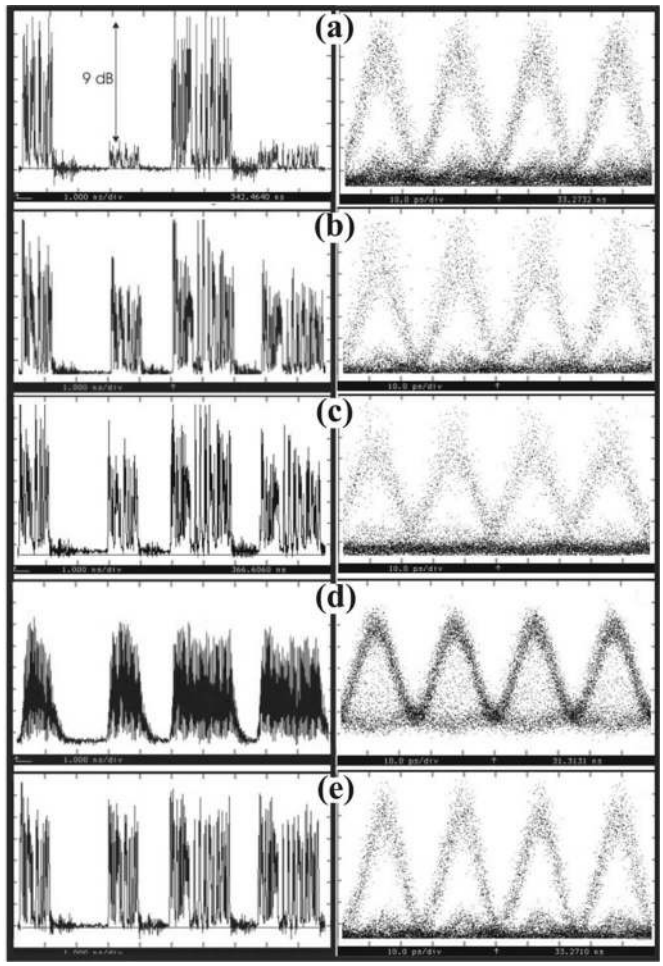

Fig. 10. Trace and eye diagrams of (a) incoming data packets, (b) power-equalized packets, (c) wavelength-converted packets, (d) packet CR, and (e) recovered data packets. The time scale is 1 ns/div for the traces and 10 ps/div for the eye diagrams.

V. CONCLUSION

We have presented an all-optical 3R BMR operating error-free with 40-Gb/s asynchronous data packets of variable length and 9-dB packet-per-packet power variation. The circuit was implemented by combining two discrete subsystems, a 2R BMR, and a 3R regenerator. Within this context, we have presented a novel scheme for 2R burst-mode reception employing a single SOA-MZI that was configured to operate as a self-switch. This setup was demonstrated to perform power equalization for 40-Gb/s variable-length asynchronous optical packets exhibiting 9-dB packet-to packet power variation, providing an error-free signal for a wide range of average input power. The 3R regenerator employed three SOA-MZIs, each performing a different functionality such as wavelength conversion, CR, and data regeneration. The 3R regenerator circuit reduced the signal rms timing jitter from 4 ps at its input to 1 ps at its output and exhibited a power penalty improvement of 2.5 dB. The MZI switches of both subsystems exhibited a stable operation after properly adjusting the incoming signal

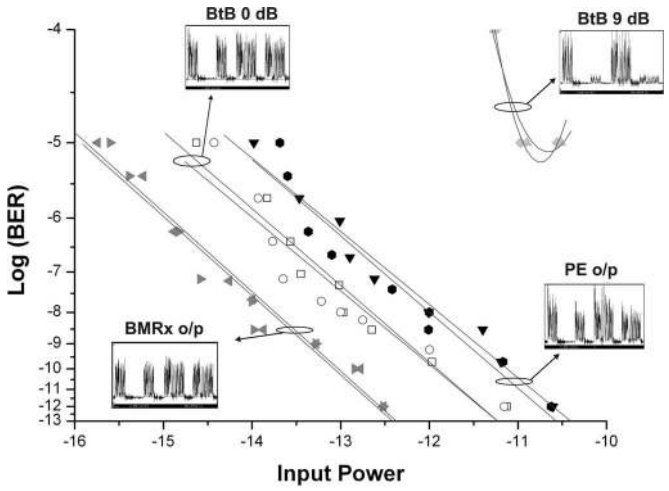

Fig. 11. BER measurements for 3R burst-mode reception.

polarization with the aid of the external polarization controllers. In addition, the MZIs were insensitive to the polarization state of the control signals since the SOAs exhibited a polarization sensitivity less than 1 dB.

By combining these subsystems, a 3R BMR was implemented using a sequence of four cascaded integrated SOA-MZI switches, demonstrating a flexible and scalable approach in terms of manufacturing. It is envisaged that, through photonic integration research, such a subsystem could be potentially integrated into a single hybrid platform, as aimed for by IST-MUlti-Functional integrated arrays of Interferometric Switches (MUFINS) project [24], through which integrated arrays of multiple interferometric switches are being developed, reaching toward photonic large-scale integration.

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