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ABSTRACT

As the focus of graphene research shifts from fundamental physics to applications, the scalability and reproducibility of experimental results become ever more important. Graphene has been proposed as an enabling material for the continuing growth of the telecommunications industry due to its applications in optoelectronics; however, the extent of its adoption will depend on the possibility to maintain the high intrinsic quality of graphene when processing it using the industry-standard approaches. We look at the challenges of scalable graphene integration and the opportunities presented by the recent technological advances.

INTRODUCTION

Within two decades from its first isolation, graphene holds the potential to significantly impact the field of optoelectronics and photonics by overcoming the limits of the existent technologies and by opening new applicative avenues.[1,2] Graphene offers ultrafast optical transitions and broadband operation with bandwidth spanning from ultra-violet to far infrared (thanks to the absence of a bandgap).[1] It has emerged as an excellent platform for broadband image sensors[3] and terahertz detectors,[4] though due to its monatomic thickness, the interaction with normal incident free-space light is limited to ∼2.3%.[5] The optical interaction of graphene can be significantly increased by placing it on a waveguide, where it can absorb ∼0.2 dB μm^{-1}, corresponding to 10 dB absorption for a 50 μm device.[6] As such, graphene has emerged as a particularly promising material for the building blocks of photonic-integrated circuits for optical communications—electro-optical modulators,[7,8] photodetectors,[9] and optical switches.[10] The enormous growth of datacom and telecom technologies over the last few decades requires constant improvement in terms of bandwidth, consumption, and cost, posing great technological challenges. The Ethernet roadmap predicts a bandwidth doubling every two years, and at the front of ever-increasing requests (e.g., bandwidth increases at constant power consumption and cost),[11] existing technology (based on $LiNbO_3$, InP, or Si for modulators and InP or Ge/Si for detectors) encounters limitations in terms of footprint, power consumption, and cost of integration.[2]

Graphene-based photonic devices have shown the potential to solve many of these issues. In particular, electroabsorption[8] and electrorefraction[12] effects enable compact graphene modulators that can reach high speed.[13] Graphene photodetectors (GPDs) have been demonstrated with data rates exceeding 100 Gbit s^{-1}.[14,15] Furthermore, GPDs based on the photo-thermo-electric (PTE) effect[16–18] can be operated without an applied bias and can, thus, have low power consumption. PTE-based GPDs require high-mobility graphene and were typically fabricated using exfoliated materials,[16–19] though, recently, it has been demonstrated that the required quality can be achieved using scalable technologies.[15,20,21] One of the main advantages of graphene-based photonics is that graphene layers can be integrated with silicon photonics platforms via transfer.[22,23] In principle, it is a simpler process than wafer bonding, flip-chip, or heteroepitaxy techniques employed for the integration of InP-[24] and Ge/Si-based photonics[25] and can be performed at back end of line (BEOL). As such, it allows graphene processing without subjecting the underlying photonic or electronic structures to high temperatures (as is the case for InP[24] or Ge[25,26] heteroepitaxy). BEOL integration could also allow the use of diffusion barriers to minimize the risk of metal contamination in electronic components.[27,28] This could enable monolithic integration of photonic circuits and driving hardware.[2] Thanks to the versatile transfer of graphene to substrates of choice[29] and the possibility of electrostatic gating,[30] double-layer graphene devices[8,13,21] (where graphene acts both as the light-interacting material and the gate, separated by an

insulating layer) can be fabricated on passive photonic waveguides (e.g., Si, Si_3N_4, or SiO_2) without the need for ion implantation, which can greatly simplify device production and can, thus, offer significant cost reduction.[2] Overall, graphene-based photonics holds the promises to overcome the limitations of existent technology by offering building blocks (i.e., modulators, detectors, and switches) that present superior performance, reduced footprint, low power consumption and potential cost-effective, and straightforward integration with existent platforms.

With these enticing prospects in mind, the successful industrial adoption of graphene in optical communications will rely on the possibility to fabricate graphene-based photonic devices on wafer scale. Figure 1 shows a timeline of technologically relevant examples of waveguide-integrated graphene photodetectors[9,14,15,17–21,31–38] and modulators.[7,8,12,13,39–43] Due to the larger device dimensions needed to effectively manipulate light, almost all modulators in the literature have been fabricated using CVD graphene, whereas in the case of photodetectors, there has been a gradual shift from non-scalable toward scalable or partially scalable materials, as the synthesis and transfer technology has evolved over time. On the other hand, for truly competitive performance of graphene optoelectronics, we will rely on the possibility to achieve graphene carrier mobility $\mu > 10\,000\,cm^2\,V^{-1}\,s^{-1}$,[2,44] directly on photonics platforms. In optical modulators, long scattering time (and thus high μ) is desired in order to achieve high transparency and, thus, low insertion loss.[44] In graphene photodetectors, high carrier mobility is needed to obtain a large Seebeck coefficient, allowing us to exploit the photothermoelectric (PTE) effect, which can lead to fast devices with low power consumption.[45] Over the last 10 years, remarkable progress has been achieved in large-area synthesis of graphene on various substrates; however, there is no widely accepted technique that is capable of addressing all the requirements of integrated photonics: high mobility, repeatability, homogeneity over wafer scale, and low metal contamination. Graphene transfer to the target substrate, a necessary step, is extremely challenging as it typically requires transferring a layer of monatomic thickness over an area of thousands of square millimeters (for a 200 mm wafer) with the inevitable formation of cracks, folds, and tears. Also, scalable encapsulation, i.e., dielectric deposition (a requirement for most types of photonic devices) and contact deposition are delicate fabrication steps that need to be optimized to realize graphene-based photonic technology.[46] All these aspects will be discussed in detail in the following sections.

WAFER-SCALE GRAPHENE SYNTHESIS

Out of various approaches for the production of graphene,[47] bottom-up synthesis from gaseous precursors, chemical vapor deposition (CVD), appears to offer the highest material quality on a large scale. In the early days of graphene research, large-area synthesis of graphene was commonly obtained by thermal decomposition of SiC,[48,49] an approach that offered many benefits for fundamental research. However, the prohibitive cost of SiC substrates and the challenging transfer of graphene have eventually limited the appeal of this material for device applications. In 2009, chemical vapor deposition (CVD) of graphene on nickel (Ni) thin films[50] and copper (Cu) foils[51] was presented. Due to a relatively low carbon solubility, Cu has eventually emerged as the optimum substrate for largely self-limiting growth of monolayer graphene.[51] Typically, graphene has only weak epitaxial relation to the copper growth substrate.[52] The growth initiates with nucleation of randomly oriented islands, which eventually join to form a polycrystalline film. The presence of grain boundaries in such graphene can lead to charge carrier scattering and, thus, reduced carrier mobility;[53] therefore, there has been a serious effort to develop ways of synthesizing highly crystalline large-area graphene. To this end, several approaches have been adopted by the research community: (1) growth of hexagonal graphene single crystals (SCs) with maximized dimensions,[54–56] (2) seamless stitching of graphene domains on monocrystalline Cu foils,[57,58] or (3) growth of graphene on semiconductor wafers with metal thin films.[59] While the research community has mostly focused on maintaining the crystallinity of graphene over the whole sample area, an enticing alternative strategy is to controllably synthesize graphene SCs with dimensions of the order of the individual photonic components (tens to hundreds of micrometers), rather than entire wafers (hundreds of millimeters), by seeded growth of graphene.[60–62] The initial works used polymeric seeds, producing crystals with dimensions of up to 30 μm.[60,61] This was improved by around an order of magnitude by patterning Cu foils with chromium (Cr) nucleation seeds.[62] Such SCs with lateral dimensions of up to 350 μm are compatible with the typical dimensions of graphene photodetectors and modulators. By depositing the nucleation seeds on Cu to match the geometry of the targeted photonic circuit, graphene crystals can be grown and transferred to coincide precisely with the photonic components.[13,21,42] Crucially, it has been demonstrated that single-crystal CVD graphene can have doping and mobility values matching those of exfoliated flakes,[63–65] though top and bottom encapsulation with hexagonal boron nitride (hBN) is necessary to reach the full potential of high-quality graphene.

Despite the promising approach of CVD growth on Cu, synthesis of graphene directly on dielectric substrates has also been studied. Some applications could benefit from direct (transfer-free) deposition of graphene on the target substrates, though the appeal of this

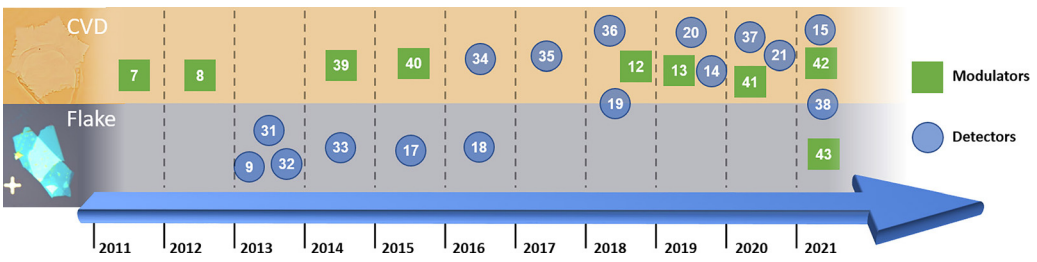

FIG. 1. Timeline of technologically relevant examples in literature of waveguide-integrated graphene modulators and detectors, classified by scalable [chemical vapor deposition (CVD)] or non-scalable (flake) fabrication techniques. References 19 and 38 used heterostructures assembled with both exfoliated and CVD materials.

approach in photonics is limited as the high synthesis temperatures are not compatible with the presence of photonic structures on the substrates. Another advantage is the elimination of any risk of metal contamination in the semiconductor processing lines.[66] This is relevant because Cu, the preferred substrate for graphene synthesis, can have highly detrimental effects to silicon transistors.[67] In particular, for applications where Front-end-of-line (FEOL) integration of graphene is needed, metal contamination should not exceed levels on the order of 10^{10} atoms/cm^2, well below the contamination levels observed in graphene transferred from Cu.[66] Several strategies for CVD growth of graphene directly on technologically relevant surfaces such as SiO_2 have been demonstrated.[68] Due to the lack of catalytic activity, they typically require either a high deposition temperature near 1200 °C (Ref. 69) (incompatible with the presence of photonic structures on the growth substrate) or rely on remote metallic catalyst[70] (and, thus, do not eliminate the contamination risk). Furthermore, such material typically has a small domain size[68] with a mobility below or around 1000 cm^2 V^{-1} s^{-1}, i.e., approximately an order of magnitude lower than single-crystal graphene transferred from Cu. Promising results have been reported when synthesizing graphene directly on sapphire.[71–73] Synthesis of graphene on 150 mm sapphire wafers with a carrier mobility of ∼2500 cm^2 V^{-1} s^{-1} (comparable to most results obtained from polycrystalline graphene grown on Cu foil) has been recently reported.[73] Furthermore, it has been shown that a polymer-based transfer approach allows to transfer 150 mm wafers of graphene on a target substrate while complying with metal contamination requirements.[73] It is likely that by finely controlling the surface reconstruction of the underlying sapphire substrate,[73] higher mobility values might be achieved, which would improve the prospects of this synthetic avenue.

Table I summarizes various graphene synthesis technologies and their relative advantages/disadvantages with respect to various aspects of photonics integration.

WAFER-SCALE GRAPHENE TRANSFER ON PHOTONIC PLATFORMS

As discussed above, transfer is a crucial step for any kind of graphene photonic devices. Successful wafer-scale graphene transfer needs to avoid mechanical defects in graphene monolayer (tears and wrinkles) while maintaining negligible contamination levels in order to meet the requirements of mobility and residual doping for photonic applications. The initial demonstration of the so-called "wet transfer" of graphene from the metal substrates opened up a new flexible approach for the integration of graphene on any platform.[50] This approach relies on etching the metallic growth substrate with iron-based etchants such as iron chloride or iron nitrate to release the graphene (typically supported by a thin polymeric film) and subsequently picking up the graphene membrane from the aqueous solution directly with the target wafer. While this method is relatively simple and does not require any specialized equipment, it poses an elevated risk of contamination due to etchant residues trapped between the graphene and the wafer. This was partially mitigated by introducing additional chemical cleaning,[76] changing the etchant chemistry,[77] and using wax-based supports,[78] though alternative strategies have been sought after

TABLE I. Comparison of different scalable graphene synthesis technologies.

	Graphene on SiC[49]	Polycrystalline graphene on Cu foil[51]	Epitaxial SC graphene on thin films[59] or SC graphene arrays[62]	Graphene on sapphire[73]
Transfer for photonics integration	− − No reliable transfer method	+ + Straightforward transfer Several methods available	+ Graphene on thin films: delamination challenging Single-crystal arrays: alignment needed	+ Dry delamination
Scalability	+ Substrates up to 150 mm Graphene up to 100 mm	+ + No scalability limitations (roll-to-roll growth and transfer)[74]	+ Scalability non-trivial but highly flexible via stamping transfer[42]	+ + 300 mm substrates available Graphene on 150 mm
Cost	− − Excessive substrate cost	+ + Very low substrate cost	+ Moderate to low substrate cost (Pre-processing needed)	+ Moderate substrate cost Possibility for re-use
Room-temperature carrier mobility (cm^2 V^{-1} s^{-1})	+ Up to 5000[75]	+ Up to 5000 25 000 in LMHs[64]	+ + Up to 10 000 on SiO_2 150 000 in LMHs[65]	− Up to 2500[73]
Contamination	+ Fab-compatible	− Currently not fab-compatible	− Currently not fab-compatible	+ Fab-compatible

to further minimize the impact of residual contamination and forces subjected to the graphene films due to surface tension effects in aqueous media. In particular, graphene delamination from the growth substrate was demonstrated to be a quicker and cleaner alternative to chemical etching of the substrate. The release of graphene can be mediated either by oxidizing the graphene–metal interface[79,80] or by electrochemically promoted means.[81,82] Graphene grown on dielectrics can also be transferred by mechanical release using laminated polymer films.[73] After release from the growth substrate, graphene supported by a polymeric membrane can be removed from the aqueous environment using a frame or a viscoelastic support, which allows its lamination onto the target substrate in dry conditions, offering further benefits with regard to its quality.[62,80,83] The existing technologies have been scaled to transfer wafer-sized graphene monolayers[80] as well as continuous roll-to-roll sheets,[74,77] though these large-area samples have not demonstrated mobility values required for high-performance photonic devices. A potential solution to overcome this hurdle is to perform repeated dry laminations single-crystal graphene arrays, thus populating a 150 or 200 mm wafer.[42] This technique is similar to the approach used for microtransfer printing of semiconductors[84,85] and allows the synthesis of graphene on a smaller scale, with greater control of its quality. When transferred with a semi-dry approach and subsequently encapsulated with hBN, single-crystal CVD graphene can show mobility values practically indistinguishable from exfoliated flakes.[65] Considering the similarity of the process, automated transfer printing systems could be adapted for graphene transfer, allowing full-wafer integration of single-crystal graphene arrays. The improved local control provided by semi-dry transfer and the consequent quality benefits may justify the increased complexity and time requirements compared to wafer-scale wet transfer.

GRAPHENE ENCAPSULATION

As discussed above, dielectric encapsulation of graphene is one of the most important steps of processing for successful adoption of graphene in industry. Sandwiching graphene between flakes of transition metal dichalcogenides (TMDCs)[86] or hBN, i.e., assembling so-called layered material heterostructures (LMHs) can allow exploiting the extraordinary electrical properties of graphene.[63,65,87] Encapsulation can also protect the graphene from environment[88] and can act as a gate dielectric for locally gated samples.[89] While hBN is the undoubted encapsulant of choice for small-scale research samples, the lack of high-quality wafer-scale hBN or equivalent materials means that thin films of high-k oxides such as Al_2O_3 and HfO_2 have typically been adopted to date.[46] These dielectrics are most commonly deposited via atomic layer deposition (ALD).[90] Due to the nature of the process, nucleation of the dielectric on flat, high-quality graphene is suppressed, making it difficult to obtain a dielectric with homogeneous thickness. Different strategies were developed to achieve high-quality ALD films.[90] Homogeneous dielectric nucleation can be achieved using an ALD seeding layer, which is introduced by the functionalization of the graphene surface with polymers,[91] thin metal films,[92] or an aqueous pre-treatment,[93] but it can often lead to reduced graphene quality due to sp^3 hybridization or increased doping. The degradation of graphene can be minimized by reducing the deposition temperature, but this occurs at the expense of the quality of the dielectric. Another possible solution to encapsulate graphene with minimal effect on its transport properties is by deposition of polymers, which can be done in ambient conditions. Indeed, poly(vinyl alcohol) (PVA) has been used as an encapsulant and gate dielectric in scalable and highly performing graphene photodetectors.[21] While samples encapsulated using aforementioned scalable materials exhibit promising stability over long time scales,[92] the increase in mobility is moderate (if any) and cannot be compared to the order of magnitude improvement observed in LMHs.[63,64,87] In fact, it has been demonstrated that such high mobility can be achieved due to the atomically perfect interface,[94,95] which is a result of a self-cleaning effect between flakes of layered materials.[86,96] Such high-mobility heterostructures can be produced with "synthetic" graphene (i.e., using CVD graphene rather than flakes);[63–65] however, samples with synthetic layered dielectrics have not exhibited remarkable mobility values to date.[97,98] It can reasonably be considered that this is partially due to polymer residues and residual humidity trapped at the interface of 2D material heterostructures, leading to bubbles of contamination.[94] Indeed, it has been shown that large-area, bubble-free 2D CVD LMHs can be obtained by layering the materials in vacuum.[99] It can also be noted that even lacking an increase in carrier mobility, using large-area 2D materials such as monolayer hBN as encapsulants can be beneficial for other purposes, such as protection of graphene for plasma-enhanced deposition of Si_3N_4[42] or as an oxidation barrier for materials, which are unstable in air such as $MoTe_2$.[100] In general, it can be expected that the development of fully synthetic large-area LMHs will help bring many of the early promises of graphene to fruition.

CONTACTING GRAPHENE FOR PHOTONICS

The possibility to fabricate graphene–metal contacts with low resistance values and high reproducibility will also be crucial for highly performing graphene optoelectronics. Research devices are typically contacted by depositing metals on top of graphene, the so-called top contacts. Different metals have been utilized for this purpose to find the material offering the optimum performance, while taking into account the potential issues in prospect of CMOS integration.[101] In addition, various contact geometries have been investigated to reduce the contact resistance, for example, by pre-patterning the graphene before metal deposition in order to increase the length of an exposed edge.[102–105] Despite the promising performance of top contacts, true industrial integration will likely rely on an industry-standard damascene process,[23] in which metal contacts are deposited through the holes (vias) etched in dielectric encapsulation.[106] While in the traditional damascene process, the etch is stopped at the active silicon layer; this is more complicated for graphene due to its monatomic thickness; therefore, the damascene process for graphene needs overetching and making the contact to the graphene edge. Indeed, edge contacts have been widely adopted for LMHs[87] as they allow full encapsulation of graphene prior to subjecting it to device fabrication steps. Edge contacts to ALD-encapsulated graphene have not been demonstrated, though when applied to encapsulation-free graphene, promising contact resistance and reproducibility were achieved.[107]

OUTLOOK

Overall, graphene-based optoelectronics promise higher data rates, lower losses, smaller footprints, lower energy consumption, lower complexity in manufacture, and, thus, lower device cost, making graphene an enticing candidate material for datacom and telecom applications. Prototype devices already demonstrate performance

exceeding that of conventional technologies, though commercial adoption of layered materials will require some technological shifts to make the transition from the lab to the fab. Some graphene products are already making their way to the market, with an Emberion broadband camera[108] using graphene electrodes available in late 2020. On the other hand, waveguide-integrated modulators or photodetectors, where graphene has a more functional role, will need further process improvements before they can be commercialized. Their fabrication will likely rely on CVD synthesis of single-crystal graphene, as polycrystalline graphene may not reach the carrier mobility requirements, unless cleaner transfer strategies are devised for large grain material. The subsequent stages of graphene integration, namely, transfer and encapsulation, also have room for improvement. One of the main hurdles is that graphene is highly susceptible to the quality of both the underlying substrate and encapsulation. The intrinsic surface roughness of photonic wafers, even after planarization, can limit the carrier mobility of transferred graphene. Likewise, the deposition of dielectric encapsulation can subject graphene to unintentional doping and strain. The quality requirements necessary for high-performance optoelectronics have been experimentally reached in LMHs, i.e., by sandwiching flake and CVD graphene between exfoliated flakes of layered semiconductors (TMDCs) and insulators (hBN). The next technological leap will be the demonstration of high-quality wafer-scale hBN and TMDCs suitable for large-area LMHs. High-quality synthesis of these materials is not a trivial problem as they are multi-element and, thus, have potential for many more types of defects compared to carbon-based graphene. Furthermore, achieving homogeneous wafer-scale growth with finite thickness suitable for encapsulation of graphene (>20 nm) will require extensive process optimization. Nonetheless, the potential of these materials has clearly been appreciated, with a significant research effort redirected from synthesis of graphene toward other layered materials, though real wafer-scale LMHs with interface quality matching that of exfoliated materials are probably still a few years away. A potential short-term solution, which could allow an incremental improvement in graphene quality necessary for waveguide-integrated optoelectronics, could be 2D–3D integration, e.g., using mono- or few-layer hBN as a protective spacer for thin film oxide or nitride dielectrics. Whichever strategy will ultimately prevail, close collaboration between the industry and research community is fundamental for its development. A good example of this is the European Union's Graphene Flagship and its recent 2D experimental pilot line (2D-EPL) project.[109] The 2D-EPL, launched in 2020, has the aim of establishing a graphene production and processing workflow compatible with the standards of the semiconductor industry. By 2024, it is expected that the 2D-EPL will have a facility capable of producing prototypes of graphene-based electronics, photonics, and sensors, demonstrating graphene's readiness for the market.

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DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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