PHOTONIC SENSORS / Vol. 6, No. 4, 2016: 366–371

All-Optical Flip-Flop Based on Coupled SOA-PSW

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Abstract: The semiconductor optical amplifier (SOA) has obvious advantages in all-optical signal processing, because of the simple structure, strong non-linearity, and easy integration. A variety of all-optical signal processing functions, such as all-optical wavelength conversion, all-optical logic gates and all-optical sampling, can be completed by SOA. So the SOA has been widespread concerned in the field of all-optical signal processing. Recently, the polarization rotation effect of SOA is receiving considerable interest, and many researchers have launched numerous research work utilizing this effect. In this paper, a new all-optical flip-flop structure using polarization switch (PSW) based on polarization rotation effect of SOA is presented.

Keywords: Polarization switch; all-optical flip-flop; nonlinear polarization effect; semiconductor optical amplifier

Citation: Lina WANG, Yongjun WANG, Chen WU, and Fu WANG, "All-Optical Flip-Flop Based on Coupled SOA-PSW," *Photonic Sensors*, 2016, 6(4): 366–371.

1. Introduction

All-optical signal processing techniques mainly rely on the devices' nonlinear effects to achieve. The intensity, frequency, phase and polarization state of the incoming optical signals can be modulated by using nonlinear effects, which can achieve wavelength conversion, logic gates [1, 3], signal regeneration, and other all-optical signal processing functions [2]. The implementation of the flip-flop [3] in this paper is based on semiconductor optical amplifiers (SOAs). The nonlinear effects of SOA can be summarized into the following four forms: cross-gain modulation (XGM) [3], cross-phase modulation (XPM), four-wave mixing (FWM), and nonlinear polarization rotation [1, 4] (NPR) effects. Compared with several other nonlinear effects, NPR effect can consider the SOA's polarization state of polarized sensitive effectively.

All-optical flip-flop [5−8] is the basic processing unit in the optical signal processing devices. Through a combination between the various flip-flops, it can achieve a variety of high-speed optical signal processing functions. The applications of flip-flops based on SOAs are widely used nowadays. In [3], all-optical flip-flop based on coupled SOA fiber ring lasers was demonstrated. It described four different types of flip-flops. In [9], a set-reset all-optical flip-flop based on Mach-Zehnder interferometer (MZI) [5−7] of SOA was proposed. All-optical flip-flop memory based on two coupled polarization switches was proposed in [10]. Each flip-flop has a different performance and structure. In this paper, a type of clocked all-optical flip-flop structure utilizing NPR effect and polarization switch is presented. We use the bit rates with 1 Gbit/s and 2.5 Gbit/s to demonstrate the feasibility of this structure.

Received: 20 May 2016 / Revised: 10 June 2016

DOI: 10.1007/s13320-016-0353-5
Article type: Regular

2. SOA-based optical logic gates

2.1 Basic equations of SOA

All-optical logic gate including optical switches, optical computing, and optical regeneration is one of the key components in the field of all-optical signal processing. In this paper, the implementations of all-optical logic gates are based on the NPR effect of SOA. The basic equations describing the working characteristics of SOA are carrier concentration rate equation and optical power transmission equation.

The rate equation of the carrier concentration change is

$$\frac{\partial N(z,t)}{\partial t}=\frac{I}{eV}-R(N)-\frac{\Gamma g(N,\lambda)P(z,t)}{h\nu A} \qquad (1)$$

where $N(z,t)$ is the carrier density of the SOA active region at position z in time t, P is the optical signal power of the SOA active region, and $g(N,\lambda)$ is the material gain coefficient of the optical signal.

The equation of the power change is

$$\frac{\partial P_k(z,t)}{\partial z}=\left[\Gamma g(N,\lambda_k)-\alpha_{\text{int}}\right]P_k(z,t). \qquad (2)$$

The SOA adopts the segmentation model to simulate

$$\Delta z=L/M \qquad (3)$$

where L is the length of the active region and M is the number of segments.

The decomposition of the polarized optical field divides into a transverse electric (TE) and transverse magnetic (TM) component. The output of light power P is given by

$$P_{\text{out}}=P^{\text{TE}}+P^{\text{TM}}\pm 2\sqrt{P^{\text{TE}}P^{\text{TM}}}\cos\Delta\phi \qquad (4)$$

where the phase difference is $\Delta\phi=\phi^{\text{TE}}-\phi^{\text{TM}}$. Equations (1)−(4) are the basic equations we use in the numerical calculations.

2.2 All-optical logic gates

In order to achieve all-optical SR and JK flip-flops, it needs two types of logic gates including "AND" and "$A\cap B\cap\overline{C}$". The paper utilizes a simple logical structure to implement logic gates. The schematic setup of all-optical logic gates based on SOA-NPR effect is shown in Fig. 1. The signal A and the signal B simultaneously inject into the SOA. The wavelength of signal A is λ_1, and the wavelength of signal B is λ_2. After two beams are coupled into the SOA, as a result of NPR effect, it implements two types of logic gates. Port 2 outputs "AND" logic gate while Port 1 outputs the "$A\cap\overline{B}$" logic gate. It needs two structures to implement the $A\cap B\cap\overline{C}$ logic gate.

The simulation results of the logic gate are shown in Figs. 2 and 3. The two results utilize different bit rates with 1 Gbit/s and 2.5 Gbit/s. The clock pulse widths are 0.3 ns and 0.15 ns, respectively. The signal A is probe light, signal B is pump light, and the extinction ratio of logic gates reaches more than 30 dB.

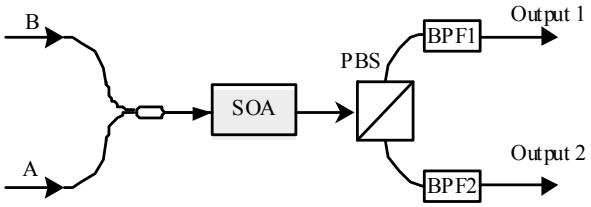

Fig. 1 SOA-based optical logic gates structure.

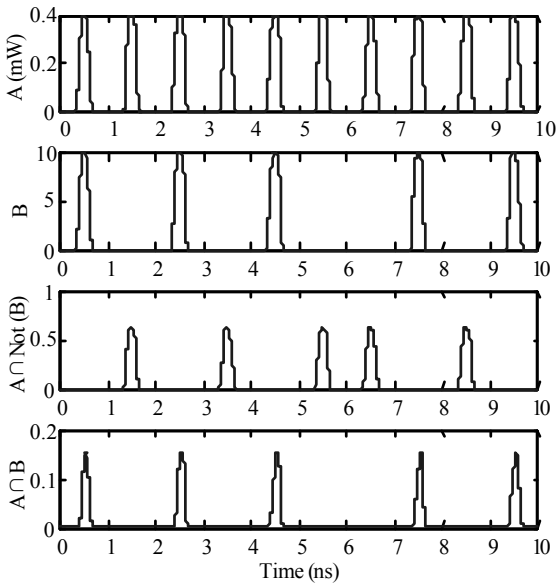

Fig. 2 Logic gate simulation results with bit rate of 1 Gb/s.

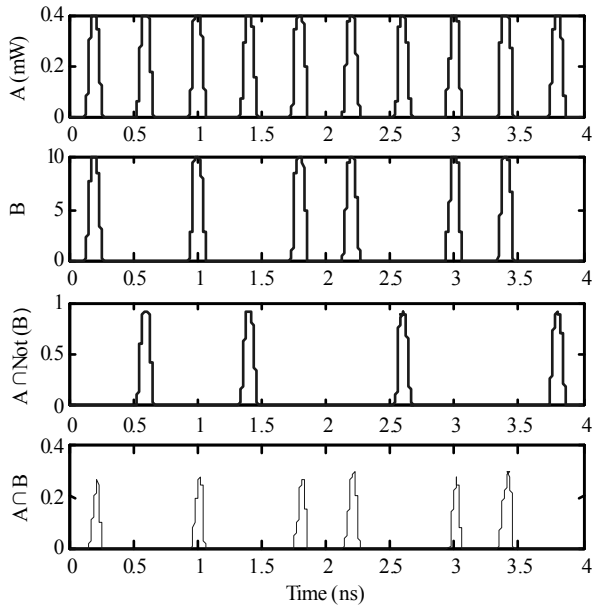

Fig. 3 Logic gate simulation results with bit rate of 2.5 Gb/s.

3. Optical SR latch based on SOA-PSW

As shown in Fig. 4, the optical SR latch has two different states. In State 1, Laser1 emits continuous wave (CW) light at wavelength λ_1 that is amplified by SOA_1, and then the output light is sent into polarizing beam splitter (PBS). The refractive index of the TE mode and TM mode is changed by the light that is fed into the SOA_2 through PBS. It makes the Laser2's output light with wavelength λ_2 after through SOA_2 can not enter PSW_1 (PSW: polarization switch). At this time, the PSW_1 is dominant and PSW_2 is subordinate. The port Output1 emits the light at wavelength λ_1 while the port Output2 has no output. Similarly, in State 2, the port Output2 emits the light at wavelength λ_2 while the port Output1 has no output. In order to change the state of the flip-flop, the light pulse of set or reset is injected into the dominant PSW, which changes the refractive index of the TE and TM modes, so that the PSW's light polarization state fails to pass PBS. Thus the SOA of the original slave PSW will not contain the injected high power light, so the light in the original slave PSW can go through PBS and thereby enter the dominant PSW, thus two PSWs swap positions and complete the state switching.

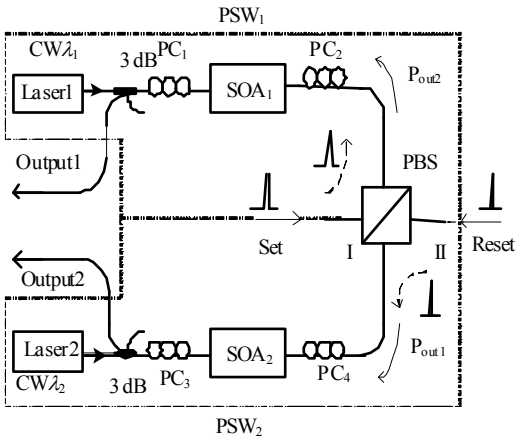

Fig. 4 Experimental setup of all-optical SR latch based on two coupled SOA-PSW.

The advantage of this structure is using two symmetrical polarization switches and an interference structure. In addition, the set and reset operations are symmetrical, the state switching speed is fast, and it only depends on the length of fiber between the two SOAs.

4. Two types of all-optical clocked flip-flops

In order to have a more detailed description of the proposed structure, this paper describes and illustrates two types of all-optical clocked flip-flops including SR and JK flip-flops. The all-optical clocked SR and JK flip-flops work with a clocked synchronization signal.

4.1 SR flip-flop

The SR flip-flop setup is shown in Fig. 5. This logic structure includes two "AND" logic gates and one optical SR latch. The clock (CLK) signal and S signal compose one "AND" logic gate, and the CLK signal and R signal form the other "AND" logic gate. Then the two outputs are separately sent into the set and reset latch ports.

In the stable operation time, the flip-flop is in a steady state. Only when a clock pulse comes in, depending on the S and R values at that time, the state transition occurs, that is so-called the state switching time. In addition to the above cases, the flip-flop no longer changes its state. That is called flip-flop's clocked synchronization.

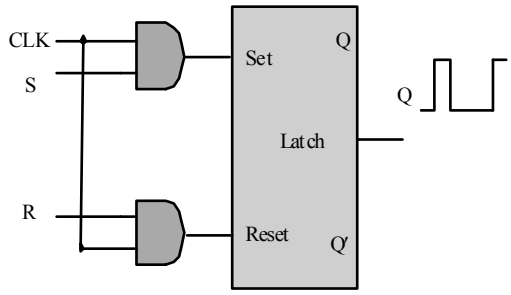

Fig. 5 SR flip-flop logic structure.

The clocked SR flip-flop experimental results are shown in Figs. 6 and 7. In Fig. 6, the clock pulse has a repetition rate of 1 GHz with a pulse width of 0.3 ns. In Fig. 7, the clock pulse has a repetition rate of 2.5 GHz with a pulse width of 0.15 ns. The figures show that the flip-flop's falling edge time is shorter than the rising edge time, because the gain increases slowly to its recovery time after a decrease in the SOA gain.

4.2 JK flip-flop

The JK flip-flop setup is shown in Fig. 8. This logical structure includes two $A \cap B \cap \overline{C}$ logic gates and one SR latch. The CLK signal, J signal, and Q signal compose one $A \cap B \cap \overline{C}$ logic gate, and the CLK signal, K signal, and inverted Q signal form the other $A \cap B \cap \overline{C}$ logic gate. Then the two outputs are separately sent into SR latch ports.

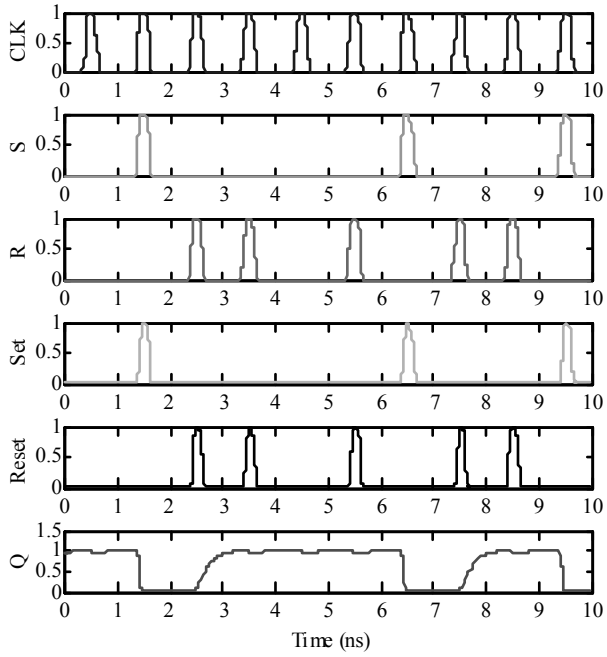

Fig. 6 SR flip-flop simulation result with bite rate of 1 Gb/s.

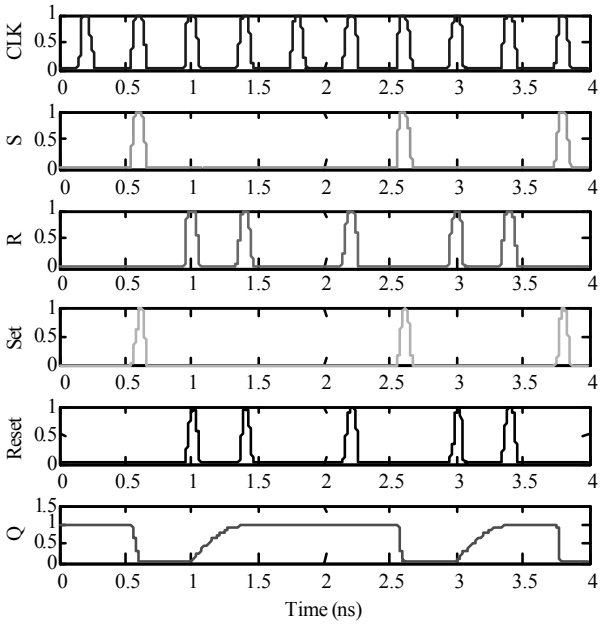

Fig. 7 SR flip-flop simulation result with bit rate of 2.5 Gb/s.

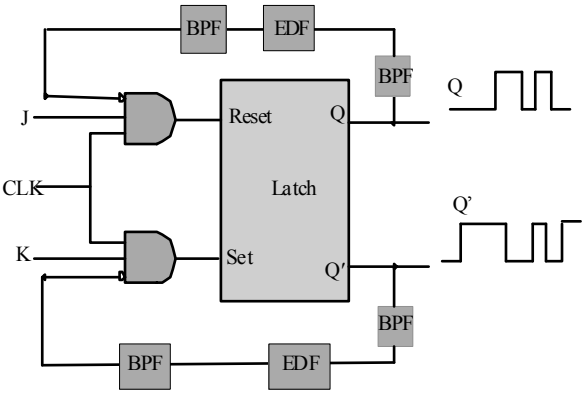

Fig. 8 JK flip-flop logic structure.

The JK flip-flop state depends on the injection of external input signals and two previous opposite states. The difference with the SR flip-flop is that the JK flip-flop requires two feedback signals as input.

In the stable operation time, the flip-flop is in a steady state. Only when a clock pulse comes in, depending on the J, K values and two feedback signals at that time, the state transition occurs. The same with the SR flip-flop, the clock pulse has a repetition rate of 1 GHz and 2.5 GHz. The external input signals' pulse width are 0.3 ns and 0.15 ns, respectively. The transition time of 2.5 Gb/s bit rate is slightly better than 1 Gb/s. In Fig. 10, the falling edge time is about 30 ps while the falling time is

about 40 ps in Fig. 9. Figs. 9 and 10 show that the flip-flop's falling edge time is shorter than the rising edge time, because the gain increases slowly to its recovery time after a decrease in SOA gain. Two different results indicate that this structure can handle different bit rates.

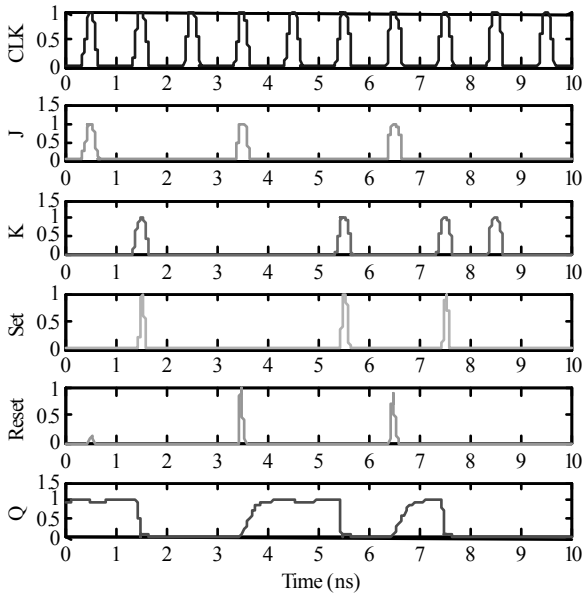

Fig. 9 JK flip-flop simulation results with bit rate of 1Gb/s.

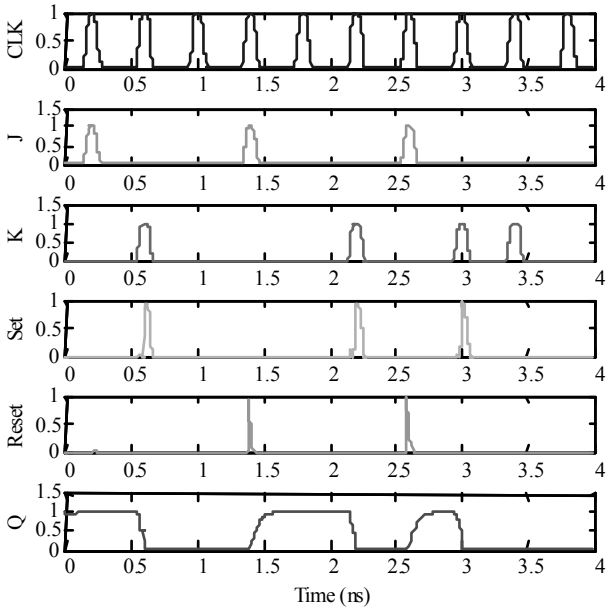

Fig. 10 JK flip-flop simulation results with bit rate of 2.5 Gb/s.

5. Conclusions

In this paper, we have discussed two aspects including the logic gates based on SOA-NPR effect and the flip-flops based on two coupled nonlinear polarization switch of SOA. According to the working principle of SOA, we achieve all-optical SR and JK flip-flops with the clock signal pulse repetition frequency of 1 GHz and 2.5 GHz, and the clock pulse widths are 0.3 ns and 0.15 ns, respectively. In the simulation, the SOA parameters such as carrier density, gain factor, the carrier lifetime, and optical gain are important to ensure the correct of the flip-flop operation. The final results show that the work in this paper has a certain significance for the study of all-optical flip-flop.

Acknowledgment

Thanks to the financial supports from the National Natural Science Foundations of China (61378061 and 61575026).

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