All-Silicon 99.35% Efficient Three-Phase Seven-Level Hybrid Neutral Point Clamped/ Flying Capacitor Inverter

Jon Azurza Anderson, Eli J. Hanak, Lukas Schrittwieser, Mattia Guacci, Johann W. Kolar, and Gerald Deboy

***Abstract*—With the increasing use of photovoltaic systems, a large demand for efficient, power-dense and lightweight grid-interface inverters is arising. Accordingly, new concepts like multi-level converters, which are able to reduce the converter losses while still keeping a low construction volume, have to be investigated. The hybrid seven-level topology analyzed in this paper comprises an active neutral point clamped stage, followed by a flying capacitor stage. Compared to a pure flying capacitor converter, the combination of these two stages allows to save more than half of the capacitor volume, while still having the same requirement for the output filter stage, and hence, the same output filter volume. Moreover, the topology employs low-voltage devices and ensures low conduction and switching losses, resulting in a higher efficiency. The principle of operation of the system is briefly reviewed, and based on a detailed component modeling, an efficiency vs. power density optimization is carried out, for which switching loss measurements of state-of-the-art 200 V semiconductors are performed. From the optimization, a high-efficiency design is selected and the practical hardware realization is discussed. The simulation and optimization results are then verified by realizing an all-silicon 99.35% efficient three-phase seven-level system, featuring a volumetric power density of 3.4 kW/dm^3 (55.9 W/in^3), a gravimetric power density of 3.2 kW/kg, and fulfilling CISPR Class A EMI requirements. Finally, it is shown that an all-silicon realization with next generation silicon switches can achieve 99.5% efficiency with the same hardware, and 99.6% with commercial state-of-the-art GaN switches.**

***Index Terms*—Flying capacitor converter, hybrid active neutral point converter, multi-level, PV inverter, ultra-high efficiency.**

I. Introduction

As photovoltaic (PV) energy generation provides a continuously increasing share to the net electricity supply [1], [2], there is a clear demand for power electronics with high efficiency, high power density, low weight and low costs [3]–[6]. For PV systems with high capacity factors, which are in operation for many hours a day, a high energy conversion efficiency is of major importance [7]. With the goal of exploring the efficiency limits, this paper presents an ultra-efficient multi-level three-phase inverter solution designed for a typical PV installation, as conceptually shown in Fig. 1, targeting a peak efficiency of 99.5% for a nominal power of 10 kW.

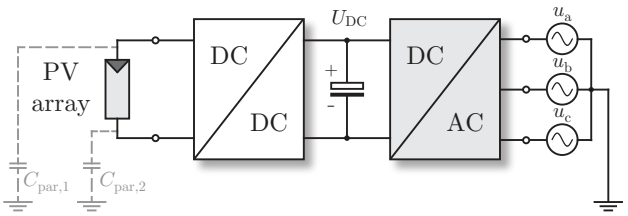

Fig. 1. System overview for transformerless transfer of PV power into the low-voltage three-phase grid (400 V_{rms}, line-to-line). The PV array is typically followed by a DC/DC converter for maximum power point (MPP) tracking and a three-phase PWM inverter (highlighted), which is the focus of this paper.

When aiming for ultra-efficient converters, the trade-off with respect to losses and volume between active (power semiconductors) and passive (magnetic and capacitive) components has to be evaluated in detail. As three-phase converters are typically hard-switched, an optimum between conduction and switching losses that favors large die areas and low switching frequencies exists [8]. However, low switching frequencies lead to bulky magnetic components. This contradiction can be solved by the use of multi-level topologies like the flying capacitor converter (FCC), illustrated in Fig. 2(a) for the case of seven levels. Multi-level converters reduce the inductance requirement of the AC-side inductors for a given current ripple amplitude quadratically with respect to the number of levels, due to the multi-level output voltage characteristic and the increase of the effective switching frequency, leading to smaller and more efficient magnetic components [9], [10]. Additionally, multi-level converters take advantage of low-voltage power MOSFETs, featuring a higher hard-switching figure of merit (FOM) compared to high-voltage power semiconductors [11]. To achieve a multi-level output voltage characteristic with an FCC, capacitors carrying an integer multiple of the lowest cell voltage are alternatingly connected to the output during operation. However, the capacitance requirement of the flying capacitors (FCs), driven by the need to constrain the switching frequency voltage ripple across them, is directly proportional to the load current (and hence, output power) and inversely proportional to the switching frequency [9]. Accordingly, ultra-high power densities can be achieved at the expense of an efficiency reduction by using high switching frequencies (in the hundreds of

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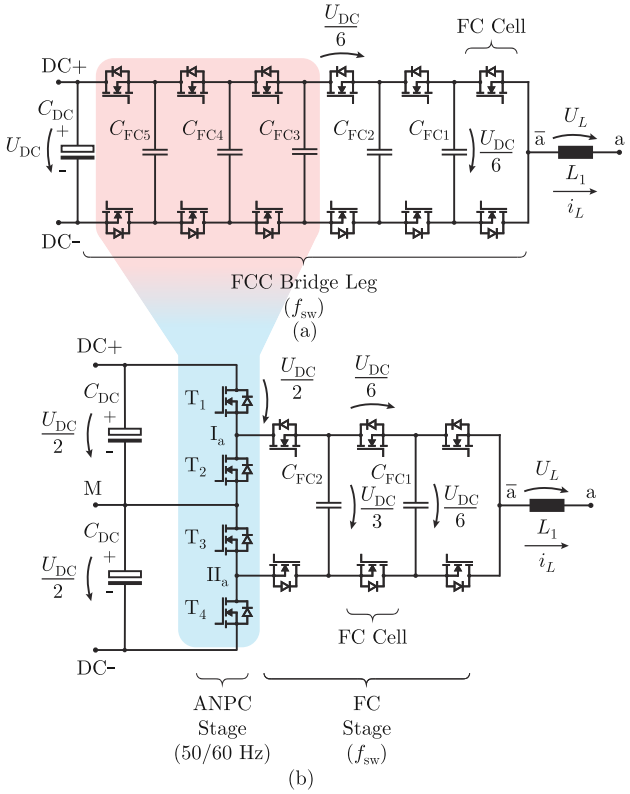

Fig. 2. Circuit schematic of a 7L-FCC bridge-leg, which is purely composed of low-voltage semiconductors operated at switching frequency (a) and the 7L-HANPC bridge-leg structure, i.e., a hybrid approach composed of an ANPC stage with semiconductors switching at 50/60 Hz, and an FC stage, with semiconductors operating at switching frequency (b). Both arrangements are shown for phase a of the three-phase (phases a, b, c) inverter topology.

TABLE I
INVERTER SPECIFICATIONS

$P_{nominal}$	10 kW
$P_{rated,\ max}$	12.5 kW
$U_{dc,\ nominal}$	720 V
U_{ac}	400 V_{rms}
f_{mains}	50 Hz
EMI Filter Requirement	Class A

kHz range), that favor the utilization of ceramic capacitors with high energy density [12], [13]. However, as already mentioned, ultra-efficient hard-switching converters designed for high power ratings are typically operated at low switching frequencies (low tens of kHz) [14], [15]. These low switching frequencies lead to higher capacitance requirements of the FCs, giving a clear incentive to research alternatives to the FCC approach, which should still offer multi-level voltage characteristics but with a smaller capacitance demand. A topology that allows reducing by more than half the number of capacitors is presented in [16], [17], where a hybrid approach between the active neutral point clamped (ANPC) converter and the FCC is proposed (cf., Fig. 2(b)), hereafter referred to as the Hybrid Active Neutral Point Clamped (HANPC) converter. This topology, besides reducing the number of capacitors, enables a further volume saving, as only the capacitors with the lowest voltages remain. This is advantageous, since the higher the voltage rating of the capacitors, the lower the capacitance density, and hence, more capacitors have to be arranged in parallel and/or series, as can be seen, e.g., for the case of a thirteen-level FCC in [18]. These characteristics of the HANPC converter outperform the FCC in terms of achieving higher power densities for ultra-efficient converters, in particular for three-phase inverters in the 10 kW range targeting 99.5% efficiency, as shown in a comprehensive multi-level topology evaluation done in [9].

Therefore, this paper focuses on the optimization and hardware realization of an all-silicon ultra-efficient passively-cooled 12.5 kW three-phase seven-level HANPC (7L-HANPC) inverter, and finally experimentally verifies a peak efficiency of 99.35% and a power density of 3.4 kW/dm^3 (55.9 W/in^3) [20]. Firstly, the principle of operation of the HANPC converter is explained in detail in Section II. In Section III a design optimization is presented for the specifications given in Table I. The hardware design and the measurement results are presented in Section IV, and finally, the paper is concluded in Section V. Additionally, a detailed comparison of the accuracy of electric and calorimetric efficiency measurement methods is made in the Appendix.

II. PRINCIPLE OF OPERATION OF THE HANPC CONVERTER

As the HANPC topology so far has only been employed in medium-voltage high-power applications [17], [21], a brief review of the principle of operation is provided in the following. Each bridge-leg of the HANPC inverter, illustrated in Fig. 2(b) for seven levels, consists of two cascaded stages: the ANPC stage connected to the DC input voltage and the FC stage finally generating the AC output voltage. The ANPC stage switches ($T_{1...4}$) connect the points I and II for positive output voltages $u_i > 0$ to the positive DC-link voltage rail (DC+) and the DC-link midpoint M respectively, and to M and the negative DC-link voltage rail (DC−) for $u_i < 0$, as shown in Fig. 3. This results in grid frequency operated ANPC stage switches that have to be rated to withstand $U_{DC}/2$. Following, there is a FC stage (for the case of a 7L-HANPC it is a four-level FC stage, as shown in Fig. 2(b)), whose semiconductors are operated at switching frequency using phase shifted PWM, and have to be rated for $U_{DC}/6$.

The fundamental difference between the HANPC converter and the FCC structure is that by actively clamping the FC stage to either the high-side or the low-side of the DC-link, the same number of levels can be obtained with a HANPC converter compared to a FCC. For the HANPC converter, the number of levels is given by

$$N_{lev,HANPC} = 2 \cdot N_{FCcell} + 1, \tag{1}$$

where N_{FCcell} is the number of FC cells, whereas for the FCC bridge-leg the number of levels is

$$N_{lev,FCC} = N_{FCcell} + 1. \tag{2}$$

From (1) and (2) it can be seen that the HANPC converter needs half the FC cells compared to the FCC to generate the same number of levels. For the case shown in Fig. 2, both the FCC and HANPC converter produce a seven-level voltage

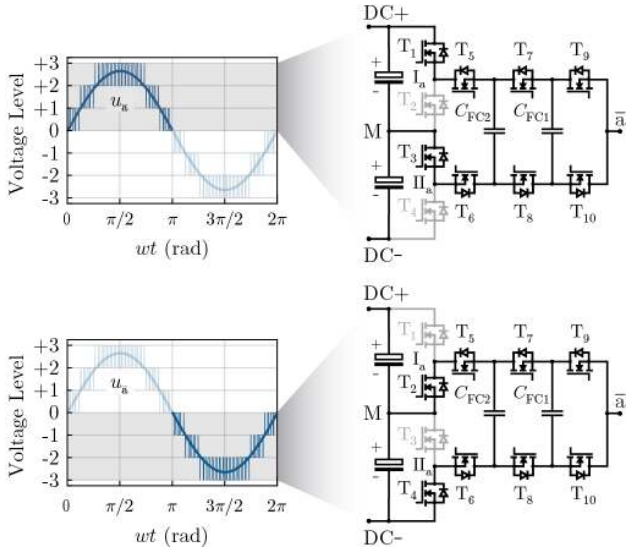

Fig. 3. Conduction states of the ANPC stage for positive and negative output voltages, shown for a bridge-leg of the 7L-HANPC. The ANPC stage switches ($T_{1..4}$) are connecting the subsequent FC stage ($T_{5..10}$) to the upper or lower half of the DC-link depending on the sign of the output voltage, while the FC stage is continuously switching at switching frequency. It has to be noted that Level 0 can be created with the FC stage clamped to either the high- or low-side of the DC-link.

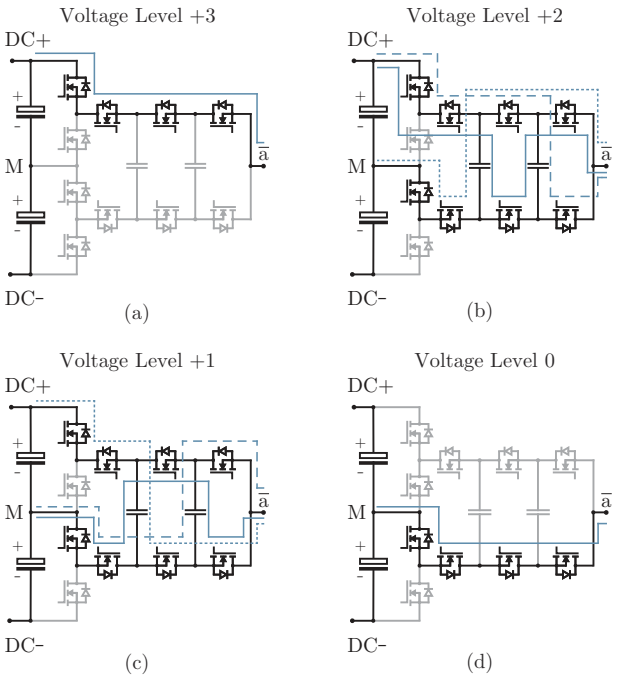

Fig. 4. Conduction states of a 7L-HANPC bridge-leg for the positive output voltage levels (a-c) and zero output voltage (d). For output voltage levels +3 and 0, the FCs are shorted by the high- and low-side FC stage switches respectively, and for levels +2 and +1, and there are three redundant switching states [19]. By ensuring equal conduction times of the three switching states, done by phase-shifted PWM, the flying capacitors are naturally balanced, as shown in Fig. 5.

output, but for the FCC the number of cells is $N_{\text{FCcell}} = 6$, and for the HANPC converter only $N_{\text{FCcell}} = 3$ is implemented. This is further illustrated in Fig. 3, where it can be seen that the +3...0 output voltage levels are created by connecting the FC stage to the upper half of the DC-link (cf., Fig. 4), whereas the output voltage levels 0...−3 are created by connecting the FC stage to the lower DC-link half. Hence, the ANPC stage acts as a selector switch, where the 0 output voltage level can be created in both ANPC stage configurations.

The effective switching frequency applied to the AC-side inductor and/or filter stage, which affects the filter design, losses and volume, is $f_{\text{sw,eff}} = N_{\text{FCcell}} \cdot f_{\text{sw}}$, with f_{sw} being the switching frequency of the individual stages. The difference in N_{FCcell} between both topologies, however, has a minor effect on the effective switching frequency as will be made visible by the following qualitative analysis: if it is assumed that there is a certain loss budget allocation for the power semiconductors of the converter, and that for optimizing semiconductor losses the die areas of the switches are chosen such that the conduction losses and hard-switching losses are similar [8], [22], then the FCC can be designed to have approximately equal conduction losses and switching losses. To adapt the design to the HANPC converter, following Fig. 2, if the conduction losses of half the FC cells of the FCC stage are chosen to be the same as the conduction losses of the ANPC stage switches (which are switching at line frequency and hence have negligible switching losses), then the available budget for the switching losses of the FC stage of the HANPC converter is equal to that of the six cells of the FCC. Therefore, the last three HANPC FC cells can switch at twice the switching frequency of their pure FCC counterpart switches, hence imposing the same effective switching frequency on the filter stage. Following the same argumentation, the dimensioning of the capacitance of the FCs, which depends on the maximum conduction time,

$$t_{\text{FC,max}} = \frac{1}{N_{\text{FCcell}} f_{\text{sw}}}, \tag{3}$$

shown in Fig. 5, remains similar for the FCC and the HANPC converter [9], [12], [23], since the product of $N_{\text{FC,cell}}$ and f_{sw} remains similar. Hence, the dimensioning of the flying capacitors follows

$$C_{\text{FC,min}} = \frac{t_{\text{FC,max}} I_{\text{ac,pk}}}{\Delta U_{\text{FC,max}}}, \tag{4}$$

where $I_{\text{ac,pk}}$ is the peak AC current, and $\Delta U_{\text{FC,max}}$ the maximum allowed peak-to-peak FC voltage ripple. This is illustrated in detail in Fig. 5, where the two-cell and three-cell FC stages are shown for the duty cycle at which $t_{\text{FC,max}}$ respectively occurs. For the case of a two-cell FC stage, $t_{\text{FC,max}}$ occurs for a duty cycle of 0.5, while in the case of a three-cell FC stage, $t_{\text{FC,max}}$ occurs at 0.66 or a duty cycle of 0.33. Hence, to have a conservative approach on the FC dimensioning (cf., (4)), it is considered that the peak output current $I_{\text{ac,pk}}$ occurs for the duty cycles that result in $t_{\text{FC,max}}$. By phase shifting the carriers by $2\pi/N_{\text{FCcell}}$, natural balancing of the FCs occurs regardless of the number of levels, as shown in Fig. 5 for C_{FC1}. Therefore, no measurement of the FC voltage is required to operate this converter. Further analysis of the modulation and switching states of the HANPC converter can be found in [17], [19], [21], a variant of the 7L-HANPC is presented and discussed in [24], and the natural balancing of FC

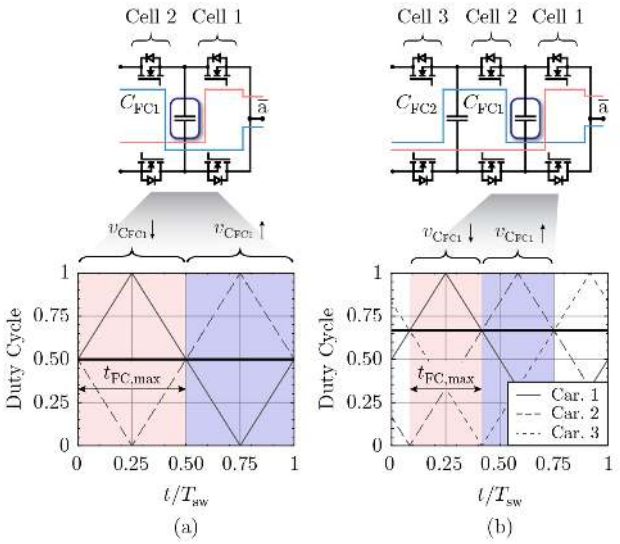

Fig. 5. Conduction states that charge (blue) and discharge (red) C_{FC1} for a two-cell (a) and a three-cell (b) FC stage. Additionally, the duty cycle that leads to the longest FC conduction time $t_{FC,max}$ is shown, where it is seen that $t_{FC,max}$ is inversely proportional to the number of levels. Due to phase-shifted PWM, the FC charge and discharge times remain equal for a whole switching period T_{sw}.

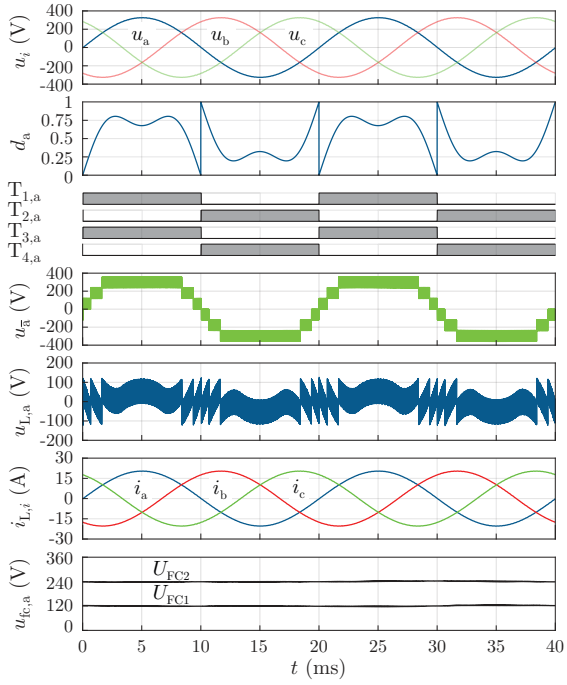

Fig. 6. Main waveforms of the 7L-HANPC inverter (cf., Fig. 2(b) and Fig. 7) operating with a DC-voltage of 720 V and an output power of 10 kW: mains phase voltages, duty cycle for phase a (d_a), gate signals for the ANPC stage switches of phase a, multi-level voltage output of node $\bar{a}$ (cf., Fig. 2(b)) referenced to the DC midpoint and filter inductor (L) voltage waveform of phase a, grid phase currents, and FC voltages of phase a. Note that a third harmonic component is superimposed in the modulation to reduce the low-frequency component of the DC-link midpoint current, as seen for d_a, with an amplitude of one-fourth of the phase output voltage.

voltages by phase-shifted PWM is covered in [25]–[28].

The main waveforms of the 7L-HANPC inverter are shown in Fig. 6 for an output EMI filter structure with the star-point of the

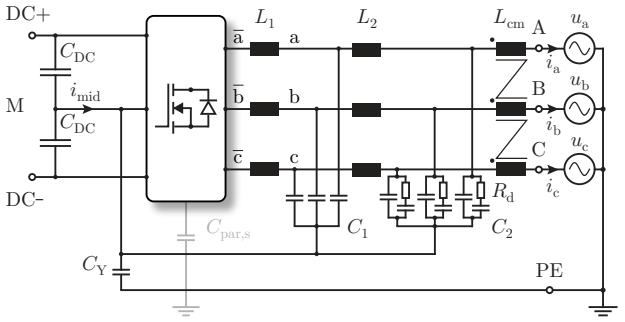

Fig. 7. EMI filter structure of the final prototype, with two *L-C* filter stages, simultaneously attenuating differential-mode (DM) and common-mode (CM) components of the output voltages of the inverter bridge-legs (with reference to the DC voltage midpoint) and a CM choke placed before the grid connection terminals.

filter capacitors connected to the DC-link midpoint as illustrated in Fig. 7. The seven output voltage levels together with the voltage applied to L_1 are shown for phase a, as well as the grid phase currents and the FC voltages, which are naturally balanced using phase shifted PWM. Finally, it has to be mentioned that, as for all NPC converters, a certain difference of the voltages of the upper and lower DC-link half arises due to the midpoint current i_{mid} (cf., Fig. 7) which has a dominant third harmonic component [19], [32]–[34]. However, this voltage difference can be reduced by either superimposing a third harmonic (zero sequence) to the modulation in such a way that the amplitude of the low-frequency part of i_{mid} is minimized, or by increasing the capacitance of the DC-link capacitors.

III. Design Optimization

To evaluate the most suitable component selection for the final hardware demonstrator, a comprehensive optimization of the 7L-HANPC inverter is performed, following the flowchart presented in Fig. 9. The optimization routine is conducted according to the converter dimensioning guidelines presented in [9], where for the FC stage, four different types of switches are considered, switching in a frequency range between 10 kHz and 40 kHz:

- two commercial 200 V silicon *OptiMOS 3* devices (*Infineon*),
- a virtual prototype of a next generation 200 V silicon device (*Infineon*), for which data has been provided by the manufacturer, and,
- the GaN power semiconductors of type *EPC2047 (EPC)*.

For the ANPC stage, however, both 600 V *CoolMOS CFD7* switches (*Infineon*) and a series-connection of the same low-voltage switches as used in the FC stage are considered [35]. This series-connection of the low-voltage switches shown in Fig. 10 would lead to the advantage of having the same semiconductors in the whole system. Its circuit schematic is similar to an FCC, but operated in a two-level configuration by adding balancing resistors (R_b) that ensure equal voltage balancing during steady-state, and capacitors (C_f) of low capacitance that ensure equal voltage balancing during the switching transients.

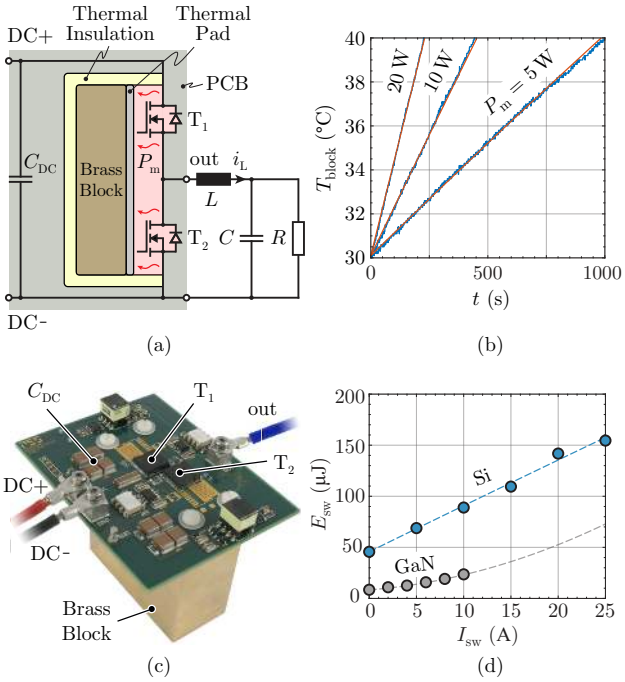

Fig. 8. Switching loss measurements of the lowest-$R_{ds,on}$-in-class low-voltage (200 V) Silicon (Si) (11.1 mΩ *IPT111N20NFD* from *Infineon*) and Gallium Nitride (GaN) (10 mΩ *EPC2047* from *EPC*) power semiconductors. The switching loss measurements are taken with a calorimetric setup based on [29]–[31], where the switching losses are determined by fitting the measured temperature rise curve from 30 °C to 40 °C to a calibrated *R-C* thermal model (a); mapping of the power losses to the temperature rise curve for the case of the Si switches (b); switching loss measurement setup for the Si switches (c), and measured hard-switching loss data at a DC-link voltage of 120 V (addition of the soft- and hard-switched transition losses of a half-bridge that occur during one switching period) for both devices (markers) together with a second order fit (dashed line) (d).

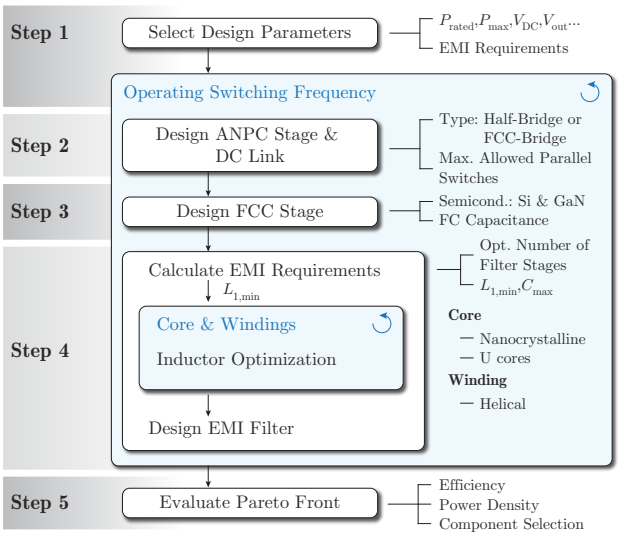

Fig. 9. 7L-HANPC converter optimization flowchart used to determine the Pareto front lines shown in Fig. 10.

Since the semiconductors, and in particular the FC stage switches, are the largest power loss contributors of the converter

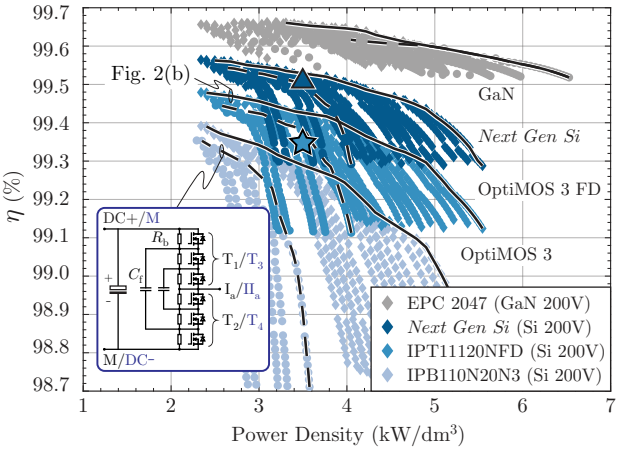

Fig. 10. Pareto optimization results for the different considered semiconductor devices and realizations of the ANPC stages. Results for the ANPC stage with 31 mΩ 600 V *CoolMOS CFD7* (*Infineon*) are shown with rhombi and continuous black Pareto lines, and the results for the series-connection of the same low-voltage MOSFETs of the ANPC stage [35] are shown with circles and dashed black Pareto lines. The efficiency is calculated at the operating point of 10 kW of the three-phase system, where the hardware prototype presented in this paper is represented by a star (four parallel devices for each switch of the ANPC stage), and the achievable performance with *next generation* 200 V silicon switches (estimation resulting from an extrapolation of recent FOM improvement) is shown by a triangle.

(cf., Fig. 11(a)), it is essential to have accurate switching loss data in order to obtain reasonable and realistic results in the converter optimization. For this reason, switching loss measurements were performed for the 11.1 mΩ 200 V Si switches of *Infineon* and the 10 mΩ 200 V GaN switches from *EPC*, which are presented in Fig. 8.

To comply with the International Special Committee on Radio Interference (CISPR) 11 Class A standard [36] on the AC-side, a *n*-stage *L-C* EMI filter structure is considered in the optimization routine ($n \in \{1,2,3\}$), which simultaneously attenuates DM and CM noise [37] as the filter stages are referenced to the DC midpoint (cf., Fig. 7). The filter design space is restricted by two factors: firstly, it should comply with the Class A EMI limits by a minimum attenuation margin of 10 dBµV, and secondly, the resonance frequency of the filter should be lower than one fourth of the effective switching frequency of the converter, to avoid unwanted excitation of the filter circuit [9]. For the filter inductor L_1, modeled and optimized according to [34], nanocrystalline cores with helical windings are used in order to reduce the losses [14], whereas for the further stage inductors (L_2, cf., Fig. 7) commercially available inductors are considered. Since low losses can be achieved with the *L-C* structure (cf., Fig. 11), a separation of the filter into dedicated DM and CM stages, which would increase the component count, is not considered.

Given the efficiency barriers obtained for different semiconductor technologies (indicated with the Pareto curves in Fig. 10), for the final design the all-silicon approach shown with a star is chosen, since the calculated efficiency difference between the commercially available silicon devices and GaN devices is only 0.25% for the same power density; with the introduction of next generation silicon devices, this difference

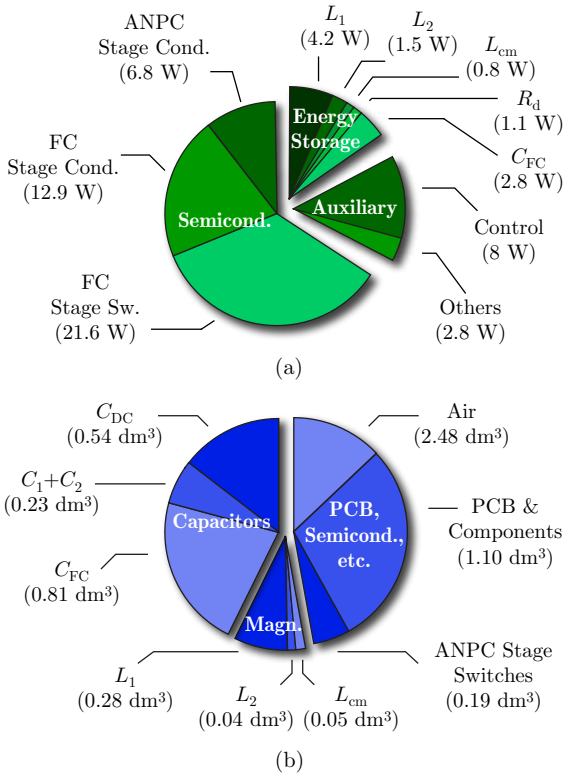

Fig. 11. Loss (a) and volume (b) distribution of the realized hardware (cf., Fig. 13), where the loss breakdown is shown for operation at 10 kW.

TABLE II
MAIN COMPONENTS OF THE FINAL DESIGN
THE EMI FILTER COMPONENT VALUES ARE GIVEN PER PHASE

Component	Value	Part Number
ANPC Stage Switches	31.0 mΩ	4 paralleled Infineon CoolMOS CFD7 600 V IPW60R031CFD7
FC Stage Switches	11.1 mΩ	2 paralleled Infineon OptiMOS 3 FD 200 V IPT111N20NFD
Gate Driver		10 A Infineon 1EDI60N12AF
L_1	113.3 µH	22 turns, Core: F3CC0008 2 mm × 5 mm wire
C_1	2.2 µF	Epcos TDK B32923H3225
L_2	15 µH	Wuerth Elek. 7443641500
C_2	13.2 µF	Epcos TDK B32924D3335
L_{cm}	400 µH (at 100 kHz)	4 turns, 2.5 mm wire Vacuumschmelze 2 x T60006-L2030-W358
C_{DC}	240 µF	Epcos TDK B32776G4406
C_{FC}	120 µF	Epcos TDK B32776G4406
C_Y	40 nF	Epcos TDK B32022A3103
R_d	1.65 Ω	pulse withstanding, through hole

is expected to be reduced to 0.15%. Regarding the ANPC stage configuration, the optimization results shown in Fig. 10 suggest that using 600 V switches for the ANPC stage (solid line Pareto front) offers superior performance both in terms of efficiency and power density compared to the series-connected 200 V device variant (dashed line Pareto front). This is due to the lower $R_{ds,on}$ of the 600 V switches compared to the 200 V switches and the need to passively balance the voltage of the 200 V switches by means of balancing resistors R_b, shown in Fig. 10. Since low switching frequencies yield designs with a high efficiency but a large volume, and high switching frequencies yield compact but more lossy designs (cf., Fig. 10), the design that is finally chosen for the hardware demonstrator reserves place for up to six parallel-connected 31 mΩ *CoolMOS CFD7* devices for the ANPC stage, and two parallel 11.1 mΩ *IPT111N20NFD* devices switching at 16 kHz, resulting in an effective switching frequency of 48 kHz for the filter stage. It has to be noted that for the case of the 600 V switches, the more switches connected in parallel, the lower the losses (negligible switching losses at grid frequency), however, at the price of increased cost and volume. It is for this reason that, in this optimization, a limit of six paralleled switches is considered for the ANPC switches for both ANPC stage configurations. The loss distribution of the selected design for the realized hardware demonstrator is shown in Fig. 11(a) for a power of 10 kW, where it can be observed that the semiconductors account for 66% of the total converter losses, out of which 84% are caused by the FC switches. The resulting contribution of the magnetic components to the loss and volume distributions is in the range of 10...15%, since with the relatively high output effective frequency and the multi-level output voltage waveform, only a small voltage-time area is applied to the inductors.

The final filter structure comprises two *L-C* filter stages, whose star point is connected to the midpoint of the DC-link to provide a return path for the CM current, as shown in Fig. 7. To further mitigate the effects of the unavoidable parasitic capacitance from the switching stage $C_{par,s}$ to ground, an additional CM-choke is placed before the grid connection terminals and a Y-rated capacitor C_Y is connected between earth (PE) and the DC-link midpoint. Finally, *R-C* damping is provided in the second filter stage with damping resistors R_d similar to [15], in order to avoid larger damping losses that would arise due to the switching voltage ripple if damping would be installed in the first stage. A list of the main power components used in the hardware prototype and their part numbers can be found in Table II.

The volume distribution of the hardware is given in Fig. 11(b), where it can be seen that the capacitors are the main volume contributors. The FC capacitance is dimensioned by the minimum capacitance requirement that is obtained by imposing a maximum switching frequency ripple of the FC voltage (see (4)), limited here to $\Delta U_{FC,max}$ = 5 V. Given the low switching frequency and high output current, the capacitance requirement is large, i.e., 107 µF for capacitors which operate at nominal voltages of 120 V and 240 V. Hence, film capacitors are chosen instead of ceramic capacitors, to avoid the need of having to

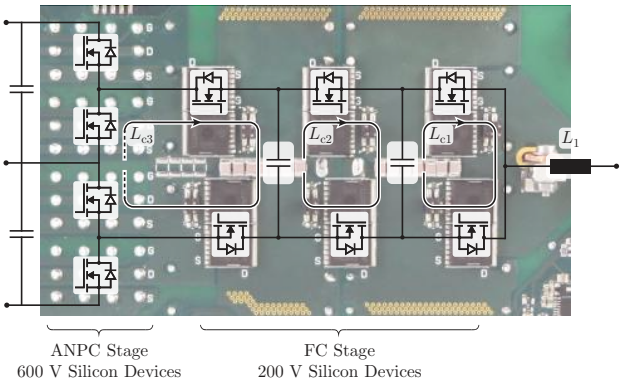

Fig. 12. Realization of the hardware layout of a three-phase 7L-HANPC inverter bridge-leg, where the FCs (film-type) are placed underneath the PCB, and ceramic capacitors are placed on top to improve the switching behavior of the MOSFETs. The commutation loop introduced by the connection of the FC stage to the HANPC stage L_{c3} is the most critical.

parallel-connect ≈ 200 capacitors per FC, which would also lead to approximately a × 15 price increase of the capacitors. However, for converters with a lower power rating (and lower load currents) and higher switching frequencies, ceramic capacitors are more suitable, since a higher volumetric energy density can be achieved [12], [18], [28], [38].

IV. Hardware Implementation and Measurement Results

To validate the presented calculations and the suitability of the 7L-HANPC topology for ultra-high efficiency applications, the hardware implementation of the 7L-HANPC and the main measurement results will be presented in the following.

A. Hardware Implementation

The first step to build the 7L-HANPC inverter is to design an optimal bridge-leg layout, especially because switching losses cause a significant part of the overall losses and depend to a large extent on layout parasitics [39]. The implemented layout and its schematic arrangement are shown in Fig. 12, where particular care has to be taken for the FC stage layout. Since there are three FC cells per bridge-leg, there are three switching frequency commutation loops that require attention in the layout, namely L_{c1}, L_{c2} and L_{c3}, out of which L_{c3} is the most critical for two reasons: firstly, the commutation path of L_{c3} always closes through either the upper side or the lower side DC-link capacitor, for which layout symmetry has to be maximized such that L_{c3} is equal for both cases, as seen in Fig. 12; secondly, given that the high-side and low-side (partial) DC-link voltages are not always equal in value due to the nature of the topology, care has to be taken if commutation capacitors are placed between the ANPC stage and FC stage switches. Since two capacitors of unequal voltage, i.e., the respective DC-link capacitor and the commutation capacitor, which has previously been connected to the opposite half DC-link capacitor, would be connected in parallel, current spikes and ringing would occur when commutating the ANPC stage switches. Note that although space

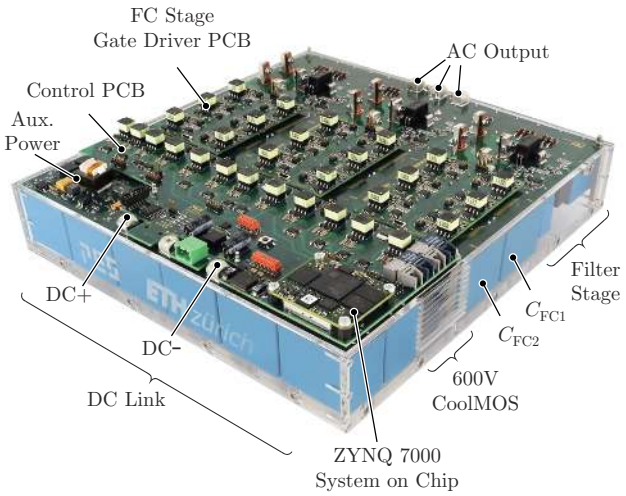

Fig. 13. Hardware prototype of the 12.5 kW three-phase 7L-HANPC inverter, measuring 256 mm × 269 mm × 53 mm (10.1 in × 10.6 in × 2.1 in). The final volumetric power density is 3.4 kW/dm^3 (55.9 W/in^3), and the gravimetric power density is 3.2 kW/kg (1.5 kW/lb).

is provided to place ceramic capacitors between the ANPC and FC stages, this has not finally been done in the current setup (cf., Fig. 12). However, L_{c1} and L_{c2} can easily be optimized by placing ceramic (commutation) capacitors in parallel to the (film-type) FCs to reduce the size of the commutation loop (cf., Fig. 12), keeping the maximum overvoltage of the FC stage switches to 30 V. All the gate drivers are placed on separate PCBs, which on the one hand has the advantage of keeping the power PCB free from the gate driver circuitry for an optimized layout, but on the other hand has the disadvantage of increasing the gate loop inductance. This inductance is minimized by using low-profile board-to-board connectors (*Samtec TMM* and *CLT* types) that result in a distance between the PCBs of only 2.77 mm (0.11 in). Each switch has its own isolated power supply, for which dedicated transformers are used to obtain isolated gate voltages of 15 V and −5 V.

The 12.5 kW hardware demonstrator shown in Fig. 13, features a volumetric power density of 3.4 kW/dm^3 (55.9 W/in^3) and a gravimetric power density of 3.2 kW/kg. It has to be noted that, for the presented measurements, four power MOSFETs were connected in parallel for implementing each switch of the ANPC stage, however, space was provided in the layout to accommodate a total of six parallel switches.

Given the high efficiency nature of the converter, there is no need for active cooling, and hence, neither fans nor heat sinks are required, thus minimizing the implementation effort and increasing the overall reliability of the system. This is particularly true for the converter at hand, where the semiconductor losses are distributed among many switches: the estimated losses of a single ANPC stage switch, housed in a TO-247 three-lead package, are of 0.14 W on average, whereas the losses for an individual SMD FC stage switch are 0.96 W. Experimental measurements yield that at thermal steady-state during operation at 10 kW and an ambient temperature of 40 °C, the 600 V switches housed in a though-hole TO-247 package have a case temperature of 64.8 °C, and that the 200 V switches housed in

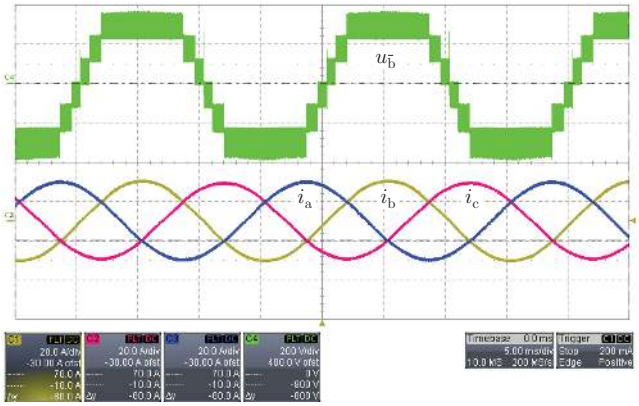

Fig. 14. Measurements of the seven-level output voltage of a bridge-leg of the 7L-HANPC inverter shown in Fig. 13 (200 V/div, referenced to the DC-link midpoint, 5 ms/div) and the currents of the three phase mains (20 A/div) during operation at 10 kW. The experimental waveforms are in accordance with the simulation results shown in Fig. 6.

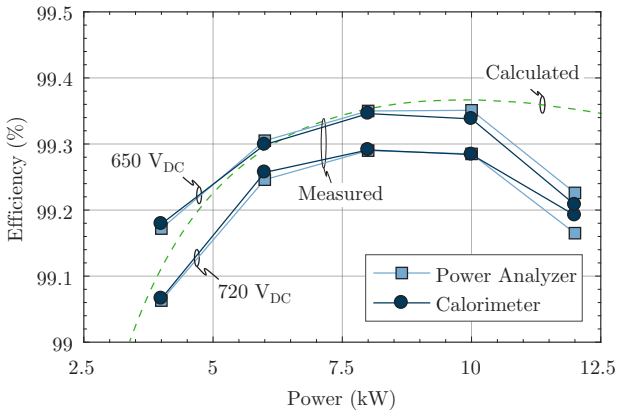

Fig. 15. Measured efficiency of the hardware demonstrator (cf., Fig. 13) reaching peak values of 99.35% for U_{DC} = 650 V and 99.30% for U_{DC} = 720 V, and calculated efficiency characteristic for V_{DC} = 720 V. All efficiency measurements are taken at a controlled ambient temperature of 40 °C.

a HSOF SMD package have a case temperature of 69.3 °C, resulting in a case-to-ambient thermal resistance of 175 °C/W and 36 °C/W, and junction temperature of 64.9 °C and 69.7 °C respectively.

B. Experimental Waveforms

The main measured waveforms taken with a resistive load (i.e., operating the system in inverter mode) are presented in Fig. 14 for 10 kW operation, where the unfiltered seven-level phase voltage measured at the output node $\bar{b}$ with respect to the DC-link midpoint and the three phase currents are shown. The voltage spikes that can be seen during the voltage zero crossings are due to the unequal switching times of the ANPC stage and FC stage switches, and last only for some few tens of nanoseconds not affecting the overall system performance. The DC-link voltage midpoint is controlled by superimposing a third harmonic to the sinusoidal modulation of one fourth of the output voltage amplitude (cf., Fig. 6), achieving a low maximum instantaneous voltage deviation between the upper half and the lower half of the DC-link of 8.9 V during nominal operation. The FC voltages are naturally balanced by phase shifted PWM [25] at their nominal voltages, i.e., at average values of U_{FC2} = 240.5 V and U_{FC1} = 120.9 V.

C. Efficiency Measurements

The efficiency of the three-phase 7L-HANPC inverter is measured both calorimetrically, with the calorimeter presented in [3], and electrically, with a *Yokogawa WT3000* precision power analyzer. The efficiency measurement results of both methods are reported in Fig. 15, together with the calculated efficiency at V_{DC} = 720 V. A peak efficiency of 99.35% is achieved for U_{DC} = 650 V, and 99.30% for U_{DC} = 720 V, where all the converter losses are considered, including those of the EMI filter stage and the auxiliary power. The fitted European weighted efficiency is 99.10%, whereas the California Energy Commission (CEC) weighted efficiency is 99.20% [40]. Since electrical power measurements with precision power analyzers have a large efficiency error band ($\Delta\eta$ = ±0.38% at 10 kW, leading to the uncertainty of the efficiency measurement to be between η = 98.92…99.68%, cf., Appendix), also calorimetric measurements were performed in order to accurately determine the overall efficiency. The calorimetric approach measures the power losses with a relative error smaller than 1% for the whole range where measurements were taken [3], leading to an efficiency accuracy of $\Delta\eta$ = ±0.0065%. The efficiency measurement points presented in Fig. 15 are taken with the converter at thermal steady-state inside the inner chamber of the calorimeter, which is controlled to have an ambient temperature of 40 °C, resulting in 2 to 3 hours of continuous operation for each efficiency measurement point. However, it has to be noted that the electric and the calorimetric loss measurements match very well, as also shown in [15], from which it can be concluded that the actual accuracy of the power analyzer is substantially higher than specified in the datasheet. An in-depth comparison of the electric and calorimetric measurement methods is provided in the Appendix.

D. Conducted EMI Measurements

The results of the conducted EMI emission measurement are presented in Fig. 16, for the frequency range between 10 kHz and 30 MHz. Two different scans are shown, the first one with the peak and average detector for a measurement time of 50 ms for frequencies < 150 kHz, and 10 ms measurement time for frequencies ≥ 150 kHz, and a second one, with the quasi-peak and average detector for a measurement time of 1 s. It has to be noted, that for the effective switching frequency (48 kHz) resulting from the converter optimization described in Section III, the filter dimensioning is limited by the need of sufficiently separating the filter resonance frequency and the effective switching frequency, in order to not excite any filter resonance, and not by the EMI filtering requirements. This can be seen in Fig. 16, since for the first harmonic above 150 kHz, the attenuation margin is well above the 10 dBµV for which the EMI filter design space was

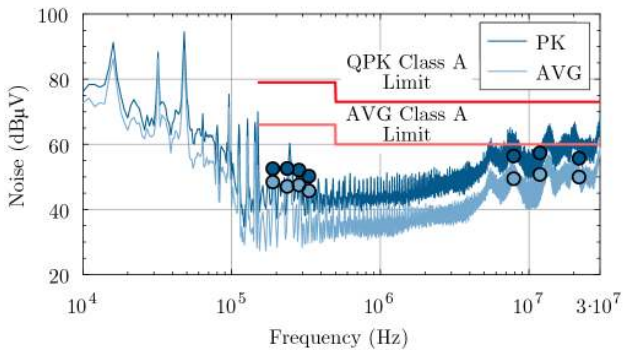

Fig. 16. Conducted EMI noise emission spectrum of the hardware demonstrator presented in Fig. 13, where the CISPR 11 peak and average detectors are used with a 1 kHz step, 200 Hz bandwidth, and 50 ms measurement time for frequencies < 150 kHz and a 4 kHz step, 9 kHz bandwidth, and 10 ms measurement time for frequencies ≥ 150 kHz. Selected peaks (markers) have been measured with quasi-peak and average detectors for a measurement time of 1 s.

restricted in the optimization.

V. Conclusion

In this paper, a 99.35% efficient 3.4 kW/dm^3 (55.9 W/in^3) all-silicon seven-level three-phase inverter is presented, setting a new benchmark for ultra-high efficient and power-dense converters. A topological alternative to the conventional FCC is employed, which has the advantage of halving the amount of FC cells by making use of a DC-link midpoint connection, and an ANPC stage front-end that uses switches rated for half the DC-link voltage and is switching at grid frequency. Substantial volume savings are obtained by halving the number of FC cells, particularly for the case of low switching frequencies, since the capacitance requirement to guarantee a certain voltage ripple of the FCs is inversely proportional to the switching frequency, which is limited for ultra-efficient converters. Additionally, no active cooling is required given the high efficiency of the system and the fact that the losses are spread among many switches and/or power components, reducing the design effort and increasing reliability.

With recently available 18 mΩ 600 V *CoolMOS CFD7* power MOSFETs (*Infineon*), which have a lower on-state resistance compared to the 31 mΩ switches used in this work, the efficiency and/or volume could be further improved, as the switching losses are negligible at grid frequency. Furthermore, a comprehensive optimization shows that it is feasible to reach the boundary of 99.5% efficiency with nextgeneration 200 V silicon devices, and 99.6% with state-of-the-art GaN devices.

Appendix

Accurate Efficiency Measurements: Electric vs. Calorimetric Methods

For power converters in the low- and mid-ninety percent efficiency range, the efficiency can be directly determined using a power analyzer. However, for ultra-efficient converters, particularly for those in the 99+% efficiency range [3], [14], [15], [41], accurately determining the efficiency characteristic requires additional calorimetric loss measurements. In the following, both the electric and calorimetric efficiency measurement methods are described, followed by a discussion and comparison between them.

A. Electric Efficiency Measurement

The first approach to determine efficiency is to measure the input and output powers, P_{out} and P_{in} respectively, using a precision power analyzer:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}}. \tag{5}$$

However, since P_{out} and P_{in} are large values in comparison with the power losses, a small error in the measurement of both power values can lead to a large deviation in the measured efficiency, and therefore has to be considered accordingly. Assuming relative measurement errors, $\varepsilon_{\text{Pout}}$ and ε_{Pin}, the worst-case absolute error of the efficiency measurement $\Delta\eta$ is

$$\Delta\eta = \eta \frac{(\varepsilon_{\text{Pout}} + \varepsilon_{\text{Pin}})}{(1 - \varepsilon_{\text{Pin}})}. \tag{6}$$

If the output and input power measurement shows the same error, ε_{P}, the error of the efficiency measurement can be approximated as

$$\Delta\eta \approx \varepsilon_{\text{Pout}} + \varepsilon_{\text{Pin}} \approx 2\varepsilon_{\text{P}}. \tag{7}$$

For the case at hand, the *Yokogawa WT3000* precision power analyzer was used to electrically measure the efficiency. To determine the efficiency measurement error, errors are specified for both the DC and the AC power measurement as follows: firstly, an error depending on the power reading, ε_{Y}, and secondly, an error depending on the power range in which the measurement has been taken, ε_{X}. With these two errors, the power measurement errors for the DC side input ε_{Pdc} and the three-phase AC power output ε_{Pac} can be calculated as

$$\varepsilon_{\text{Pdc}} = \frac{P_{\text{DC}}(1 + \varepsilon_{\text{Y,dc}}) + X_{\text{Pdc}}\varepsilon_{\text{X,dc}}}{P_{\text{DC}}} - 1 \tag{8}$$

$$\varepsilon_{\text{Pac}} = \frac{3\,(P_{\text{AC,1}\phi}(1 + \varepsilon_{\text{Y,ac}}) + X_{\text{Pac}}\varepsilon_{\text{X,ac}})}{P_{\text{AC,1}\phi}} - 3, \tag{9}$$

where X is the power range of the efficiency measurement. For an efficiency measurement at 10 kW, (8) yields $\varepsilon_{\text{Pdc}} = \pm 0.25\%$ and (9) $\varepsilon_{\text{Pac}} = \pm 0.13\%$, leading to a large error of the efficiency measurement of $\Delta\eta = \pm 0.38\%$.

B. Calorimetric Efficiency Measurement

For ultra-high efficiency converters, a second approach that leads to more accurate efficiency measurements is used, i.e., a calorimetric measurement, which by directly measuring the

power losses P_{loss}, allows to calculate the efficiency as

$$\eta = 1 - \frac{P_{loss}}{P_{in}}. \tag{10}$$

An error in the loss measurement leads to an absolute error in the efficiency of only

$$\Delta\eta = \frac{\Delta P_{loss}}{P_{in}} = (1 - \eta)\,\varepsilon_{loss}, \tag{11}$$

where ε_{loss} is the relative error in the power loss measurement.

The employed calorimeter is presented in [3], and determines the power losses by measuring the coolant volume flow $\dot{V}$ and the coolant temperature difference between the input and output of the calorimeter ΔT, with

$$P_{loss} = c_p \rho \dot{V} \Delta T, \tag{12}$$

where c_p is the specific heat capacity of the coolant, and ρ is the mass density [42]. The main advantage of calorimetric measurement method is that the power losses can be measured independent from the power processed by the converter, and its accuracy therefore only depends on the error with which P_{loss} can be measured. In this case, since the accuracy of both $\dot{V}$ and ΔT profit from higher measured values, which occur when measuring higher values of P_{loss}, the accuracy of the employed calorimeter increases for higher measured power losses, as shown in Table III. Finally, it has to be noted that the accuracy of the calorimetric measurements benefit further from calibration, which is performed before taking measurements on a device under test.

C. Accuracy Comparison of Electric and Calorimetric Efficiency Measurements

A general comparison between both measurement methods can be done by finding a relation between ε_P and ε_{loss}, which with (6) and (11) yields:

$$\varepsilon_{loss} = \frac{\eta\,(\varepsilon_{Pout} + \varepsilon_{Pin})}{(1 - \varepsilon_{Pin})(1 - \eta)} \approx \frac{2\varepsilon_P}{(1 - \eta)}. \tag{13}$$

The relation between ε_P and ε_{loss} can be seen in Fig. 17, where additionally the errors for the efficiency measurement for the converter at hand for 10 kW operation are shown for both the electric measurement with the precision power analyzer and the calorimeter. It is seen that for the electric efficiency measurement, the relative error in the power loss determination is above 50%. Accordingly, in order to achieve the same performance as with the calorimeter (ε_{loss} = 1%), the accuracy when measuring the input and output power would have to be 0.003%, which is not possible with state-of-the-art precision power analyzers.

Finally, the difference of the efficiency calculation confidence interval for both measurement methods is shown in Fig. 18 for the presented converter. It can be seen that for operation at two different power levels (2 kW and 10 kW), the uncertainty in the calorimetric efficiency measurement is much smaller than with an electric measurement.

TABLE III
CALORIMETER ACCURACY SPECIFICATIONS [3]

P_{loss}	Error (ε_{loss})
< 10 W	< ±3.5 %
< 100 W	< ±1 %
< 200 W	< ±0.5 %

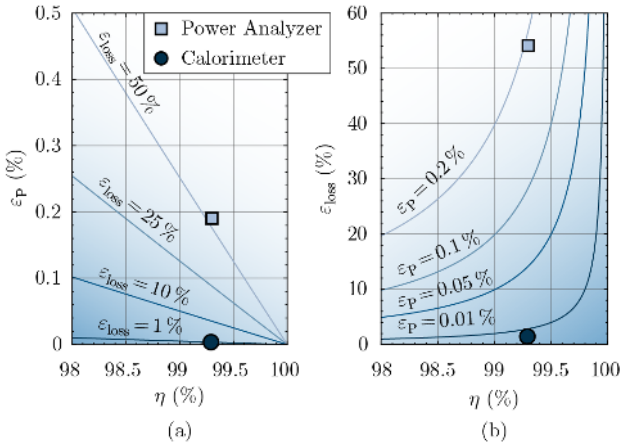

Fig. 17. Graphical representation of the relative power loss calculation error ε_{loss} as a function of the relative power measurement error ε_P and efficiency η (a), and vice versa (b). The accuracy of the performed efficiency measurements with the *Yokogawa WT3000* precision power analyzer (square symbol) and the calorimeter (round symbol) [3] is shown for a processed power of 10 kW.

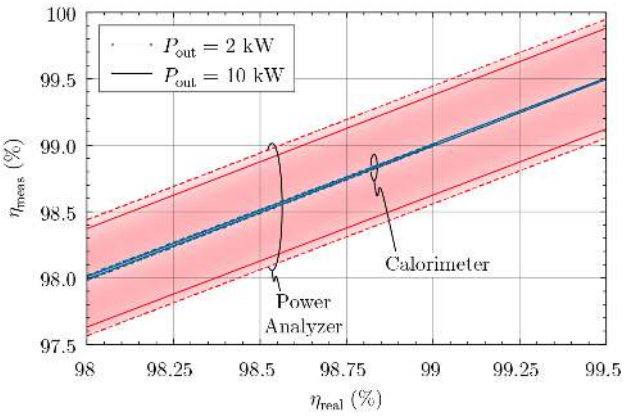

Fig. 18. The confidence interval for the measured efficiency (η_{meas}) vs. the real efficiency (η_{real}) for the presented inverter, where $\eta_{meas} = \eta_{real} \pm \Delta\eta$. Both electric (*Yokogawa WT3000* precision power analyzer) and calorimetric [3] efficiency measurements are shown for 2 kW and 10 kW of processed power.

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