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Amorphous In–Ga–Zn–O coplanar homojunction thin-film transistor

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A fabrication process of coplanar homojunction thin-film transistors (TFTs) is proposed for amorphous In–Ga–Zn–O (*a*-IGZO), which employs highly doped contact regions naturally formed by deposition of upper protection layers made of hydrogenated silicon nitride (SiN_X:H). The direct deposition of SiN_X:H reduced the resistivity of the semiconductive *a*-IGZO layer down to 6.2×10^{-3} Ω cm and formed a nearly ideal Ohmic contact with a low parasitic source-to-drain resistance of 34 Ω cm. Simple evaluation of field-effect mobilities (μ_{sat}) overestimated their values especially for short-channel TFTs, while the channel resistance method proved that μ_{sat} was almost constant at 9.5 $cm^2\ V^{-1}\ s^{-1}$. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3112566]

Since the report by Nomura *et al.*,[1] much efforts have been devoted to develop thin-film transistors (TFTs) using amorphous In–Ga–Zn–O (*a*-IGZO) for their active channels. Amorphous IGZO TFTs have excellent features such as high field-effect mobilities (~10 $cm^2\ V^{-1}\ s^{-1}$), small subthreshold voltage swings,[2] good short-range uniformity owing to the amorphous structure,[3] and electrical stability better than hydrogenated amorphous Si (*a*-Si:H) TFTs.[4] Furthermore, *a*-IGZO TFTs are fabricated at low temperatures (<300 °C) and most parts of the fabrication process are compatible with the existing technology employed for mass production of *a*-Si:H TFTs. These features make *a*-IGZO TFTs a promising candidate for active-matrix backplanes of future flat-panel displays (FPDs) such as large-size liquid-crystal displays and organic light-emitting diode (OLED) panels.[5,6]

For an application of *a*-IGZO TFTs to active-matrix backplanes, however, we still have some issues to be solved. One of the essential issues is that it is difficult to form good electrical contacts between an *a*-IGZO channel and source/drain electrodes. For the source/drain electrodes of *a*-IGZO TFTs, various materials have been examined, which include Au/Ti,[2,3] Mo,[7] MoW,[8] Al,[9] Pt/Ti,[10] indium tin oxide (ITO),[1] and indium zinc oxide (IZO).[11] Park *et al.*[10] fabricated *a*-IGZO TFTs with Pt/Ti source/drain electrodes and found that the device performance of the *a*-IGZO TFTs was significantly improved by applying an Ar plasma treatment to the *a*-IGZO electrode regions prior to the deposition of the Pt/Ti electrodes. They attribute this improvement to reduction of the contact resistance between the *a*-IGZO channel and the Ti electrodes that resulted from electron doping to the *a*-IGZO contact regions by the Ar plasma treatment. Shimura *et al.*[12] investigated the contact resistance between *a*-IGZO channels and various source/drain electrodes, such as Ag, In, Ti, Au, Pt, ITO, and *a*-IZO, and observed that the contact resistance affected the drain current of TFTs. They also found that the contact resistance strongly depended on the carrier concentration of the *a*-IGZO films. Na *et al.*[9] reported that a highly conductive *a*-IGZO buffer layer helped to form a good Ohmic contact between a semiconductive *a*-IGZO channel and Al electrodes. These facts indicate that it is necessary to enhance the carrier concentration of an *a*-IGZO layer at the contact interfaces by depositing a highly conductive *a*-IGZO buffer layer or by a postdeposition process like an Ar plasma treatment in order to obtain a good Ohmic contact in *a*-IGZO TFTs.

To solve the contact issues in polycrystalline silicon TFTs, coplanar homojunction TFT structure has been reported,[13] but this fabrication process requires expensive doping techniques such as ion implantation, diffusion of impurities, and a high-temperature activation process. For *a*-IGZO, fabrication of coplanar homojunction TFTs has recently been reported by using plasma treatments such as Ar (Ref. 14) and H_2 (Ref. 15) plasma to form highly conductive *a*-IGZO source/drain regions. Park *et al.*[14] report improved performances such as a saturation mobility μ_{sat} ~5 $cm^2\ V^{-1}\ s^{-1}$, but the Ohmic contact between the channel/source/drain *a*-IGZO and the wiring metal is not satisfactory. Furthermore, in general, the TFTs used for backplanes of FPDs must be covered with insulating layers (protection layer) to protect themselves from the subsequent stacking of upper devices such as liquid-crystal cells and OLEDs and from the influence of an environment. It has been reported that the formation of upper insulating layers can easily affect conductivity of *a*-IGZO channels and TFT characteristics, which is usually thought to be a drawback of *a*-IGZO. Actually, we have observed that direct deposition of hydrogenated silicon nitride (SiN_X:H) by plasma-enhanced chemical vapor deposition (PECVD) onto a semiconductive *a*-IGZO film increased its conductivity significantly.

In this letter, we report a simple technique to form a coplanar homojunction TFT, which does not require an extra fabrication process, by employing the above drawback of *a*-IGZO. It is realized as a natural consequence of the forma-

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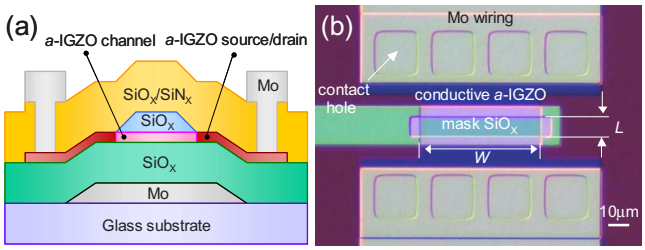

FIG. 1. (Color online) (a) Cross-sectional schematic structure of coplanar homojunction *a*-IGZO TFT. (b) Plan-view optical microscopic image of a coplanar homojunction *a*-IGZO TFT with the designed channel length $L_{des}=10\ \mu m$ and the channel width $W=60\ \mu m$.

tion of the protection SiN_X:H layer, the deposition of the SiN_X:H layer forms highly conductive *a*-IGZO source/drain regions in the same plane of the *a*-IGZO channel and solves the contact issues.

Figure 1(a) shows the structure of the bottom-gate-type coplanar homojunction *a*-IGZO TFTs. The TFTs were fabricated on a glass substrate (Corning 1737). Mo layers (100 nm thick) were sputtered as the bottom-gate electrodes and the wiring from the *a*-IGZO source/drain regions. A SiO_X layer (200 nm thick) was deposited by PECVD at 340 °C as a gate insulator. A semiconductive *a*-IGZO layer (30 nm thick) was deposited as a channel layer by direct-current magnetron sputtering using an 80% Ar/20% O_2 gas at room temperature (RT), followed by electrical isolation by wet etching to form channel region islands. A SiO_X layer (100 nm thick) was deposited by radio-frequency magnetron sputtering at RT as mask SiO_X islands that covered the channel regions. A SiN_X layer (300 nm thick) and a SiO_X layer (50 nm thick) were deposited sequentially in this order by PECVD at 250 °C as a protection layer on top of the mask SiO_X islands/*a*-IGZO layer structure. In the deposition process of the SiN_X layer, the exposed areas of the *a*-IGZO layer (i.e., not covered with the mask SiO_X islands) were converted to highly conductive source/drain regions. All the patterns were defined by photolithography and etching processes. The fabricated coplanar homojunction *a*-IGZO TFTs were subjected to post-thermal annealing in air at 270 °C. Figure 1(b) shows a plan-view optical microscope image of a fabricated TFT. The size of the mask SiO_X island determines the designed channel length (L_{des}) and the size of the isolated *a*-IGZO island determines the channel width (W). The channel width was fixed at 60 μm. L_{des} was varied from 3 to 120 μm. The electrical characteristics of the TFTs were measured with an Agilent 4156C precision semiconductor parameter analyzer in dark.

The resistivities of the *a*-IGZO regions with or without the effect of the SiN_X:H deposition were measured using the van der Pauw configuration electrodes made of a stacked layer of Ti/Au/Ti (5/100/5 nm thick). We confirmed that the resistivity of the *a*-IGZO film covered with a SiO_X mask island was $3.9\times10^{1}\ \Omega$ cm even after the SiN_X:H deposition. On the other hand, the resistivity of the *a*-IGZO film was decreased to $6.2\times10^{-3}\ \Omega$ cm by the direct deposition of a SiN_X:H layer. This is similar to the result reported by Son *et al.*,[16] and also analogous to the hydrogen doping effects in another amorphous oxide semiconductor $CdO\cdot GeO_2$ (Ref. 17) and crystalline ZnO.[18] The formation of shallow donor states by hydrogen doping is also confirmed by first-principles calculations for crystalline IGZO.[19] The present

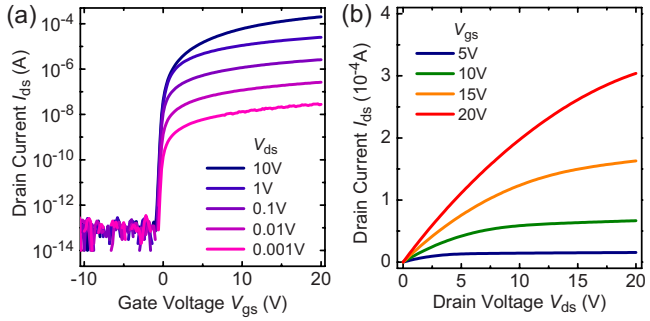

FIG. 2. (Color online) (a) Transfer characteristics of a coplanar homojunction *a*-IGZO TFTs with $L_{des}=10\ \mu m$ and $W=60\ \mu m$. V_{gs} was swept from −10 to 20 V at V_{ds} varied from 0.001 to 10 V. (b) Output characteristics of the coplanar homojunction *a*-IGZO TFT.

result suggests that incorporation of hydrogen forms shallow donor states also in *a*-IGZO.

Figure 2(a) shows transfer characteristics (drain-to-source current I_{ds} as a function of gate-to-source voltage V_{gs}) of a TFT with $L_{des}=10\ \mu m$ and $W=60\ \mu m$ measured at drain-to-source voltages (V_{ds}) of 0.001–10 V. The TFT shows an excellent performance with the subthreshold voltage swing (S) of 0.13 V decade^{-1}, the threshold voltage (V_{th}) of 0.13 V, and the on-to-off current ratio (I_{on}/I_{off}) larger than 10^9 at $V_{ds}=10$ V, where V_{th} was determined as a horizontal-axis intercept of a linear fitting to a $I_{ds}^{1/2}$-V_{gs} plot. These values are comparable to those of previous reports.[2,3] In addition, the slopes of the log I_{ds}-V_{gs} plots in the subthreshold region are very steep even at very small V_{ds} down to 0.001 V, demonstrating that the coplanar homojunction TFT exhibits excellent switching characteristics in the wide range of operation voltage. Figure 2(b) shows the output characteristics of this TFT. It shows excellent output characteristics with steep rise in the low V_{ds} region.

The parasitic source-to-drain resistance (R_{sd}) and the effective channel length (L_{eff}) were evaluated using the channel resistance method[20] with TFTs having different L_{des}. Figure 3(a) shows the transfer characteristics at $V_{ds}=0.1$ V for TFTs with $W=60\ \mu m$ and various $L_{des}=3-120\ \mu m$. Using the transfer characteristics in Fig. 3(a) at $V_{ds}\ll V_{gs}$, the total resistance (R_{tot}) of the TFTs are related to R_{sd} and L_{eff} by

$$R_{tot}=\frac{V_{ds}}{I_{ds}}=R_{sd}+\frac{L_{des}-\Delta L}{\mu_{eff}C_{ox}W(V_{gs}-V_{th})}, \quad (1)$$

where ΔL is defined as $L_{des}-L_{eff}$, μ_{eff} is the effective mobility, and C_{ox} is the capacitance of the gate insulator per unit

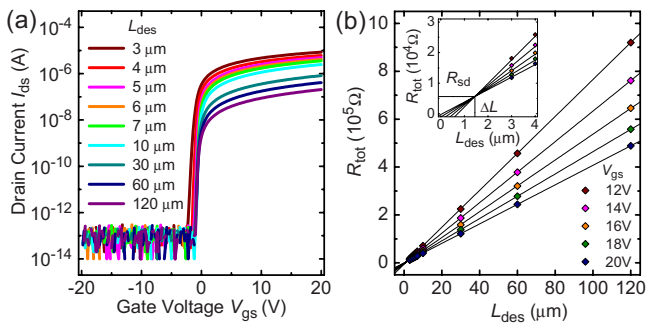

FIG. 3. (Color online) (a) Transfer characteristics of TFTs with various L_{des} and $W=60\ \mu m$ at $V_{ds}=0.1$ V. (b) R_{tot} vs L_{des} as a function of V_{gs} for TFTs with $W=60\ \mu m$. The inset shows a magnified view in the small L_{des} region.

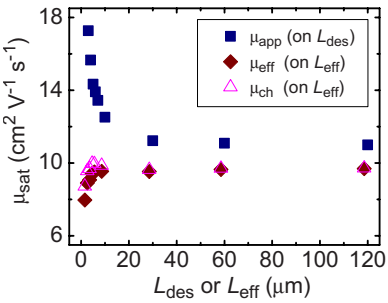

FIG. 4. (Color online) Dependences of μ_{app}, μ_{eff}, and μ_{ch} on L_{des} or L_{eff} at $V_{ds}=12$ V.

area. Figure 3(b) shows the dependence of R_{tot} on L_{des} at $V_{gs}=12-20$ V. Based on Eq. (1), R_{sd} and ΔL were evaluated from the intersection point of the R_{tot}-L_{des} straight lines, as shown in the inset of Fig. 3(b). Thus the width-normalized $R_{sd}(R_{sd}W)$ is evaluated to be 34 Ω cm. Note that this value is much lower than those reported previously [113 Ω cm (Ref. 8) and 330 Ω cm (Ref. 10)]. This observation confirms that very low Ohmic contacts are formed in the coplanar homojunction *a*-IGZO TFTs fabricated in the present process. The shrinkage of the channel length $\Delta L=1.5$ μm would be attributed to the critical-dimension loss in the patterning size of the mask SiO_X islands and/or to the decrease in the channel length caused by hydrogen side diffusion from the edges of the mask SiO_X islands.

The above results provide more reliable information about size effects of *a*-IGZO TFTs. Saturation mobilities μ_{sat} are derived from the following equation under the condition $V_{ds} \gg V_{gs}-V_{th}$:

$$I_{ds}=(\mu_{sat}C_{ox}W/2L)(V_{gs}-V_{th})^2. \quad (2)$$

The L value is often taken as a designed channel length but it might give a large error to estimate μ_{sat} especially for short-channel TFTs. Figure 4 shows apparent μ_{sat} evaluated using $L_{des}(\mu_{app})$ and corrected μ_{sat} using $L_{eff}(\mu_{eff})$ at $V_{ds}=12$ V. It shows that μ_{app} increases with decreasing L_{des} and becomes ~50% larger than those of the long-channel TFTs. However, μ_{eff} is almost constant at 9.5 $cm^2\ V^{-1}\ s^{-1}$ down to $L_{eff}=4$ μm. The present results prove that the μ_{app} values are not the real ones and are affected by the shrinking of the effective channel region. μ_{eff} shows a trend to decrease with decreasing L_{eff}, which is attributed to R_{sd}. μ_{ch} in Fig. 4 shows the channel mobility, which is defined as μ_{eff} corrected further for R_{sd} using the following equations:

$$g_m(\text{obs})=g_m/[1+(R_{sd}/2)g_m], \quad (3)$$

$$g_m=dI_{ds}/dV_{gs}=(\mu_{ch}C_{ox}W/L_{eff})(V_{gs}-V_{th}), \quad (4)$$

where g_m(obs) and g_m are the observed and the net transconductances, respectively.[21] Although there still remains a small drop in the μ_{ch}-L_{eff} plot for the shortest channel TFT, all the TFT characteristics are explained well by the constant channel mobility if the parasitic resistance and the shrinkage effect are considered.

In summary, coplanar homojunction *a*-IGZO TFTs were fabricated utilizing the deposition of a hydrogenated protection layer. The fabricated TFTs exhibited good performances such as $\mu_{sat}=9.5$ $cm^2\ V^{-1}\ s^{-1}$, $V_{th}=0.13$ V, $S=0.13$ V $decade^{-1}$, and $I_{on}/I_{off}>1\times10^9$. The width-normalized parasitic resistance $(R_{sd}W)$ was as low as 34 Ω cm. These results indicated that good Ohmic characteristics are obtained in this coplanar homojunction structure.

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