Journal Name

ARTICLE TYPE

Cite this: DOI: 00.0000/xxxxxxxxxx

Amorphous InGaZnO and metal oxide semiconductor devices: An overview and current status

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Received Date
Accepted Date

DOI: 00.0000/xxxxxxxxxx

The past 20 years has witnessed a rapid expansion of applications using metal oxide semiconductor devices that ranges from displays technology, to clothing and packaging. Details of these technological applications have been the subject of technical reviews, but the materials and specifically the metal oxide devices have not been coherent reviewed. This work brings together a wide range of information to present an overview of the history and development of metal oxide devices, from their earliest inception to the most recent advances. This begins with a discussion of the first developments of metal oxides and their applications, and the earliest realisations of metal oxide semiconducting devices and moves on to a discussion of the factors that need to be considered in designing metal oxide semiconducting devices, including; material choice, deposition methods and device structure. This is followed by an in-depth review of the effects of material defects and concludes with a review of the current state of applications based on metal oxide semiconductors.

1 Introduction

Over the past two decades there has been a rapid increase in the volume of technological applications that use metal oxide semiconductor-based devices. These applications include display technology and a variety of fast moving consumer goods (FMCGs). There are a number of technical reviews that cover these technologies in great detail[1–6], while the details of the oxide materials, devices concepts and the device details that form the underpinning basis of these technological solutions have not been coherently reviewed. This work aims to provide an accessible overview of these developments from their earliest inception and summarises the current status.

To begin, transparent conductive metal oxides (TCOs) are introduced and the application of these TCOs in electronics is described. This is followed by a detailed review of the developments of metal oxide based thin-film transistors (TFTs), which includes key considerations in the choice of material, the materials deposition methods and the different structural forms developed for functional devices. After this, an in-depth discussion of the effects of material defects in devices, with a particular focus on amorphous indium gallium zinc oxide (IGZO), is presented. This details the origin and the effects of the key defect types, and the post-deposition treatments employed to minimise their impact on device functionality. The review finishes with a survey of the current applications of a-IGZO, and related materials, devices including displays and flexible electronics applications.

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2 Transparent Metal Oxides

Optically transparent metal oxides have a variety of applications in electronics and beyond. This section of the overview has a particular focus on dielectric and conductive materials in transparent and flexible applications, while the review of semiconducting applications is presented in the next section.

2.1 Transparent Metal Oxides as Dielectric Materials

One of the most wide spread applications of metal oxides in electronics is as a dielectric material, particularly as the gate dielectric in transistors.

In conventional electronics, as the size of silicon transistors has reduced due to commercial pressure to produce ever higher functionality at lower costs, the thickness of the dielectric (traditionally SiO_2) has reduced in line with other dimensions[7]. However, as the thickness of the SiO_2 continues to reduce, gate leakage (the current flow due to direct tunnelling of electrons through the film) has become a limiting factor, such that by the early 2000's, with SiO_2 thicknesses less than 1.4 nm, the leakage current could reach 1 A cm^{-2} at 1 V[8,9].

This device scaling problem has driven the search for materials with higher dielectric constants, κ, to replace SiO_2. These high-κ dielectrics have been in many forms, most commonly metal oxides such as Ta_2O_3[10], $SrTiO_3$[11], Al_2O_3[7], and many others[12–23] (see figure 1). As highlighted in figure 1, the dielectric constant

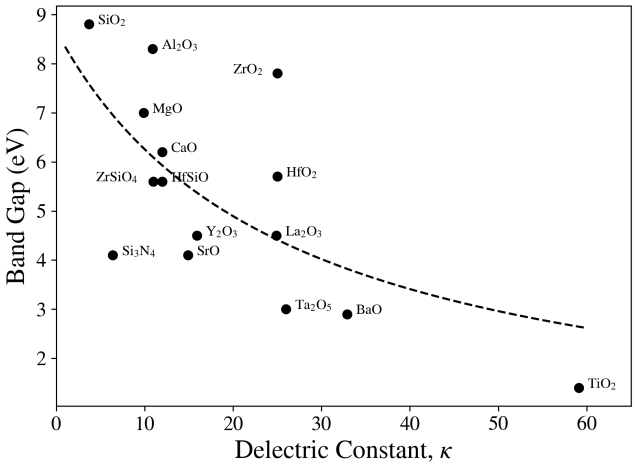

Fig. 1 Band gap as a function of static dielectric constant for some metal oxides, adapted from Robertson et al.[33]. The dielectric constant is approximately inversely proportional to the band gap, as represented by the dashed trend line.

is crudely inversely-proportional to the band gap of the material, requiring a balance between a high κ and the large band gap required to ensure good insulating behaviour. A key feature to note is that, in addition to providing good electrical isolation between the gate electrode and semiconductor, the large band gap of these high-κ dielectrics means they do not absorb light in the visible spectrum, making them optically transparent and therefore a suitable choice for transparent electronics[24]. For a comprehensive review of the requirements, potential materials, and developments in high-κ dielectrics see the review articles by Wilk et al.[7] and Wang et al.[24].

Due to its large band gap (≈ 8 eV) and reasonable dielectric constant (≈ 9), Al_2O_3 has become one of the most common choices for the gate dielectric material[24]. Al_2O_3 is also advantageous due to the wide range of deposition techniques that can be used and the uniformity of important characteristics, such as dielectric constant and refractive index, particularly in the amorphous phase[25–31]. For current device applications, Al_2O_3 is thus a good choice for the dielectric. However, due to the lower value of κ than many other metal oxides, more recent work has sought to create multilayered dielectrics incorporating other, high-κ, materials to further enhance device performance[27,32].

2.2 Transparent Metal Oxides as Transparent Electrodes

The second major application of transparent metal oxides in electronics is as a conductive component, known as transparent conductive oxides (TCOs), the main application of which is as electrodes, particularly for display applications.

The first report on TCOs came in 1907 with Badeker's discovery of the conductive properties of CdO, Cu_2O, and PbO[34], although further developments of the field were limited throughout the first half of the 20^{th} century by the limitations of the vacuum technology at the time. The thermal oxidation of a sputtered metal film, demonstrated by Badeker, was later used to produce tin oxide[35] and indium oxide[36] films, following which chemical deposition (in the form of pyrolysis) was developed for both[37–39]. The same materials were later deposited by reactive sputtering of metal films in an Ar/O_2 atmosphere, which was also used to produce iron oxide[40].

The second half of the 20^{th} century saw a proliferation of TCO applications such as in anti-static coatings, heat reflecting glass coatings, window heating elements, and many others[41,42], in addition to significant usage in electronics.

The overwhelming majority of electronics applications have used indium-tin-oxide (ITO), in part because it was one of the first TCOs to be developed in a controllable manner[43–45] and also because the control of the film conductivity that was achieved by controlling level of Sn incorporation[46,47]. Alongside the development of ITO, there has been work on SnO_2 and ZnO-based films, although the former has a significantly higher resistivity and the later has only recently achieved low resistivity values comparable with ITO[48].

The main use of TCOs within electronics has been as electrodes in optical devices, initially as the front electrode in rectifying photocells[49] and later as the gate electrode in flat panel displays (FPDs)[50–53]. ITO has also been used as both the gate electrode and source/drain electrodes in the fabrication of fully transparent TFTs[54,55], which are discussed further in section 3. Details of the physical basis for simultaneous good 'metallic' conductivity and 'non-metallic' transparency is well described in the review by Edwards et al.[56].

While there are advantages of using TCO electrodes, particularly in optoelectronic applications, there are also considerable limitations. One of the most apparent, and detrimental, is the resistivity of these TCOs. For all electrodes in a TFT the minimum possible resistivity (ρ) is desired, as this reduces voltage losses and signal noise. ITO and ZnO both have reported minimum resistivity of around 10^{-4} Ω cm[48], compared to commonly used thin metal films with resistivities in the range of 10^{-7} Ω cm$<\rho<10^{-5}$ Ω cm (for example $\rho<10^{-6}$ Ω cm for gold[57], $\rho \sim 6\times10^{-6}$ Ω cm for titanium[58,59], and $\rho \sim 2\times10^{-6}$ Ω cm for aluminium[60] in typical thin film thicknesses at room temperature). ITO further presents cost challenges for manufacturing due to the increasing rarity of indium[41,61,62]. Finally, as the field of thin-film electronics moves towards flexible applications, the use of ITO is limited as it fails quickly under strain[61,63].

The choice of electrode material, therefore, is highly dependent on the specific application, with TCOs (still predominantly ITO) continuing in established FPD manufacturing, while new alternatives such as carbon nanotubes, graphene, and metallic grids stand to replace ITO when optical transparency is still required but cost and/or flexibility become concerns[41,61,64–67], while simple metal films (or bi- and tri-layer stacks of metals) can be used where transparency is unnecessary and material and processing costs are dominant[68–70], discussed further in section 3.2.4.

3 Transparent Metal Oxides in Metal Oxide Thin-Film Transistors

The history of thin-film transistors (TFTs) actually pre-dates the now ubiquitous silicon transistor technology, at least in a theoretical sense. The first TFT designs were patented by Lilienfeld[71–73] and Heil[74] in the early 1930's , but due to the lack of understanding of either semiconductors or vacuum technology, these were purely concept patents with no demonstration of functionality. While these early designs where just concepts, they are very similar to modern designs, with Lilienfeld's first patent, granted in 1930, describing a metal-semiconductor field-effect transistor (MESFET) and another, in 1933, describing a metal-oxide-semiconductor field-effect transistor (MOSFET) of almost exactly the type seen today. It was not until the '60s, with significant advances in vacuum technology, that the first practical demonstration of TFTs was achieved by Weimer using polycrystalline cadmium sulphide (CdS) semiconductor with gold electrodes and a silicon monoxide (SiO) insulator[75,76].

Around the same time as Weimer was working on CdS TFTs at RCA Laboratories, Klasen and Keolmans developed a new back-side exposure process for photolithography of transparent, semiconducting, SnO_2 to create a self-aligned TFT structure[54]. Significantly, although there are few details of the device performance, this is the first reported instance of not only an oxide being used as the semiconductor in a TFT, but also of fully transparent transistors and electronics in general. Further demonstrations of metal oxide based TFTs were made by Boesen and Jocobs in 1968[77] with lithium doped zinc oxide (ZnO:Li), and by Aoki and Sasakura in 1970[78] with SnO_2, although both showed poor electrical performance, with low drain current (I_D) showing no saturation. Work continued sporadically on metal oxide transistor devices with reports on antimony doped SnO_2[79] and In_2O_3[80]. The focus of this work was not on device performance, but rather on hysteresis effects for memory applications, so little electrical characterisation was included. It was not until 2003, with the work of Hoffman et al. on ZnO[81], that good electrical performance was shown for a metal oxide based TFT.

3.1 Development beyond ZnO TFTs

The work of Hoffman et al., along with work from Carcia et al. and Masuda et al.[82,83] marked the beginning of a new phase of research in metal oxide semiconductors and transparent electronics.

ZnO was known as a semiconducting oxide since the early '50s[84], but until the work of these groups, commercial application was limited to passive devices such as transparent conducting films, sensors, photocatalysts, and varistors[85]. While the electronic performance achieved by Hoffman and Masuda was on a par with hydrogenated amorphous silicon (a-Si:H) and organic TFTs at the time, in terms of carrier mobility (at $\mu \leq 2.5$ cm^2 V^{-1} s^{-1}), ZnO was limited by the requirement for high processing temperatures, with devices exposed to process temperatures up to 600 °C. However, Carcia showed that similar performance could be achieved by depositing the ZnO using radio frequency (r.f.) sputtering at room temperature. Following this initial work on ZnO devices, many improvements in performance and variations in fabrication methods were reported[86–89], as well as work exploring SnO_2 and In_2O_3 film and ZnO nanowires[90–94]. These advances lead to demonstrations of ZnO replacing a-Si:H in flat panel displays (FPDs) for both active-matrix LCDs[95,96] and AM-OLEDs[97,98].

While devices based on binary semiconducting oxides (ZnO, SnO_2, In_2O_3, etc.) showed good performance, there were limitations, in particular with the control of the threshold voltage (V_{th}), device stability, and performance uniformity. These problems are attributed to the high defect concentration within the oxide, leading to an excess of free electrons, and the presence of grain boundaries in the polycrystalline binary oxide materials[1]. Some control of V_{th} was achieved by Lim et al. through doping the ZnO with nitrogen during deposition[99,100], however, the creation of grain-boundary free ZnO over large areas, either single crystal or amorphous, remains very challenging and ultimately leads to variations in device performance across the polycrystalline ZnO devices.

In an effort to mitigate these issues more complex oxides were proposed by Nomura et al. in 2003, particularly $InGaO_3(ZnO)_5$ (IGZO)[101]. Initially single crystal IGZO (sc-IGZO) was produced that removed issues linked to grain boundaries and greatly reduced the density of defects, such that normally-off TFTs (where there is no current flow at 0 V gate bias) were demonstrated[101]. These devices showed excellent functional characteristics, with high mobility μ=80 cm^2 V^{-1} s^{-1}, V_{th}=-3 V, and an on-off current ratio of 10^6. It was not, however, until the following year with work from the same group showing similar results using amorphous IGZO (a-IGZO)[55], that IGZO became widely acknowledged as the leading material for next generation thin-film semiconductors. This work was particularly significant as it showed that good device characteristics, i.e. $\mu_e \approx$8.3 cm^2 V^{-1} s^{-1}, V_{th}=1.6V, and on-off ratio $\approx 10^3$, could be achieved with processing at room temperature, enabling compatibility with the process constraints of flexible substrates. Additionally, it showed that the amorphous phase, which is stable up to around 500 °C in IGZO[102,103], was able to perform nearly as well as the single crystal phase while being significantly easier to produce.

The origin of the insensitivity of the electronic properties to to the details of the material structure can be understood as follows: The movement of electrons in a crystalline material such as silicon can be visualised as travelling along the sp^3 orbitals of the atoms, which overlap in the regular crystal structure, known as sp^3 hybridisation (visualised in figure 2**a**, top). However, if the crystal structure is disrupted by defects, or the material is amorphous, this conduction pathway is broken (figure 2**a**, bottom) leaving electrons to hop between orbitals in a process known as tail-state hopping[1]. This dramatically reduces the mobility of the material. For example, in silicon the electron mobility in single crystal material can reach over 1000 cm^{2}V^{-1} s^{-1} [104], but in the amorphous state this can drop to less than 0.05 cm^{2}V^{-1} s^{-1} [105]. In contrast, metal oxide semiconductors do not rely on the overlap of these sp^3 orbitals to provide the conduction

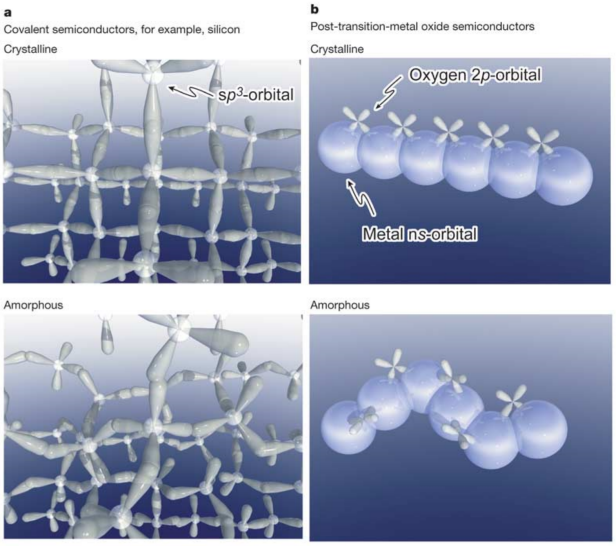

Fig. 2 Schematic orbital illustrations showing the carrier transport paths (that is, conduction band bottoms) in crystalline and amorphous semiconductors. **a** Covalent semiconductors have carrier transport paths composed of strongly directive sp^3 orbitals, so structural randomness greatly degrades the magnitude of bond overlap, that is, carrier mobility. Note that the orbitals shown do not show exact wavefunctions. **b** Amorphous oxide semiconductors composed of post-transition-metal cations. Spheres denote metal s orbitals. The contribution of oxygen $2p$ orbitals is small. Direct overlap between neighbouring metal s orbitals is rather large, and is not significantly affected even in an amorphous structure. Reproduced from Nomura et al.[55]

band pathway. Instead, the large s orbitals associated with the transition metal cations overlap to provide a conduction path, (figure 2**b**)[55]. As the s orbitals are spherically symmetrical, this overlap is the same whether the atoms are ordered in a regular crystal structure, or completely disordered in the amorphous form. Further details of the difference in transport mechanisms between traditional silicon and metal oxide semiconductors can be found in the review of the subject from Kamiya et al.[1]. The initial work from Nomura sparked a rush of publications on multicomponent oxides as the semiconductor component of TFTs. This research spanned both IGZO and many other combinations of cations with electron configuration $(n\text{-}1)d^{10}ns^0$ $(n\geq 4)$[106], including Sn-doped ZnO (ZTO)[107–111], In-Zn-oxide (IZO)[112–115], and hafnium indium zinc oxide (HIZO)[116–118]. For further reviews of the development of the general field of metal oxide TFTs see the papers by Kamiya et al., Fortunato et al., Park et al., and Petti et al.[1,2,4,5].

3.2 The growth of IGZO TFTs

Since the demonstration of IGZO by Nomura, many groups have contributed to the current understanding of these materials, both through the empirical study of devices, and through computational studies that use molecular dynamics and density functional theory.

The remainder of this section reviews the development of IGZO devices and the understanding of various issues surrounding device fabrication. While this section focuses primarily on IGZO, much of the discussion is directly applicable to other metal oxide devices.

3.2.1 IGZO Atomic Composition

One area of interest for the development of IGZO has been the ionic composition of the material. The single crystal devices originally produced by Nomura et al., with the stoichiometry $InGaO_3(ZnO)_5$, were grown by reactive solid-phase epitaxy on to an yttria-stabilized zirconia substrate[101,119,120]. The amorphous-IGZO demonstrated by the same group was deposited by pulsed laser deposition (PLD) from a polycrystalline $InGaZnO_4$ target in an oxygen atmosphere and had a cation ratio, measured by X-ray fluorescence spectroscopy, of In:Ga:Zn=1.1:1.1:0.9 (in atomic ratio)[55]. Systematic studies of the effect of material composition have been carried out by Hosono[121,122], Iwasaki et al.[123], and Barquinha et al.[124]. Hosono evaluated electron mobilities and concentrations through Hall effect measurements, as well as the crystalline nature of the materials, for various film compositions deposited on glass by PLD under oxygen partial pressure P_{O_2} = 1 Pa. Figure 3 shows tertiary composition maps of the amorphous formation regions, the electron mobilities and the concentrations evaluated from the Hall effect. The crystalline tendencies of ZnO and In_2O_3 are disrupted by mixing either with each other or with Ga_2O_3. In the case of the $(ZnO)_x(In_2O_3)_{1-x}$ combinations, this is attributed to mismatch between the wurzite structure of the ZnO and the bixbyite structure of the In_2O_3 as well as differences in the oxygen coordination numbers[125]. The inclusion of Ga_2O_3 with ZnO or In_2O_3 (or both), further disrupts the formation of the crystalline phase, again due to a difference in oxygen coordination numbers and the tendency of pure Ga_2O_3 to exist in the amorphous phase. It was also shown that the Hall mobility of the system is relatively insensitive to composition, but that the inclusion of Ga^+ ions largely suppresses the electron carrier concentration.

Baraquinha's work, summarised in the review by Fortunato[2] and shown in figure 4, investigated IGZO deposited by r.f. sputtering from a range of different composition ceramic targets, while Iwasaki used co-sputtering with 3 separate oxide targets to prepare IGZO. Both groups obtained similar trends with regard to electron mobility, which are also in agreement with the work of Hosono, although with the field effect mobility, μ_{FE}, quoted in figure 4 rather than the Hall mobility, μ_{Hall}. This work also agreed with the trend for increasing positive turn-on voltage (V_{on}) with increased gallium content. This later trend matches Hosono's finding of suppression of the electron carrier concentration, forcing the fabricated devices into enhancement mode with increasing gallium content.

Given the results above, many groups and commercial application projects have focused solely on material with a target composition of In:Ga:Zn=1:1:1 (in atomic ratio), as a compromise between high mobility, a V_{on} near to 0 V, and an intermediate carrier concentration that balances the need for an acceptable carrier density in the on-state with a low off-current and near zero turn-on-voltage[55,126–136].

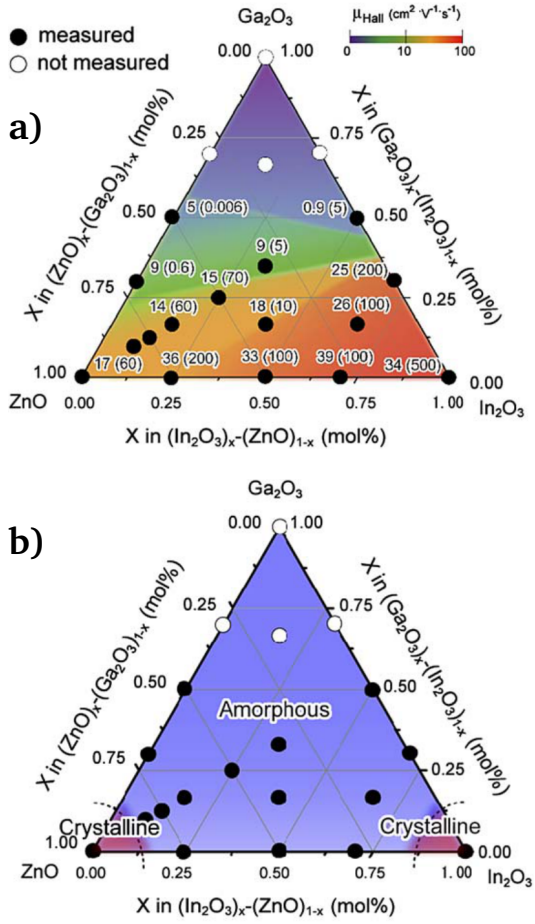

Fig. 3 The amorphous formation region (**a**) and the electron mobilities and concentrations evaluated from the Hall effect for the amorphous thin films (**b**) in the In_2O_3-Ga_2O_3-ZnO system. Numbers in the parentheses denotes carrier electron concentration ($\times 10^{18}$ cm^3). Reproduced from Hosono et al.[121].

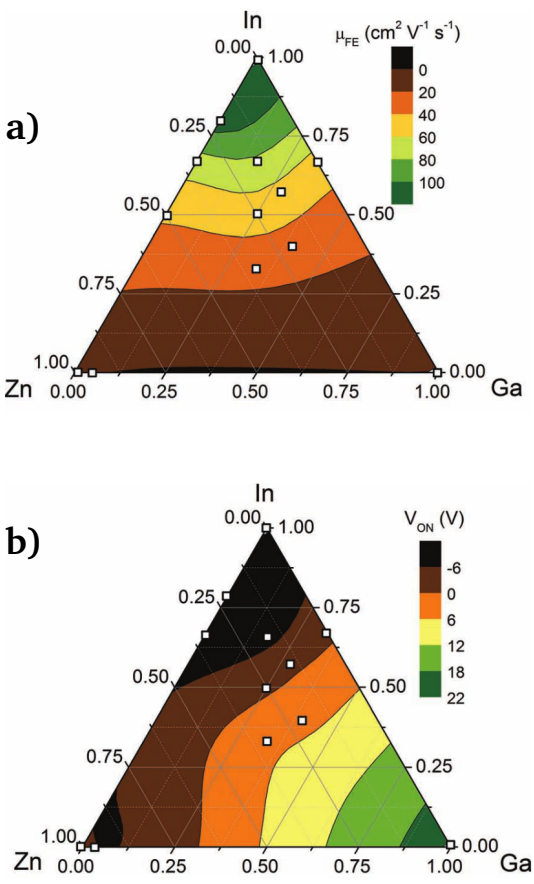

Fig. 4 a) Field effect mobility, μ_{FE} and **b)** turn-on voltage, V_{on}, obtained for TFTs with different oxide semiconductor compositions, in the gallium-indium-zinc oxide system. Devices annealed at 150 °C, with $\%O_2$ = 0.4%. Reproduced from Fortunato et al.[2].

3.2.2 Deposition Techniques for a-IGZO

Another area of interest to both researchers and industry is the method by which a-IGZO is deposited.

The majority of the work on a-IGZO deposition (more than 90% of published papers up to 2012[2]) has concentrated on sputtering. The main advantage of sputtering is the availability of tools and their compatibility with existing production-scale fabrication infrastructure, along with the capacity to deposit high quality films at, or near, room temperature[5]. This continues to be the dominant method of deposition. However, in recent years, there has been a rise in alternative methods for depositing a-IGZO at lower costs and higher throughput, by eliminating the need for vacuum deposition. In most cases this has taken the form of solution processing methods such as spin coating, inkjet printing, or spray pyrolysis[137–140]. There is also a growing body of work using spatial atomic layer deposition (S-ALD) that began in 2015 with work from Illiberi et al.[141] and has expanded to several research groups in the last few years[142–145].

While the possibility of depositing IGZO under atmospheric conditions is exciting, with potentially valuable applications in large area and roll-to-roll processing, it remains very much a developing area with significant challenges, and is partially reviewed in the recent work from Sheng et al.[145]. For solution processing routes these challenges are mostly in terms of the material properties, as solution processed a-IGZO has a significantly lower density than the sputtered material, which leads to reduced device performance in terms of carrier mobility, threshold control, and device stability (see section 4 for discussion of the link between density, defects, and device performance). In contrast, the main drawback of S-ALD is the cost of the equipment, which is not compatible with existing fabrication facilities aimed at a-Si:H fabrication, and also the relative scarcity of precursor materials, both of which may become less problematic as this technique develops.

3.2.3 TFT Device Structures for a-IGZO and other Metal Oxide TFTs

There are many possible device structures that have been investigated for metal-oxide TFTs. The most common structures are illustrated in figure 5. These configurations are typically categorised with respect to the position of the gate and

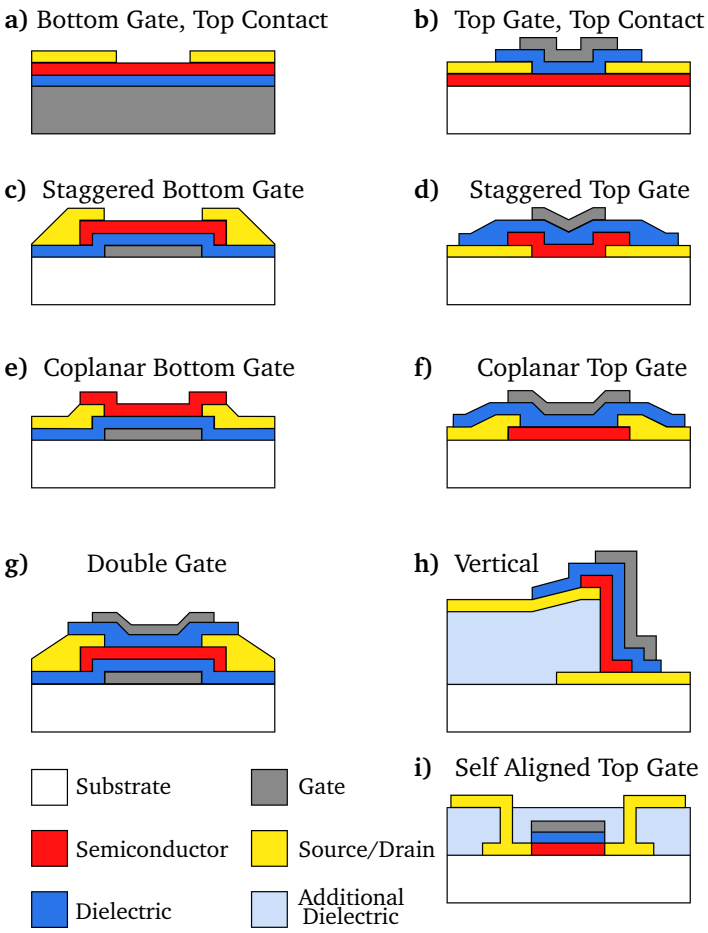

Fig. 5 Common device architectures:**a)** Bottom Gate, Top Contact with the substrate acting as the gate, **b)** Top Gate, Top Contact, **c)** Staggered Bottom Gate (sometimes Inverted Staggered or Bottom Gate, Top Contact), **d)** Staggered Top Gate, **e)** Coplanar Bottom Gate, **f)** Coplanar Top Gate, **g)** Double Gate, **h)** Vertical, **i)** Self Aligned Top Gate.

source/drain electrodes relative to the oxide semiconductor and to each other[146].

The general principle of all designs is the same - a semiconducting layer is patterned with two electrodes (the source and the drain) in direct contact with the semiconductor. A third electrode (the gate) is isolated from the semiconductor by a dielectric layer[2]. This third electrode modulates the conductivity of the semiconductor by capacitive interjection of charge carriers close to the dielectric/semiconductor interface. This is known as the *field effect* and is the basis for all field effect transistors (FETs)[147]. The main device configurations fall under two naming conventions, the first based on the gate position relative to the semiconductor, i.e. top-gate or bottom-gate devices. The second is based on the source/drain position relative to the gate and the semiconductor, such that when the gate and the source/drain are the same side of the semiconductor layer it is termed a coplanar device, while if they are on opposite sides of the semiconductor layer this is called a staggered device structure[146].

Structures optimised for Epitaxial Deposition The first two device structures, **a)** and **b)**, in figure 5 are perhaps the simplest designs and were the first to be studied. These designs have two advantages: First they require very few lithographic steps (just one in the case of figure 5**a)**) making device production relatively cheap and quick. Secondly, the deposition of the semiconductor onto a flat, stable surface allows for epitaxial growth of single crystal material[101,119]. The bottom-gate, top contact (BGTC) structure, sometimes referred to as staggered bottom-gate, shown in figure 5**a)**, is commonly used in research settings as commercially available Si wafers with a thermally grown SiO_2 layer can be used as the gate electrode and gate insulator respectively, meaning device structures can be created with just a single patterning step[1]. This design is, however, incompatible with commercial requirements due to the large overlap of the source/drain with the gate, causing high parasitic capacitance which acts to significantly reduce the switching speed of devices.

Bottom-gate TFT Structures Another disadvantage of device 5**a)**, that is common to all bottom-gated designs (5 **a)**, **c)** and **e)**), is the exposure of the semiconducting back-channel to environmental contaminants and/or damage during the source/drain definition process. The issue of back-channel exposure has been investigated by many groups. To prevent environmental contamination and the ingress of gases, devices can be encapsulated with a passivation layer, such as SiN_x, SiO_x, Al_2O_3, various polymers and even nano-cellulose material[4,116,148–154]. Devices with such a passivation layer, but which do not protect the back-channel from the effects of source/drain etching during fabrication, are known as back-channel etch (BCE) devices. In order to protect the back-channel from the effects of etching during source/drain electrode defininition, an additional layer, termed an etch-stopper (ES) can be introduced. This allows for more accurate etching of the source/drain electrodes[155] and enhanced device performance[4,156,157]. While these bottom-gated structures require additional processing steps to create stable, high performance devices, they also have some major advantages. One advantage, which has increased the speed with which IGZO devices have been integrated into commercial products, is that existing display manufacturing using a-Si:H uses a BCE design making the transfer from a-Si:H to IGZO very easy[1,4]. In addition IGZO is particularly prone to degradation in device characteristics when exposed to light[158–161], particularly UV light, as is the case when operating in display applications with a back-light (AM-LCD and some AMOLED displays for example[149]). In back-gated devices, where the gate is opaque to light the gate protects the channel region from the effects of the back-light, thereby reducing illumination bias stress effects (see section 4.4.3[162,163]).

Top-gate TFT Structures An alternative way of protecting the semiconducting material from environmental contamination is to fabricate the dielectric and the gate layers on top of the device in a top-gate configuration[4,55,128,164], as illustrated in figures 5 **b)**, **d)**, and **f)**. This configuration reduces the number of fabricationsteps , while protecting the conduction channel.

Two further key advantages exist for top-gate designs: For devices exposed to light from the top, such as in typical OLED displays, the gate protects the channel from the deleterious

light in the same way as discussed for the bottom-gated devices above[116,164,165]. Furthermore, the use of a top-gate design allows for a self-aligned gate, defined by exposing the photoresist from the back side of the device (through transparent substrate and semiconductor layers) with the light masked by the source/drain to minimise parasitic capacitance and maximise device response speed[117,164,166–168]. A final advantage of top-gated designs concerns epitaxial growth as discussed above. By depositing IGZO epitaxially on an inert substrate, crystalline material can be produced in both 5**a)** and 5**b)** structures. However, structure 5**a)** requires a silicon substrate, making production of transparent devices impossible. Conversely, by using a top-gated design with transparent electrodes (see section 2.2), fully transparent devices can be produced, with reasonable performance thanks to the reduced overlap of the gate and source/drain electrodes[55,82,83,109,169].

Coplanar vs Staggered Contacts in TFTs The second part of the device naming convention is concerned with the position of the source/drain contacts with regard to the semiconductor and the gate. Staggered structures have these contacts on the opposite side of the semiconductor to the gate, as in figures 5 **b)**, **c)**, and **d)**. A staggered structure with a bottom gate (also known as an inverted staggered structure) is the dominant architecture of a-Si:H devices used in commercial display manufacturing, and is therefore an attractive structure for the migration of IGZO into displays to replace a-Si:H. Conversely coplanar devices, with the contacts and the gate on the same side of the semiconductor, have advantages, including easier manufacture for crystalline devices grown epitaxially[101] and lower contact resistance between the source/drain contacts and the semiconductor[170,171].

Double-Gated TFT Structures Some research has also investigated structures with gate electrodes both above and below the semiconductor layer, in a so-called double-gate structure, figure 5**g)**[172–174]. This structure requires more processing steps due to the addition of an extra gate and dielectric layer, as well as necessitating a larger device footprint to accommodate the additional lithographic alignment tolerances and a more complex driving scheme[157]. The benefit of these more complex device is in significantly improved device performance. This includes improvements in the field effect mobility, μ_{FE}, and reduction of the subthreshold swing SS, as reported Lim et al., who showed nearly a doubling of μ_{FE} and halving of SS[175], while device stability is improved[176], and there is a reduction in device noise[177] owing to the change in field distribution within the channel. However despite these improvements, double-gate structures currently remain a research interest, with little development thus far towards commercial devices.

Vertical TFTs The final device structure, depicted in figure 5**h)**, is the vertical TFT. This design has come to attention as the push for reduced device footprint has forced researchers to consider alternatives to planar geometries[5]. Here the channel is defined by the thickness of a device layer, commonly an additional dielectric layer as in figure 5**h)**[143,178–181], although the channel can also be defined by the thickness of the gate or the semiconductor itself[182–185]. This approach is currently very new and only a small amount of work on it exisists.

3.2.4 Electrode Composition

In addition to the semiconductor composition, deposition method, and architecture, a significant effect on device performance comes from the electrode material, in particular the source/drain electrodes.

The choice of electrode material is determined by the application, with transparent metal oxides selected for flat panel displays, and while alternative transparent materials are being explored for other optoelectronic devices, and metal films are predominant where transparency is not required.

The primary consideration for the contact electrodes is then the contact resistance (R_{con}) that arises from the interface between the source/drain electrodes and the semiconductor. The total resistance (R_{tot}) between two contacts is the sum of this contact resistance and the resistance of the semiconductor, which is obtained from the sheet resistance of the semiconductor (R_{sq}). Resistance values can be extracted using transmission line measurements (TLM) in which contact pads of width W are deposited onto a sheet of semiconductor at varying distances (d), or directly from TFTs with variable channel lengths (d) and widths (W), following[186]

$$R_{tot} = R_{con} + R_{sq}\frac{d}{W}. \quad (1)$$

High contact resistance degrades the device characteristics, particularly μ_{FE} and the operating frequency[5,187,188] and therefore should be minimised. The contact resistance is dependent upon both the choice of electrode material and the nature of the interface between the electrode and the semiconductor.

The lowest contact resistances for a-IGZO devices have been achieved with metallic contacts. Early work from Shimura et al. showed that a range of materials including Ag, In, Ti, ITO with a-IZO have contact resistances $<10^{-4}$ Ω cm^2,[189]. In the following decade there has been a focus on improving the contact resistance with multilayered materials, such as Ti/Au (Au on Ti)[190], Ti/Al/Ti[128], AZO/Ag/AZO (aluminium doped ZnO with Ag)[191], becoming common[192–195], while the inclusion of other materials, such as a thin films of carbon, either amorphous[186] or graphene[196,197], has been reported.

As mentioned, the interface between the contact material and the semiconductor is important. Ti has often been included in contacts in order to promote good adhesion between the main contact metal and the a-IGZO, however, there is now evidence that the Ti acts to reduce the a-IGZO, creating TiO_x at the interface with metallised a-IGZO below, which leads to more Ohmic behaviour at the contact, improving device performance. This effect was clearly demonstrated by Choi and Kim, see figure 6[198] and was the basis of recent studies that used other treatments to reduce the a-IGZO below the contacts, such as the inclusion of a thin layer of calcium[199] or a helium plasma treatment[200].

The source/drain contact is a very active and evolving areas of research for a-IGZO and metal oxide TFTs and the discussion

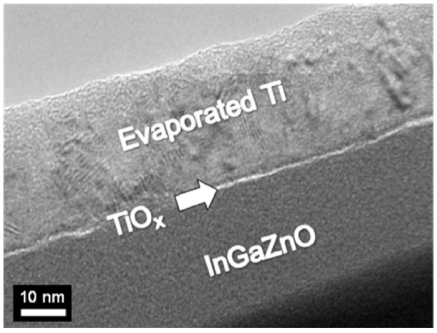

Fig. 6 Cross sectional high-resolution TEM image of a-IGZO TFT with Ti source/drain electrode with thin interfacial TiO_x layer indicated. Reproduced from Choi and Kim [198].

above provides a snapshot of recent achievements, but it does not detail the emerging routes for creating transparent contacts, such as nanowires [201,202] and micropatterned meshes [203], or the range of work on conductive transparent metal oxides that specifically addresses optoelectronic applications. For a detailed review of these areas see the excellent recent work from Naghdi et al. [204].

3.2.5 Buffer Layer in TFTs

Where devices are fabricated with a top gate, particularly when using a polymer substrate for flexible applications, it is common to include a buffer layer between the substrate and the a-IGZO. This buffer layer helps create a smooth, stable platform onto which the a-IGZO is deposited, and is necessary as most flexible substrates have a high native roughness (polymer substrates typically have a surface roughness of around 50 nm to 500 nm depending on the preparation conditions, much higher than, for example, typical silicon wafer roughnesses of less than 1 nm). This buffer layer also acts as a barrier against the ingress of moisture and gases from the polymer and/or environment [199,205–208]. While this buffer layer does not show any direct electrical behaviour, defects at the interface with the semiconductor can play a significant role in determining device characteristics, as described below in the discussions of defects. The inclusion and optimisation of such a buffer layer, often Al_2O_3, has been shown to significantly improve device characteristics, in particular negative bias stress (see section 4.4.2) [208,209].

4 Defects in a-IGZO and general Metal Oxide TFTs

Having detailed the development of amorphous metal oxide applications, and specifically that of a-IGZO TFTs, this review now turns to the understanding and control of defects in a-IGZO TFTs. This is broken down into a discussion of the major defect types, their effect on device performance, and the various measures reported to limit or harness these effects.

Significantly, while most defects are detrimental to device performance, some defects actually contribute to the high carrier density found in a-IGZO that makes it such a useful material. The topic of defects in a-IGZO TFTs has recently been well described by de Jamblinne de Meux [210].

4.1 Defects in the Channel Region

There are three main defect types present in the channel region of an a-IGZO TFT: oxygen vacancies, metal-metal bonds, and incorporated hydrogen [4]. The effects of these on the static transfer characteristics are discussed here, while their effect on device stability is considered separately below.

4.1.1 Oxygen Vacancies

Oxygen vacancies (V_O) are perhaps the most complex and impactful defects in the bulk channel. Vacancies can form during deposition of the a-IGZO or through the removal of oxygen atoms post deposition. The oxygen content in a film is related to the level of oxygen vacancies, although it is not a direct measure as oxygen can also be included in the film as interstitial, i.e. an unbound species in an amorphous structure. The precise level of oxygen required to enable semiconducting behaviour in a-IGZO is not well characterised as reports of the oxygen content in films are limited (most works report the stoichiometry of the target and the O_2 partial pressure during deposition). However, there are indications that films with as little as 60% of the stoichiometric oxygen content can show semiconducting behaviour, although the behaviour is significantly poorer than the performance of material containing more oxygen [211].

In the vicinity of an oxygen vacancy several local structures can arise, depicted in figure 7. These local features each have different effects on the electronic properties of the devices, particularly the density of sub-gap states within the density of states (DOS).

Where an oxygen vacancy is surrounded by a small number of cations, as in 7**(a)**, or if the vacancy is next to a large free space void, as in 7**(b)**, both deep and shallow electron traps are formed [212]. These trap sites have a significant effect on the transfer characteristics of devices, and impact upon the operational stability (discussed separately below).

As the name suggests, these sites trap electrons (two electrons are trapped at an oxygen vacancy to create a neutral defect), reducing the carrier concentration and increasing the subthreshold swing (SS) while also contributing to hysteresis in the transfer characteristics. SS is directly related to the density of sub-gap trap sites according to [1]

$$SS = ln10 \cdot \frac{k_B T}{q}\left(1+\frac{qD_{sg}}{C_G}\right)[meV\,decade^{-1}] \qquad (2)$$

where k_B is Boltzmann's constant, q is the elementary electron charge, C_G is the gate dielectric capacitance and D_{sg} is the trap density, made up of trap states at the dielectric-semiconductor interface, D_{it}, and in the bulk channel, N_{sg}. Evaluated at 300K SS becomes

$$SS = 59.5\left(1+\frac{qD_{sg}}{C_G}\right)[meV\,decade^{-1}] \qquad (3)$$

As $N_{sg} \gg D_{it}$ (around 5 orders of magnitude of difference have been reported [1,213]), defects in the channel bulk are effectively responsible for the magnitude of SS. Since SS is a measure of how much voltage is required to switch the device from off to on, a lower SS is desired to reduce the device operating voltage [214]. The majority of defects that influence SS are deep within the band

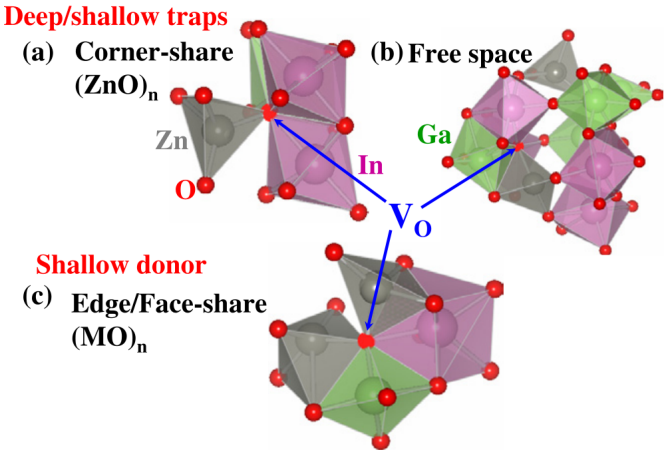

Fig. 7 Local coordination structures of some oxygen deficiencies. The red spheres represent O ions, green spheres are Ga, grey spheres are Zn and pink spheres are In atoms. The red spheres indicated by the arrows are oxygen vacancy sites. 'Corner-share', 'Free-space' and 'Edge/Face-share' notation describes the structures around these oxygen vacancy sites. Reproduced from Kamiya et al.[1].

gap. Shallow trap states, around 0.1-0.3 eV below the valence band, contribute to hysteresis in device performance, as they trap electrons under positive gate bias, but release them under negative gate bias. Thus additional bias is needed to release these carriers before switching is observed[1,215,216].

Alternatively, where a vacancy is surrounded by many cations, particularly where these form a dense edge-sharing network, a shallow donor level is created, figure 7**(c)**.. The shallow donor level is the main source of charge carriers in a-IGZO and is therefore vital for charge transport in devices[55,211,217].

There are a variety of methods reported that aim to control the oxygen vacancies within a-IGZO. One such approach is controlling the level of vacancies in the material during deposition. This has been demonstrated in sputtered and pulsed laser deposited a-IGZO, where the increasing the partial pressure of oxygen is shown to decrease the level of V_O, corresponding to a reduction in the carrier concentration[218–221].

Post deposition annealing has also been shown to reduce V_O by annealing either in a pure O_2 atmosphere or in air[222–224]. In such cases, care must be taken to prevent excess oxygen inclusion in the material, as this can degrade device performance[102]. While most demonstrations of annealing have taken place at relatively high temperatures, low temperature annealing has also been shown to contribute to a reduction of V_O[136,154].

4.1.2 Metal-Metal Bonds

The presence of metal-metal bonds is associated with oxygen vacancy defects, in particular in oxygen-poor materials. These bonds form where there is insufficient oxygen, leaving under-coordinated metal ions that bond together to eliminate dangling bonds. These metal-metal bonds induce additional deep sub-gap states in the upper half of the band gap, below the conduction band minimum (CBM)[225,226], with their exact position determined by the surrounding ionic environment. The ill-defined positions of these states leads to a wide distribution of observed states, and ultimately to tail-states extending throughout the band gap[227]. The presence of extended tail-like states throughout the band gap can significantly increase leakage current in the off state, I_{off}.

Reduction of the density of metal-metal bonds follows similar routes as for decreasing V_O, because the metal-metal bonds are most commonly found in oxygen poor materials, so the prevention of metal-metal bonds during deposition and post deposition annealing can both be utilised. However, once metal-metal bonds are formed they are harder to eliminate than oxygen vacancies due to the energy required to break these bonds, so post deposition annealing requires higher energies (i.e. higher temperatures). The thermal budget for processing of flexible substrates is relatively low (as discussed later in this review) such that high temperatures cannot be used with flexible devices, so for flexibles it is preferable to deposit the material under optimised conditions.

4.1.3 Hydrogen Incorporation

The final major defect type that is common in the bulk of the channel layer is the incorporation of hydrogen. This can happen during deposition[228], with annealing under certain conditions[228–230], or via diffusion from the materials above and below the a-IGZO, i.e. the gate dielectric, etch stopper or passivation layer (in bottom gated devices), or, in some top-gated cases the buffer layer.

There has been much debate about the role of hydrogen within a-IGZO, but a general consensus has emerged over the last few years[207,231]. The effect of hydrogen has two components that dominate at different H concentrations.

At lower concentrations, up to around 2×10^{21} cm^{-3} according to Han et al.[207], hydrogen in the film either bonds to weakly bound oxygen to create -OH groups[232] or replaces oxygen at vacancy sites passivating the vacancy[207,233,234]. By passivating these oxygen related defects, hydrogen improves device performance, giving lower subthreshold swing, reduced hysteresis (due to reduction in defect density) and increased carrier concentration[231,235]. This last effect results from the fact that singly charged hydrogen states are stable, meaning the hydrogen acts as a shallow donor[231,233].

At higher concentration levels, above 2×10^{21} cm^{-3}, hydrogen no longer improves device performance. Instead, the additional hydrogen creates a conductive channel near the dielectric interface that negatively shifts the turn-on voltage in proportion to the level of additional hydrogen[207]. As hydrogen is a particularly mobile species it can be hard to control the levels of hydrogen in a film.

While a consensus has started to emerge in recent years, a coherent overview of all mechanisms and potential treatments is still lacking. The field of a-IGZO (and more generally metal oxide TFTs) would benefit greatly from the publication of a comprehensive review of this topic.

4.2 Defects in the Gate Dielectric

The gate dielectric itself can also host defects that have a significant effect on device performance. Specifically, where hydrogen is incorporated into the dielectric layer, such as in Al_2O_3, HfO_2, SiN_x, SiO_x or any of the other gate dielectrics used, it acts as a charge trapping site[236–238]. Similarly, any oxygen vacancies or under-coordinated species in the layer can act as deep or shallow trap sites, much as they do in SiO_2 in traditional silicon electronics[239,240]. These traps, for the most part, are quite shallow, such that they trap electrons under positive gate bias and release them during negative bias. This weak trapping has only a small impact on long term device performance, discussed below, it does contribute significantly to hysteresis in the device characteristics, because the trapped electrons act to shield the a-IGZO channel from the gate bias[241].

Similar to the approaches to eliminate oxygen vacancies and metal-metal bonds in a-IGZO, attempts to reduce the defect density in the dielectric have taken two routes: optimisation of the deposited material and post-deposition annealing. By reducing the level of native defects through optimising the deposition process for the gate dielectric, much additional processing is eliminated. However, it has been shown that where non-optimised deposition is necessary, annealing can significantly improve the device performance[242,243].

4.3 Defects at the interface between the channel and the surrounding dielectrics

Finally, the remaining locations of defects with significant impact on device performance are at the surface of the a-IGZO channel, at the interface between either the gate dielectric (the front channel) or the passivation/etch stopper/buffer layer (the back channel). Defects at these interfaces can occur for a variety of reasons, including diffusion of material at the interface (that may be the deposited material or unintentionally included species such as hydrogen), the native roughness of the material onto which the a-IGZO is deposited or damage from the deposition and patterning of subsequent materials following the a-IGZO deposition. These defects can act as trap sites, contributing to both hysteresis and device stability.

Where bottom-gate devices are concerned, the most effective route to reducing such defects is the inclusion of an etch stopper layer, which is now common practice[155,156,244,245], although care must be taken during deposition of the etch stopper as this may itself cause defects in the a-IGZO[246]. For top-gate coplanar devices, where the contacts are deposited on top of the a-IGZO and the channel then defined through lithography, the etching of the contacts can cause significant damage to the interface[247] so either an etchant that does not significantly etch a-IGZO, such as H_2O_2 should be used[174,247], or an off-set structure can be used as in the self-aligned coplanar structure of figure 5i), for example that shown by Hong et al. in figure 8[248].

4.4 Device stability

The issue of device stability is treated separately here for two reasons; first, because it is an important issue with a significant volume of research focused upon it and secondly, because it is impacted by almost all types of defect.

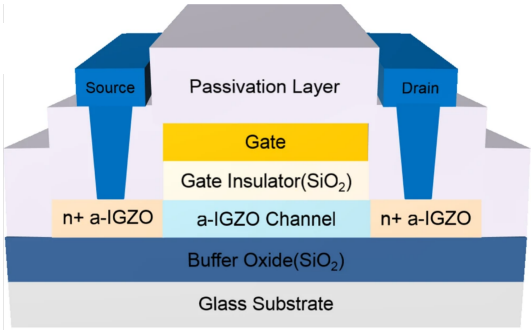

Fig. 8 Cross-sectional schematic of a top-gate self-aligned coplanar a-IGZO TFT. Reproduced from Hong et al.[248].

Device stability here refers to how much the parameters characterising the quasi-static IV cycle (i.e. SS, V_{th}, I_{on}, I_{off}, μ) change during or after some level of voltage stress. This stability is typically assessed by holding the gate electrode at the positive (for positive bias stress, PBS) or negative (for negative bias stress, NBS) extreme of the expected functional range of the device whilst holding the source electrode at ground and either applying a voltage equal to the gate voltage (for constant current measurements) to the drain electrode or holding it at ground. Biasing is then applied for various times under different environmental conditions that often includes light and/or temperature.

The significance of device stability stems from the need for devices to perform uniformly within defined tolerances and consistently over extended periods of time and many thousands of cycles. In display applications, small variation in device characteristics can cause obvious and immediate variation in the display output[249], while sensing applications rely on consistent operation of comparators with fixed V_{th} to make accurate measurements, and low power circuits, such as RFID tags require "normally-off" devices with a stable $V_{th}>0$ V, so that no power is wasted and to ensure proper modulation of the carrier signal.

4.4.1 Positive Bias Stress

It has been shown, for almost all conditions that have been considered, that applying positive gate bias stress (PBS) causes a positive shift in the transfer curve for devices (ΔV_{th}), but very little change in mobility (μ) or subthreshold swing (SS)[165,250–257], see for example figure 9**a)** from Lee et al.[165].

In conventional a-Si TFTs PBS testing has identified two degradation mechanisms: Defect creation in the channel and charge trapping in the dielectric or at the interface between the dielectric and the channel[258,259]. Defect creation degrades both μ and SS, while charge trapping causes a positive shift in V_{th}. As PBS on a-IGZO devices only causes a shift in V_{th}, it has been concluded that only charge trapping occurs, with no additional defect creation[1,4,157].

This charge trapping can occur at any of the trap sites discussed above, most significantly in the dielectric or at the interface between the dielectric and the a-IGZO. This process is almost

identical to that which causes hysteresis between the forward and reverse transfer characteristics, i.e. the trap sites capture an electron, creating a negatively charged layer that shields the a-IGZO from the positive gate bias, which reduces the effective bias of the a-IGZO, so V_{th} increases. However, unlike with hysteresis, the electrons become tightly bound and remain stable at the defect sites even under negative gate bias. In addition, it has been shown that recovery of the original V_{th} is possible after a relaxation period, as shown in 9**b)**. This recovery is hastened by elevated temperatures[1,2], but has been shown to occur even at room temperature[253,256].

An additional contribution to PBS occurs in bottom gated devices with an exposed back channel, where ambient water and oxygen can be adsorbed/desorbed from the surface, which causes an additional shift in V_{th}[214,260,261], although this can be effectively eliminated with the inclusion of a passivation layer[262,263].

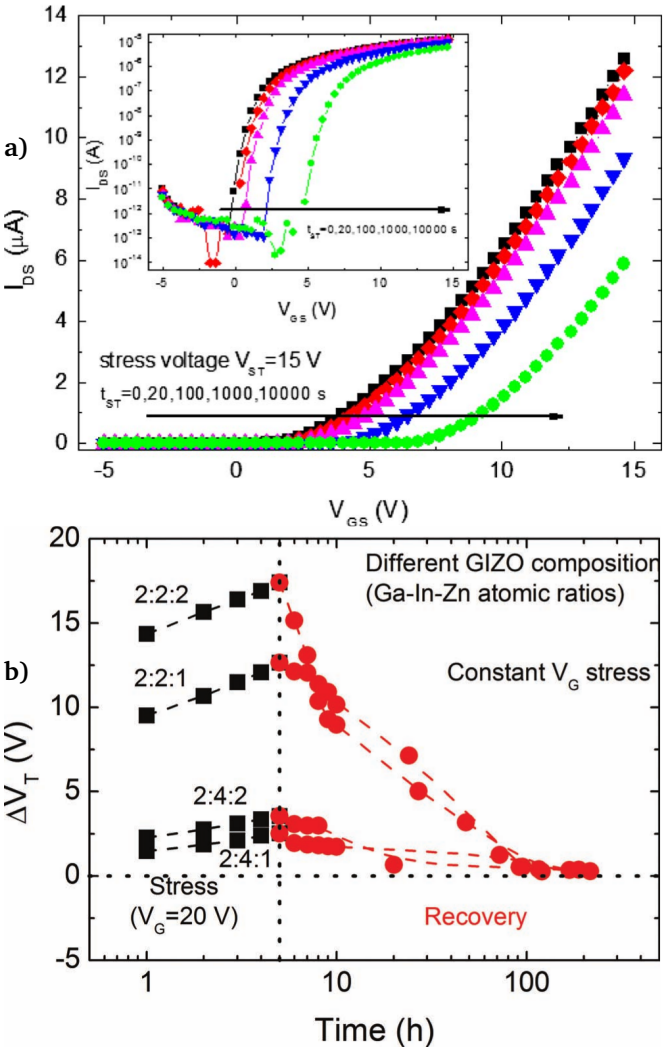

Fig. 9 a) Linear transfer I_{DS}-V_{GS} curves for a-IGZO TFTs as a function of bias stress time (t_{ST}). The inset shows the bias-stress-induced shift of log(I_{DS})-V_{GS} curve. The sweep was done at V_{DS}=0.5 V in both. Reproduced from Lee et al.[165]. **b)** ΔV_T under gate-bias stress measurements over 5 hours stressing for oxide TFTs with different IGZO composition, annealed at 150 °C. Reproduced from Fortunato et al.[2].

4.4.2 Negative Bias Stress

In contrast to positive bias, negative biasing of devices shows remarkably little effect on device characteristics when carried out in the dark[1,264,265]. The small shifts that have been observed are similar to the PBS, with no change in μ or SS, and a small ΔV_{th}<1 V, with the original characteristics recovered after a short anneal. This is explained similarly to PBS, now with trapping of holes at defect sites causing a positive shielding effect and a subsequent lowering of V_{th}[157]. As a-IGZO is an intrinsic n-type semiconductor, there is a very low density of holes native to the material and so little positive charge to trap, which limits ΔV_{th}.

4.4.3 Illumination Bias Stress

Many applications of a-IGZO involve illumination of devices. In display applications this comes either from the back light used in LCDs or from the pixels themselves in OLED displays, while in transparent, and many non-transparent circuits the light comes from the ambient environment.

It has been shown that such illumination has a negligible effect on PBS[266], but a significant effect on the negative bias stress, known as negative bias illumination stress (NBIS).

Figure 10 shows a typical response to NBIS with **a)** illumination wavelength, **b)** stressing time with illumination at an energy less than the band gap, and **c)** stressing time with illumination at an energy greater than the band gap. This figure shows that NBIS causes two significant changes in the transfer characteristics: enhanced negative ΔV_{th} and an increase in the off-current, I_{off}. These results also show that the effects of NBIS are dependent on the wavelength of the illuminating light, with little change when the energy is significantly below the band gap of ≈3 eV, some enhancement in the negative shift with wavelengths near the band gap energy and a significant negative shift and increased I_{off} for illumination above the band gap energy. This has been explained with a hole-trapping model proposed by Lee et al.[267], in which illumination excites electrons from the valence band to subgap electron traps and the resulting holes are transported to trap sites at the dielectric-semiconductor interface.

While this model explains the enhanced negative ΔV_{th}, it does not explain the increase in I_{off}. Kamiya et al. proposed a slightly different model in which electrons are promoted from deep-subgap states (such as those created by some oxygen vacancies and metal-metal bonds) to the conduction band. This model explains both the shift in V_{th}, and the increased I_{off} as there is a higher concentration of charge carriers in the conduction band even in the “off" state. These models are supported by the reported dependence of ΔV_{th} on the thickness of the channel, where devices with a thicker channel show greater ΔV_{th} due to an increase in the volume in which photoexcitations can occur[268].

4.4.4 Control of mechanisms that lead to device instability

The instability of device performance that results from the presence of defect sites can be improved in various ways. The reduction of defects in the dielectric and at the dielectric/a-IGZO interface are clear routes to reducing instability effects, since fewer defects means fewer charge trap sites and therefore smaller

shifts in V_{th}.
For the dielectric layer this is achieved by optimising the deposition process. For example, it has been shown that higher temperature (250 °C) ALD deposited dielectric produced more stable devices than identically fabricated devices with lower temperature (200 °C) ALD dielectric[269].
As with routes to reducing V_O and metal-metal bonds, the most effective method for reducing defects at the dielectric/a-IGZO interface is post-deposition thermal annealing[270]. This has been shown by many groups to reduce device instability, particularly NBIS[102,160,230,268], which is in part due to local relaxation that accommodates defects and partly due to diffusion of material at the interface that pacifies charge traps[271].
It is significant to note that most of the annealing work demonstrating improvements in device stability involves temperatures at the top end or above the temperatures compatible with processing polymeric substrates.

5 Metal oxides for TFTs in flexible form factors

Truly flexible electronics has captured the imagination of the public for at least 60 years, with ideas of rollable, foldable displays and technology permeating science fiction and popular culture throughout the second half of the 20th century, back to *The Mechanical Monarch* by E.C. Tubb, published in 1958[272]:

> *"Against one wall a wide sheet of clear material suddenly flared with light and swirling colour. It steadied and a woman stared from the screen."*

This was followed by other similar ideas, such as electronic newspapers and smart contact lenses, appearing over the following 40 years[273–276], becoming an absolute expectation in the science fiction of the 21st century. Academia and industry have been working towards the demonstration and realisation of this vision for many years, first by thinning down crystalline silicon (c-Si) chips and reducing their size to create flexibility (although the silicon itself remains rigid), followed by the introduction of truly flexible silicon in its amorphous (a-Si)[277,278] and low-temperature polycrystalline (LTPS) forms[279,280], and then the revolution in organic electronics[281–283].
While excellent electrical performance can be maintained with c-Si, true flexibility is not possible. Conversely, good flexibility is possible with both a-Si and organics, but the electronic functionality is poor in comparison to c-Si (mobilities of <1 $cm^{-2}V^{-1}s^{-1}$ and <10 $cm^{-2}V^{-1}s^{-1}$ are reported for a-Si and organics respectively[5]). LTPS does offer good performance in a flexible form, but the manufacturing costs and high processing temperatures make it an unattractive option for most flexible applications.
Finally, thin-film metal oxides deposited on flexible substrates provide an effective route through which truly flexible, high performance low cost displays and wider electronic technologies can be enabled.

5.1 Advantages of electronics on flexible substrates

While the appeal of flexible displays for the general public is largely tied to the novelty of such technology, there are many practical advantages to migrating display, communication and sensing technologies on to flexible substrates.
The use of most flexible substrates greatly reduces the weight of devices, particularly displays which have traditionally been based around heavy, rigid glass and silicon, and for which there is a continuing drive for higher resolution and larger screens. This weight reduction improves handling, shipping, and production costs, and enables integration into a wide variety of products.
Flexibility can also bring advantages in terms of product robustness, which stems from the ability of the circuits to reversibly deform under impact, meaning that device interconnects are not broken by small shear forces, such as induced by vibrations.
However, flexible, particularly polymeric, substrates present difficulties for making robust interconnects between discrete components in the first place, particularly as the conventional methods of wire bonding may not be compatible due to the elevated temperatures required. Instead there is a great deal of work looking at the use of anisotropic conductive adhesives to make robust interconnects, which is covered in detail by Kim et al.[284] for rigid-to-flexible bonding, although no review yet exists covering flex-to-flex bonding.
A further advantage of flexible circuits is the opportunity to integrate electronic functionality into new form factors that are not accessible with traditional rigid circuits. These applications can include medical implants[285–288], intelligent packaging[289], wearable devices[290], and artificial skin[285,291], as well as flexible displays that can be rolled up into a very small size[292–298].

5.2 Materials for flexible substrates

There is a wide range of materials on which metal oxide TFTs can be fabricated, in principle the only limitation is the need for a relatively smooth (roughness <100 nm at least), continuous area on which the devices can be fabricated. In practice, however, the vast majority of flexible substrates used are polymers, either free standing or laminated onto a glass carrier for ease of processing.
The most commonly used polymers found in literature are polyimide (PI), polyethylene terephthalate (PET), and polyethylene naphthalate (PEN), although many others have been demonstrated. PET and PEN are attractive due to their very low cost, while having good chemical resistance, reasonable thermal stability below their glass transition temperature, T_g, and good transparency (both have cut-off wavelengths, λ_c in the ultraviolet). PI offers similar advantages in terms of chemical resistance and thermal stability, while having a significantly higher glass transition temperature (T_g=300 °C for PI compared to 120 °C for PEN and 80 °C for PET). However, standard PI has an optical cut-off λ_c=500 nm, making it appear yellow, although recent work has developed colourless PI (CPI)[299,300].
There have also been reports of TFTs fabricated on paper[301–303], thin metal foils[304–306], and ultra-thin flexible glass[307–309]. While paper and metal foils are clearly not transparent, they do have

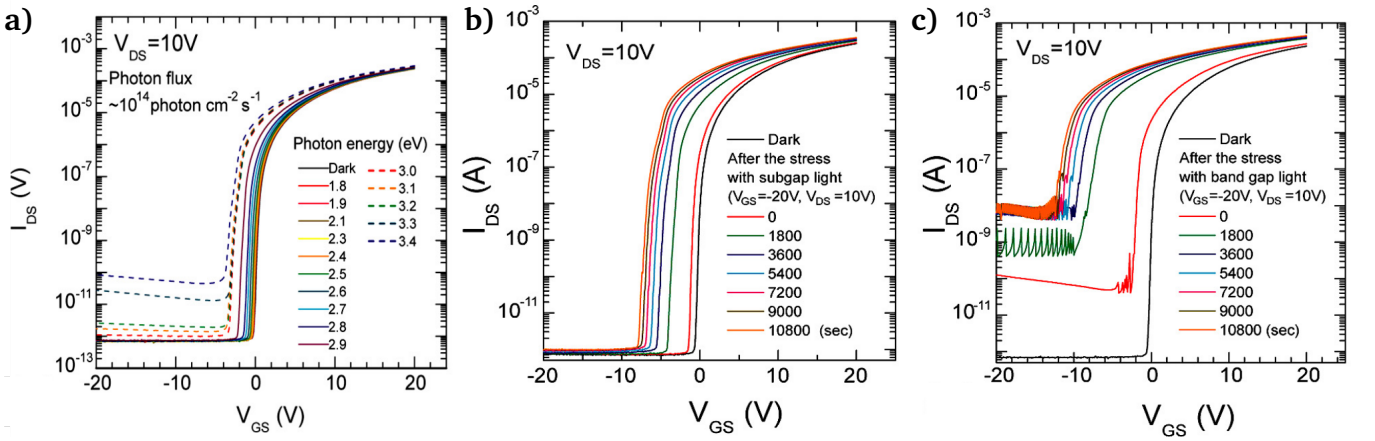

Fig. 10 a) I-V transfer curves for wet-annealed TFT in dark conditions and under monochromatic illumination with photon energies from 1.8 to 3.4 eV (λ = 700âĂŞ365 nm). **b)** Variation of transfer curves with subgap photon (E = 2.7 eV) illumination. **c)** Variation of transfer curves with band-gap photon (E = 3.4 eV) illumination. Reproduced from Nomura et al.[213].

benefits of low cost and high temperature processing capabilities respectively[310]. Ultra-thin glass, on the other hand, offers both transparency and high processing temperature, along with increased mechanical protection for devices, but at a significantly higher cost and reduced flexibility (the maximum bending radius is >1 mm).

5.3 Additional considerations for electronics on flexible substrates

While there are significant advantages of flexible electronics, they give rise to additional challenges to device manufacturing. There are several additional considerations for fabricating devices on flexible substrates, the most obvious being the flexibility of the substrate itself.

The flexibility of the substrate may be an issue during production as it may be prone to movement during the manufacturing processes. This influences the accuracy of lithographic processes such that the design tolerances must be greater, increasing device footprint and therefore defect counts, the parasitic capacitance, and the overall circuit size. To minimise substrate motion it may be held under tension during lithography, but this introduces residual stress into the films deposited, which may lead to delamination or cracking in some layers. Alternatively, the substrate can be laminated onto a rigid carrier for fabrication, although this may lead to subsequent challenges with releasing the substrates from the carrier.

A further issue with flexible substrates, particularly polymers, is that of differential thermal expansion with the added materials which may affect the film properties. PI is one of the most thermally stable polymers, with a coefficient of thermal expansion that is comparable to that of the materials used to make up the TFTs, making it a good choice to limit this effect.

Another significant effect of introducing flexibility is the impact on performance of devices with bending. This was recently reviewed by Heremans et al.[311] who showed that for many candidate materials (particularly LTPS and organic semiconductors), bending has a major negative impact on the carrier mobility. However, for a-IGZO strikingly little variation with stress has been observed[312,313], demonstrated in figure 11 that shows the variation in threshold voltage, subthreshold swing, on current, and mobility with bending to a radius of 2 mm, showing that all parameters remain almost constant. This insensitivity to bending is attributed to the same mechanism that gives rise to the good electronic characteristics that IGZO demonstrates, even in the amorphous form, i.e. conduction occurring through the overlap of the spherically symmetric *s* orbitals of the cations, discussed previously. This makes a-IGZO an excellent choice for flexible electronics, particularly in applications that may be expected to function in a flexed configuration, such as in packaging and curved displays.

6 Applications of a-IGZO and other metal oxide TFTs

The remaining section of this review considers common applications of a-IGZO and other metal oxide TFTs. Current, and likely future, applications of such materials can be broadly split into two categories, namely, display technologies and low cost flexible circuits, which have predicted market values of around $49B and $7B respectively by 2020[314]. Both applications are covered here, although the discussion of usage within display technologies is somewhat truncated, as several comprehensive reviews already exist[315–319].

6.1 Display Technology

Display applications have been the driving force in metal oxide, and particularly a-IGZO, TFT development[5]. Indeed, it took just one year from Nomura's demonstration of a-IGZO TFTs in 2004 for the first demonstration of a display backplane (for black and white e-paper) based on a-IGZO TFTs by Toppan Printing Co. Ltd.[126], which was shortly followed by a demonstration of an active matrix OLED (AM-OLED) display a year later by LG Electronics Inc.[320,321]. Many other companies have adopted a-IGZO, including Samsung[132,245], Hitachi[322], and AU Optronics Corp.[323], demonstrating progressively larger displays, as well

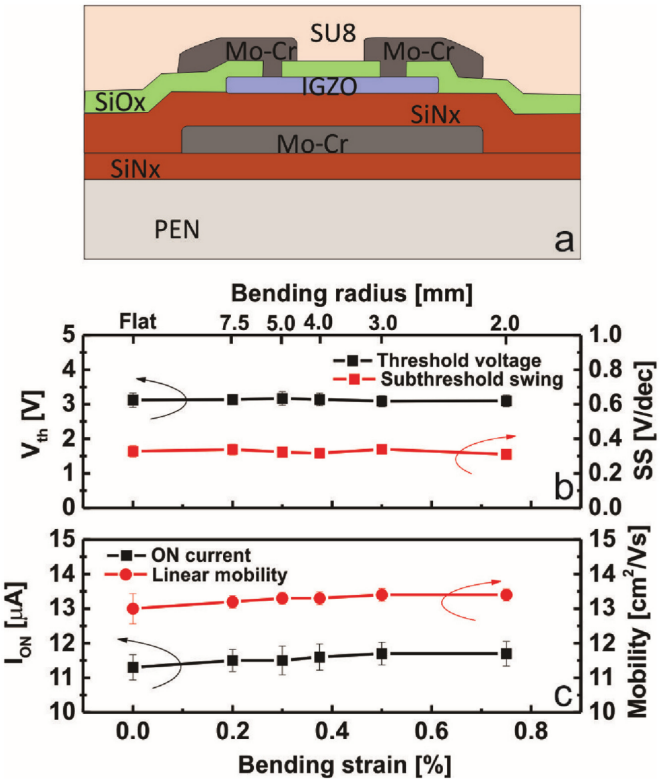

Fig. 11 Electronic properties in response to bending of a-IGZO thin-film transistors on 25 μm poly(ethylene naphthalate) (PEN): a) device structure and materials used (MoCr for the electrodes; silicon oxide (SiO_x), silicon nitride (SiN_x), and an epoxy photoresist (SU8) are used as dielectrics). b) Threshold voltage and subthreshold swing; c) ON current and mobility as a function of bending strain and corresponding bending radius. the channel length and width of the TFT are 20 μm and 60 μm respectively. Linear transfer curves were characterized at a drainâĂŞsource voltage V DS = 1 V and gateâĂŞsource voltage V GS = 10 V. Reproduced from Heremans et al.[311] .

as LCD back panels. Commercial production of a-IGZO based displays, by Sharp in 2012[324], commenced just 8 years after Nomura's initial work.

As discussed above, part of the appeal of a-IGZO for displays comes from the advantages afforded by flexible displays - light weight substrates, increased durability, and the popular appeal of a bendable display, which was considered from the very first demonstrations of a-IGZO[126]. Beyond simply being flexible, a-IGZO outperforms other competitive materials because of it's transparency. As discussed previously, when deposited on to a suitable substrate a-IGZO, along with other metal oxide semiconductors, can be used to form fully transparent circuits. In combination with suitable OLED display technology this creates the possibility for displays that are completely transparent in the off-state and become full displays when activated, see figure 12. Development to achieve this has recently taken a step forward with a slew of patents from Samsung that include both transparent and bendable mobile phones[325,326].

As depicted in figure 12**a)**, a-IGZO also outperforms both a-Si and organic transistors in terms of the mobility and approaches that achieved with LTPS[327]. This relatively high mobility allows devices with high operating frequencies, that are capable of driving high frame rate displays.

While LTPS matches or beats a-IGZO in mobility and operating frequency, it requires higher processing temperature (>350 °C) and significantly reduced uniformity that make it an unsuitable choice for larger display screens. Organics semiconductors also suffer from a lack of areal uniformity that results from the solution based processing used to deposit them over large areas. Uniformity is particularly important in display applications because the output of a given OLED pixel is highly dependent on the driving TFT's characteristics. It has been reported that a variation in threshold voltage of just 0.1 V can lead to up to a 20% variation in that OLED pixel's luminosity[249,328].

6.2 a-IGZO for logic, sensing and communications

Alongside the development of a-IGZO for display applications, work has been ongoing to develop a-IGZO and other metal oxides in applications such as logic circuits, sensing, power transmission, and wireless communication[5]. The advantages of metal oxides in these areas are similar to those for display applications but for somewhat different reasons. For example, large area uniformity now enables large volumes of consistent device production rather than large area displays; transparency facilitates creation of non-visible circuitry for, for example, security applications; flexibility allows integration of devices into previously inaccessible form factors while increasing the mechanical durability of circuits; and the low cost of production allows access to markets for which silicon-based devices are too expensive (such as fast moving consumer goods (FMCGs)).

6.2.1 Logic circuits

The development of metal oxide circuitry started a few years after the rapid growth in metal oxide research in the years around 2000, with Presley et al. demonstrating the first fully transparent circuits based on IGO in 2006[337]. This circuit, similar to most early circuitry, comprised a ring oscillator made of an odd number of inverters (in this case 5), connected in series as in figure 13**b)**. Each inverter, in turn, comprises a control TFT and a load (either a second TFT or a resistor), see figure 13**a)**. The use of ring oscillators allows the measurement of propagation delay, which is widely used as a benchmark for determining the maximum operating speed of a TFT[338]. The initial work by Presley produced relatively poor results, with the 5 stage oscillator operating at 9.5 kHz, corresponding to a stage delay of 11 μs/stage, which was largely due to significant parasitic capacitance arising from the large source/drain to gate overlaps in the device structure.

Shortly after the demonstration from Presley, Ofuji et al. demonstrated a similar system, this time using IGZO TFTs and significantly smaller overlaps, achieving 410 kHz, that equates to a propagation delay of 0.24 μs/stage, which is half that reported for a-Si:H[339] and one third of that for organic TFTs[340].

Since this early work, further improvements in speed have been obtained, circuit complexity has increased (for example shift registers[341] and scan drivers[342] have been demonstrated) and devices on flexible substrates have been produced that yield

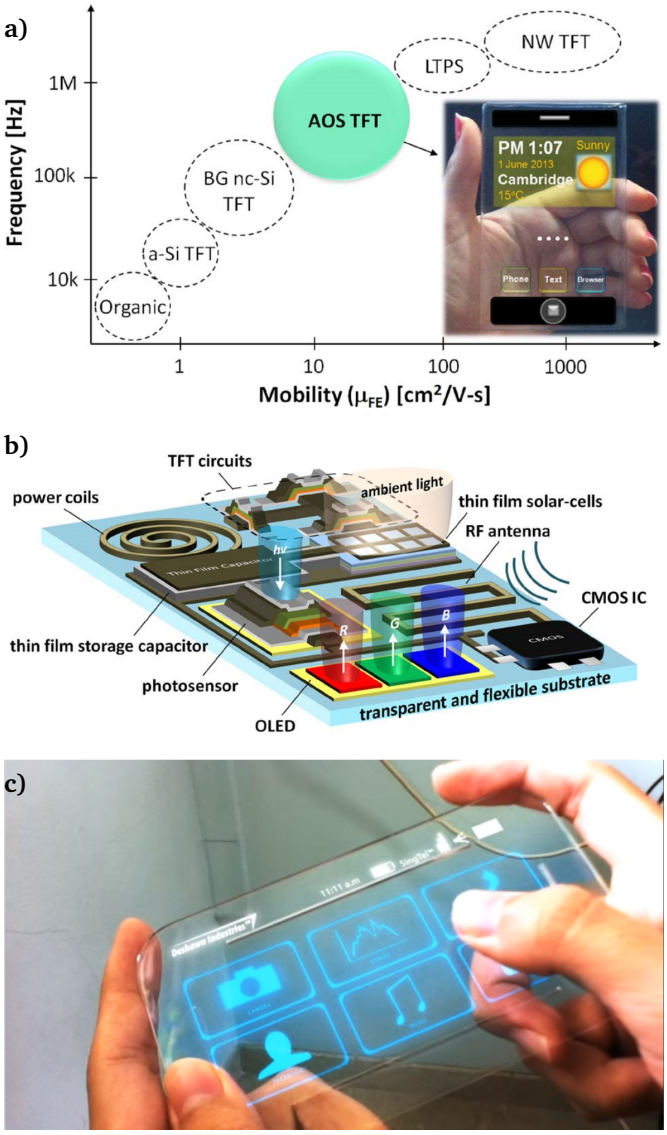

Fig. 12 a) Materials for TFTs mapping the relationship between frequency capability and carrier mobility. Inset: conceptual image of a transparent smart phone. **b)** Conceptual illustration of future transparent and flexible systems where display elements, sensors, circuits, RF functionality, and energy devices are heterogeneously integrated using oxides and other thin film technologies, including silicon CMOS. Here, for better illustrative purposes, transparency is disregarded. **a)** and **b)** Reproduced from Lee et al.[318] with data compiled from[2,55,82,319,329–335]. **c)** Image of a transparent PDA device featured in the film Iron Man 2[336].

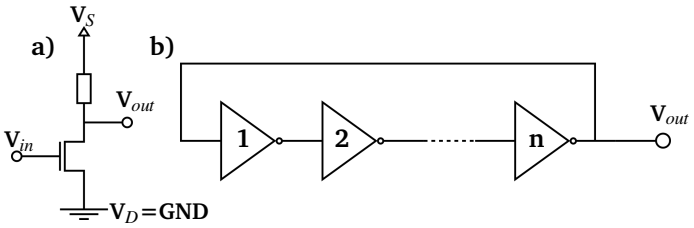

Fig. 13 a) Simple NMOS inverter with a resistive load, the resistor can be replaced by a second TFT wired as a diode (gate and drain shorted together). **b)** Ring oscillator using n inverter stages where n is always odd.

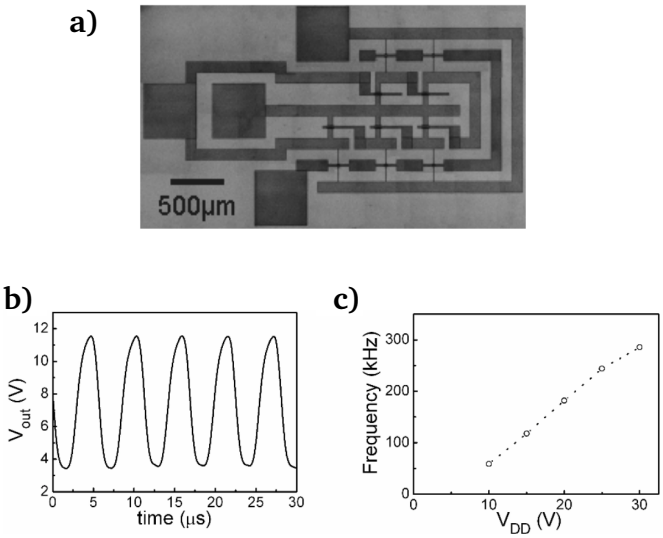

Fig. 14 a) Photo of an a-IGZO five-stage ring oscillator. **b)** Output characteristics of a five-stage ring oscillator at V_{DD} = 20 V, and **c)** oscillation frequency as a function of V_{DD}. Reproduced from Hsieh et al.[227]

good performance. See for example the first demonstration of a five-stage ring oscillator on colourless PI from Hsieh et al.[343], showing an operating frequency of 182 kHz, equivalent to a stage delay of 0.55μs/stage, at 20 V driving voltage, with a linear increase in frequency with voltage, figure 14, or work from Mativenga et al. showing high performance shift registers on PI which are still operational while rolled to a radius of just 4 mm, figure 15. These improvements have lead to demonstrations of full microprocessors, initially using crystalline IGZO[344–346], and recently with an amorphous metal oxide on flexible substrates reported by PragmatIC Printing Ltd. and ARM Holdings[347,348].

6.2.2 Sensing applications of metal oxide semiconductors

Alongside the development of logic elements, many groups have looked at the application of metal oxide to sensing[5]. Sensing capabilities are attractive as they open up possibilities within many more areas, including smart implants[350], artificial electronic skin[351], food safety[352], and temperature monitoring[353–355]. These sensors are in the early stages of development, but show great promise in a research setting and are now being integrated into industrial production.

Metal oxide sensors broadly operate along one of two lines: either multiple sensing and control gates are inductively coupled to the TFT gate, as in the work from Liu et al.[356], see figure 16, or a sensing surface (an externally coupled membrane[357], the TFT gate[355,358], or even the channel layer[359–361]) interacts with the local environment, ad/absorbing gas or liquid molecules, creating a shift in potential or electrical characteristics of the TFT.

An alternative route to sensing applications takes the form of integrating metal oxide circuitry with existing analogue sensors. For this metal-oxide-based analogue-to-digital convertors (ADCs), comprising comparators and the surrounding logic

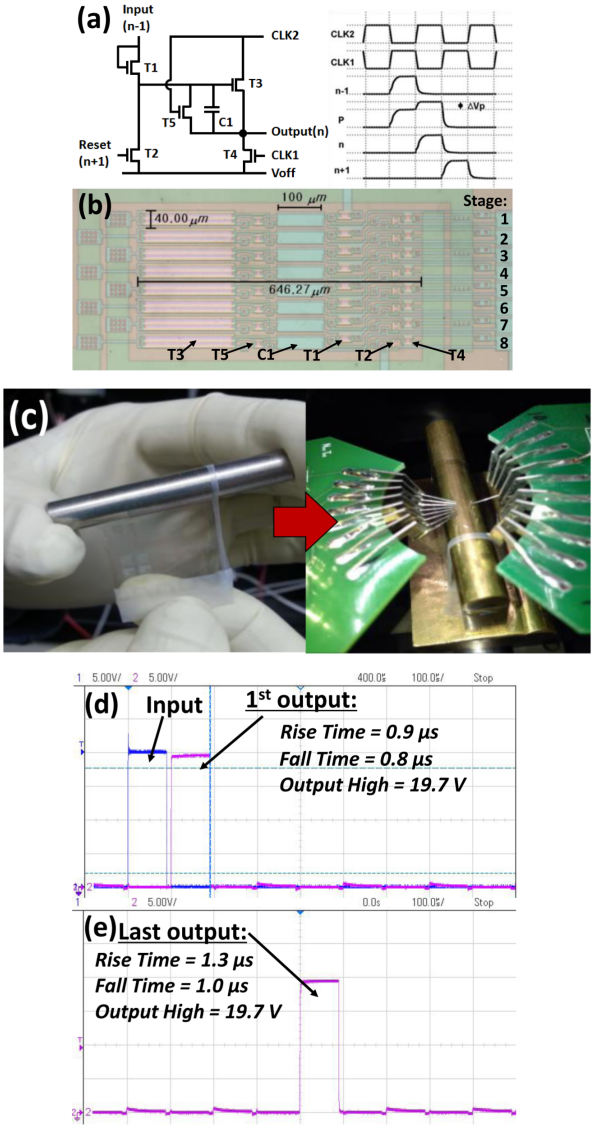

Fig. 15 Operation of a fully transparent and rollable a-IGZO TFT shift register (SR): **(a)** One stage circuit schematic and timing diagram of the two-clock, five transistor (5T), and one capacitor (1C) SR; **(b)** optical micrograph of a measured eight-states SR; **(c)** image of the sample containing the SR as it being rolled to a cylinder and the measurement set-up for the SR, while under bending stress. **(d)** and **(e)** First output and last output of the eight-stage SR under bending radius of 2 mm for input voltage VDD = 20 V. All rV_{th}eproduced from [349]

need to be integrated with existing bio-sensors. Practical demonstrations of this have recently been shown [362,363], although widespread implementation has been limited by device variability, both between devices and as device performance changes due to stability issues. Such systems are particularly sensitive to variability as the comparators here compares an input signal to a reference voltage, and any variation in threshold characteristics are directly translated into a variable output of the devices. These applications highlight the need for truly stable and uniform devices.

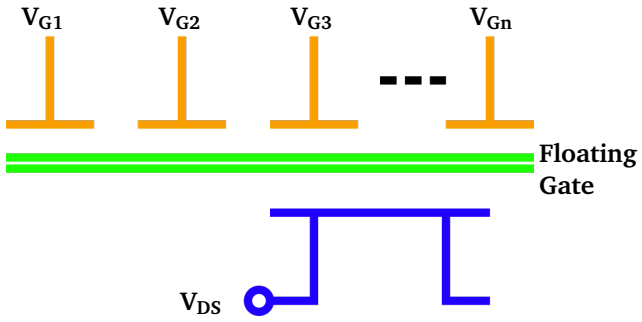

Fig. 16 Schematic illustration of a capacitive network for a flexible neuromorphic transistor. The carrier density of the channel is modulated by the weighted sum of all inputs of sensing gate and control gates. Adapted from Liu et al. [356]

6.2.3 Energy Harvesting

In order to leverage the low cost functionality made possible with a-IGZO technology, a power source is needed. In high value applications typically suited to silicon technology, this can be supplied by either a fixed supply or an integrated battery. This is, however, associated with high cost (both traditional coin cell batteries and next generation printed carbon batteries have a price floor one or two orders of magnitude greater than the cost per circuit for a-IGZO systems) and reduced flexibility (traditional batteries are rigid, while new printed batteries are much greater in size than the circuits being produced). This provides an opportunity for the supply of power via contactless transmission. Contactless power transmission can be realised with inductively coupled coils (source and receiver) and a rectifying circuit to convert AC input power into a usable DC supply. The receiving coil may be either a traditional metal coil, as commonly used in current RFID tags or, if transparency is desired, a TCO (typically ITO) although this comes at an efficiency cost. The rectifying circuit can be a diode or simply a TFT in a diode-load configuration (where the gate and drain are connected together) [364].

If a diode is used it may be one of several different forms. Most reminiscent of traditional silicon diodes is the p-n junction diode, in which a p- and an n-type semiconductor are in contact forming a p-n junction, for example NiO and IGZO as the p- and n-type materials respectively demonstrated by Münzenrieder et al. [365], as well as many other combinations [158,366,367]. Alternatively, Schottky diodes with a metal-semiconductor junction are possible. However, due to the large electron affinity of most metal oxide semiconductors only a small Schottky barrier is possible [310], although Chasin et al. have successfully demonstrated Schottky diodes using a-IGZO with a Pd contact [368], as has Zhang et al. with an Al contact [369]. Additionally, metal-insulator-semiconductor (MIS) [370], Metal-insulator-metal (MIM) [371] and self-switching diodes (SSD) [372–374] have been demonstrated, but each has limitations that currently restrict them to academic interest rather than practical application.

The most efficient and most common arrangement for rectifying circuitry is the bridge rectifier shown in figure 17. This uses

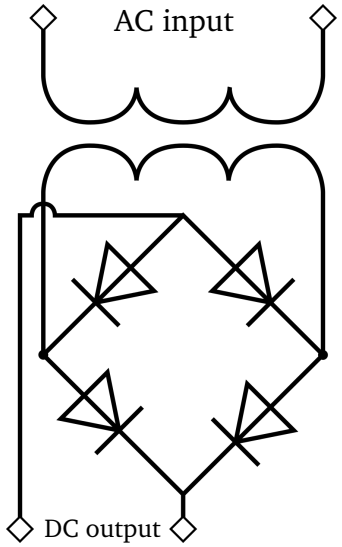

Fig. 17 Circuit schematic of a bridge rectifier using 4 diodes or diode-load TFTs.

4 diodes (or diode load configuration TFTs) to access both the positive and negative part of the AC waveform. Using this configuration with p-n diodes Münzenrieder et al. demonstrated a DC voltage of 2.1 V at an input frequency of 125 kHz with a peak-to-peak voltage (V_{PP}) of 12 V[365] and Chen et al. obtained 2.5 V up to 27 MHz with V_{PP}=8 V using Cu_2O instead of NiO[375]. Using Schottky diodes in the same configuration, Chasin et al. demonstrated the significant speed advantage inherent in Schottky devices, showing a DC voltage of 1.7 V for an input V_{PP} of just 3 V up to 1.1 GHz[376].

Using diode-loaded a-IGZO TFTs Kawamure et al. showed a DC voltage of 5 V for an input V_{PP} of 20 V up to at least 25 MHz, demonstrating that diode-loaded a-IGZO TFTs are capable of rectifying at driving frequnecies significantly above the threshold of 13.56 MHz required for RFID purposes, while operating at sufficiently high voltage to power a display[377].

6.2.4 Data Storage

Data storage is also needed to create a fully integrated, wholly a-IGZO-based, electronic system. Consequently, recent work has focused on non-volatile a-IGZO memory. Suresh et al. and Zhang et al. both used charge storage in the dielectric to create multilevel memory. Suresh achieved this by doping a AlO_x gate dielectric with Pt nano-particles, which showed charge retention of the order of a few hours[378], while Zhang demonstrated a double layer of IGZO separated by a thin Al_2O_3 charge tunnelling layer, with charge retention of around 1 day[379]. Both systems essentially leverage the creation of charge trapping defects, discussed previously, to create hysteresis in the a-IGZO TFT behaviour, which is then used to store information.

Ferroelectric dielectric behaviour was utilised by van Breemen et al. for data storage (see sections II and III of the review from Petti et al. for discussion of ferroelectric behaviours[5]) showing a 16 × 16 IGZO TFT array using ferroelectric P(VDF-TrFE) gate dielectric, with retention times up to 12 days[380].

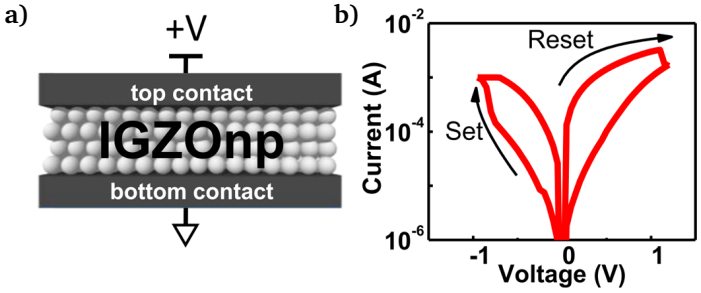

Fig. 18 a) schematic illustration of a memristor device and **b)** representative IV characteristics for the memristor set and reset processes. Reproduced from Rosa et al.[381]

Memristors have also been considered as a route to achieve stable data storage, as demonstrated by Rosa et al.[381] with solution processed a-IGZO, figure 18. Here conducting filaments were induced in the a-IGZO material during the writing phase, which were then disrupted during the reset phase. This system also showed data retention of the order of a few hours.

In addition to these and other emerging implementations of metal oxide memory, work is ongoing to create hybrid systems combining metal oxides with other existing technologies to meet memory requirements for many different applications. These are not discussed here but are covered well in recent reviews by Wong (looking at Metal-Oxide resistive switching RAM (RRAM))[382], Zhao (looking at high-*k* dielectric non-volatile memory)[383], Meena (looking at the general field of new non-volatile memory technologies)[384], and Sacchetto[385] and Mladenov[386] (looking at memristor technology).

6.2.5 RFID/NFC Communication

One of the most promising applications of a-IGZO outside of display technology is high volume, lost cost, and disposable wireless communications systems such as RFID/NFC tags[387]. As well as the low cost, tags based on a-IGZO benefit from their flexibility, allowing integration in packaging, clothing, and in multiple different form factors, as well as the potential for being non-visible, allowing integration into windows, mirrors, and food packaging[5]. Building on earlier designs for organic RFID tags[388–390], Ozaki et al. first demonstrated a fully a-IGZO based RFID tag working at 13.56 MHz in 2011[387,391], which has now been replicated by many other research groups on both rigid and flexible substrates, including fully transparent versions[169,392,393].

One remaining component of the RFID tag, not discussed above, is the load modulator. This is simply an additional TFT placed directly in the DC power supply line, with the RFID code encoded to the gate voltage, see figure 19. By modulating the gate of this TFT with the code, the DC supply is turned on and off, altering the power consumption of the tag and therefore the power harnessed by the tag's receiver coil. This modulation of the power consumption creates fluctuations in the electromagnetic field that can be interpreted by the RFID reader and decoded into the data to be transferred.

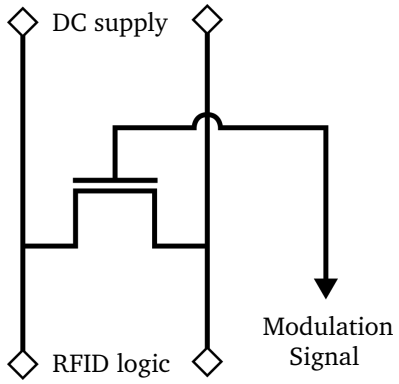

Fig. 19 Schematic illustration of the load modulator used to encode signal in RFID tags.

7 Conclusion

The aim of this review has been to provide an accessible overview of both the development of metal oxide electronics, in particular a-IGZO devices and the variety of applications to which a-IGZO is now being applied. It is clear that a huge volume of research and development work has been undertaken on these systems over the past 15 years, with significant advances in understanding of the fundamental physics and materials science of metal oxides, and their potential in applications across a wide variety of sectors. Importantly, this work shows an understanding of the current limitations of these semiconducting materials, particularly due to native and induced defects.

Many challenges remain, particularly in relation to the control of defects and device stability, which must be over come before a-IGZO, and metal oxide semiconductors in general, become wide spread in technology, but the further development and application of these materials for next generation electronics looks set to expand significantly.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This work is supported through a Knowledge Transfer Partnership, funded by Innovate UK, and by PragmatIC Printing Ltd.

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