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Amorphous-InGaZnO Thin-Film Transistors Operating Beyond 1 GHz Achieved by Optimizing the Channel and Gate Dimensions

Yiming Wang, Hanbin Wang, Jiawei Zhang, He Li, Gengchang Zhu, Yanpeng Shi, Yuxiang Li, Qingpu Wang, Qian Xin, Zhongchao Fan, Fuhua Yang, and Aimin Song, *Senior Member, IEEE*

Abstract—Amorphous indium-gallium-zinc oxide (a-InGaZnO or a-IGZO) has already started replacing amorphous silicon in backplane driver transistors for large-area displays. However, hardly any progress has been made to commercialize a-IGZO for electronic circuit applications mainly because a-IGZO transistors are not yet capable of operating at GHz frequencies. Here, nanoscale a-IGZO thin-film transistors (TFTs) are fabricated on a high-resistivity silicon substrate with a Ta₂O₅ gate dielectric. Carrier mobilities up to 18.2 cm²V⁻¹s⁻¹ have been achieved. By optimization of the TFT channel length and contact overlap, we are able to demonstrate current-gain and power-gain cut-off frequencies at 1.24 and 1.14 GHz, respectively, both beyond the 1 GHz benchmark. Such a performance may have implications in developing at least medium-performance, a-IGZO-TFTs-based circuits for low-cost or flexible electronics.

Index Terms—thin-film transistor, a-InGaZnO, high frequency, current gain

I. INTRODUCTION

HERE have been rapid developments in oxide semiconductors in the last decade [1], [2], [3]. One of the important aspects of most oxide semiconductors is that the electron mobility remains largely the same even when the semiconductor changes from crystalline to amorphous phase, because the isotropic s orbitals of metal atoms effectively overlap to form conduction band, in contrast to silicon. Polycrystalline silicon and single-crystal silicon can have high carrier mobilities from 50 to 1000 cm²V⁻¹S⁻¹. Cut-off frequencies beyond 2 GHz have been achieved in TFTs using mechanically transferred single crystalline silicon onto a polyethylene substrate [5], [6]. To the best of our knowledge, there has not been report on GHz TFTs based on amorphous silicon. This is because amorphous silicon has a carrier mobility greatly reduced from that of the crystalline silicon, typically only 1 cm²V⁻¹S⁻¹ or below. In contrast to amorphous

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Yiming Wang, Hanbin Wang, He Li, Gengchang Zhu, Yanpeng Shi, Yuxiang Li, Qingpu Wang, Qian Xin are with the Center of Nanoelectronics and School of Microelectronics, Shandong University, Jinan 250100, China (e-mail: xing@sdu.edu.cn).

Jiawei Zhang and Aimin Song are with the School of Electrical and Electronic Engineering, The University of Manchester, Manchester M13 9PL, U.K. (e-mail: A.Song@manchester.ac.uk).

Zhongchao Fan and Fuhua Yang are with the Engineering Research Center for Semiconductor Integration Technology, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China (e-mail: zcfan@semi.ac.cn; fhyang@semi.ac.cn). silicon, amorphous indium-gallium-zinc-oxide (a-IGZO), has drawn much attention due to its high mobility (typically 10 to 100 cm²/Vs), high transparency (> 80% in visible light region), mechanical flexibility, and high uniformity [7]. As such, a-IGZO has started replacing amorphous silicon in display backplane drivers. While most oxide semiconductors are *n* type, recent advances in *p*-type oxide semiconductors, such as SnO [8], [9], [10], [11] Cu_xO [12], [13] and NiO [14], [15], already resulted in fully oxide-based complementary logic gates [9], [16], [17] which are the fundamental building blocks towards large-scale integrated circuits (ICs). However, hardly any progress has been made in commercializing a-IGZO for ICs, largely due to the low operation frequencies of a-IGZO thin-film transistors (TFTs) to date.

Extensive efforts have been made in order to improve the speed of oxide-semiconductor-based TFTs [18], [19], [20], [21], [22], [23]. Single crystalline ZnO/ZnMgO TFTs on GaAs substrates showed a current-gain cut-off frequency, $f_{\rm T}$, of 1.75 GHz and a maximum oscillation frequency, f_{max} , of 2.45 GHz [24]. Nanocrystalline ZnO TFTs on high-resistivity silicon substrates have also demonstrated a high-frequency response ($f_T = 2.45$ GHz, $f_{max} = 7.45$ GHz) [21]. High performance was also achieved by depositing c-axis aligned crystalline IGZO on heated substrate using a sophisticated nanoscale 3D gating structure [25]. However, single crystalline materials require complex and expensive deposition technique and hence are usually incompatible with low-cost, large-area manufacturing. Nanocrystalline materials can suffer from low-yield issues due to the uncontrollable grain boundaries. In contrast, a-IGZO can be deposited by industrial-compatible, radio-frequency (RF) sputtering technique, and its amorphous nature ensures high uniformity and hence high yield in high-density IC manufacturing.

So far, a-IGZO TFTs using self-alignment or quasi-vertical fabrication processes on flexible substrates showed current-gain cut-off frequencies around 100 MHz [20], [26], [27], [28]. In 2015, a-IGZO TFTs with a gate length of 1.5 µm demonstrated an improved current-gain cut-off frequency of 384 MHz on glass substrates [18]. As frontend rectifiers, a-IGZO Schottky diodes on rigid and flexible substrates operating beyond a milestone value of 2.45 GHz have been reported [23], [29]. However, a-IGZO TFTs operating at GHz frequencies have not been demonstrated yet, making them unable to compete with ubiquitous silicon ICs that are typically clocked at a few GHz. In this work, by optimizing the topological structures and shot-channel effects, we demonstrate high-speed a-IGZO TFTs beyond the 1 GHz benchmark. The record f_T and f_{max} of 1.24 GHz and 1.14 GHz show the potential of using a-IGZO TFTs in transparent ICs

and microwave electronics.

II. EXPERIMENTAL PROCEDURE

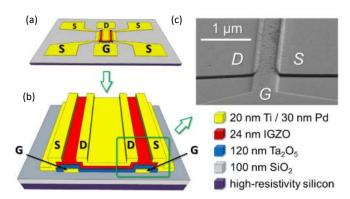


Fig. 1. Schematic illustrations and SEM image of the IGZO TFTs. (a) Schematic of the three-dimensional perspective view of the device layout. (b) Schematic of the cross-sectional perspective view of the device. (c) Tilt-view SEM image of the smallest TFT with $L_{\rm ch}$ = 360 nm and $L_{\rm ov}$ = 150 nm.

The devices were fabricated on high-resistivity (> 10 $k\Omega \cdot cm$) Si wafers coated with 100-nm-thick thermally oxidized SiO₂. Ti/Pd (20 nm/30 nm) gate electrodes were deposited using electron-beam evaporation. A 120-nm-thick Ta₂O₅ gate insulator was deposited by RF sputtering at room temperature (RT). The optimized deposition conditions for the Ta₂O₅ dielectric were as follows: the RF power, chamber pressure, Ar flow rate, and O₂ flow rate were maintained at 90 W, 1.73 mtorr, 6 sccm, and 3 sccm, respectively. A 24-nm-thick a-IGZO film was immediately sputtered after Ta₂O₅ without breaking the vacuum at an Ar flow rate of 20 sccm and RF power of 90 W. A 3" a-IGZO target was used with In₂O₃:Ga₂O₃: ZnO = 1:1:1 mol%. Ti/Pd (20 nm/30 nm) source and drain were formed using the electron-beam evaporator. Finally, a post-annealing was performed at 200 °C in air for 30 min to improve the electronic properties of IGZO [30], [31]. The patterning of sputtered Ta₂O₅ and a-IGZO layers was achieved by electron-beam lithography and lift-off process, which is more controllable than etching technique and involves fewer chemicals to cause potential contaminations.

III. RESULTS AND DISCUSSION

Figures 1(a) and (b) show the schematic diagrams of the TFT structure used in this work. A two-finger bottom-gate configuration was adopted. A ground-signal-ground (GSG) layout compatible with co-planar microwave probes was used as the contact pads for high-frequency characterizations. TFTs with different gate lengths were fabricated at the same condition. The dimensions of the TFTs were determined using scanning electron microscope (SEM). In Fig. 1(c), the SEM image of the TFT shows a channel length (L_{ch}) of 360 nm and an overlap length ($L_{ov} = L_{ov}$, GS + L_{ov} , GD, the sum of the gate-to-source and gate-to-drain overlap lengths) of 150 nm. Each device had two-finger gates with a width of 50 μ m resulting in a total gate width of 100 μ m. There are in total 12

devices with channel lengths of 360 nm, 750 nm, 1.2 µm, 5µm

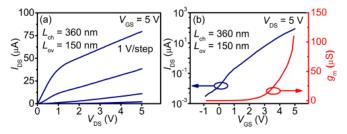


Fig. 2. (a) Output characteristics and (b) transfer characteristics of the smallest TFT with L_{ch} = 360 nm and L_{ov} = 150 nm.

and overlap lengths of 150 nm, 10 μ m, 20 μ m in order to systematically study the effects of the dimensions. As the most important parameter that describes the high-frequency properties of TFTs, the current-gain cut-off frequency in the first approximation is given by

$$f_{\rm T} = \frac{g_{\rm m}}{2\pi C_{\rm G}} \approx \frac{\mu_{\rm eff}(V_{\rm GS} - V_{\rm th})}{2\pi L_{\rm ch}(L_{\rm ch} + L_{\rm ov})},\tag{1}$$

where g_m is the transconductance, V_{GS} is the gate voltage, V_{th} is the threshold voltage, μ_{eff} is the effective mobility, and the gate capacitance, $C_{\rm G}$ is the sum of the gate-to-source, gate-to-drain, and gate-to-channel capacitances [32]. The effective mobility is extracted from the device transfer characteristics, which are realistic reflection of the effective gate modulation ability of the TFTs after considering the influence of the contact resistance, $R_{\rm C}$. As described in Eq. 1, it may appear that if reducing L_{ch} , a higher f_T can be obtained. However, in short-channel devices, μ_{eff} becomes lower than the a-IGZO intrinsic mobility, μ_0 , due to the contact resistance becoming more and more dominant with decreasing L_{ch} . It is critical to optimize L_{ov} in order to improve the cut-off frequency. While increasing L_{ov} reduces the contact resistance by gate-induced carriers at the contacts particularly in the linear transport region, which improves $f_{\rm T}$ [33], the parasitic overlap capacitance due to the overlap shall also have an adverse effect on $f_{\rm T}$ [26]. In this study, devices with various channel lengths (360 nm, 750 nm, 1.2 µm, and 5 µm) and overlap lengths (150 nm, 10 µm, and 20 µm) were fabricated.

The output and transfer characteristics of the smallest device $(L_{ch} = 360 \text{ nm}, L_{ov} = 150 \text{ nm})$ are shown in Figs. 2(a) and (b), respectively. The effective mobility, threshold voltage, and on/off current ratio were found to be 1.18 cm²V⁻¹s⁻¹, 1.84 V, and 4×10^4 for the smallest device, in comparison with 18.2 cm²V⁻¹s⁻¹, 2.84 V, and 1.4 \times 10⁶ for the largest device with $L_{ch} = 5 \ \mu m$ and $L_{ov} = 10 \ \mu m$. It is noted from the output characteristics in Fig. 2(a) that the device was not completely pinched off. This is due to the short-channel effect becoming more pronounced with decreasing channel length, which can be explained by the charge-sharing model and drain-induced barrier lowering [34], [35]. This effect is inevitable for short-channel thin-film- transistors. Nevertheless, the on/off ratio, 4×10^4 , is still sufficient for most logic applications, which typically requires an on/off ratio higher than 1000 [36]. In our experiment, the short-channel effect was observed in devices with $L_{\rm ch} < 1.2 \,\mu {\rm m}$.

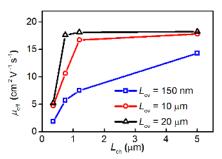


Fig. 3. Effective carrier mobility as a function of channel length for different gate-channel overlaps.

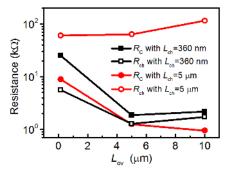


Fig.4 Channel resistance and contact resistance as a function of overlap length with channel lengths of 360 nm and 5 μ m at $V_{GS} = 5$ V and $V_{DS} = 5$ V, respectively. The results were obtained according to Ref. [4] by assuming the intrinsic field-effect mobility of IGZO being 18.2 cm² V⁻¹s⁻¹.

As shown in Fig. 3, the effective mobilities of the short-channel devices dropped sharply because the total resistance between source and drain is dominated by the contact resistance (R_c) rather than the channel resistance (R_{ch}). This is in contrast to long channel devices, where R_{ch} is much higher than $R_{\rm C}$. As a result, in short-channel devices, the effective carrier mobility is determined by both L_{ch} and L_{ov} as shown in Fig. 3. Based on Eq. (1), therefore, the improvement of TFT speed is non-trivial since all three key parameters (μ_{eff} , L_{ch} , and L_{ov}) are interplayed due to the influence of short-channel effect and contact resistance. When Lov is larger than the transfer length, $L_{\rm T}$, which describes the distance that 63% carriers flow from the semiconductor into the electrode [37], the contact resistance remains almost constant. However, when $L_{ov} < L_{T}$, the contact resistance becomes much larger, because it is determined not only by the overlap resistance region with a higher gate-induced carrier concentration [33], but also by a spreading resistance a-IGZO region which has a much lower intrinsic carrier concentration [32]. The contact resistances can be obtained in the linear region by parallel-mode capacitance-voltage method [38], but the drain contact resistance in the saturation region is expected to be much larger than the source contact resistance due to strong depletion. In Figure 4, when $L_{ch} = 360$ nm, the contact resistance is larger than the channel resistance, indicating a strong short-channel effect. When $L_{ch} = 5 \mu m$, the channel resistance remains almost the same but the contact resistance increases with decreasing L_{ov} , which makes the short-channel effect more pronounced for the device with L_{ov} of 150 nm. The smallest contact resistance is found to be 953 Ω , which is a typical Ti/IGZO contact resistance. Under this condition, the

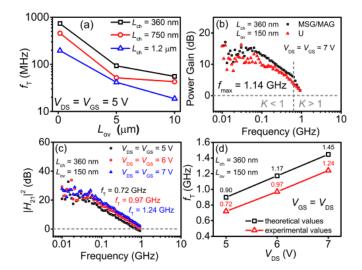


Fig. 5 High-frequency properties of IGZO TFTs. (a) Current-gain cut-off frequency as a function of overlap length of the devices with channel lengths of 0.36 μ m (black line), 0.75 μ m (red line) and 1.2 μ m (blue line), respectively. (b) Maximum available gain, maximum available gain, and unilateral power gain of the smallest TFT at $V_{\rm DS} = V_{\rm GS} = 7$ V. MAG exists when stability factor K > 1. (c) Small-signal current gain H₂₁ as a function of frequency of the smallest TFT at different $V_{\rm DS}$ and $V_{\rm GS}$. (d) Simulated $f_{\rm T}$ compared with experimental results of the smallest TFT.

effective mobility can be expressed as:

$$\mu_{\rm eff} = \frac{F_0}{1 + \mu_0 C_{\rm ox} \, W(V_{\rm GS} - V_{\rm th}) F_{R_C} / L_{\rm ch}},\tag{2}$$

where C_{ox} is the dielectric unit capacitance, and F_{R_c} is a function of L_{ov} , describing the total contact resistance [26].

Considering the effective mobility as well as the parasitic capacitance caused by the overlap length, the current-gain cut-off frequency is given by [26]:

$$f_{\rm T} = \frac{\mu_0 C_{\rm ox} W (V_{\rm GS} - V_{\rm th})}{2\pi (C_{\rm ox} L_{\rm ch} + C_{\rm ox} L_{\rm ov}) \left(L_{\rm ch} + \mu_0 C_{\rm ox} W F_{R_c} (V_{\rm GS} - V_{\rm th}) \right)}, (3)$$

It shows that the cut-off frequency is affected by both parasitic-capacitance-dependent term, $C_{\rm ox}L_{\rm ov}$, and contact-resistance-dependent term, $g_{\rm m0}F_{R_c}$. Thus, in order to improve the high frequency performance in short-channel devices, it is necessary to experimentally evaluate the influence of each factor.

The small-signal RF characterizations of the TFTs were measured from 0.01 to 1 GHz with an input power of -10 dBm by using a vector network analyzer connected to a two-channel source-measure unit through bias tees. Cut-off frequencies, including $f_{\rm T}$ and $f_{\rm max}$, can be extracted from the current gain, H₂₁, maximum stable gain, MSG, maximum available gain, MAG, and unilateral power gain, U, which can all be calculated from S-parameters. The measured current gain, H₂₁, describes the ratio of RF output current, I_{out}, to RF input current, I_{in} , which is a function of transconductance and operating frequency [39]. The current-gain cut-off frequency, $f_{\rm T}$, of a transistor is defined as the frequency at which the magnitude of H₂₁ approaches unity [39]. The maximum frequency of oscillation is defined as the frequency at which the unilateral power gain equals unity. Figure 5(a) shows the $f_{\rm T}$ of the TFTs as a function of $L_{\rm ov}$ with $L_{\rm ch}$ of 0.75 µm and 1.2 um, respectively. It is found that the cut-off frequency increases with a decreasing L_{ov} , indicating that for short-channel devices, parasitic capacitance caused by L_{ov}

significantly influences the frequency response. Thus, in this work, the TFT with the shortest L_{ov} of 150 nm and L_{ch} of 360 nm is expected to exhibit the highest operation frequency.

Figures 5 (b) and (c) show the small-signal microwave characteristics of the smallest TFT. The current gain H_{21} curves, at a slope of -20 dB/decade as expected [40], showed cut-off frequencies of 0.72 GHz, 0.97 GHz, and 1.24 GHz at $V_{DS} = V_{GS} = 5$ V, 6 V, and 7 V, respectively. In Fig. 5(c), MSG (stable factor K < 1) and MAG (K > 1) are also shown as a function of frequency. The maximum oscillation frequencies extracted from both MAG and U are the same, both at 1.14 GHZ, as shown in Fig. 5(b). The good agreement between the f_{max} obtained from MAG and U suggests that the total measured capacitance is dominated by the device capacitance [41]. According to Eq. 1 and the measured effective mobilities shown in Fig. 4, the theoretical $f_{\rm T}$ can be obtained. As shown in Fig. 5(d), the theoretical values are also in a good agreement with the experimental results. The slight differences may arise from the self-heating effect and/or the extra cable and probe resistance from the measurement setups.

To further analysis the relationship between capacitance, channel length and overlap length. Capacitance extracted from s-parameter measurement using a vector network analyzer after calibration based on equations (4), (5) and (6).

$$S_{11} = \Gamma = \frac{\hat{Z}_T - Z_0}{Z_T + Z_0'}$$
(4)

$$Z_T = Z_0 \frac{1 - S_{11}}{1 + S_{11}},\tag{5}$$

$$C = -\frac{1}{2\pi f * Imag(Z_T)'} \tag{6}$$

Here Γ is reflect factor, Z_T is transfer impedance, Z_0 is characteristic impedance, S is s-parameter and C is total gate capacitance. As shown in Fig. 6, the parasitic capacitance is found to mainly depend on overlap length.

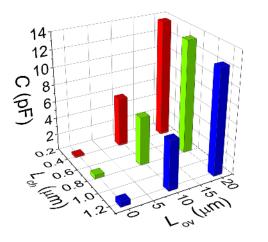


Fig.6 Capacitance as a function of device dimensions extracted from s-parameter measurements.

IV. CONCLUSION

In summary, we have demonstrated a record speed beyond 1 GHz of a-IGZO TFTs. Despite of the use of non-flexible, opaque silicon substrate, our demonstrated device

performance could well be transferred to low-cost, flexible substrates such as polyimide. This work may also have useful implications to improvement of operation speed of other oxide- and organic-based TFTs. With the rapid development of *p*-type oxide semiconductors in the last few years, similarly fabricated GHz *p*-type TFTs may be integrated to realise high-performance, fully oxide-based complementary logic gates for a range of electronics applications.

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Yiming Wang was born in Jinan, Shandong province, in 1980. He received the B.S. degree in Physics and Microelectronics from Shandong University in China in 2002, M.S. degree in Physics from Shandong University in 2009. He is working toward the Ph.D. degree in microelectronics and solid state electronics from Shandong University,

Jinan. His research focuses on metal oxide semiconductor, two-dimensional materials and devices, high frequency devices.



Hanbin Wang received the B.S. and M.S. and Ph.D. in School of Microelectronics, Shandong University, Jinan, China, in 2010, 2013 and 2017, respectively. He is now working in the Micro-Nano Technology Lab, Microsystem & Terahertz Research Center in Chengdu, China. His research interests include Terahertz nanoelectronics and Micro-nano technology on compound semiconductor.

Third J. Zhang received the B.S. degree in physics from Shanghai Jiaotong University, Shanghai, China, in 2010, the M.S. degree in photon science, and the Ph.D. degree in electronics from the University of Manchester, Manchester, UK, in 2012 and 2016 respectively.

Since 2016, he has been a Research Assistant with the School of Electrical and Electronic Engineering, the University of Manchester. His research interest includes the oxide semiconductors, thin-film transistors, high-frequency electronics and 2D materials.



Li He received the B.S. degree in microelectronics from Shandong University, Jinan, Shandong, in 2013 and the M.S. degree in microelectronics and solid-state electronics from Shandong University, Jinan, Shandong, in 2016.

From 2013 to 2016, he studied at Center of Nanoelectronics, Shandong University, Jinan, Shandong, China. His research

interest includes devices based on III-V and amorphous metal oxide semiconductor, and fabrication of micro- or nanostructured semiconductor devices.



Gengchang Zhu is currently studying for the Ph.D degree in microelectronics and solid state electronics at Shandong University, Jinan, China. His research interests include fabrication and applications of GaN HEMTs.



Yuxiang Li received the B.S. and M.S. degrees in polymer chemistry in 1988 and 1991, respectively, and the Ph.D. degree in material physics and chemistry in 2007 from Shandong University (SDU), Jinan, Shandong, China.

She is currently a Professor with the School of Microelectronics at SDU. In 1991, she joined the Institute of Optoelectronic Materials & Devices, SDU, and has been an Assistant Professor in 1994 and Associate Professor in 1997, respectively, working in the new-type cleaning techniques of electronic industry. Since 2008, she has been a Professor with the School of Physics, where she studied new non-volatile memory devices. She authored and coauthored technical papers, and holds five patents.



Prof. Li is an Associate Editor of the journal *European Physical Journal – Applied Physics*.

Qingpu Wang: Date of birth: September, 1963; he received B.S. degree and M.S. degree both in Physics from Shandong University (SDU), Jinan, China, in 1987 and 1998, respectively; and the Ph.D. degree in Condensed Matter Physics from Shandong University (SDU), Jinan, China, in 2003.



Since July 1987, he has been with the Department of Physics of SDU. From January 2013 to May 2016, he was working in School of Information Science & Engineering Shandong University. From May to today 2016, he was working in School of Microelectronics Shandong University, and works as Vice Dean. From March to May, 2006, he was

a Senior Visiting Scholar in the Department of Electronic Engineering, University of Manchester in UK.

Prof. Wang is the author or co-author of more than 50 journal and conference papers. He is a member of Chinese Physical Society and Shandong Physical Society; He is the reader of Journal of Semiconductor, Chinese Physics Letter, and Journal of Chinese Physics B etc. His current research interests include semiconductor material and device etc.



Qian Xin was born in Shandong Province, China in 1982. She received B.S. and Ph.D. degrees in Material Science at Shandong University, China, in 2003 and 2008, respectively. From 2009 to 2012, she was a Postdoc in surface and Interface science at Chiba University, Japan. Since 2012, she has been an associate professor in the School of Microelectronics, Shandong

University. Her research interests include metal oxide semiconductors, flexible electronics and displays, and surface and interface electronic structure studies by photoemission spectroscopy.



Aimin Song (M'02-SM'07) received the Ph.D. degree from the Chinese Academy of Sciences in 1995.

After three years of fellowships at the University of Glasgow and the University of Munich by the Royal Society and Alexander von Humboldt Foundation, he was with the Nanometre Consortium, Lund University, as

a Guest Lecturer before moving to Manchester as a Lecturer in 2002. He became a Professor of nanoelectronics in 2006. His research is focused on novel nanoelectronic devices and thin-film electronics. Dr. Song's work has led to awards including "Researcher of the Year" Distinguished Achievement Medal of the University of Manchester, Royal Society Brian Mercer Feasibility Award, and a number of best conference paper awards. The potential of practical applications of the nanodevices for printable electronics and energy harvesting have motivated а number of commercialization activities including 15 patents/patent applications and a spin-out company.