EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN/EF 89-9 Rev.
6 September 1989

AMPLEX
A LOW-NOISE, LOW-POWER ANALOG CMOS SIGNAL PROCESSOR FOR MULTI-ELEMENT SILICON PARTICLE DETECTORS

Eric Beuville[3a], Kurt Borer[1], Enrico Chesi[3], Erik H.M. Heijne[3],
Pierre Jarron[3], Bohdan Lisowski[3b] and Simon Singh[2]

Presented by: P. Jarron

1 Laboratorium für Hochenergiephysik, Universität Bern, Switzerland
2 Cavendish Laboratory, University of Cambridge, UK
3 CERN, EF Division, 1211 Geneva 23, Switzerland
a Permanent address: Université de Strasbourg, France
b Permanent address: Institute of Phys. of Polish Academy of Sciences

ABSTRACT

AMPLEX is a monolithic analog signal processor fabricated in 3 μm n-well CMOS and originally designed for the inner silicon detector of the UA2 Experiment at the CERN SPS Collider. However, it is suitable for various other types of detectors, and results are also given for a MultiWire Proportional Chamber (MWPC). The chip contains 16 channels, each consisting of a charge amplifier, a shaper amplifier and a track–and–hold stage. The channel outputs are connected to an analog multiplexer which is controlled by digital circuitry. For a power consumption of 1 mW per channel and an adjustable peaking time of 600 to 800 ns, the equivalent noise charge is 400 r.m.s. electrons plus 33 r.m.s. electrons per pF of input capacitance. The DC stabilisation of the charge amplifier is obtained using a non-linear feedback resistor. This novel MOS element is a key feature of the design and enables low noise as well as DC stability of the charge amplifier, even for increased detector leakage current up to several hundred nA. Such operating conditions can occur following radiation damage of silicon pad detectors.

Presented at the 5th European Symposium on Semiconductor Detectors
21–23 February 1989, Munich, Germany

[Proceedings published by Nucl. Instr. and Methods]

1. INTRODUCTION

The need for full custom ASICs for front–end electronics was first felt in connection with silicon microstrip detectors. However, it now becomes feasible to apply monolithic CMOS Integrated Circuits (ICs) for reading out signals in a whole variety of detectors used in particle physics. The AMPLEX chip [1] is one of the first of this kind, and is designed in a 3 μm n–well CMOS process, which is available commercially(*) . CMOS full custom design offers the unique possibility to trade–off different design parameters to meet particular specifications. The main trade-offs are noise against power, speed against power, and noise against speed. The detector capacitance, which is often a given constraint in the detector sytem, determines the speed and noise performance for a specific biasing condition.

For the AMPLEX design applied to silicon detector readout in the UA2 inner detector [2], there are two key specifications. The first is the power consumption, which is limited to 1 mW per channel (3 W for the entire detector system), because cooling of a detector system around the beam pipe is very difficult in a collider experiment. The second is the signal processing time which should be between 600 and 800 ns to be compatible with the cycling time of 3.5 μs of the CERN $p\bar{p}$ collider [2]. This value of the processing time is also the result of a trade–off; the noise caused by the detector leakage current increases for increasing processing time, while the electronic noise contribution of the charge amplifier circuit decreases with increasing time. With these specifications, and for a total input capacitance of 20 pF, an Equivalent Noise Charge (ENC) referred to the input of the charge amplifier of ~ 1000 r.m.s. electrons could be obtained.

The AMPLEX design is presented in sect. 2. It differs from several other, recent analog front–end chips in its application of DC coupling and in being continuously sensitive to input signals (asynchronous operation mode). Both features rely on a special MOS feedback resistor. The main issues in the design of this non–linear and low–noise MOS resistor are discussed in sect. 3. In sect. 4 the experimental characteristics of the AMPLEX chip are presented. The noise performance is discussed in sect. 5 and in particular it is shown theoretically and experimentally that noise can be reduced by the application of a potential between bulk (or n-well) and the source. A brief comparison with front–end electronics of the synchronous type is made in sect. 6.

(*) Mietec N.V., Oudenaarde, Belgium.

2. AMPLEX CHIP ARCHITECTURE AND PRINCIPLES

The schematic of AMPLEX in fig. 1 shows the charge amplifier stage which is directly connected (DC) to the silicon pad detector, the shaper or filter amplifier, followed by the track–and–hold, and the analog multiplexer.

The analog circuit design of the charge amplifier and the shaping amplifier is based on the continuous time filtering technique. The charge amplifier, built around a transconductance amplifier (POTA), uses a resistive feedback element R_f, to stabilize its DC operating point like in traditional discrete component charge amplifier circuits. The shaper amplifier is constructed around a second transconductance amplifier NOTA. Semi–gaussian shaping is used to optimize the noise performance. The track–and–hold circuit stores the pulse height of the amplified and filtered output pulse signal, if a properly–timed external hold signal is applied. This stage has a storage capacitor, C_h , a switch SWH and a unity gain buffer amplifier. Figure 2 illustrates the response of the readout system.

The analog multiplexer consists of a simple array of switches SWM 1 to SWM 16 connected to the analog bus line "Analog Out". The digital control of these switches is performed by means of the signals "Clear", "Clock–in" and "Clock–out", allowing for a daisy–chain configuration of several AMPLEX chips. The maximum number of chips (channels) per analog readout line depends on the allowed readout time, the signal voltage droop during the readout sequence and the leakage current of the multiplexer switches. It may well be up to 32 chips (512 channels) if a fast ADC system is used.

In a multilevel trigger system the switches SWH enable to return from the hold mode into the track mode without executing the readout sequence, thus making the system sensitive to a new event within ~ 1 µs after a negative trigger decision.

2.1 Design of the charge amplifier stage

The transconductance amplifier POTA is a building block for the charge amplifier of AMPLEX. It uses the principle of the folded cascode stage introduced for charge amplification by V. Radeka [3]. The input device (M1 in fig. 3) is a p–channel MOS transistor with a large W/L = 5000/3 to achieve low–noise performance, both by reducing the flicker noise contribution and by increasing the transconductance g_m. The transistor is operating close to weak inversion, with a drain current of 50 µA providing a transconductance $g_m \cong 1.4$ mA/V. The open loop DC gain is 66 dB, and the dynamic range is ±3 V for $V_{DD} = -V_{SS} = 5$ V.

The transconductance stage POTA is configured in the AMPLEX architecture as a charge amplifier and has a rise time constant, T_{rise}, which can be calculated according to the following expression:

$$T_{rise} \cong (C_{in}/C_f)(C_{load}+C_f)/g_m, \text{ with } C_{in} = C_{gsi} + C_{det}\,, \qquad (1)$$

where $C_{gsi} \cong 10$ pF is the capacitance from gate to source of the input transistor, C_{det} is the detector capacitance, C_f is the feedback capacitor (1 pF) and $C_{load} \cong C_{diff}$ the output loading capacitance.

Using the actual values of capacitors and bias current, the rise time calculation gives $T_{rise} \sim 200$ ns. This is, in fact, one of the poles of the continuous time filter embedded in the charge amplifier stage. The measured impulse response of the charge amplifier agrees with this calculation.

The detailed CMOS circuit configuration is shown in fig. 3. The amplifier part consists of the folded cascode stage. M1 is the low–noise, p–channel input transistor, M2 is a current source which is degenerated to reduce its noise contribution and M5 is the cascode device. The output current source consists of the stacked current mirror made up of transistors M3 and M4. The bias current I_{bias} (POTA) which controls the transconductance can be varied between 10 and 100 µA via an external resistor (see also fig. 1). The external voltage V_{Gf} controls the feedback resistor and will be discussed in sect.3.

2.2 Filter, track–and–hold and multiplexer stage

The filtering scheme shown in fig. 4 is based on the well–known CR–$(CR)^n$ principle. The values of the filtering parameters are given in table 1. The four main integrating time constants are produced by R_{fS} C_{fS}, the time constant of the track–and–hold, and the dominant poles p1 and p2 of the POTA and NOTA stages. The value of these time constants is between 150 and 200 ns. Differentiation is achieved by the interstage coupling capacitor C_{diff} (7 pF) which isolates the shaping amplifier from DC fluctuations of the charge amplifier introduced by variations in the detector leakage current. C_{diff} contributes to the dominant pole of the charge amplifier stage and determines therefore the rise time given in expression (1).C_{diff} is the dominant component of the output loading capacitance C_{load}. The two integrating time constants embedded in NOTA and POTA and the diferentiating time constant can independently be adjusted by tuning the transconductances g_{m1} and g_{m2} via external resistors. Figure 5 illustrates the frequency response of the filter for the biasing conditions I_{bias} (POTA) = 50 µA and I_{bias} (POTA) = 100 µA.

Figure 6 shows the MOS circuit diagram of the filter and track–and–hold amplifier. The transconductance amplifier NOTA has also a folded cascode configuration, with an n–channel input transistor M1 with ratio W/L = 2000/3 working in weak inversion for minimum power consumption at a given transconductance. The unity gain buffer of the track–and–hold stage consists of a source follower matched with the input device in order to achieve an output offset close to zero. This matching is performed by an

appropriate current mirroring which imposes an identical current density in the transistors M1 and M13.

2.3 Layout considerations

Figure 7 shows a picture of the AMPLEX chip. The die size is 4.1 x 4 mm^2. The layout of each channel is a long rectangle which is compatible with the pitch of the input pads of 200 μm. The biasing parts of the transconductance amplifiers POTA and NOTA are common to all channels and are located along the edge of the chip.

The large input transistors have a waffle iron topology, as used in MOS power transistors. This geometry reduces the parasitic resistances and capacitances associated with the source, drain and gate. Figure 8 gives the equivalent circuit of the MOS transistor, including r_D and r_S, the series drain and source resistances. These parasitic elements reduce the transconductance of the MOS transistor, so that the effective transconductance g_m becomes

$$g_m = g_{mi}\,[1 - g_{DS}\,(r_S + r_D)]/(1 + g_{mi}\,r_S)\ , \qquad (2)$$

where g_{mi} is the ideal transconductance and g_{DS} the drain to source conductance. By using the waffle structure, the effective transconductance g_m can be made almost identical to the ideal transconductance.

3. THE NON–LINEAR LOW–NOISE MOS RESISTOR

The AMPLEX design is based on the continuous time filtering technique for both the charge amplifier and shaper amplifier. Since many years this technique is generally used in low–noise charge–amplification circuits fabricated with discrete components [3]. In monolithic CMOS design it is difficult to integrate a large low–noise resistor. Although it is theoretically possible to use a lightly doped polysilicon layer, this approach is generally not possible in commercial CMOS processes. Moreover, a linear resistor of 10 to 100 MΩ, would not solve the problem in the case of a detector with a large leakage current as this would cause a baseline shift large enough to saturate the preamplifier stage.

To overcome this difficulty, a non–linear MOS element has been used which consists of an n–channel MOSFET operating from weak to strong inversion in the linear region. Figure 9 shows the feedback configuration which offers low–noise performance as well as DC stabilisation of the charge amplifier. To maintain the feedback transistor in the linear region, the source is connected to the output and the drain to the amplifier input. Therefore, the drain voltage of the feedback resistor, V_{Df}, is equal to the input voltage V_{in} of the POTA stage. In first–order approximation V_{in} is regarded equal to the threshold voltage of the POTA input transistor, $V_{To} \cong -0.8$ V, under the condition that the bulk

source voltage $V_{BS} = 0$ V. A transistor is in the linear operating region if the drain and source voltages never exceed the pinch–off voltage [4]. Hence linear operation occurs if

$$V_{Sf}, V_{Df} < (V_{Gf} - V_{To})/n \tag{3}$$

is always satisfied. Note that V_{Gf} is the gate voltage, V_{To} is the threshold voltage of the transistor and n is the slope factor [4]. The circuit configuration of the feedback transistor is like in a common gate stage, because the transistor is controlled by the source. But the electrical behaviour of this transistor is equivalent to that of a resistor R_{eq} since it is working in the linear region. A simplified analysis of the MOS transistor operating in strong inversion and in the linear region gives the expression for the drain current,

$$I_D = \mu C_{ox} (W/L) \ (V_{Df} - V_{Sf}) \ [V_{Gf} - V_{To} - (V_{Df} + V_{Sf}) \ n/2] \ , \tag{4}$$

where μ is the carrier mobility in the MOS channel, C_{ox} is the normalized gate capacitance, W/L is the gate aspect ratio and V_{Sf} is the source voltage of the transistor. This particular circuit configuration has the following node equations for a positive I_D:

$$V_{out} = V_{Sf} = V_{in} + R_{eq} I_D, I_D = -I_{leak} \text{ and } V_{in} \cong V_{To} \ . \tag{5}$$

Using expressions (4) and (5) the value of equivalent resistor R_{eq} is a function of the current I_D

$$R_{eq} = V_{To} / [\mu C_{ox} (W/L) \ (V_{Gf} - V_{To}) / n + I_D / 2] \ . \tag{6}$$

One may also express the equivalent conductance G_{eq} as a function of I_D,

$$G_{eq}(I_D) = G_o + \Lambda I_D \ , \tag{7}$$

where the conductance G_o for $I_{leak} = 0$ is

$$G_o = \mu C_{ox}(W/L) \ (V_{Gf} - V_{To}) / nV_{To} \tag{8}$$

and

$$\Lambda \cong 1 / (2 V_{To}) = dG / d I_{leak} \tag{9}$$

is the slope of the conductance variation as a function of the leakage current, when the device operates in strong inversion. The interesting feature of this non–linear device as feedback resistor is its capability to adjust its equivalent resistance value if the leakage current varies such that the base line of the charge amplifier is automatically stabilized.

Figure 10 shows the experimental results obtained with a test chip. For an aspect ratio $W/L = 3/180$ of the MOSFET device, the term dG/dI is found to be practically 1 Siemens per Ampere in the strong inversion region; the value of the equivalent conductance is 50 nS, or in terms of equivalent resistance R_{eq} = 20 MΩ for V_{Gf}–V_{To} = 0.3 V. This value is in good agreement with the calculations of eq. (6), using known parameters of the CMOS device.

In the weak inversion region ($I_D < 10$ nA), the previous analysis is no longer valid. As shown in fig. 10, the equivalent feedback conductance, in this case, decreases exponentially to zero and not to G_0. This property is interesting in terms of the noise performance, because for low leakage currents this non–linear resistor reaches a very large value, in the order of GΩ, and then contributes very little noise to the amplifier.

The noise contribution of the current dependent conductance term ΛI_D can be calculated as expressed by Van der Ziel, by its noise power density [5],

$$S_{ng} = 4\, kT\, \Lambda\, I_D \quad , \tag{10}$$

where k is the Boltzmann constant and T is the operating temperature. The power density of the detector leakage current shot noise is

$$S_{ni} = 2q\, I_{leak} \quad , \tag{11}$$

The ratio $S_{ng}/S_{ni} = (kT/q)\, V_{To}$ is ~ .025. Therefore, the noise contribution of the conductance is negligible compared with the shot noise contribution of the detector leakage current. No excess noise has been observed.

4. EXPERIMENTAL RESULTS

4.1 Electrical measurements

The measurement of the signal amplification and noise characteristics are performed by injecting a known charge through a test capacitor at the inputs. Table 2 summarizes the electrical characteristics of the measured chips. Measured were output offset voltage, overall charge gain, linear dynamic range, peaking time, noise at $C_{det} = 0$ and noise slope expressed in ENC [r.m.s. electrons].

The spread in gain is attributed to the non–homogeneity of the capacitor oxide thickness over the wafer which affects the value of capacitors C_f and C_{diff}. The impact on system performance from this technological imperfection has been limited by accepting only chips with a gain within ± 3% of nominal value. This selection was performed as part of the wafer probing test procedure.

The spread in offset is due to the non–homogeneity of the MOSFET threshold voltage and topology variations on the die. This has been found acceptable for the UA2 Experiment , because the readout system uses offset subtraction.

Linearity was found to be better than 2% for an output dynamic range of ± 400 mV, which is equivalent to the signal generated by 20 MIPs (Minimum Ionizing Particles) traversing a 300 μm Si detector. The intrinsic dynamic range of the transconductance amplifier is much larger, but the limitation is due to the poor performance of the source follower used as a buffer in the track–and–hold stage.

As shown in fig. 11 the adjacent crosstalk is negligible while there is a global crosstalk of –1%, proportional to the total charge received by the chip. The origin of this effect is not yet understood. The measurement on channel 8 was done by completely removing the wire bonds from the on–chip pads for the inputs 6, 7 and 9, 10 to avoid additional crosstalk introduced via the test board.

A major limitation of DC coupling of the detector to the amplifier is usually a base line shift of the charge amplifier due to the detector leakage current. This difficulty has been overcome in AMPLEX by using the non–linear MOS resistance as feedback resistor of the charge amplifier, as discussed in sect. 3. Figure 12(a) shows the gain decrease as a function of the detector leakage current, which is –10% at 400 nA. Figure 12(b) shows how the detector leakage current degrades the pulse shape at 10 and 400 nA, at the same time decreasing the gain by a ballistic deficit of the pulse height.

Power and peaking time tuning is demonstrated in fig. 13(a) which shows how the peaking time varies with the bias current. This tuning is not done exactly at constant gain, as shown in fig. 13(b), because of the variation of the transconductance with the bias.

4.2 AMPLEX in connection with silicon detectors

The first application of the AMPLEX circuit has been as signal processor for the inner silicon detector array of the UA2 Experiment at the CERN SPS Collider. A detailed description is given elsewhere in these proceedings by Ansari et al., [2]. The effective detector capacitance at the input corresponds to 20 pF, so that a typical noise performance of 1000 electrons r.m.s. is obtained, as mentioned in table 2. The present AMPLEX circuit has been designed to correspond optimally to the UA2 requirements, in particular, regarding signal speed, readout time, number of channels per chip and power dissipation.

In full custom design it is relatively simple to adjust the AMPLEX characteristics to different detector parameters. But, even in its present form AMPLEX could be used with a variety of detectors.

4.3 Test with a gaseous detector

In the frame of the development of a fast Ring Imaging Cherenkov detector (RICH), a Multi–Wire Proportional Chamber (MWPC) is used to detect Cherenkov UV photons via their conversion into single electrons in an appropriate gas mixture (methane + TEA) [6]. A bidimensional localization is realized by measuring the induced signals of the avalanche in the cathode "pads" of 8 x 8 mm^2 size.

The MWPC had 256 pads equipped with 16 AMPLEX chips, connected to a fast multiplexing readout card called DRAMS [7]. Figure 14 shows a pulse height distribution of typical exponential shape, measured at the pads. The signals originated from a single electron extracted at the cathode by the photo–electric effect. The minimum detectable charge and the mean value of this distribution are respectively 1.2 fC and 10 fC, providing a detection efficiency for single electrons close to 100%. The noise charge was 850 electrons r.m.s. (0.14 fC). Cherenkov rings were observed, with on average 8 photo–electrons per ring detected at the pads.

5. NOISE CONSIDERATIONS

Charge amplification for particle detectors requires low–noise performance in order to detect charge signals in the fC range. The limiting factor in CMOS technology is the flicker noise of the drain current generated by interface state traps under the gate oxide. To find the best approach in the CMOS technology used to fabricate AMPLEX, a test chip containing large p–channel and n–channel MOS transistors was used for preliminary investigation of the noise performance.

Figure 15 shows the measured spectral noise power density for p–channel and n–channel transistors with a W/L ratio of 11 000/3, and biased at 1 mA drain current. In first approximation, the flicker noise is usually given by the following noise power expression,

$$S_V = A_f / f^a \quad , \tag{12}$$

where f is the frequency in Hertz, and a is a constant close to 1.

The noise constant A_f, which is the value of the noise power at 1 Hz is found experimentally to be equal to 9×10^{-13} and 3×10^{-14} [V^2/Hz] for n–channel and p–channel devices respectively. A ratio of 30 exists in favour of the p–channel MOSFET, which makes this device the better candidate for a low–noise input device for the CMOS charge amplifier.

A noise source not often taken into account in the noise modelling of a MOS transistor is the thermal noise contribution originating from the bulk resistance of the n–channel and the well resistance of the p–channel devices. Jindal has proposed a model for this noise contribution for short–channel NMOS devices [8]. This analysis can also be used for a p–channel transistor in CMOS technology, as shown in the noise model fig. 16. One introduces the bulk (or well) transconductance g_{mB} in addition to the usual transconductance g_m. The resulting transconductance seen from the source is then

$$g_m + g_{mB} = n.g_m$$

with the slope factor n, approximated in weak inversion by $n \cong 1 + C_{dep}/C_{ox}$, where C_{dep} [9] is the depletion capacitance from channel to bulk. The thermal noise contribution of R_B can be referred to the gate as a noise voltage source with noise power [9],

$$S_{VB} = 4\,kT\,R_B\,(g_{mB}/g_m)^2 = 4\,kT\,R_B\,(n-1)^2 \quad . \tag{13}$$

This analysis enables to see that the best noise performance is obtained by biasing the well in such a way that the source–well voltage is large enough to significantly decrease the bulk transconductance and the factor n and therefore make negligible the bulk noise contribution.

Together with the channel white noise we obtain,

$$S_{VB} + S_{VD} = 4\,kT\,[R_B\,(n-1)^2 + (2/3)\,\Gamma/g_m] \quad , \tag{14}$$

where Γ is the excess noise factor.

Figure 17 shows the noise spectral power density measured in the p–channel device for source voltages $V_{BS} = 0$ V and 5 V. The corresponding noise values found at 100 kHz are 4.8 and 1.8 nV/$\sqrt{\text{Hz}}$. With the bulk bias, the total white noise is practically limited to the drain conductance noise, given by the second term of the expression (14).

The noise spectral density measured at 100 kHz is not flat. This is probably due to some remaining flicker noise which, in fact, diverges slightly from the simple 1/f law [10].

Figure 18 gives the noise measured as a function of the detector capacitance. The value of the noise slope is 33 r.m.s. electrons or 0.005 fC per pF, and agrees fairly well with the ENC slope in fC given by the expression calculated for a RC-CR^2 from Radeka [11],

$$ENC / C_{det} = \left[(e^4/64)\,4\,kT\,(2/3)\,\Gamma/g_m\,\tau\right]^{1/2} \tag{15}$$

with $g_m = 1.4$ mA/V, the transconductance of the low–noise input p–channel device for $I_{bias} = 50$ µA, and the filter time constant $\tau = 350$ ns of the CR–RC^2 filter.

In conclusion, a p–channel MOS transistor operating in weak inversion, employed as input device for the charge amplifier, achieves a good noise performance and low–power consumption. In the latter respect, a junction FET is less favourable. The factor Γ has been calculated to be 1.4 for p–channel MOS, which is a small noise penalty compared to the noise performance of a JFET transistor for which $\Gamma = 1$.

6 DISCUSSION

ASICs developed for the read–out of silicon microstrip particle detectors have been recently designed using the switched capacitor technique [12–15] which is an alternative for continuous feedback. The reset of the charge amplifier is performed by using an auto–zeroing switch across the charge feedback loop. A synchronous clock closes this switch periodically in order to reset the charge stored in the feedback capacitor. This technique is simple but it has some limitations. The switching action of the auto–zero operation causes charge injection via clock feed–through at the input of the charge amplifier. As a result, a large dynamic offset shifts the base line of the charge amplifier stage. A second dynamic offset can occur if the charge amplifier is DC connected to a leaky silicon pad detector. In this case the droop rate slope given by,

$$dV_{out}/dt = -I_{leak} / C_f \tag{16}$$

is visible at the output. For instance, with $C_f = .5$ pF and $I_{leak} = 500$ nA, after 1 μs of integration the shift reaches 1 V, which easily brings the charge amplifier stage in saturation. Finally, the need to synchronize the reset clock with the arrival time of particles to be detected, limits the field of application of the auto–zeroing technique with correlated double sampling filter to situations where the particles to be detected are not random but predictible.

The continuous time filtering technique discussed in this paper is more flexible because the signal processor is continuously sensitive and does not rely on external controls. In the present architecture only the track–and–hold control signal must be given from an external source Such a signal could also be provided internally.

After four months of operation in the CERN $p\bar{p}$ Collider, no measureable degradation of performance of AMPLEX has been observed, although silicon detectors have had a strong degradation of their leakage current caused by radiation damage [16].

Acknowledgements

The authors wish to acknowledge P. Darriulat, L. di Lella, O. Gildemeister, C. Gössling from CERN and A. Clark from FNAL for their encouragement and support; C. Das, L. Folens and B. de Mey from IMEC for the MPC organization and layout verification.

REFERENCES

[1] E.H.M. Heijne and P. Jarron, Proceedings of 14th Europ. Solid-state Circuits Conference (ESSCIRC 1988), Manchester, UK (1988) 66-69.

[2] R. Ansari et al., Successful operation of a new Si-pad detector with ASIC read–out at the CERN $p\bar{p}$ Collider, Nucl. Instr. and Methods, these proceedings.

[3] V. Radeka, State of the art of low–noise amplifier, proceedings of the Versailles Conferences (1969).

[4] E. Vittoz, Design of MOS VLSI circuits, in Circuits for Telecomunications, Editor I. Tsividis, Prentice-Hall (1985) 111.

[5] A. Van der Ziel, Noise: sources, characterisation, measurement, Englewood Cliffs, NJ: Prentice-Hall (1970).

[6] E. Chesi et al., Fast rich detector using a MWPC at atmospheric pressure with a pad structure read–out by VLSI circuits, presented at the Wire Chamber Conference, Vienna (February 1989), submitted to Nucl. Instr. and Methods.

[7] E. Chesi et al., DRAMS, a digital, read–out for multiplexed systems, internal note CERN/JETSET/EP (1988).

[8] R. P. Jindal, Distributed substrate resistance noise in fine line NMOS field-effect transistors, IEEE Trans. El. Dev., ED-32 (1985) 2450 (and private communication).

[9] H. Nyquist, Thermal agitation of electric charge in conductors, Phys. Rev. 32 (1928) 110.

[10] V. Radeka, 1/f noise in charge measurement, Nucl. Instr. and Meth., these proceedings.

[11] V. Radeka, Low–noise preamplifiers for nuclear detectors, Nucleonics (July 1965) 55.

[12] J. Walker et al., Development of high density read–out electronics for silicon strip detector, Nucl. Instr. and Meth.226 (1984) 200.

[13] W. Buttler, et al., Low–noise low–power monolithic multiplexing read–out electronics for silicon strip detectors, Proceedings Intern. Europhysics Conference on High–energy Physics, Uppsala (June 1987).

[14] P. Seller, A CMOS integrated circuit for silicon strip detector read–out, Proceedings ESSCIRC 1987, Berlin, VDE-Verlag (1987) 281.

[15] S. Kleinfelder et al., A flexible 128–channel silicon strip detector instrumentation integrated circuit with sparse data readout, IEEE Trans. Nucl. Sci. NS-35 (1989) 171.

[16] E. Beuville et al., Measurement of degradation of silicon detectors and electronics in various radiation environments, Nucl. Instr. and Methods, these proceedings.

TABLE 1

Amplifier characteristics

POTA	NOTA
Transconductances	
$g_{m1} \approx q\, I_{bias}$ (POTA) / n kT = 2.5 mA/V	$g_{m2} \approx q\, I_{bias}$ (NOTA) / n kT = 1.0 mA/V
DC open loop gain	
$A_{o1} = - g_{m1}/g_{o1} \approx 1500$	$A_{o2} = - g_{m2}/g_{o2} \approx 1000$
Input resistance	
$R \approx 1/g_{m1}\, C_f/(C_f + C_{diff}) \approx 3.0\ k\Omega$	
Poles	Integrating time constants
$p1 = g_{m1}/2\,\pi\, C_{diff}$	$\tau_1 = (1/p1)(C_{det} + C_f)/C_f$
$p2 = g_{m2}/2\,\pi\, C_h$	$\tau_2 = (1/p2)(C_{diff} + C_{fS})/C_{fS}$
$p3 = 1/2\,\pi\, R_{fS}\, C_{fS}$	$\tau_3 = R_{fS}\, C_{fS}$
$p4 = 1/2\,\pi\, R_{SWH}\, C_h$	$\tau_4 = R_{SWH}\, C_h$
Filter input resistance	Differentiating time constant
$R_{diff} = (1/g_{m2})\,(C_h + C_{fS})\,/\,C_{fS}$	$\tau_{diff} = R_{diff}\, C_{diff}$ $C_{diff} = 7$ pF

TABLE 2

Summary of characteristics of AMPLEX

Gain	5 mV/fC for $C_{det} = 20$ pF 18 mV/min. ionizing part. in 300 µm Si detector (MIP)
Gain uniformity	2% within chip, 5% from chip to chip
Gain versus C_{det}	0.6% gain decrease per pF
Noise	ENC 1000 r.m.s. electrons for $C_{det} = 20$ pF
Linearity	Better than 2% integral up to 70 fC input charge (corresponds to ~ 20 MIP)
Output DC offset	+ 15 mV
Offset spread	± 10 mV
Output Droop rate	< 20 mV/s
Maximum acceptable detector leakage current	450 nA
Power consumption	1.1 mW per channel for biasing conditions: $I_{bias\ (POTA)} = 50$ µA, $I_{bias\ (NOTA)} = 10$ µA
Peaking time	750 ns

FIGURE CAPTIONS

Fig. 1 Overall schematic of the 16–channel AMPLEX chip.

Fig. 2 Output response in track–and–hold mode: (a) is the input step voltage for input charge injection; (b) is the signal pulse produced at the output of the shaper amplifier; (c) output signal with a hold control signal applied at the peaking time of the output pulse (700 ns).

Fig. 3 CMOS circuit configuration of the charge amplifier with POTA including its biasing circuits. The external voltage V_{Gf} controls the feedback resistor.

Fig. 4 The various components which enter into the CR–RC^n filter scheme, as implemented in AMPLEX. The switch SWH has an on–resistance of R_{SWH}. The values of the filtering parameters can be found in table 1.

Fig. 5 Gain as a function of frequency for the combined charge amplifier and shaping amplifier, measured respectively for I_{bias} (POTA) of 50 µA and 100 µA and I_{bias} (NOTA) of 10 µA and 20 µA.

Fig. 6 CMOS circuit configuration of the filter amplifier with NOTA and the following track–and–hold, and multiplexer stages.

Fig. 7 Picture of the 16–channel AMPLEX chip. The size is 4.1 x 4 mm^2.

Fig. 8 Equivalent circuit of a MOS transistor showing the parasitic resistances.

Fig. 9 Principle of the CMOS circuit configuration for charge amplification, providing DC stabilisation of the charge amplifier and cancellation of the detector leakage current effect. $V_{Df} = V_{in}$ and $V_{Sf} = V_{out}$. A bias voltage V_{Gf} is applied to the gate.

Fig. 10 Experimentally measured equivalent conductance as a function of I_{leak} of the non–linear MOS resistor with an aspect ratio W/L = 3/180 as used in AMPLEX design for different applied V_{Gf}.

Fig. 11 Measurement of the crosstalk; channel 8 is the stimulated input. The input leads to channels 6, 7, 9 and 10 were disconnected on the chip. Otherwise some cross–talk via the board interconnections would appear.

FIGURE CAPTIONS (Cont'd)

Fig. 12 (a) Measurement of the gain as a function of the detector leakage current.

(b) Influence of the detector leakage current on the gain and pulse shape. The upper trace is the response for I_{leak} = 10 nA, the lower for I_{leak} = 400 nA.

Fig.13 (a) Dependence of the peaking time on the power consumption, which can be adjusted via the bias currents.

(b) Variation of the gain as a function of the power.

Fig.14 Pulse height distribution for single electrons detected at the pads of a MWPC cathode. The average pedestal width in r.m.s. (not shown) is 0.45 ± 0.05 ADC bins, equivalent to 850 electrons (0.14 fC).

Fig. 15 Experimental results of the spectral noise power density of n–channel and p–channel MOS transistors with an aspect ratio W/L = 11 000/3 and biased at a drain current value of 1 mA. The well or bulk bias V_{BS} was 5 V.

Fig. 16 Noise model of the MOS transistor including the contribution of the thermal noise from the distributed resistor R_B in the well or in the bulk.

Fig. 17 Experimental spectral noise–power density measured with a p–channel transistor W/L = 11 000/3, for n–well biasing voltages: V_{BS} = 0 V and V_{BS} = +5 V. The drain current was 1 mA.

Fig. 18 Equivalent noise charge of AMPLEX measured as a function of the external detector capacitance to which stray capacitance of 10 pF is added. The noise at the origin comes mainly from the parasitic capacitances of the input transistor in parallel with the feedback capacitance, with a combined value ~ 10 pF.

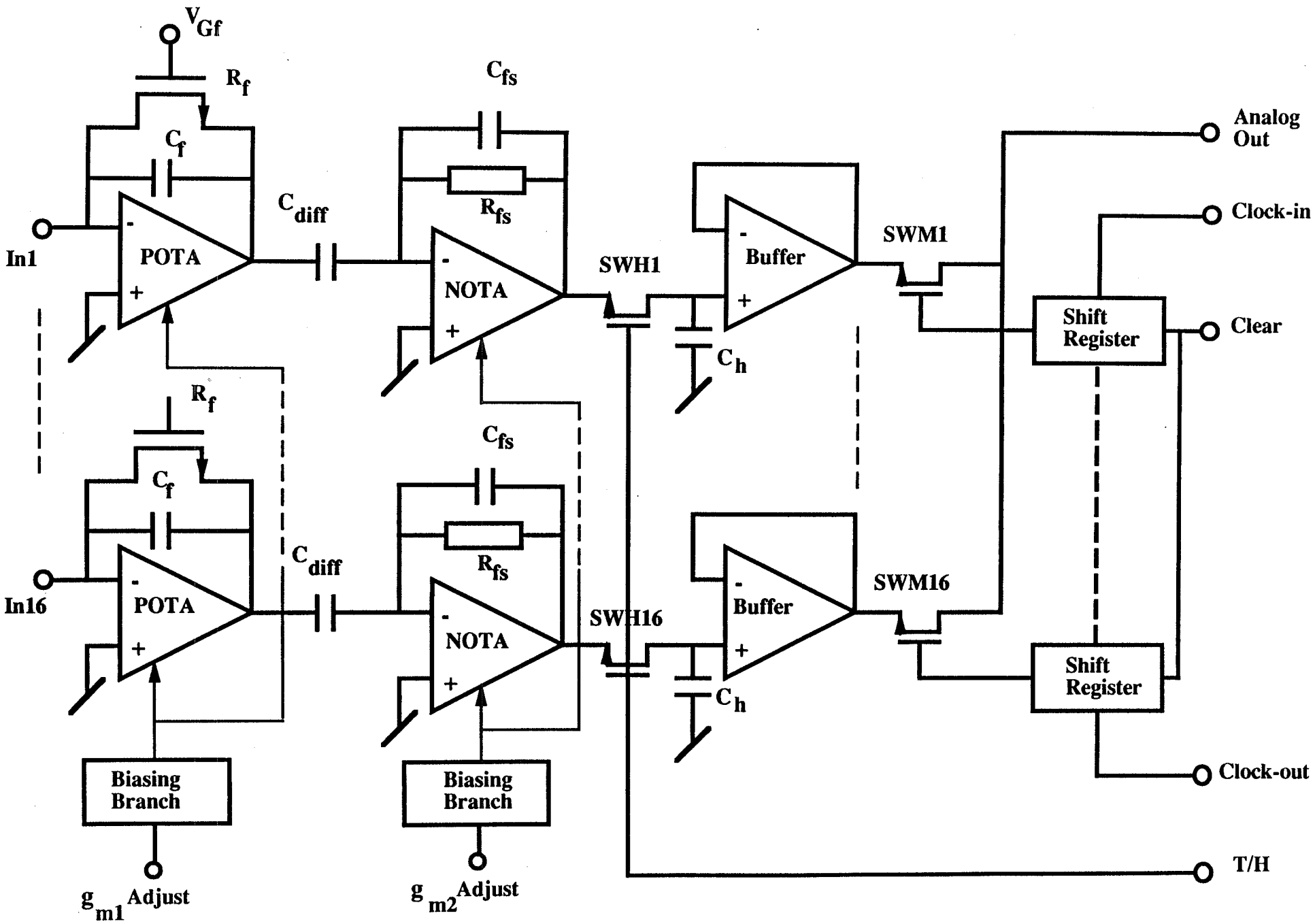

V_{Gf}
R_f
C_f
C_{diff}
C_{fs}
R_{fs}
In1
POTA
NOTA
Buffer
SWH1
SWM1
C_h
Analog Out
Clock-in
Clear
Shift Register
In16
SWH16
SWM16
Biasing Branch
g_{m1} Adjust
g_{m2} Adjust
Clock-out
T/H

Fig.1

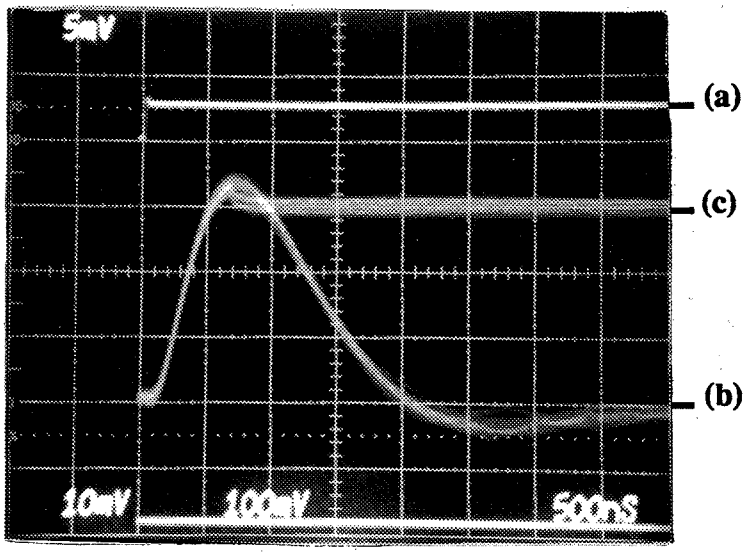


Fig. 2

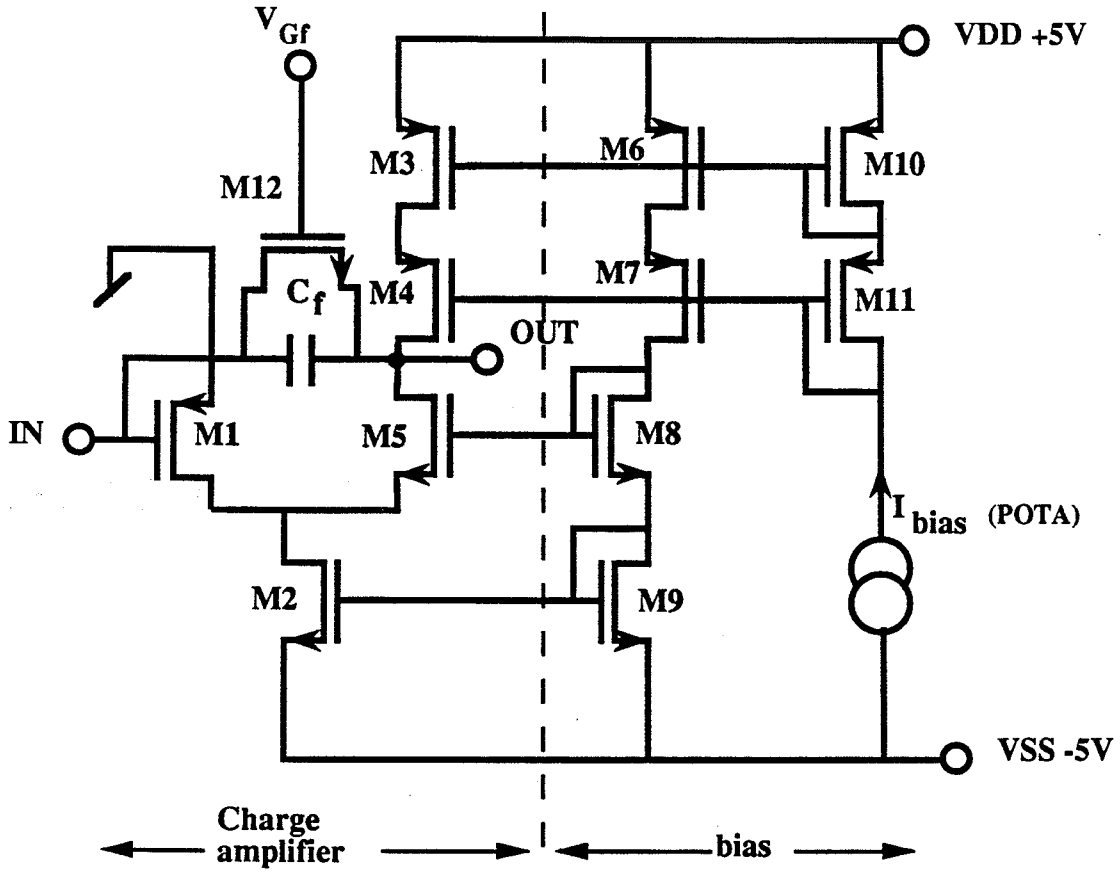

V Gf
VDD +5V
M12
M3
M6
M10
C f
M4
M7
M11
OUT
IN
M1
M5
M8
I bias
(POTA)
M2
M9
VSS -5V
Charge amplifier
bias

Fig. 3

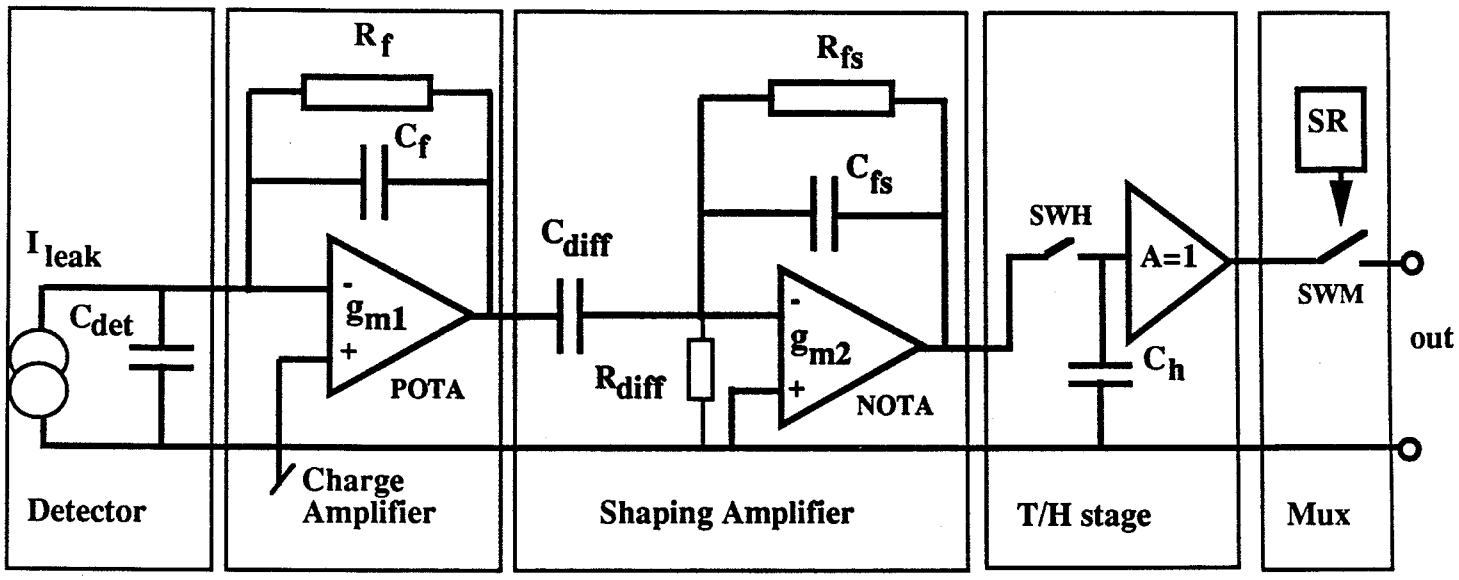

R_f
C_f
R_fs
C_fs
I_leak
C_det
C_diff
R_diff
g_m1
POTA
g_m2
NOTA
SWH
A=1
C_h
SR
SWM
out
Detector
Charge Amplifier
Shaping Amplifier
T/H stage
Mux

Fig. 4

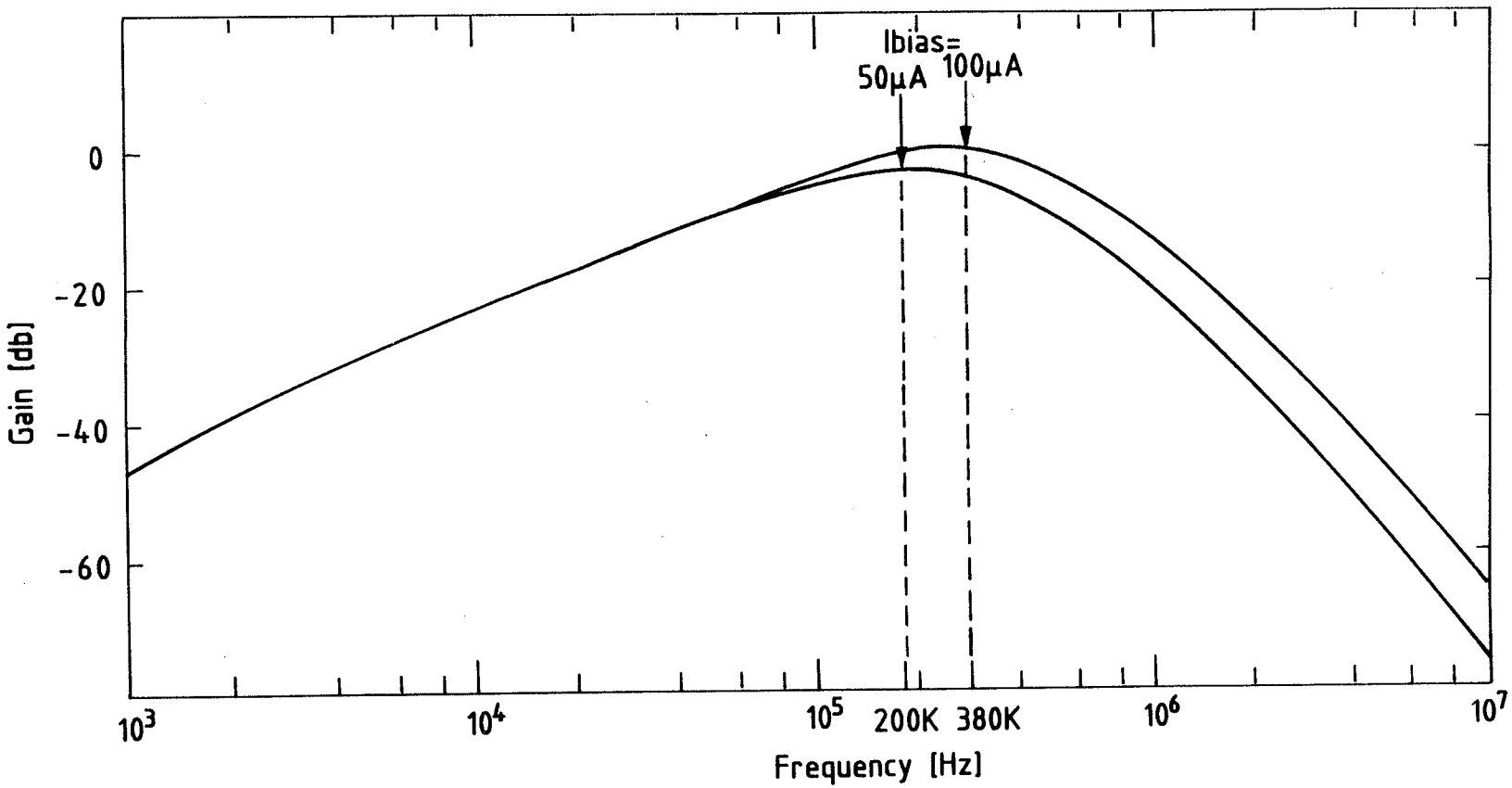

Ibias=
50μA
100μA
0
-20
-40
-60
Gain [db]
10^3
10^4
10^5
200K
380K
10^6
10^7
Frequency [Hz]

Fig. 5

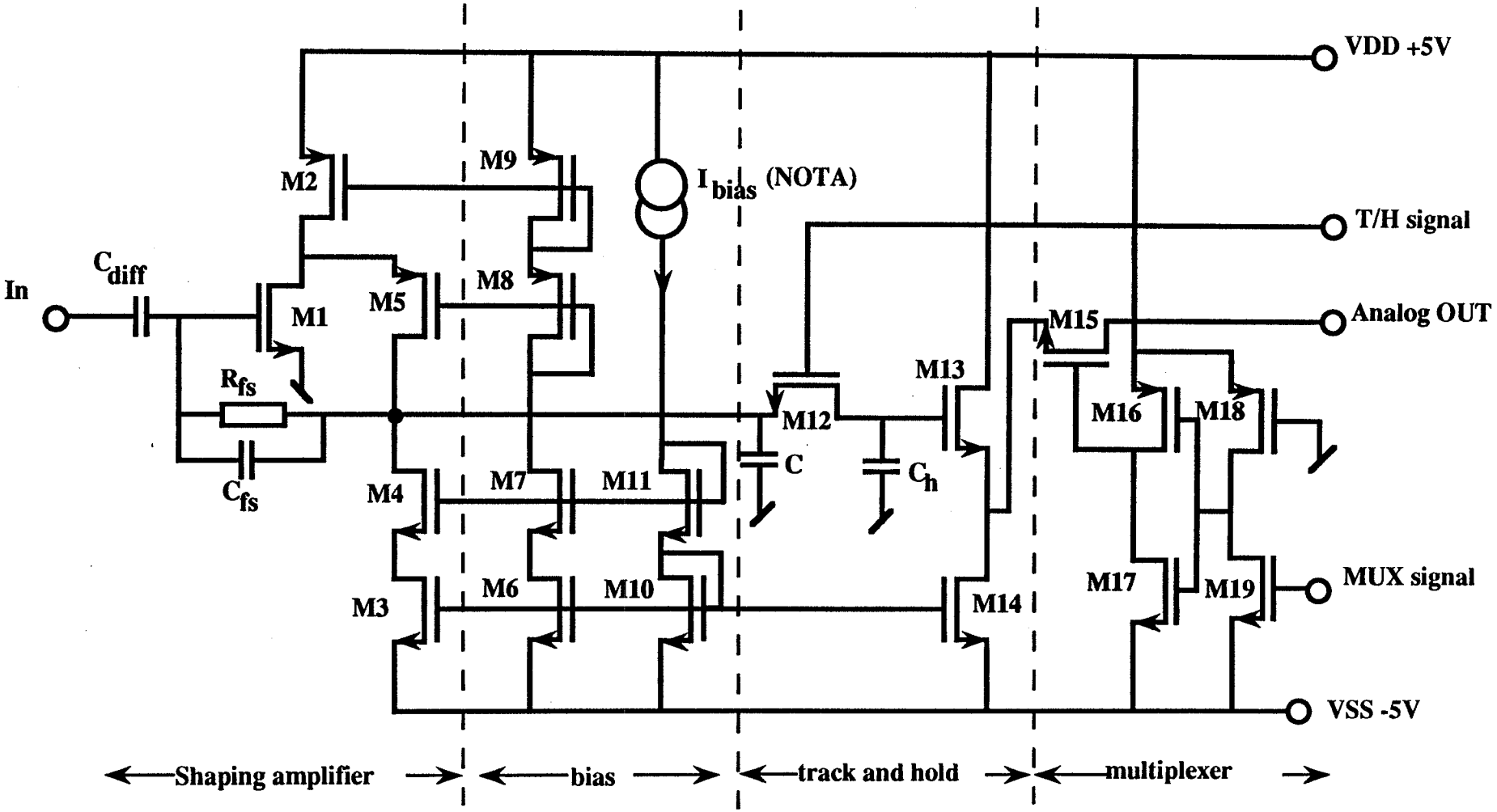

VDD +5V
T/H signal
Analog OUT
MUX signal
VSS -5V
In
C_{diff}
R_{fs}
C_{fs}
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
I_{bias} (NOTA)
C
C_h
Shaping amplifier
bias
track and hold
multiplexer

Fig. 6

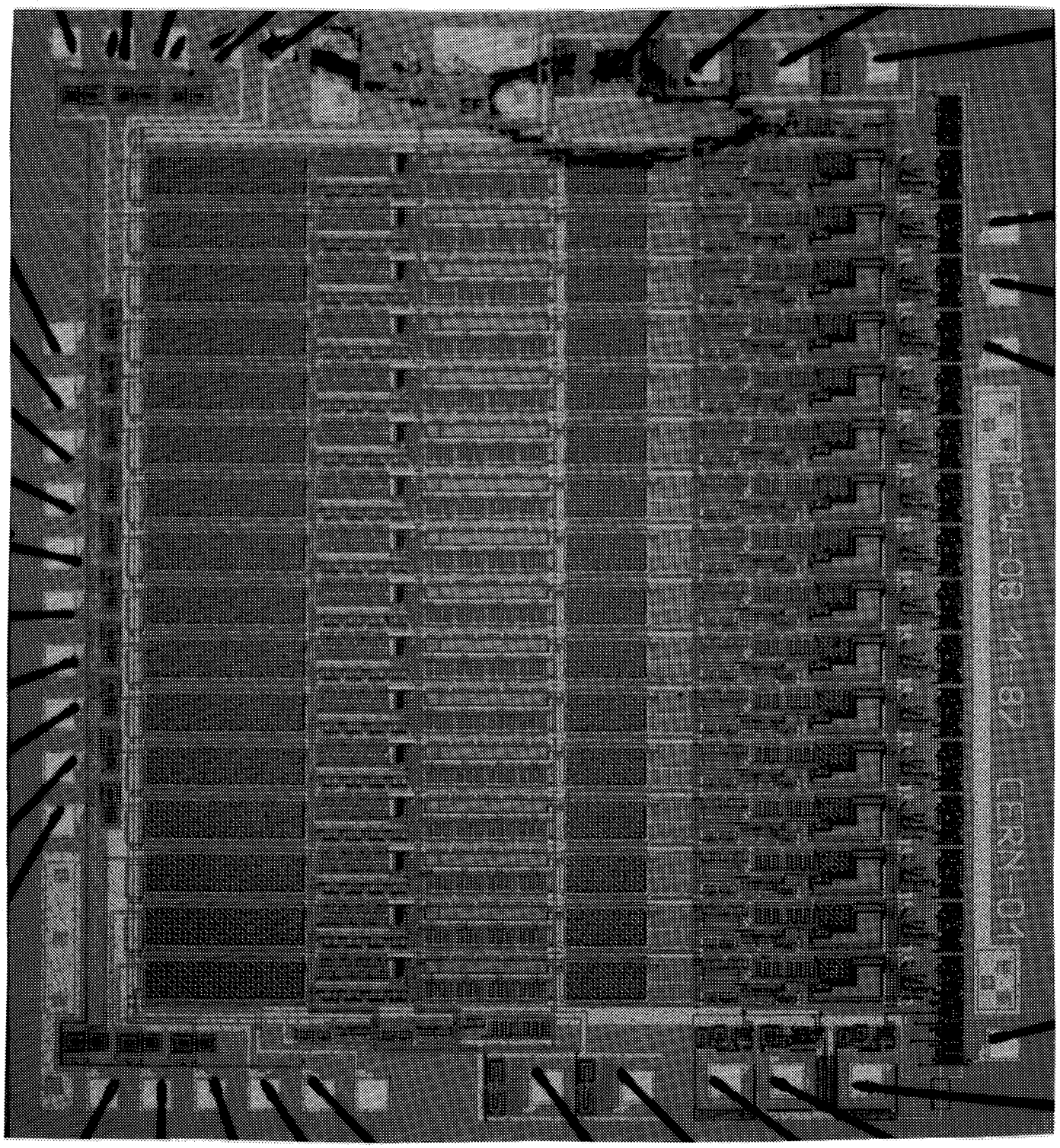
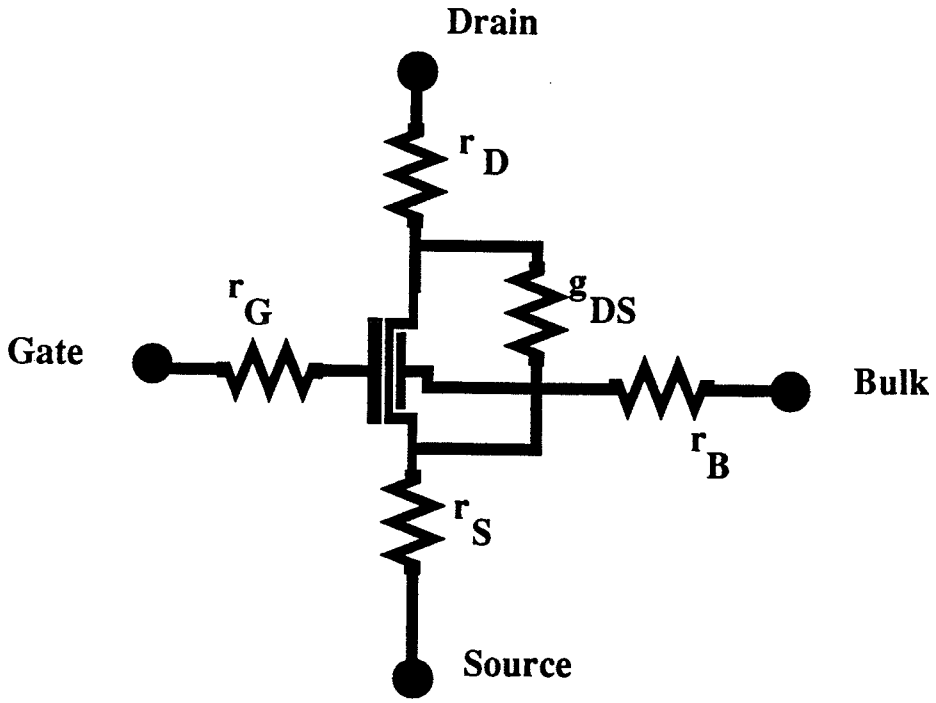
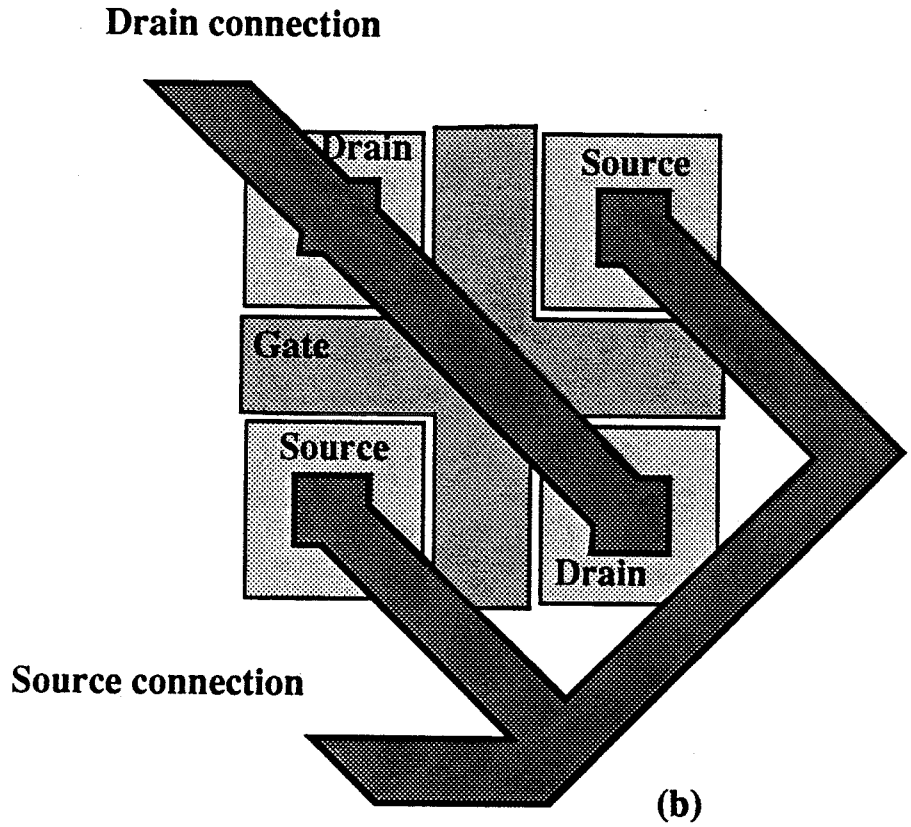


Fig. 7


Drain
r_D
r_G
g_{DS}
Gate
Bulk
r_B
r_S
Source

(a)


Drain connection
Drain
Source
Gate
Source
Drain
Source connection

(b)

Fig. 8

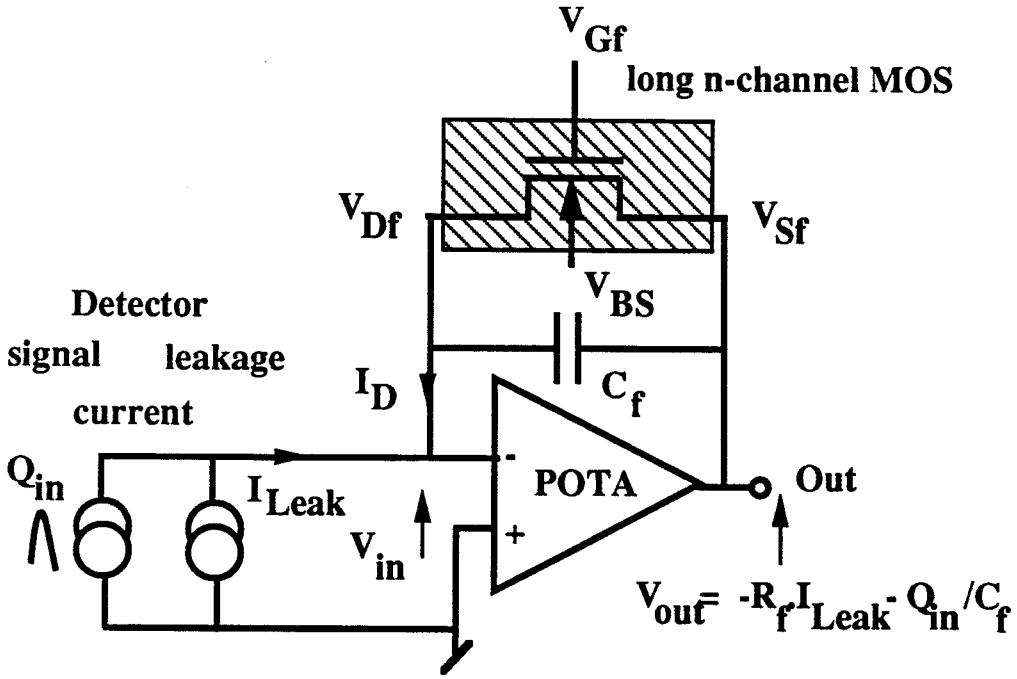

V_{Gf}
long n-channel MOS
V_{Df}
V_{Sf}
V_{BS}
Detector
signal leakage
current
I_D
C_f
Q_{in}
I_{Leak}
POTA
Out
V_{in}
$V_{out} = -R_f I_{Leak} - Q_{in}/C_f$

Fig. 9

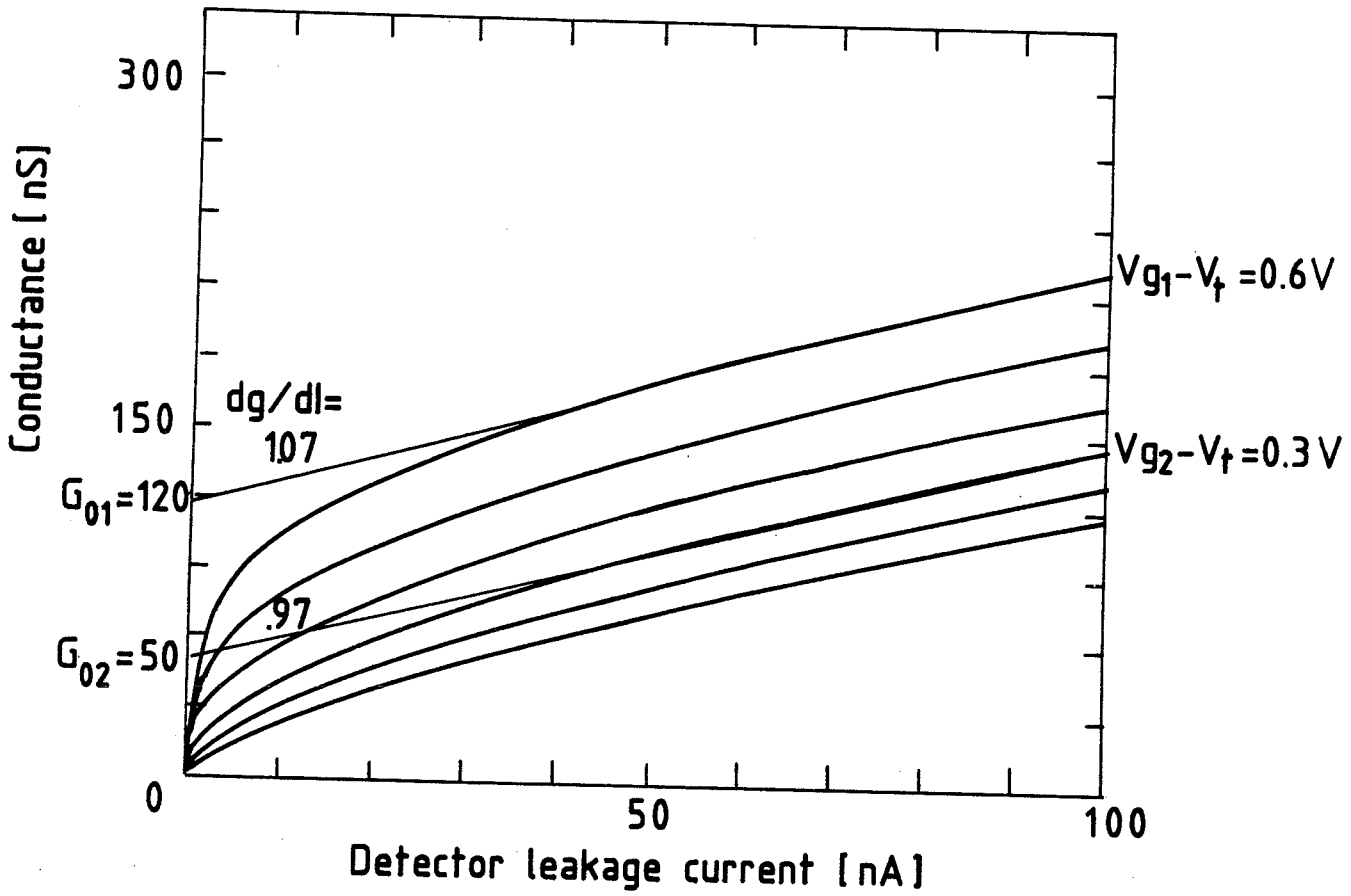

300
150
0
Conductance [nS]
dg/dI=
107
.97
G_{01}=120
G_{02}=50
Vg_1-V_t =0.6V
Vg_2-V_t =0.3V
50
100
Detector leakage current [nA]

Fig. 10

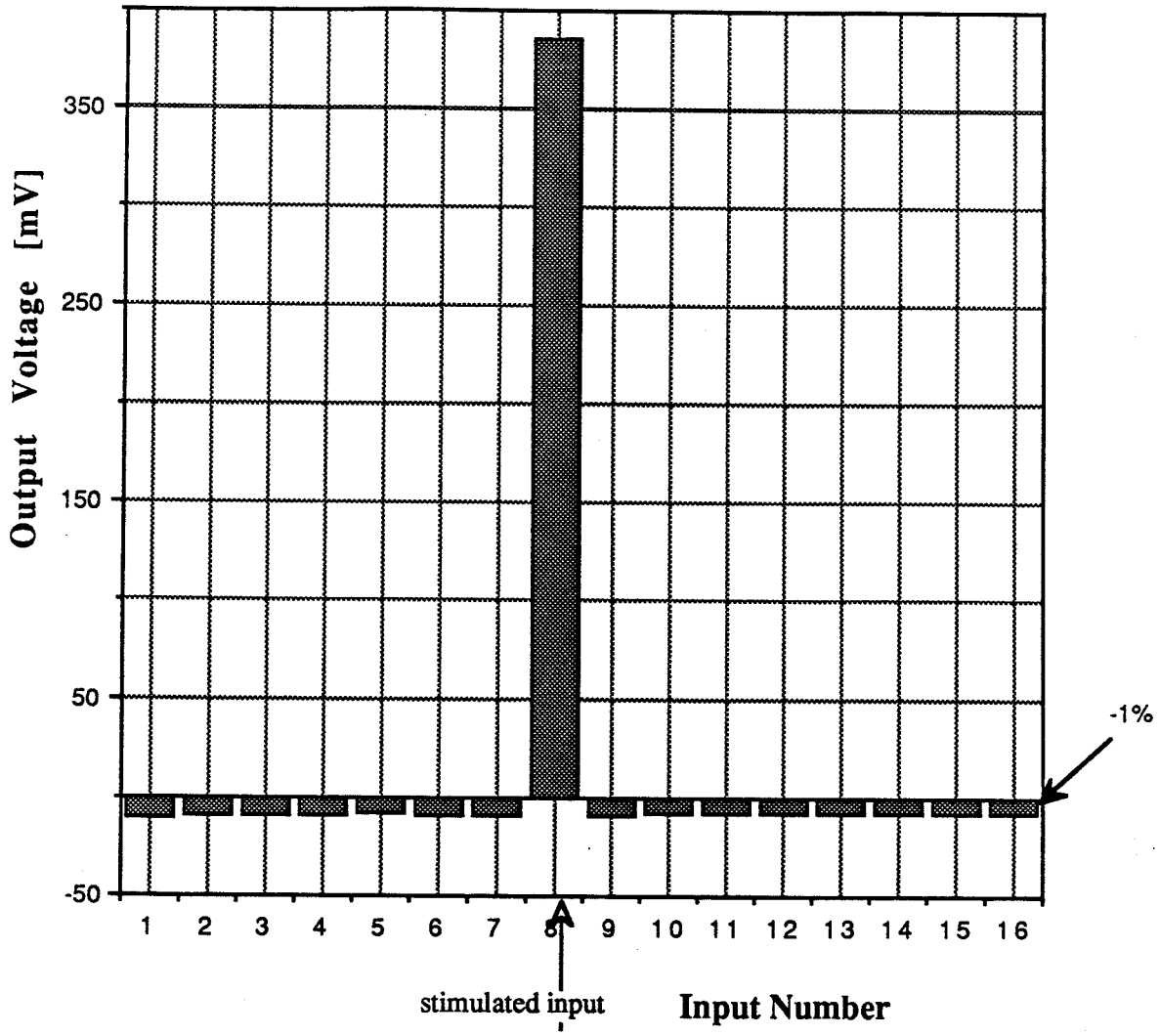
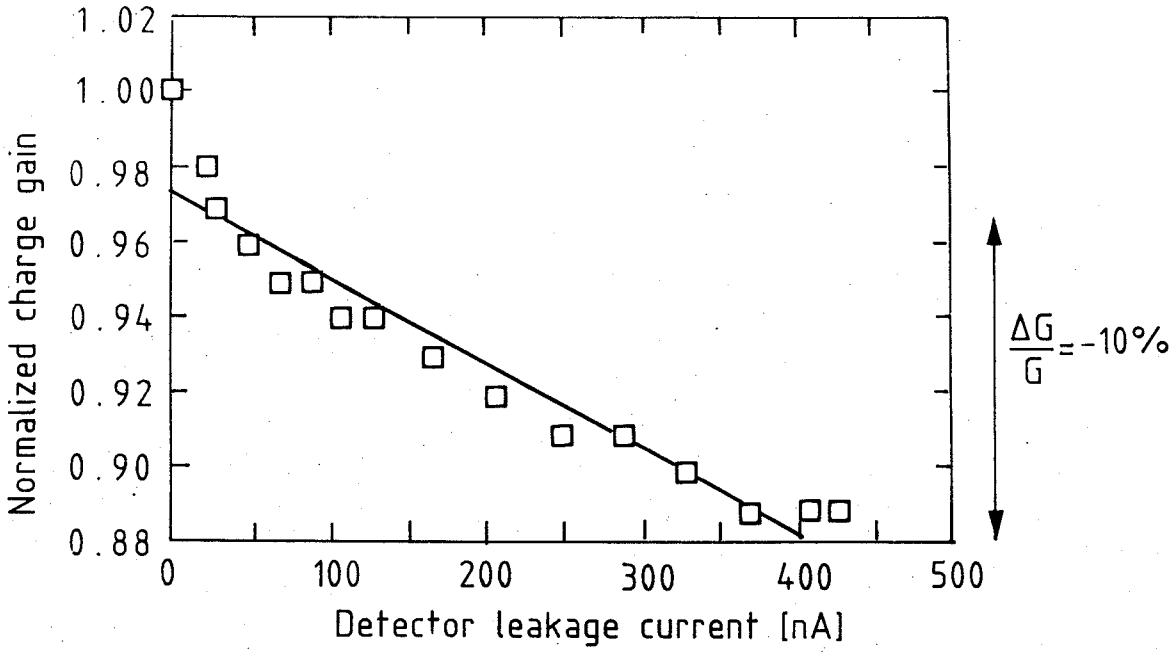

Output Voltage [mV]
350
250
150
50
-50
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
-1%
stimulated input
Input Number

Fig. 11

a)


1.02
1.00
0.98
0.96
0.94
0.92
0.90
0.88
Normalized charge gain
0
100
200
300
400
500
Detector leakage current [nA]
ΔG/G = -10%

b)

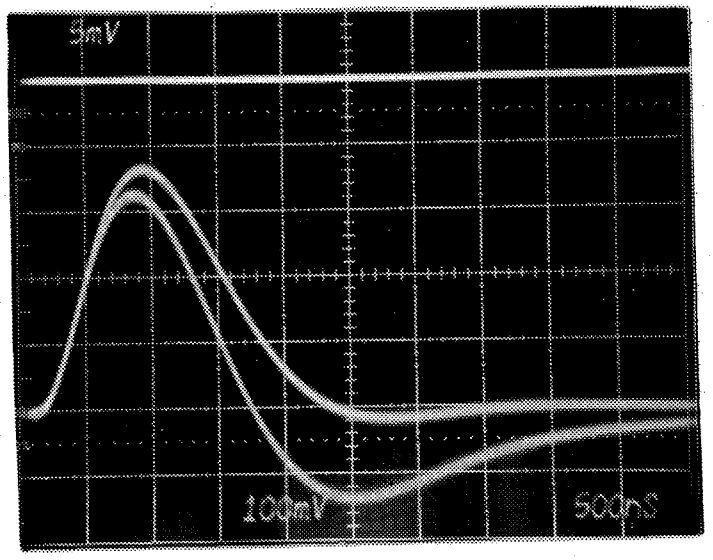

5mV
100mV
500nS

Fig. 12

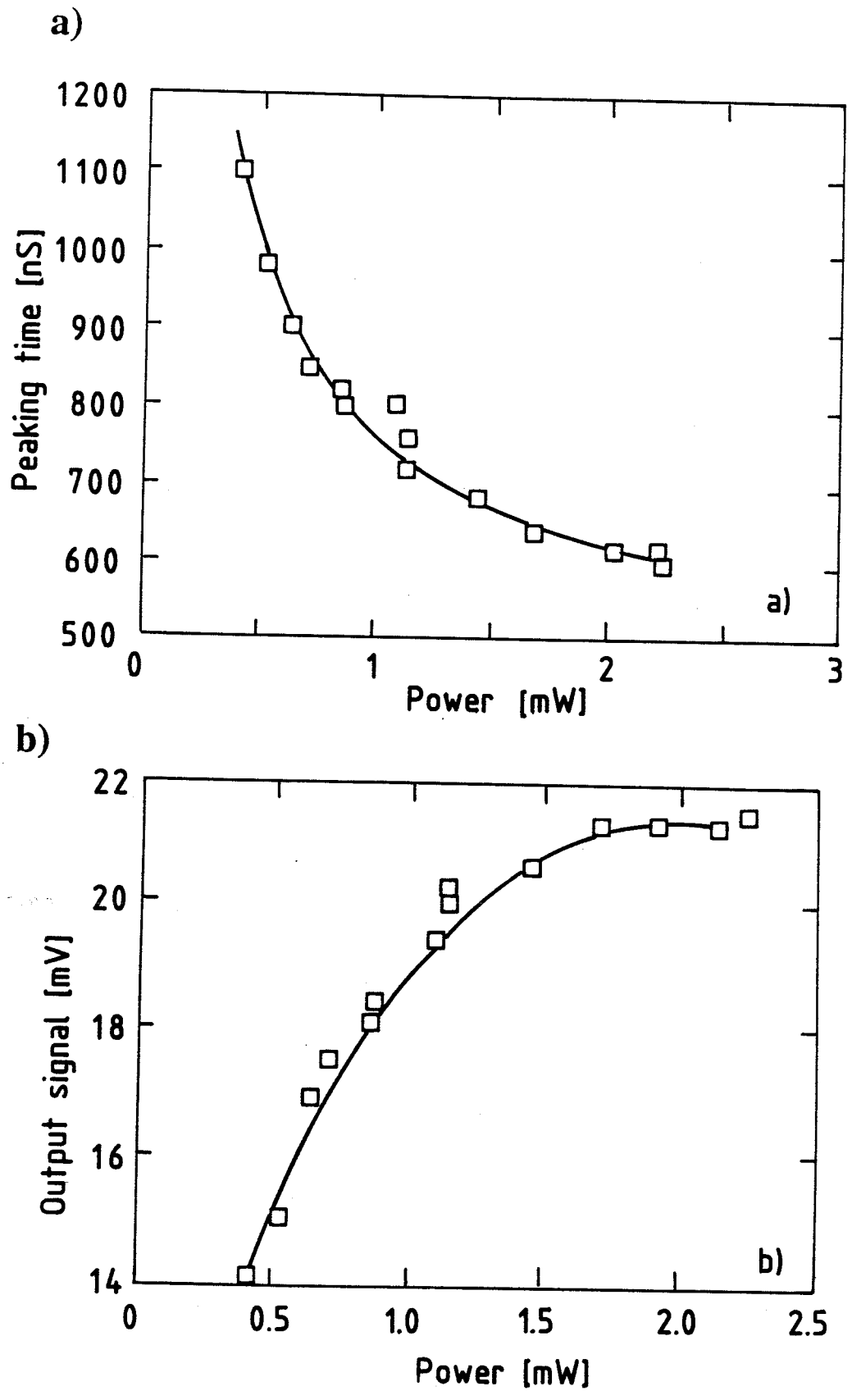

a)
1200
1100
1000
900
800
700
600
500
Peaking time [nS]
0
1
2
3
Power [mW]
a)
b)
22
20
18
16
14
Output signal [mV]
0
0.5
1.0
1.5
2.0
2.5
Power [mW]
b)

Fig. 13

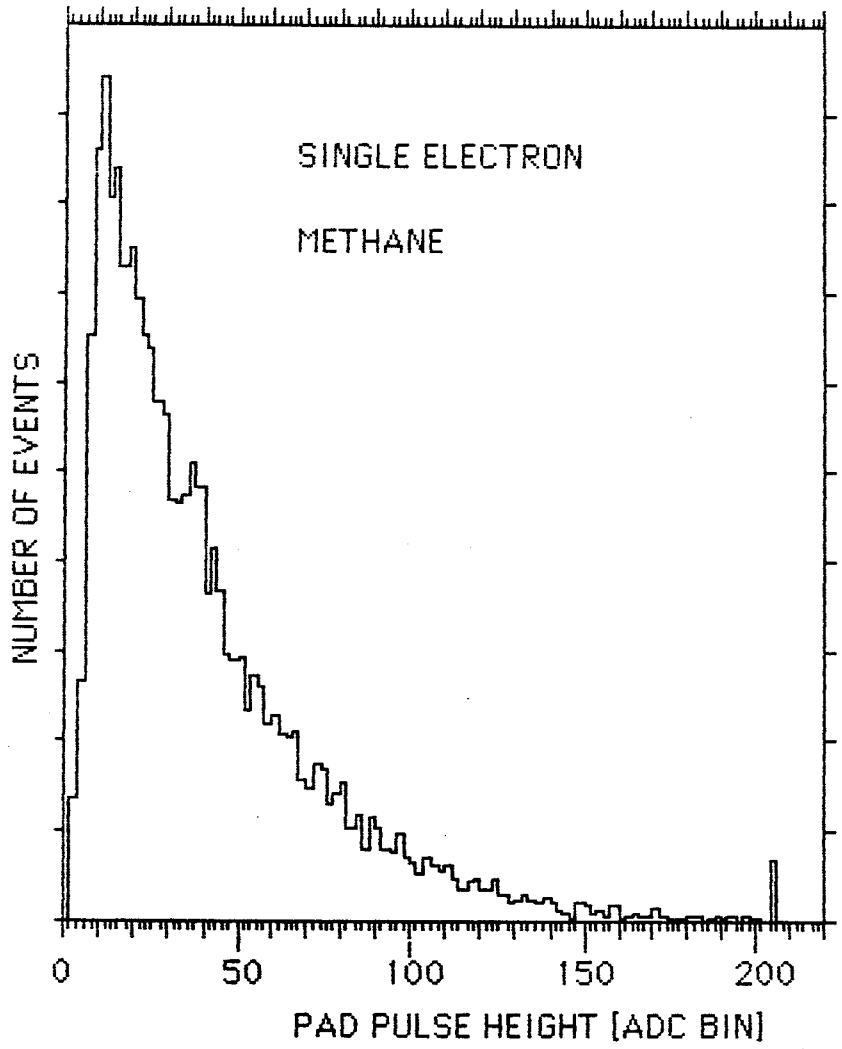

SINGLE ELECTRON
METHANE
NUMBER OF EVENTS
0
50
100
150
200
PAD PULSE HEIGHT [ADC BIN]

Fig. 14

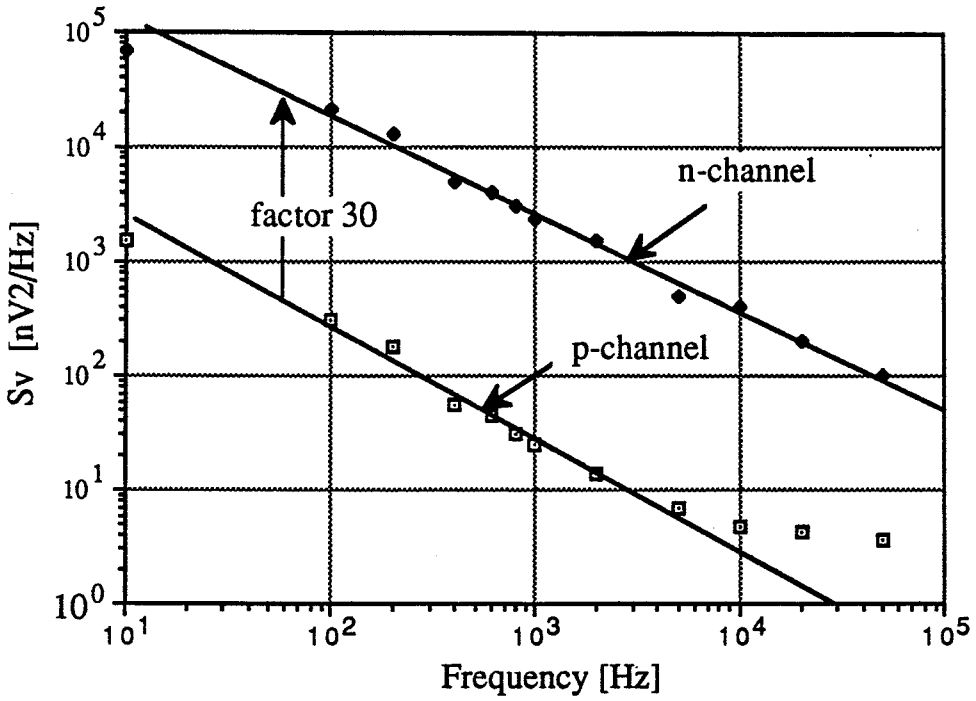

10^5
10^4
10^3
10^2
10^1
10^0
Sv [nV2/Hz]
factor 30
n-channel
p-channel
10^1
10^2
10^3
10^4
10^5
Frequency [Hz]

Fig. 15

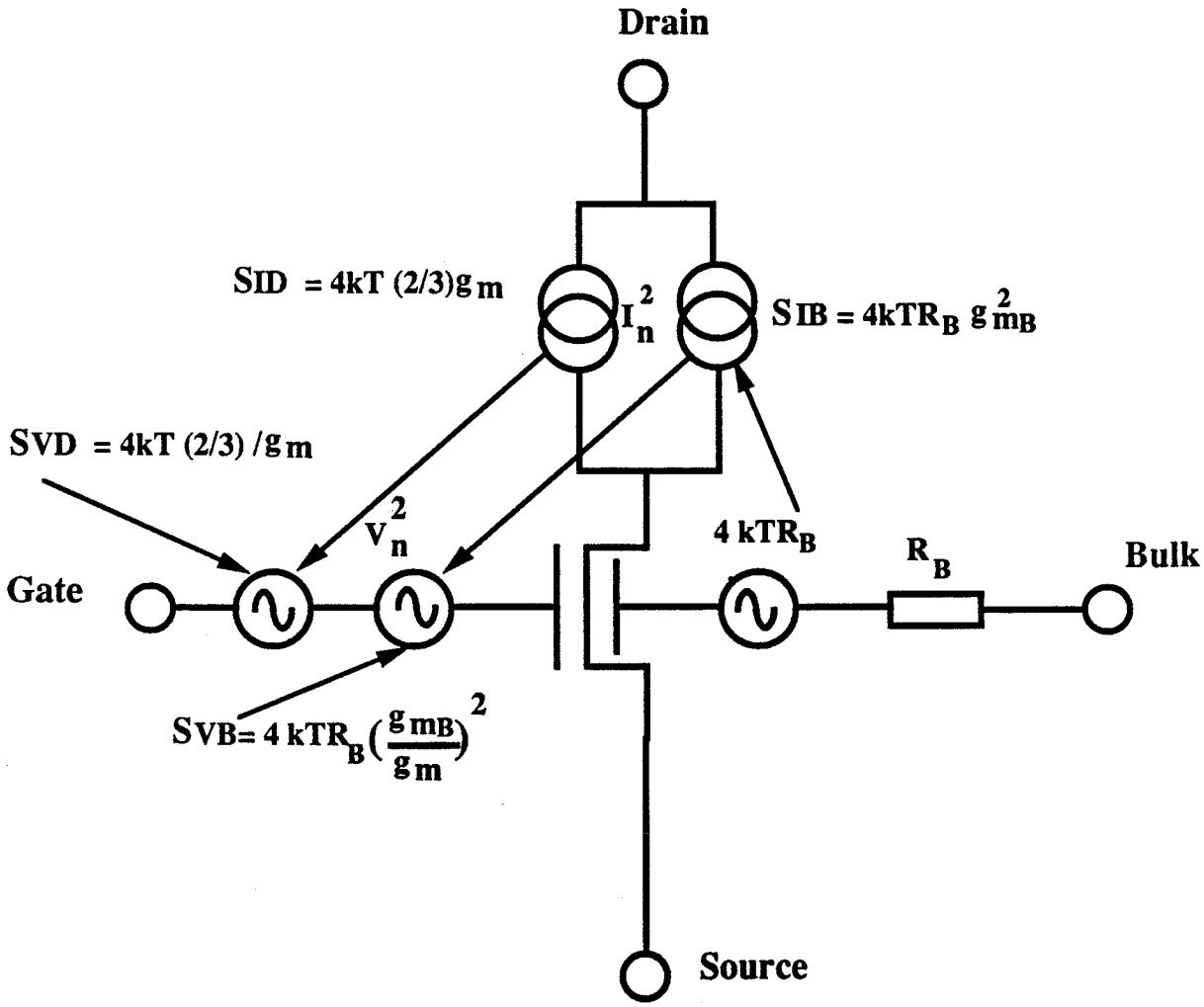

Drain
SID = 4kT (2/3)gm
I_n^2
SIB = 4kTR_B g_mB^2
SVD = 4kT (2/3) /gm
V_n^2
4 kTR_B
R_B
Bulk
Gate
SVB= 4 kTR_B(gmB/gm)^2
Source

Fig. 16

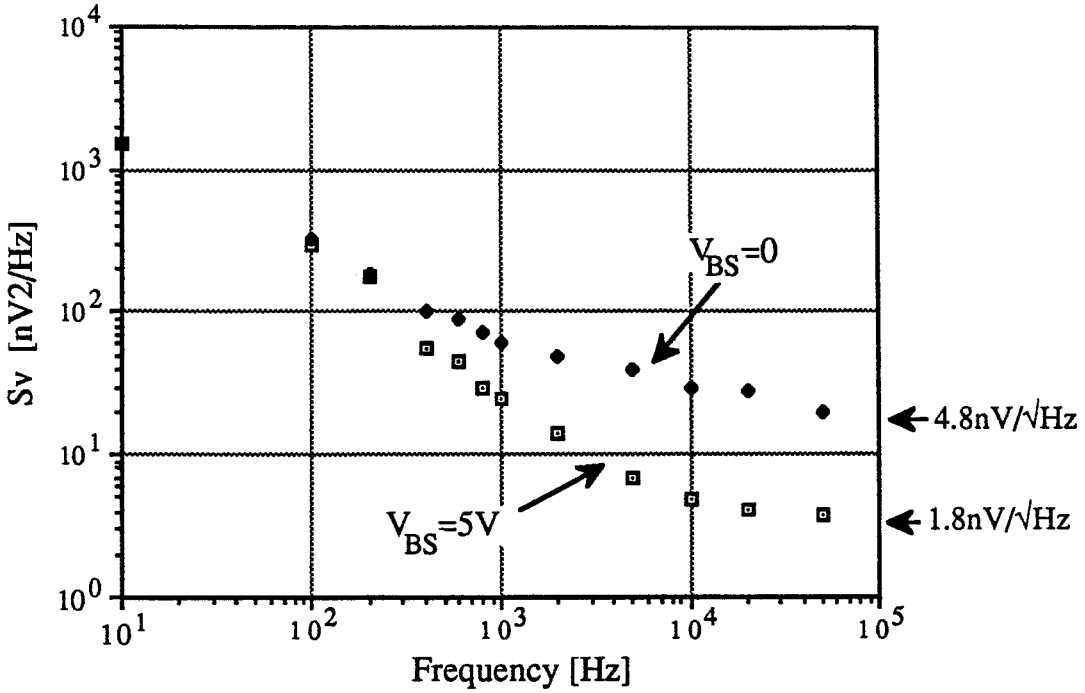

10^4
10^3
10^2
10^1
10^0
Sv [nV2/Hz]
10^1
10^2
10^3
10^4
10^5
Frequency [Hz]
V_{BS}=0
V_{BS}=5V
4.8nV/√Hz
1.8nV/√Hz

Fig. 17

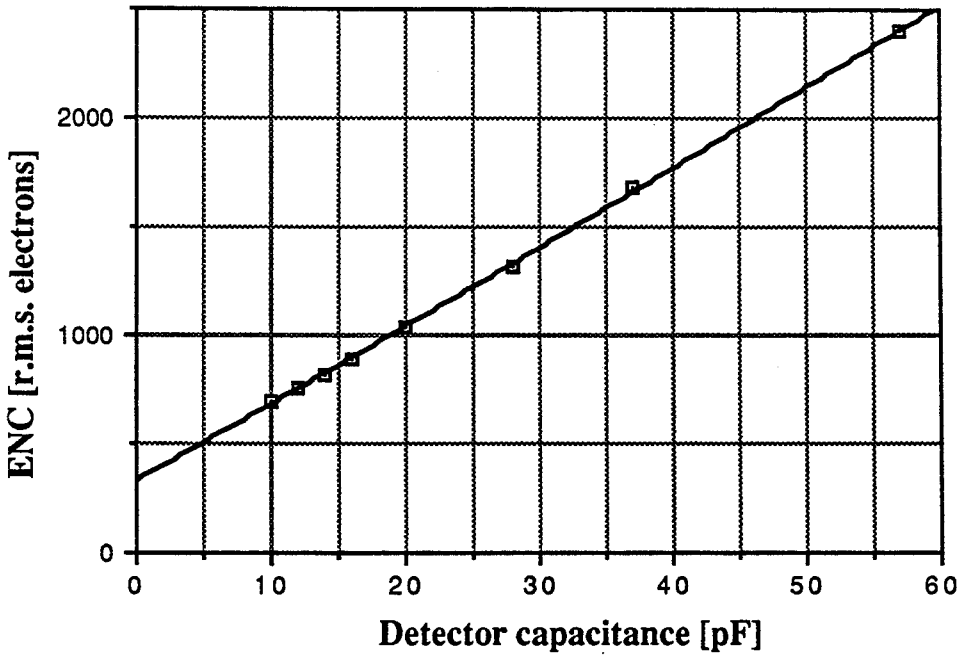

ENC [r.m.s. electrons]
2000
1000
0
0
10
20
30
40
50
60
Detector capacitance [pF]

Fig. 18