An 0.5-μm CMOS Analog Random Access Memory Chip for TeraOPS Speed Multimedia Video Processing

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***Abstract*— Data compressing, data coding, and communications in object-oriented multimedia applications like telepresence, computer-aided medical diagnosis, or telesurgery require an enormous computing power—in the order of trillions of operations per second (TeraOPS). Compared with conventional digital technology, cellular neural/nonlinear network (CNN)-based computing is capable of realizing these TeraOPS-range image processing tasks in a cost-effective implementation. To exploit the computing power of the CNN Universal Machine (CNN-UM), the CNN chipset architecture has been developed—a mixed-signal hardware platform for CNN-based image processing. One of the nonstandard components of the chipset is the cache memory of the analog array processor, the analog random access memory (ARAM). This paper reports on an ARAM chip that has been designed and fabricated in a 0.5-μm CMOS technology. This chip consists of a fully addressable array of 32 $\times$ 256 analog memory registers and has a packing density of 637 analog-memory-cells/mm^2. Random and nondestructive access of the memory contents is available. Bottom-plate sampling techniques have been employed to eliminate harmonic distortion introduced by signal-dependent feedthrough. Signal coupling and interaction have been minimized by proper layout measures, including the use of protection rings and separate power supplies for the analog and the digital circuitry. This prototype features an equivalent resolution of up to 7 bits—measured by comparing the reconstructed waveform with the original input signal. Measured access times for writing/reading to/from the memory registers are of 200 ns. I/O rates via the 16-line-wide I/O bus exceed 10 Msamples/s. Storage time at room temperature is in the 80 to 100 ms range, without accuracy loss.**

***Index Terms*— Analog image processing, analog memories, mixed-signal circuits.**

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I. Introduction

CELLULAR neural networks (CNN's) are analog nonlinear dynamic processor arrays in which direct interconnections among the basic processing units are restricted to a finite local neighborhood [1]. Their potential for image processing applications was advanced shortly after their invention [2] and is based on the fact that many image processing tasks can be realized by means of weighted local interactions between neighboring pixels [1], [3]. Because of their inherently parallel processing architecture, CNN's achieve a high computation speed in the realization of these tasks. Besides, their uniformity and local connectivity make them especially suited for VLSI implementation [4]–[8].

The CNN paradigm provides the framework for the definition of an algorithmically programmable analog array computer with supercomputer power on a chip: the CNN Universal Machine (CNN-UM) [9]. Its dual-computing property enables the realization of highly complex image processing tasks by means of an on-chip analogic—analog and logic—stored program, and renders it a highly competitive alternative to the conventional digital approach to parallel image processing [3]. For example, almost 10^4 Pentium processors[1] are required for the TeraFLOPS array computer shipped by Intel Corporation in 1997 [10]. Whenever accuracy in the computation is not a critical issue, as it actually happens in early-vision tasks [11], CNN-UM analogic chips are advantageous in terms of power consumption and computation speed as compared to these digital counterparts [12].

The working CNN-UM chips reported to date, with up to 20 $\times$ 22 [5], 16 $\times$ 16 [6], and 48 $\times$ 48 [7] cells, respectively, contain a much smaller number of pixels than practical image sizes. For instance, conventional television applications require 644 $\times$ 483 pixels per frame, not including the necessary scanning overhead involved in any display system [13]. Although larger chips will be available in the near future—64 $\times$ 64 [8]—processing of practical size images requires the adoption of system-level solutions to overcome technology limitations on the number of parallel processing cells [14]. Particularly, multiplexing the CNN-UM processors, i.e., making them operate onto a fraction of the complete input image at a time, appears sometimes the only way of operation.

[1] Pentium is a registered trademark of Intel Corporation.

One possible strategy is using space-multiplexed, or multichip, CNN hardware [15]. In a multichip CNN, large arrays are built by interconnecting chips with a smaller number of cells. Each module operates simultaneously onto a fraction of the input image which is, in this way, processed in parallel. One drawback of this approach is the random fluctuations of the process parameters among the different processors. This may cause incorrect or inaccurate operation and, thus, requires the incorporation of different correction strategies; for instance, using tuning to correct parameter deviations during the generation of the analog weights [16]. However, the major drawback of multichip CNN's is the very large number of chip modules and, especially, the off-chip interconnections needed. For instance, around 8E3 chips and 4.1E5 connections are required to process a 644 $\times$ 483 pixel video frame using the 6 $\times$ 6-cell CNN module reported in [17]. And around 75 chips and 3.8E4 connections are needed using the 64 $\times$ 64 last generation analogic processor reported in [8].

A different approach to using small-size CNN chips for large images is time-multiplexing. By taking advantage of the computing power of the CNN-UM, a single chip can be used to process a complete video frame by operating on a fraction of the image at a time. A frame rate of 40 Hz—adequate for high-quality video applications [13]—represents a data flow of 12.3E6 pixels per second. Real-time processing of such a rate demands 81 ns processing time per pixel. Thus, by allowing for a two-pixel-wide overlap between image subsets in each scan direction—required for correct processing of the border pixels [18]—a 32 $\times$ 32 CNN chip should be capable of processing each subimage in about 73.8 μs; and 320 μs for a 64 $\times$ 64 chip. Because the time constant of CNN-UM chips is in the range of 1 μs [4], [8] we can conclude that the time-multiplexed approach is feasible and, hence, constitutes a more cost-effective solution than the multichip one.

The time-multiplexed approach requires the definition and development of an appropriate hardware platform for the CNN processor: the CNN chipset [19]. It is designed to support high-speed data transmission and interfacing of the analogic processor to the sensory devices and the digital host circuitry. The analog RAM (ARAM) is one of the nonstandard parts of this chipset. It is a high-speed, short-term memory buffer that operates as the cache memory [20] of the CNN processor. A straightforward realization of the required functionality would be the use of a conventional digital RAM interfaced with A/D and D/A converters. However, the resulting I/O rates between the memory and the processor would render this solution impractical, as will be discussed later. In order to realize a direct data interchange between the memory and the processor, avoiding data conversion, the implementation of a truly analog RAM chip is proposed. For full compatibility with the digital host environment and reduced fabrication cost, this ARAM should be designed using standard CMOS.

The problem of on-chip analog signal storage has been faced by different authors in connection to quite diverse applications. Particularly, CMOS realizations of scanning delay-lines for video processing are presented in [21], and a high-speed SC sampling circuit is reported in [22] to capture analog waveforms from an array of sensory devices. However, no random access or nondestructive reading of the memory contents can be done. An ARAM for early vision applications was reported in [23]. However, its accuracy relies on mismatch compensation, and no switching error reduction strategies are adopted. In this paper, an improved version of a well-known sample-and-hold (S/H) circuit is proposed to implement a fully addressable analog memory chip. It is realized in a 0.5-μm CMOS single-poly triple-metal technology and allows nondestructive reading and random access to 32 $\times$ 256 memory locations with a cell density of 637 cells/mm^2. It features around 7 bits equivalent resolution with writing/reading access times of 200 ns/200 ns and storage time at room temperature in the 80 to 100 ms range. Besides, its power consumption is only 73 mW from a 3.3-V power supply—achieved through multiplexing of the active S/H circuitry.

In the next section, a brief review of video signal processing with CNN's is given together with the specifications of the ARAM in the CNN chipset. Section III presents the details of the ARAM prototype chip architecture and circuit design. Test results are displayed and discussed in Section IV. Finally, a summary of concluding remarks is given.

II. Video Signal Processing with CNN's

A. CNN-Based Image Processing and ARAM Chip Specifications

In the CNN Universal Machine—which has been demonstrated to be universal in the Turing sense [24]—programmable nonlinear analog dynamics are combined with programmable logic operations and analog and logic distributed memories. Complex image processing tasks are described by an *analogic* program [25], consisting of a sequence of analog and logic operations. This analogic program has to be compiled into a platform-dependent machine code to be executed by a particular hardware implementation. Fig. 1 depicts a diagram of the CNN-UM and its principal building blocks: the basic processing units (cells), and the global analogic programming unit (GAPU). The GAPU stores the analogic program and controls its execution. For this purpose, it is divided into two main functional blocks. The first one is the storage unit consisting of the analog program register (APR), the logic program register (LPR), and the switch configuration register (SCR). They contain the machine code instructions for the analog and logic operations and the switch configuration, respectively. The second one is the global analogic control unit (GACU) that decodes these instructions into a microcode that is transmitted to the cells. Inside the basic cell, three parts can be distinguished which are responsible for signal processing, storage, and control of the operation (Fig. 1). For the implementation of the programmable analog dynamics, the CNN core contains the integrator and the limiter blocks. Synaptic operators can be considered a part of the analog processing unit. A local logic unit (LLU) realizes

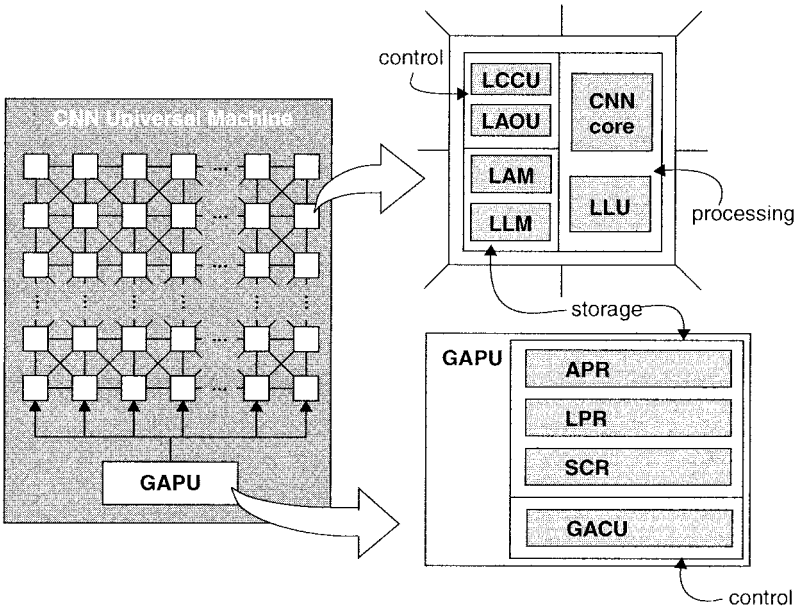


Fig. 1. CNN Universal Machine architecture, basic processing cell, and global analog-and-logic programming unit.

programmable logic operations between stored binary magnitudes. Short-term storage of intermediate signals is realized by local analog and logic memories (LAM's and LLM's). Signal transference and operation control is performed by the local communication and control unit (LCCU). And, finally, data exchange between the cell array and the external circuitry is realized via the local analog output unit (LAOU).

In order to exploit the computing power of this architecture, the CNN chipset shown in Fig. 2 has been developed to interface the CNN-UM processor to the sensors and the digital environment. Data transmission is supported by three different buses. A high-speed analog bus connects the processor, the ARAM, and the video signal sources. The width of this analog bus is determined by the I/O bus of the CNN-UM chip, otherwise it would limit the total throughput of the system. Digital data are transmitted via the digital bus, which is interfaced to the analog bus through A/D and D/A converters. In addition, there is a digital instruction bus. The required storage capacities and local throughput values have to be evaluated to determine the specifications for the nonstandard parts, i.e., the CNN-UM and the ARAM.

Assume an input image composed of $M_i \times N_i$-pixels (Fig. 2). It has to be decomposed into $M_a \times N_a$-pixel subsets that are temporarily stored one-by-one in the analog RAM chip for their processing. However, pixels in the border of this $M_a \times N_a$ window will not be properly processed unless a certain overlap between the image fractions is allowed. Therefore, m_o and n_o pixel overlaps in the vertical and the horizontal directions, respectively, are considered. Taking this into account, a straightforward calculation shows that

$$k_s = \frac{(M_i - m_o)(N_i - n_o)}{(M_a - m_o)(N_a - n_o)} \tag{1}$$

subimages are needed to cover the whole image. Each of these

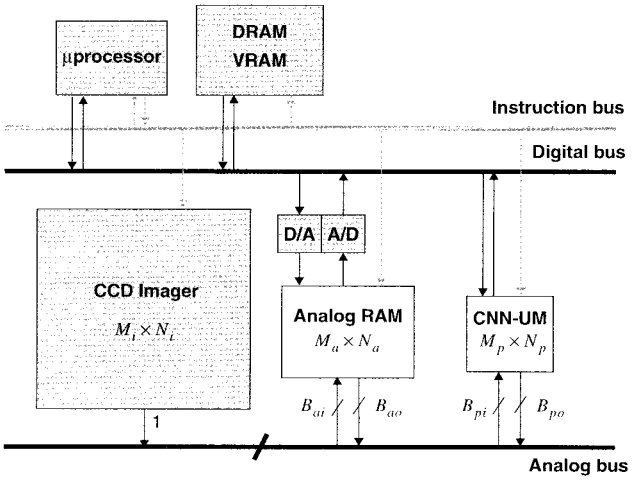


Fig. 2. Diagram of the CNN chipset architecture.

subimages has to be captured, processed, and downloaded, thus resulting in the following total processing time T_i for the $M_i \times N_i$ input frame:

$$T_i = \frac{(M_i - m_o)(N_i - n_o)}{(M_a - m_o)(N_a - n_o)} \cdot (T_{\mathrm{ai}} + T_{\mathrm{ap}} + T_{\mathrm{ao}}) \tag{2}$$

where T_{ai}, T_{ao}, and T_{ap} are the times required to acquire, download, and process each subimage, respectively. For the former two times, and assuming that B_{ai} and B_{ao} are the widths of the input and output buses of the ARAM, the following is obtained:

$$\begin{aligned} T_{\mathrm{ai}} &= \frac{M_a \cdot N_a}{B_{\mathrm{ai}}} \cdot \tau_{\mathrm{ai}} \\ T_{\mathrm{ao}} &= \frac{M_a \cdot N_a}{B_{\mathrm{ao}}} \cdot \tau_{\mathrm{ao}} \end{aligned} \tag{3}$$

where $\tau_{\rm ai}$ and $\tau_{\rm ao}$ are the times required for writing and reading, respectively, an analog register of the ARAM chip.

With regard to the processing time $T_{\rm ap}$ in (2), we have to take into account that, in the more general case, the processor size is smaller than the ARAM size. Hence, the necessity arises for another multiplexation. Assume the size of the processor is $M_p \times N_p$ and that each analogic program contains n_i data acquisition steps, $n_{\rm ap}$ analog processing steps, $n_{\rm lp}$ logic processing operations, and n_d data downloads. Thus, the time needed to perform the analogic algorithm on each $M_a \times N_a$ subset is given by

$$T_{\rm ap} = \frac{(M_a - m_o)(N_a - n_o)}{(M_p - m_o)(N_p - n_o)} \cdot T_{\rm pp} \tag{4}$$

where

$$T_{\rm pp} = n_i T_{\rm pi} + n_{\rm ap} T_{\rm pap} + n_{\rm lp} T_{\rm plp} + n_d T_{\rm po} \tag{5}$$

with $T_{\rm pap}$ and $T_{\rm plp}$ as the times required for the analog and the digital circuitry of the CNN-UM to settle and complete the logic operation, respectively. These parameters are part of the timing specs of the CNN-UM chip. $T_{\rm pi}$ and $T_{\rm po}$ in the expression above represent I/O times which are given by

$$\begin{aligned} T_{\rm pi} &= \frac{M_p \cdot N_p}{B_{\rm pi}} \cdot \tau_{\rm pi} \\ T_{\rm po} &= \frac{M_p \cdot N_p}{B_{\rm po}} \cdot \tau_{\rm po} \end{aligned} \tag{6}$$

where $B_{\rm pi}$ and $B_{\rm po}$ are the widths of the input and output buses of the CNN-UM, respectively, and $\tau_{\rm pi}$ and $\tau_{\rm po}$ are the times required for updating and downloading analog data from one cell of the CNN array—also defined as temporal specs of the processing chip. But let us focus on the specifications for the analog memory chip.

Assume a frame rate of N_f frames per second. The following must be accomplished in order to process the whole input image $(M_i \times N_i)$ in real-time:

$$T_i \leq \frac{1}{N_f}. \tag{7}$$

Thus, from the mathematics above, the following design equation can be obtained:

$$\begin{aligned} \frac{1}{N_f} \geq{}& \frac{M_a N_a (M_i - m_o)(N_i - n_o)}{(M_a - m_o)(N_a - n_o)} \left(\frac{\tau_{\rm ai}}{B_{\rm ai}} + \frac{\tau_{\rm ao}}{B_{\rm ao}} \right) \\ &+ \frac{(M_i - m_o)(N_i - n_o)}{(M_p - m_o)(N_p - n_o)} T_{\rm pp}. \end{aligned} \tag{8}$$

It can be rewritten in order to leave all the terms corresponding to the ARAM on one side

$$\begin{aligned} &\frac{M_a N_a}{(M_a - m_o)(N_a - n_o)} \left(\frac{\tau_{\rm ai}}{B_{\rm ai}} + \frac{\tau_{\rm ao}}{B_{\rm ao}} \right) \\ &\quad \leq \frac{1/N_f}{(M_i - m_o)(N_i - n_o)} - \frac{T_{\rm pp}}{(M_p - m_o)(N_p - n_o)}. \end{aligned} \tag{9}$$

Several considerations can be made based upon this formula. First, the faster or the larger the CNN processor, the less restrictive the specifications on the ARAM are. Second, the larger the analog memory buffer and the wider the I/O analog buses, which is trivial, the longer I/O times can be allowed.

We find it convenient to illustrate this design equation using some typical values and compare the results with the conventional digital approach, which includes A/D and D/A conversion for storing and retrieving data from conventional DRAM or SRAM. For instance, consider a frame rate of 40 frames per second, an input image of 512 $\times$ 512 pixels, an analog memory buffer of 32 $\times$ 256 registers, and a CNN array of 32 $\times$ 32 cells. Consider as well a two-pixel-wide overlap in both vertical and horizontal scanning directions. Then, allowing 40 μs to be the total processing time required by the CNN processor for each 32 $\times$ 32 subimage [4], [8], I/O times divided by their respective bus widths cannot add up to more than 48 ns. This can be achieved by the prototype chip presented in this paper by means of a measured 200-ns access time and the implemented 16-line I/O bus. On the other hand, an analog RAM based on a DRAM and the corresponding A/D and D/A converters requires a duplication of the hardware in order to achieve the required speed if we consider a 10-ns conversion time and 20-ns memory access time.

Furthermore, concurrent implementation of analog signal storage embedded with CNN processing circuitry will result in an excessive area occupation if realized using digital blocks.

Therefore, the specifications for the ARAM block result as follows.

- *Nonvolatility*. The analog information contained in the memory registers should be maintained for a sufficiently long time. In this case, and because of the high speed of the computation, a storage time of 100–200 ms should be enough. Being a cache memory, power-off nonvolatility is not necessary.
- *Resolution*. Accuracy levels for a wide range of early-vision tasks are in the 0.8–1.5% range. It represents an equivalent resolution of 6–7 bits. Cooperative phenomena derived from the parallel processing nature of CNN's, like hyperacuity [26], allow for a moderate resolution requirement.
- *Random Access*. Some analogic algorithms designed for the CNN Universal Machine [27] require repeated reading and writing to a specific location of the memory. Thus, random access to any memory register should be provided.
- *Nondestructive Reading*. For the same reason, reading any memory location should not affect the contents, because access to them might be required several times in an analogic program.
- *High Speed*. Narrow access times to the memory allow for a faster operation. Although difficult to achieve, access times smaller than 100 ns will be required to realize complex image processing tasks in real-time.
- *Input/Output*. On the one hand, a serial analog input channel is needed to interface the image acquisition

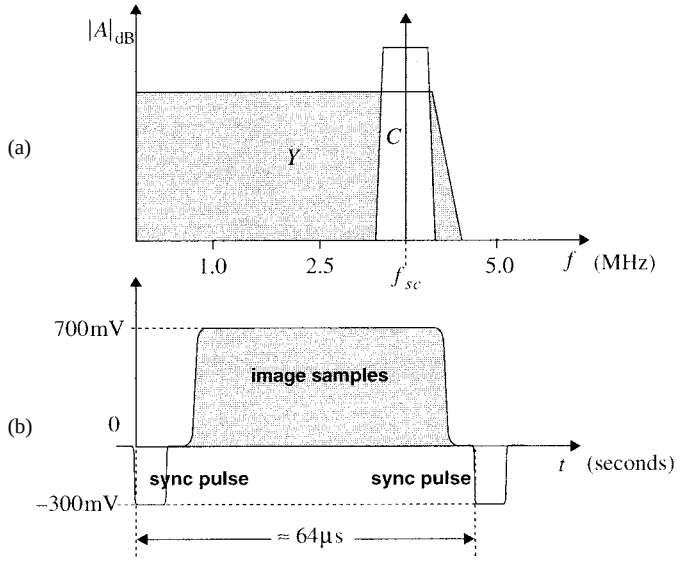


Fig. 3. (a) Envelope spectrum of an NTSC signal, showing the luminance (Y) and the chrominance (C) centered around the color subcarrier ($f_{\rm SC} = 3.86$ MHz), and (b) waveform of a scan line of the associated 525/59.94 scanning standard.

devices—CCD imager, composite-video signal source. On the other hand, the communication with the CNN-UM processor is accelerated by the use of parallel analog channels of width $B_{\rm pi}$ and $B_{\rm po}$—see Fig. 2.

Obviously, the memory cell should be the smallest possible to allow obtaining the largest possible memory arrays without important yield problems. Besides, compatibility with digital CMOS voltage levels is implicitly assumed for integration with a digital environment at the system level via the instruction and digital data buses.

B. Video Signal Interface to the CNN Chipset

A standard composite video signal has a limited bandwidth of 5 MHz and must, hence, be sampled at a minimum rate of 10 Msamples/s. The maximum time interval between consecutive samples is hence 100 ns. In addition, the composite video signal carries information on the luminance and chrominance of each pixel and a synchronization pulse generated by the raster scanning of the object picture. Fig. 3 displays the envelope spectrum of an NTSC-coded signal and the waveform of a scan line. Although NTSC is a color encoding standard, it is also commonly used to refer to its associated scanning standard 525/59.94. A simple implementation of a video-signal interface to the CNN chipset is portrayed in Fig. 4. It can be built up by using off-the-shelf components. Here, the incoming video signal (NTSC-coded in this case) is fed into a video decoder chip. It is decomposed into its luminance (Y) and chrominance (C) components plus the recovered timing signals. By now, only the luminance component will be of interest as we are not considering color information processing. After some amplification and level shifting, if required, the ARAM chip takes samples of the input via the serial input channel. A programmable logic device generates control signals and memory address

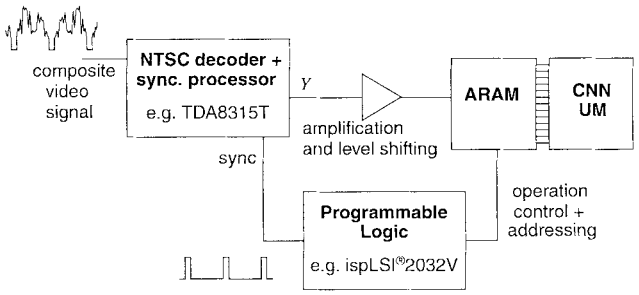


Fig. 4. Composite video signal interface to the CNN chipset.

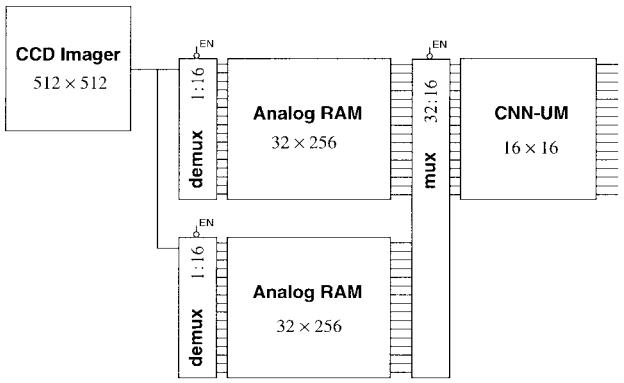
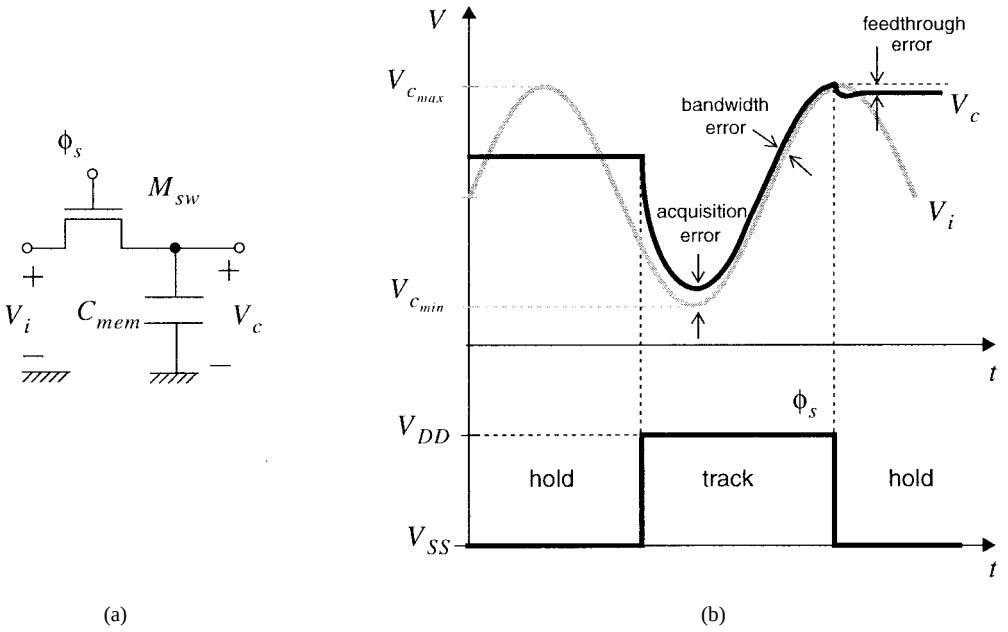


Fig. 5. ARAM chip interleaving for a pipelined architecture of the CNN chipset.

codes using the synchronization pulses that the NTSC decoder has extracted from the raw input. Time requirements for the ARAM in this video interface can be easily derived. Each frame in the 525/59.94 scanning standard is composed of 780 × 525 pixels, including the required blanking intervals, if a square pixel grid is employed—equal horizontal and vertical sample pitches. This means that each line of the image, containing 780 pixels, will be transmitted in 64 μs approximately. Acquisition of this serial data stream has to be realized at more than 12 Msamples/s; this means a time interval of 82 ns between samples. With the use of the ARAM input bus (16-lines wide) and an appropriate demultiplexing of the analog data stream, samples can be taken at 1.31 μs. It is interesting to point out that one of the tasks to be performed by the ARAM chip is the reorganization of the information in such a way that it can be processed by the CNN chip. Lines of the image are sampled by the ARAM one by one, but the processor operates on $M_p \times N_p$-pixel pieces of the input. Full addressing of the memory array and random access to its contents make this re-ordering feasible.

A different approach using interleaved memory chips and a pipelined structure is depicted in Fig. 5. The pixel rate of the CCD imager is about 10.49 Mpixels/s for a frame rate of 40 Hz, which means 95 ns per pixel in a serial transmission. Using the 16-line input bus of the ARAM, samples can be taken at 1.53-μs intervals. This means that we have a 0.78-ms time period for updating the contents in the memory chip. By means of a second analog RAM, the



(a) (b)

Fig. 6. (a) Storage capacitor and pass transistor and (b) errors in the sampling process.

process can be pipelined in such a way that the first ARAM is working with the CNN processor while the second is being updated with the next 16 lines of the input image. After that, the role of the memory chips is reversed, thus speeding up the system to meet the requirements for real-time image processing.

III. Circuit Design and Prototype System Architecture

A. Errors in the Sampling Process: Speed–Accuracy Tradeoff

The nonidealities in the S/H process are evaluated by using the circuit of Fig. 6(a), composed of a pass transistor and a storage capacitor [28]. Its operation is affected by deterministic and random errors.

Let us consider the deterministic errors first. During the track phase—while the pass transistor is ON—the finite ON resistance of the pass transistor originates a sample acquisition delay. Let us call the minimum and maximum input signal voltages $V_{c_{\min}}$ and $V_{c_{\max}}$, respectively. The full-scale input signal voltage can thus be defined as $A = V_{c_{\max}} - V_{c_{\min}}$. The maximum step size occurs when the preceding sampled value is $V_{c_{\min}}$ and the next one is $V_{c_{\max}}$ or vice versa, that is, the input signal goes from one end to the other of its full scale A [see Fig. 6(b)]. In this case, the capacitor voltage is given by

$$V_c(t) = V_{c_{\min}} \exp\left(-\frac{t}{\tau}\right) + V_{c_{\max}}\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] \quad (10)$$

where $\tau = R_{\rm ON}C_{\rm mem}$, $R_{\rm ON}$ being the ON resistance of the pass transistor. Therefore, the acquisition error decreases exponentially with time

$$\varepsilon_a(t) = -A \cdot \exp\left(-\frac{t}{R_{\rm ON}C_{\rm mem}}\right) \quad (11)$$

establishing the maximum sampling rate. The minimum acquisition time required for this error to be smaller than 1/2 LSB—that is, less than $A/2^{N+1}$, where N is the number of bits corresponding to the equivalent digital resolution, is given by

$$\Delta t \geq (N+1)\tau \ln 2. \quad (12)$$

Once the acquisition transient settles, the S/H circuit is in track mode. Now, the voltage at the capacitor attempts to follow the input voltage. The circuit formed by the pass transistor and the storage capacitor $C_{\rm mem}$ acts as a single-pole low-pass filter. Although it does not have an important incidence on the amplitude of the tracked output, the phase shift introduced by this low-pass characteristic can be especially harmful when it is operating on signals modulated in phase. For a given frequency of the input signal V_i, this phase shift is calculated as

$$\phi_{\rm shift} = -\text{atan}(R_{\rm ON}C_{\rm mem}2\pi f). \quad (13)$$

A further deterministic error arises at the falling edge of the clock due to clock feedthrough. It manifests itself as a small discrepancy between the sampled voltage and the magnitude actually held, which can be expressed as

$$\varepsilon_f \approx \frac{C_{g\rm ds}}{C_{\rm mem} + C_{g\rm ds}}[V_{\rm SS} - V_{c_0} - V_T(V_{c_0} - V_{\rm SS})] \quad (14)$$

where V_{c_0} is the undegraded sampled voltage value, $C_{g\rm ds}$ is the parasitic overlap capacitor, and $V_T(V_{c_0} - V_{\rm SS})$ is a nonlinear function which accounts for the substrate effect. The feedthrough error is, hence, signal-dependent, and will therefore induce harmonic distortion at the output. For the computation of the harmonic distortion terms, V_c must be expanded as a series of harmonics of a single-tone input voltage $A \cdot \cos\omega t$. The second and third harmonic distortion

terms, calculated as the ratio of the amplitudes of the second and third harmonics with respect to the principal, result in

$$\mathrm{HD}_2 = \frac{1}{8}A\left|\frac{\frac{C_{gds}}{C_{\mathrm{mem}}+C_{gds}}\cdot\frac{\gamma}{4\left(\phi_B+V_{C|_Q}-V_{\mathrm{SS}}\right)^{\frac{3}{2}}}}{1-\frac{C_{gds}}{C_{\mathrm{mem}}+C_{gds}}\cdot\left(1+\frac{\gamma}{2\sqrt{\phi_B+V_{C|_Q}-V_{\mathrm{SS}}}}\right)}\right| \tag{15}$$

and

$$\mathrm{HD}_3 = \frac{1}{96}A^2\left|\frac{\frac{C_{gds}}{C_{\mathrm{mem}}+C_{gds}}\cdot\frac{3\gamma}{8\left(\phi_B+V_{C|_Q}-V_{\mathrm{SS}}\right)^{\frac{3}{2}}}}{1-\frac{C_{gds}}{C_{\mathrm{mem}}+C_{gds}}\cdot\left(1+\frac{\gamma}{2\sqrt{\phi_B+V_{C|_Q}-V_{\mathrm{SS}}}}\right)}\right| \tag{16}$$

where γ is the body-effect constant, ϕ_B is a surface potential value close to the onset of strong inversion, widely taken as twice the Fermi-level $2\phi_F$, and $V_{C|_Q}$ is the dc component of V_c.

Equation (12) shows that the acquisition time decreases with the capacitor size and inversely with the aspect ratio—W/L—of the pass transistor. Such measures also reduce the phase shift given by (13). However, this causes an increase on the feedthrough error. Also, the use of large switching devices results in heavy clock loads, producing an excessive clock skew and, consequently, serious aperture jitter—a random variation of the delay between the edge of the gate signal and the actual instant in which the circuit enters in hold mode.

This speed–accuracy tradeoff makes it necessary to calculate optimum sizes for the sampling capacitor and the access switch. On one side, the acquisition error is especially noticeable at higher frequencies because of the single-pole low-pass characteristic of the switch-capacitor circuit. Forcing a desired acquisition time, ε_a can be expressed as a function of the capacitor size and the access transistor width, given that $R_{\mathrm{ON}} = f(W)$. On the other side, while sampling low frequency signals, the tracking period is large enough to allow a proper settling of the S/H circuit dynamics. Therefore, the switching error ε_f is the major source of inaccuracy. Being $C_{gds} = W \cdot \mathrm{CGSO}$, where CGSO is the vendor-provided SPICE parameter for this process, the feedthrough error can also be expressed as a function of the capacitor and switch sizes. Now, combining (11) and (14), and assuming a comparable influence of these two effects being the optimal solution, the capacitor size for each value of the pass transistor width can be obtained by solving this equation:

$$\varepsilon_a(C_{\mathrm{mem}}, W) = \varepsilon_f(C_{\mathrm{mem}}, W) \tag{17}$$

which has been done applying a graphical method in Fig. 7.

There is also a random contribution to the sampling error. When the pass transistor is ON, it can be considered as a resistance that introduces a white noise, with Gaussian amplitude and distribution, of thermal origin. Its noise power density is $\overline{\nu}_i^2 = 4kTR_{\mathrm{ON}}\Delta f$. In addition, the single-pole low-pass filter formed by the access switch and the sampling capacitor limits the bandwidth of the noise to an equivalent noise bandwidth $(4R_{\mathrm{ON}}C_{\mathrm{mem}})^{-1}$. This results in a total noise power at the output, the storage node in this case, being

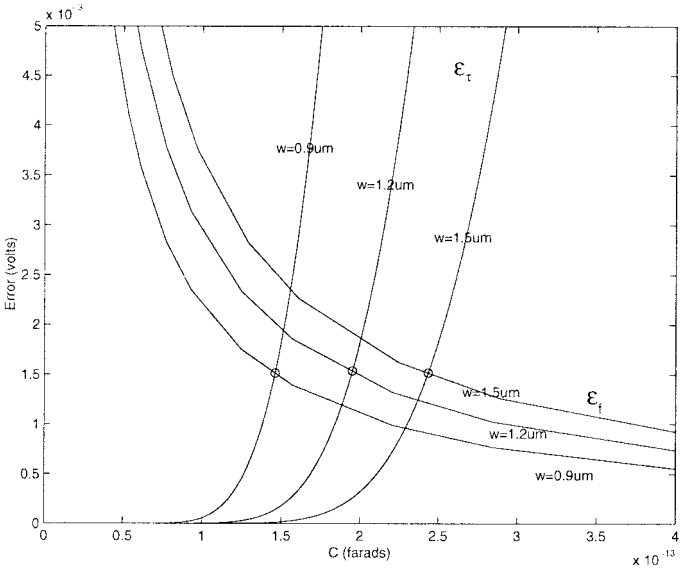


Fig. 7. Speed–accuracy tradeoff.

$$\overline{\nu}_c^2 = \int_0^\infty |A_\nu(j2\pi f)|^2 \cdot \frac{\overline{\nu}_i^2}{\Delta f}\, df = \frac{kT}{C_{\mathrm{mem}}} \tag{18}$$

which is independent of the transistor size and can be reduced by using, once again, a larger sampling capacitor. Notice that $\sqrt{kT/C_{\mathrm{mem}}}$ constitutes a limit to the dynamic range of the system. For an S/H circuit that operates over the whole rail-to-rail scale (3.3-V power supply voltage) with a 0.1-pF sampling capacitor, the maximum achievable dynamic range will be approximately 84 dB. This is not a crucial issue in our case because of the relatively low system resolution requirements, but it can restrain the use of analog signal processing in some other applications.

B. Sample-and-Hold Stage Design

The ARAM chip includes 32 identical S/H lines whose schematic is depicted in Fig. 8. It is based on the S/H circuit reported in [29] and employs bottom-sampling of the analog signal to realize an offset-free and nondestructive recovery of the sampled data with reduced harmonic distortion. Assume first that the opamp has infinite dc gain and that clock feedthrough and the parasitic capacitor C_p are negligible. The difference between the input voltage and a reference voltage V_{REF}, selected for an adequate operation of the CMOS primitives, and the opamp offset voltage V_{os} is stored at C_k during phase ϕ_1 yielding $V_{c_k} = V_i - V_{\mathrm{os}} - V_{\mathrm{REF}}$. Then, during the next phase ϕ_2, the positive capacitor electrode is switched to the output node giving $V_o = V_{c_k} + V_{\mathrm{os}} + V_{\mathrm{REF}}$ and, hence, $V_o = V_i$, with no trace of the opamp offset voltage.

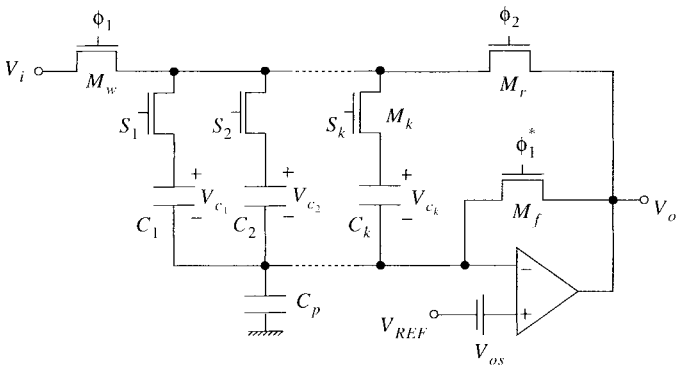


Fig. 8. S/H line schematic including parasitic capacitance and opamp offset.

Consider now that feedthrough is not negligible. Because this S/H circuit employs bottom-plate sampling, the harmonic distortion introduced in the sampling process due to feedthrough can be eliminated. Here, an extra switch M_f is employed to isolate the bottom-plate of the capacitor at the end of the sampling phase. It is controlled by the signal ϕ_1^* that falls slightly before ϕ_1. In this way, the feedthrough error is introduced via the bottom-plate of C_{mem}, which is maintained at a constant voltage V_{REF} by the opamp. Now, ε_f is independent of the input and, therefore, its derivatives with respect to V_i are equal to zero. Consequently, no harmonic distortion due to clock feedthrough will be present at the output. The stored voltage is only affected by an additional voltage offset: a small pedestal error of magnitude

$$\varepsilon_f = \frac{C_{g\text{ds}}}{C_{\text{mem}} + C_{g\text{ds}}} \cdot [V_{\text{REF}} + V_T(V_{\text{REF}} - V_{\text{SS}}) - V_{\text{SS}}]. \tag{19}$$

If the finite dc gain and the parasitic capacitor are accounted for, the output voltage is an attenuated copy of the input, and an offset term appears

$$V_o \approx \left[1 + \frac{1}{A_0}\left(1 + \frac{C_p}{C_k}\right)\right]^{-1} V_i + \frac{1}{A_0}\left(1 + \frac{C_p}{C_k}\right) V_{\text{os}}. \tag{20}$$

Fig. 9 shows the opamp schematic, which has been realized by means of a folded cascode architecture to better fit the 3.3-V power supply voltage. For 7-bit equivalent resolution of the S/H circuit, and assuming that a 16-mV error is allowed for each sample, the opamp output swing has to be larger than 2 V. Other opamp specifications are: *GBW* of 20 MHz—required to follow the input during the tracking phase; and slew-rate (SR) of 8 V/μs—required to sample 4 MHz bandlimited signals with up to 2 V amplitude (peak-to-peak).

Let g_{m_1} be the small-signal transconductance of the transistors in the input differential-pair of the opamp, and I_B be the tail current. A relation between the transistors' aspect ratio and I_B can be derived from the *GBW* specifications. Because $GBW = g_{m_1}/(2\pi C_L)$ and assuming operation within

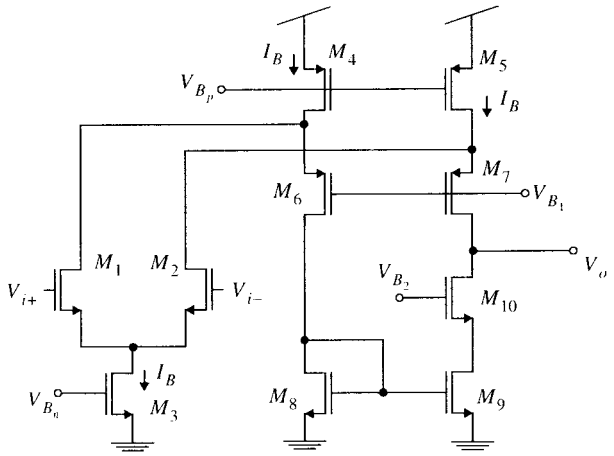


Fig. 9. Opamp schematic.

TABLE I
TRANSISTOR SIZES

$M_1 - M_2$	24/1.2
M_3	16/1.2
$M_4 - M_5$	48/2.4
$M_6 - M_7$	48/1.2
$M_8 - M_9$	24/2.4
M_{10}	24/0.6

the saturation region in strong inversion, one obtains

$$\frac{W}{L} = \frac{(2\pi C_L \cdot GBW)^2}{2k_n I_B} \tag{21}$$

where k_n is the intrinsic transconductance of the MOS transistor. On the other hand, the necessary tail current is fixed by the slew-rate

$$I_B = SR \cdot C_L. \tag{22}$$

This current determines the appropriate aspect ratio of the input differential pair for a constant *GBW* of 20 MHz. The folded-cascode output stage is specified by the dc gain. By providing at least 60 dB for the dc gain—$A_0 = g_{m_1} R_o$—the error introduced by the parasitic capacitance is reduced to 0.1%. As g_{m_1} is now fixed, the output stage has to be designed so as to achieve the necessary output impedance. Final compromises are resolved by phase margin and matching considerations. Table I shows transistor sizes.

C. Leakage Currents and Storage Time

During the hold period, several leakage currents attempt to discharge the storage capacitor, contributing to a degradation

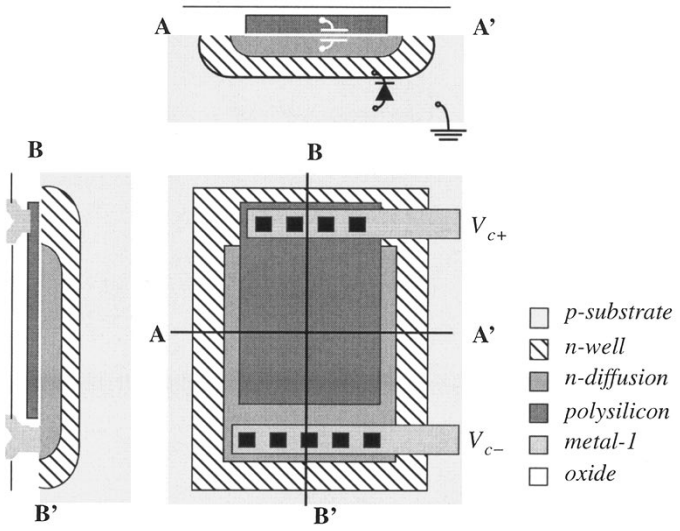


Fig. 10. Polysilicon over n-diffusion capacitor.

of the sampled voltage value. In the first place, the reverse-biased junction formed by the n-diffusion area, corresponding to the source terminal of the pass transistor and the substrate, pumps out a current from the upper plate of the capacitor which can be approximated by the reverse-biased saturation current of the parasitic diode. Another leakage is due to the subthreshold drain-to-source current of the pass MOS transistor. These effects add up, resulting in a total current in the range of the picoampere. Here, capacitors are implemented by a poly-over-diffusion structure lying on top of a weakly doped n-well (Fig. 10). The n-well/p-substrate junction is then reverse-biased, and the current that flows out of the bottom plate of the capacitor corresponds to the associated reverse-bias saturation current. Since it is in the femtoampere range, it limits the effect of the upper plate leakage. Stored voltage degradation in time during the hold period is now given by

$$\frac{dV_c}{dt} = -\frac{1}{C_{\text{mem}}} \cdot \frac{dq^-}{dt} \approx -\frac{I_{\text{self}}}{C_a A} \tag{23}$$

where C_a is the capacitance per unit area of the poly-over-diffusion structure. In these conditions, a self-discharge rate, independent of the capacitor size, is defined

$$r_{\text{self}} = \frac{q}{C_a}\left(\frac{D_p p_{n0}}{L_p} + \frac{D_n n_{p0}}{L_n}\right) \tag{24}$$

where q is the charge of an electron, D_p and D_n are the diffusion coefficients for holes and electrons, L_p and L_n their diffusion lengths, and p_{n0} and n_{p0} are the minority-carrier concentrations on each side of the junction. In this technology, r_{self} is 50 mV/s. The voltage at the capacitor decays then linearly in time during the hold period. A maximum storage time can be defined in terms of the accuracy requirements. For an equivalent resolution of N bits and a full-scale range of the input signal given by A, the maximum storage time (t_{sto}) is the period in which the difference between V_c and the initially stored voltage does not exceed $A/2^{N+1}$, which is 1/2 LSB,

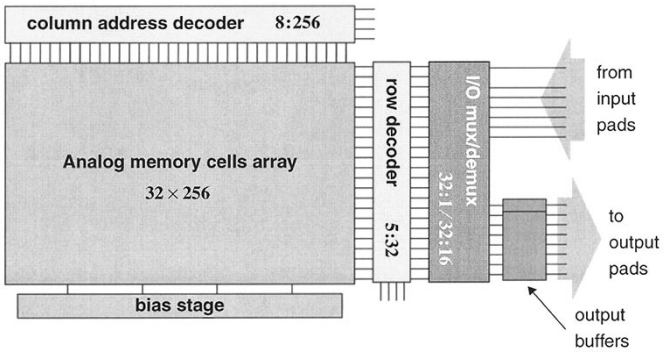


Fig. 11. System architecture of the ARAM chip.

resulting in

$$t_{\text{sto}} = \frac{A}{r_{\text{self}} \cdot 2^{N+1}} \tag{25}$$

which is in the 200 ms range for a 10-mV error. These figures, however, must be understood only as a guideline because of the strong sensitivity of the leakage currents to the operating temperature. Also, the incidence of light on the circuit surface can seriously degrade the contents of the memory because of the light-induced generation of an extra amount of carriers.

D. ARAM Chip Floorplan

This CMOS ARAM chip is composed of an array of 32 × 256 analog memory cells. Each one contains a capacitor, a pass transistor, and some local logic for address decoding. The system also includes some digital control circuitry and an I/O interface consisting of an analog MUX/DEMUX and 16 output buffers. Fig. 11 shows a picture of the ARAM chip floorplan. The memory matrix is arranged into 32 S/H lines with 256 capacitors each. Random access to any memory location is available with the help of two-binary-to-one-hot address decoders. A code of 5 bits activates one out of the 32 row selection lines, by means of the row address decoder. Similarly, each one of the 256 columns is selected by an 8-bit code. Different access schedules can be implemented by an adequate programming of the address codes. In order to avoid the selection of more than one capacitor per row at a time, which would seriously degrade the operation, a global clock controls the duty cycle of the access signals, leaving a tunable guard time interval for address codes to change. Now, with respect to the I/O interface, the 32 data lines of the array are multiplexed either to the 16-line wide I/O bus or the serial I/O channel. A digital control signal sets the serial or parallel I/O mode. Row selection signals are employed to scan the 32 data lines with either the I/O serial channel or the 16-line I/O bus. Some test pads have been added to characterize the output buffers for a better analysis of the test results.

Guidelines concerning signal interaction prevention in mixed-signal IC's have been followed in the development of the prototype. It is a well-known fact that the integration of a significant amount of digital circuitry along with analog signal processing in the same substrate can potentially degrade

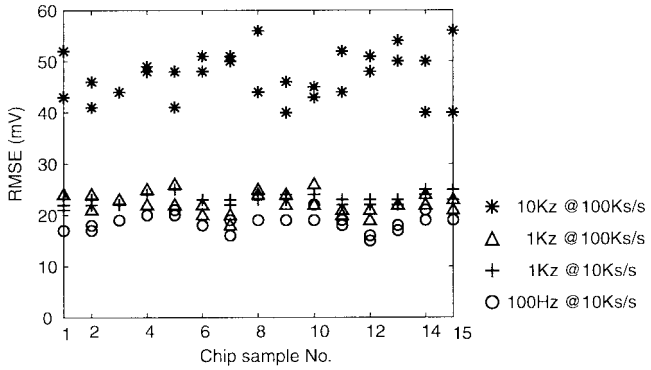


Fig. 12. Measured rms error in the reconstructed waveform.

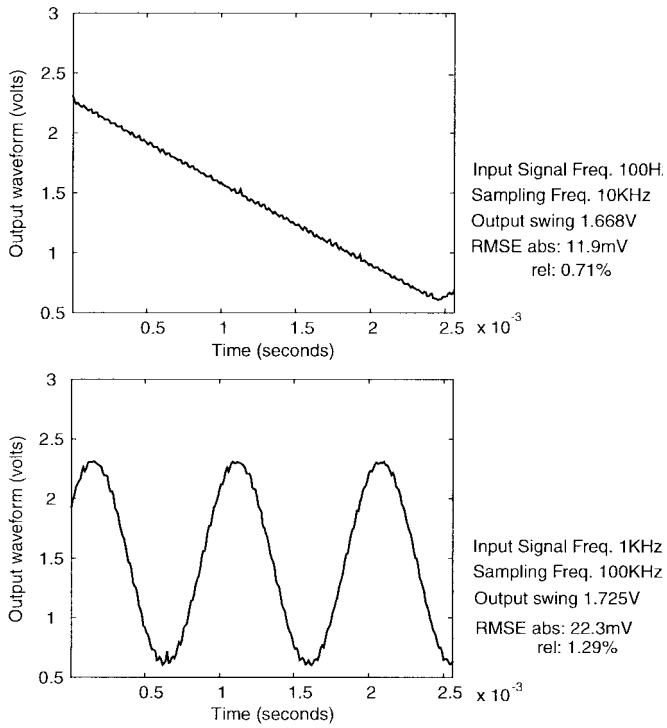


Fig. 13. Recovered triangular and sine waveforms.

system performance. A conservative layout style, with an extensive use of grounded guard rings, reduces signal coupling by opening alternative return paths to the currents induced into the substrate [30]. This is reinforced by the implementation of separated power supply and ground connections for the analog and digital circuitry and guard rings [31]. Digital lines switching at higher rates have been routed over insensitive areas and critical crossings have been shielded with a grounded metal intermediate layer. Also, analog bus lines are made wider and are separated to a larger distance than recommended by technology rules, in order to reduce crosstalk at higher frequencies.

IV. Experimental Results

The first prototype of this ARAM chip has been integrated in the Hewlett-Packard 0.5-μm CMOS process offered by the MOSIS service. The 24 available samples of the chip

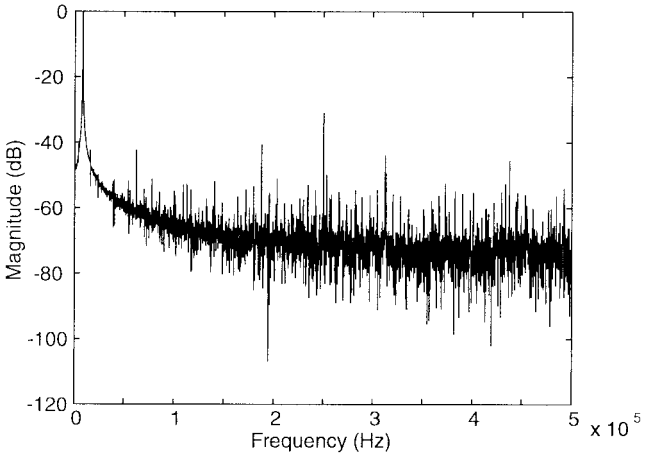


Fig. 14. Spectrum of the output sine wave at 10 KHz (no filtering of the readings).

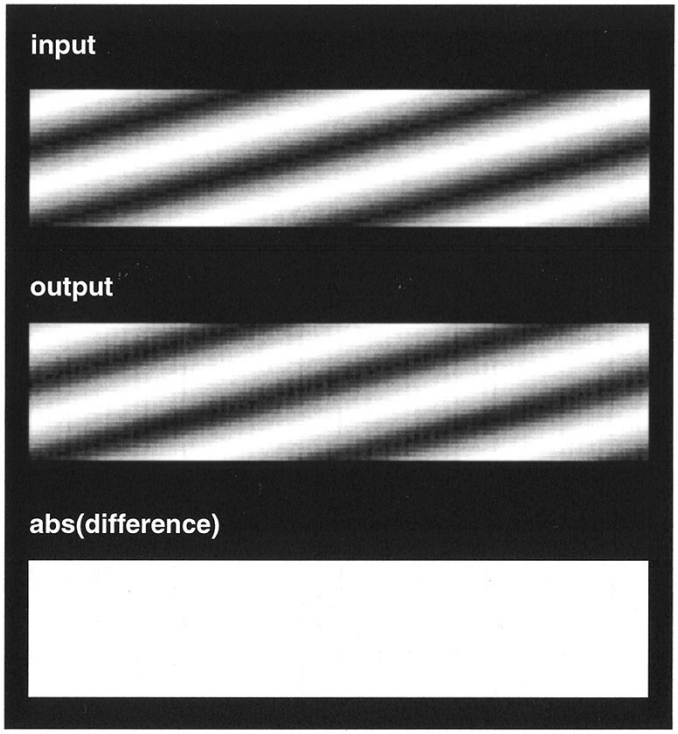


Fig. 15. Input and output images (256 gray levels).

have been tested and proved to be functional. No major discrepancies have been found during the test of the different samples. First of all, a functional characterization test has been developed. Several input sine waves of different frequencies have been sampled at different rates. Fig. 12 shows a plot of the measured root-mean-square error during the reconstruction of the input waveform. It has been computed by taking the square root of the average of the squared difference between the input signal and the recovered waveform over the N samples of the input wave

$$\mathrm{RMSE} = \sqrt{\frac{1}{N} \cdot \sum_{k=1}^{N} (V_{i_k} - V_{o_k})^2}. \tag{26}$$

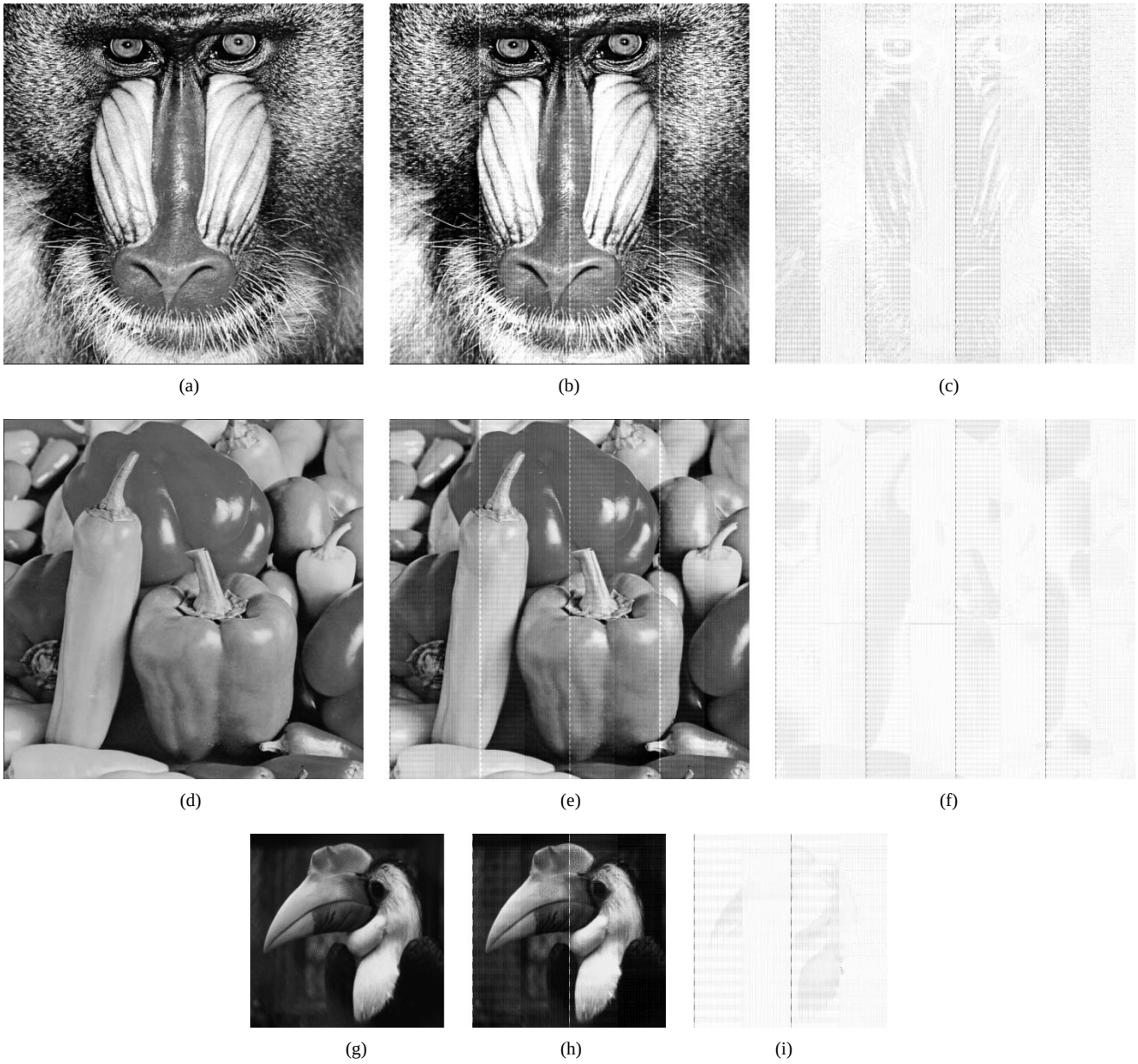


Fig. 16. Test input and output images.

It is important to mention that no correction of the output buffer offset or the feedthrough-induced pedestal error has been made. Fig. 13 displays a reconstructed triangular wave sampled at 10 kHz and a recovered sine wave sampled at 100 kHz. The computed absolute RMSE is in the 13–25 mV range, which means a relative error of 0.7–1.4% for a 1.8-V output swing.

A revealing picture of the test results is obtained by computing the FFT of the output signal. In this case, a 10-kHz sine wave has been sampled at 250 ksamples/s. It has been fed to the ARAM chip through the serial input channel, therefore, 8192 samples of the input waveform have been taken. Fig. 14 shows the spectrum of the output signal, directly measured from the output of the chip without eliminating irrelevant information or filtering the digitizer readings. This means that not only the stored voltage samples but also the voltage peaks occurring during address changes are captured. The magnitude of the single-tone at 10 kHz is nearly 80 dB above the background level. The following peak in magnitude, which takes place at the sampling rate, is approximately 30 dB below the sine wave tone. Fig. 15 displays the input and the output signals as 32 $\times$ 256-pixel images using a linear 256-level grayscale (8 bits deep). Each pixel in the image represents the voltage at a memory capacitor in the array. The absolute value of the difference between the input and output images is represented in the same grayscale.

Besides, some real images have been loaded to the chip at 200 ns per pixel and downloaded at 800 ns, using the PC-controlled CNN chip set implementation described in [32]. Higher speeds, 200 ns/200 ns, have been measured in a dedicated PCB. Fig. 16 displays the input and output pictures together with a grayscale representation of the

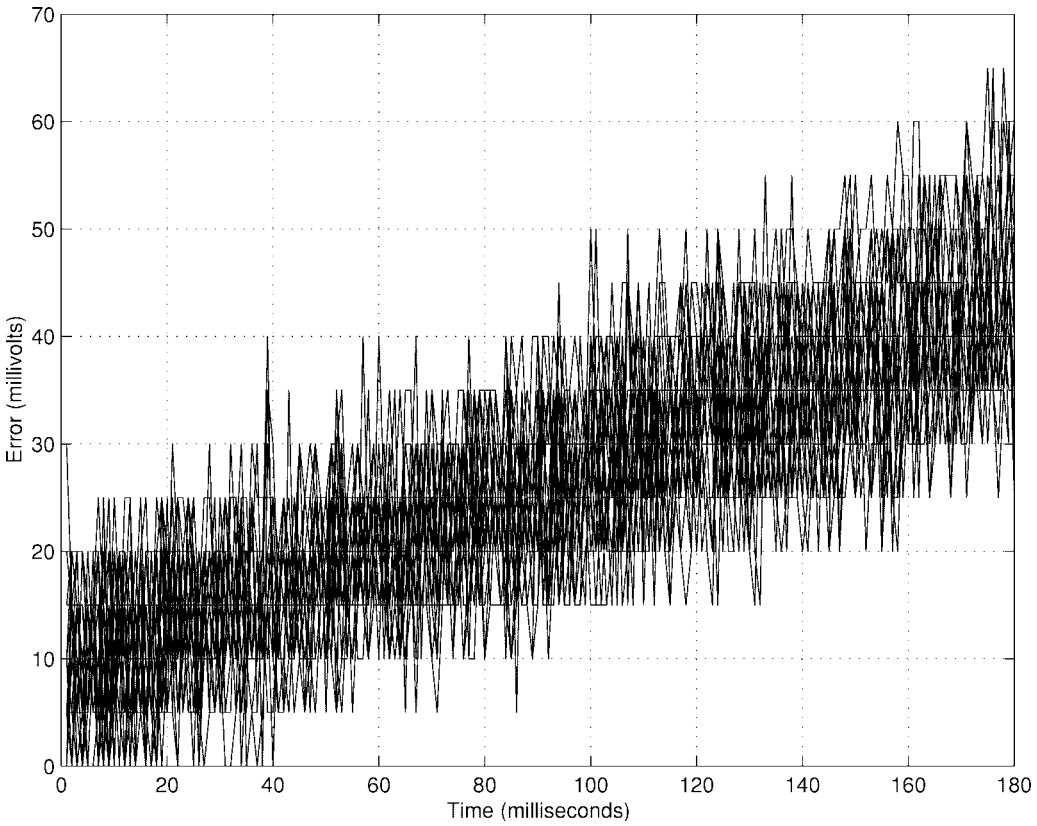


Fig. 17. Degradation of the stored voltage (24 cells).

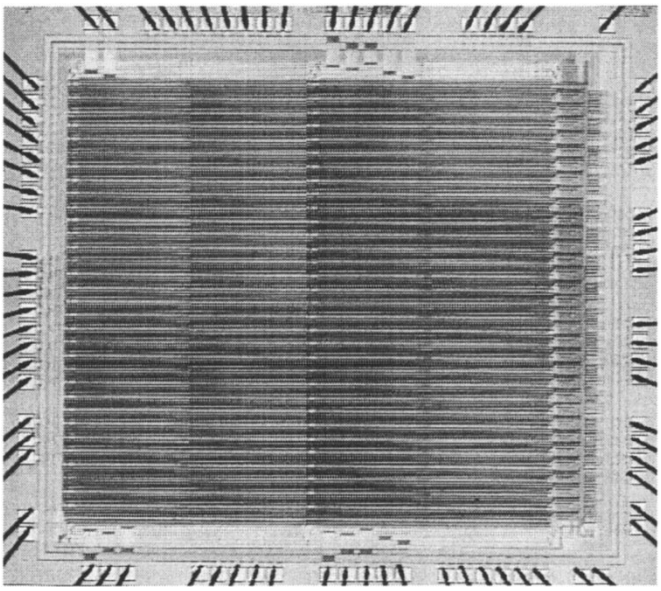


Fig. 18. Die photograph of the ARAM prototype.

TABLE II
ARAM PROTOTYPE DATA

Number of pixels	$8192(32 \times 256)$
Cell-array area	$3.73\text{mm} \times 3.45\text{mm}$
Cell-density	$637\text{cells}/\text{mm}^2$
System area (w/o pads)	$4.13\text{mm} \times 3.89\text{mm}$
Die Area	$4.77\text{mm} \times 4.47\text{mm}$
Package (used pins)	PGA-84M(81)
Power supply	3.3V
Power dissipation	72.86mW @3.3V
Sampling time	200ns
Reading time	200ns
I/O rates (via 16-lines bus)	above 10Msamples/s
Input range	[0.6,2.4]V
Output swing	[0.6,2.4]V
Storage time (1.5% error)	80-100ns
Measured resolution	6-7bits (0.7-1.5%)

absolute difference between them. The first two examples are 512 × 512-pixel pictures in a 256-level grayscale. The last one is a 256 × 256-pixel color picture. They have been processed in 32 × 128-pixel pieces because of test equipment requirements. Some spatial noise can be detected in the output picture. It is partly due to image partitioning and, on the other side, due to an improper tracking of the input at the beginning of each pixel group—vertical lines at the first, one-hundred-twenty-ninth, two-hundred-fifty-seventh, and three-hundred-eighty-fifth pixels. Because of the clocking

scheme adopted to avoid the selection of more than one memory register at a time, the feedback loop of the opamp in the S/H stage is left open for a certain period. Consequently, the voltage of the output node goes up to the power supply voltage or down to the negative rail. In these conditions, the slew-rate of the opamp is insufficient to catch up with the input in the required acquisition time.

Finally, storage time has been measured for randomly selected cells of the array. Fig. 17 shows the difference between the initially stored voltage and the measured voltage through time. These data represent 24 cells in the 24 different samples of the chip. Stored voltage degradation exceeds the required accuracy levels after 80–100 ms. Recursive reading of the same memory spot does not have a noticeable influence on the stored voltage.

Finally, Fig. 18 shows a photograph of the prototype circuit and Table II provides a survey of data extracted from the tests results.

V. Conclusions

The only missing part of the CNN chipset architecture has been implemented. A random access analog memory chip has been designed and integrated in a standard 0.5-μm CMOS single-poly triple-metal technology. Measured equivalent resolution is about 7 bits. Storage time is larger than 80 ms at room temperature. DC power dissipation remains 73 mW for a 3.3-V power supply. Access times of 200 ns have been obtained. Higher sampling and output rates can be achieved using the 16-line wide analog I/O bus. In future generations of the CNN Universal Chip, an embedded and distributed version of this analog RAM will be implemented. The reported prototype is now being employed in different experiments related to video signal processing in multimedia applications.

Acknowledgment

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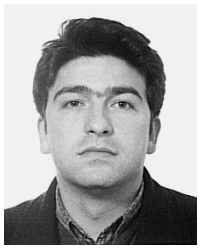
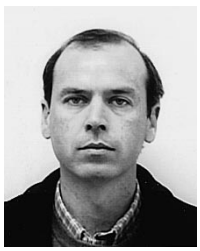


Ricardo Carmona-Galán received the five-year degree in physics in the speciality of electronics (Licenciado en Física Electrónica) from the University of Seville, Spain, in July 1993. From 1994 to 1996, he was granted by IBERDROLA S.A. as a Ph.D. student at the Department of Analog Circuits Design of the Institute of Microelectronics of Seville, IMSE-CNM-CSIC. He is currently finishing the Ph.D. thesis in the Department of Electronics and Electromagnetism, University of Seville.

From 1996 to 1998, he was an Assistant Specialist in the Electronics Research Laboratory, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. He is currently a Research Assistant at the Institute of Microelectronics, Department of Electronics and Electromagnetism, University of Seville. His main areas of interest are linear and nonlinear analog and mixed-signal integrated circuits, in particular, VLSI implementation of cellular neural networks, real-time image processing, and vision chips.

Ángel Rodríguez-Vázquez (M'80–SM'95–F'96) is a Professor of electronics in the Department of Electronics and Electromagnetism, University of Seville, Sevilla, Spain. He is also a Member of the Research Staff of the Institute of Microelectronics of Seville—Centro Nacional de Microelectrónica (IMSE-CNM)—where he is heading a research group on analog and mixed-signal VLSI. His research interests are in the design of analog interfaces for mixed-signal VLSI circuits, CMOS imagers and vision chips, neuro-fuzzy controllers, symbolic analysis of analog integrated circuits, and optimization of analog integrated circuits.

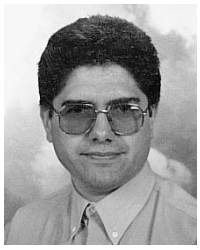
Dr. Rodríguez-Vázquez served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 1993 to 1995, as Guest Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I Special Issue on "Low-Voltage and Low-Power Analog and Mixed-Signal Circuits and Systems" (1995), as Guest Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II Special Issue on "Advances in Nonlinear Electronic Circuits" (1999), as Guest Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I Special Issue on "Bio-Inspired Processors and Cellular Neural Networks for Vision" (1999), and as Chair of the IEEE-CAS Analog Signal Processing Committee (1996). He was Co-Recipient of the 1995 Guillemin–Cauer Award of the IEEE Circuits and Systems Society and the Best Paper Award of the 1995 European Conference on Circuit Theory and Design. In 1992, he received the Young Scientist Award of the Seville Academy of Science. In 1996, he was elected Fellow of the IEEE for "contributions to the design and applications of analog/digital nonlinear IC's."



Servando Espejo-Meana received the Licenciado en Física degree, the M.S. equivalent in microelectronics, and the Doctor en Ciencias Físicas degree from the University of Seville, Spain, in June 1987, July 1989, and March 1994, respectively.

From 1989 to 1991, he was an Intern in AT&T Bell Laboratories, Murray Hill, NJ, and an employee of AT&T Microelectronics of Spain. He is currently a Professor in electronic engineering, Department of Electronics and Electromagnetism, University of Seville, and also with the Department of Analog Circuit Design, Institute of Microelectronics of Seville, IMSE-CNM-CSIC. His main areas of interest are linear and nonlinear analog and mixed-signal integrated circuits, including neural networks electronic realizations and theory, vision chips, massively parallel analog processing systems, chaotic circuits, and communication devices.

Dr. Espejo-Meana was co-recipient the 1995 Guillemin–Cauer Award of the IEEE Circuits and Systems Society and the Best Paper Award of the 1995 European Conference on Circuit Theory and Design.



Rafael Domínguez-Castro received the five-year degree in electronic physics (Licenciado en Física Electrónica) in 1987, the M.S. equivalent in microelectronics in 1989, and the Doctor en Ciencias Físicas degree in 1993, all from the University of Seville, Spain.

Since 1987, he has been with the Department of Electronics and Electromagnetism, University of Seville, where he is currently Professor in electronic engineering and in neural networks. He is also with the Department of Analog Circuit Design, Institute of Micro-electronics of Seville, IMSE-CNM-CSIC. He has research interests in the design of analog and mixed-signal VLSI circuits for nonlinear signal processing, in particular optimizers and vision chips. He also has interest in optimization of analog integrated circuits.

Dr. Domínguez-Castro was co-recipient of the 1995 Guillemin–Cauer Award of the IEEE Circuits and Systems Society and the Best Paper Award of the 1995 European Conference on Circuit Theory and Design.

Tamás Roska (M'87–SM'90–F'93) received the Diploma in electrical engineering from the Technical University of Budapest, Budapest, Hungary, in 1964 and the Ph.D. and D.Sc. degrees in Hungary in 1973 and 1982, respectively.

Since 1964, he has held various research positions. From 1964 to 1970, he was with the Measuring Instrument Research Institute, Budapest. From 1970 to 1982, he was with the Research Institute for Telecommunication, Budapest (serving also as the Head of Department for Circuits, Systems, and Computers), and since 1982, he has been with the Computer and Automation Institute, Hungarian Academy of Sciences, where he is Head of the Analogic and Neural Computing Research Laboratory. He has taught several courses at various universities. Presently, at the Technical University of Budapest, he is teaching graduate courses on "Emergent Computations" and "Cellular Neural Networks." In 1974, and in each year since 1989, he has been Visiting Scholar at the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, and recently a Visiting Research Professor at the Vision Research Laboratory, University of California, Berkeley. His main research areas are cellular neural networks, nonlinear circuits and systems, neural circuits, and analogic spatiotemporal supercomputing. He has published more than 100 research papers and four books (some as co-author), and held several guest seminars at various universities and research institutions in Europe, the United States, and Japan.

Dr. Roska is a co-inventor of the CNN Universal Machine (with L. O. Chua), a U.S. patent of the University of California with worldwide protection, and the analogic CNN Bionic Eye (with F. Werblin and L. O. Chua), another U.S. patent of the University of California. He has contributed also to the development of the various physical implementations of these inventions making this cellular analogic supercomputer a reality. He is a member of several Hungarian and international scientific societies. Since 1975, he has been a member of the Technical Committee on Nonlinear Circuits and Systems of the IEEE Circuits and Systems Society. Between 1987 and 1989, he was the founding Secretary and later served as Chairman of the Hungary Section of the IEEE. Recently, he has served twice as Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, as Guest Co-Editor of special issues on Cellular Neural Networks of the *International Journal of Circuit Theory and Applications* (1992, 1996, 1998/1999) and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (1998). He is a member of the Editorial Board of the *International Journal of Circuit Theory and Applications*. He was elected IEEE Fellow for "contributions to the qualitative theory of nonlinear circuits and the theory and design of programmable cellular neural networks." In 1993, he was elected a member of the Academia Europaea (European Academy of Sciences, London) and the Hungarian Academy of Sciences. For technical innovations, he received the D. Gabor Award for establishing a new curriculum in information technology and for his scientific achievement, he was awarded the A. Szentgyörgyi Award and the Széchenyi Award, respectively. In 1994, he became the elected active member of the Academia Scientiarium et Artium Europaea (Salzburg).

Tibor Kozek, photograph and biography not available at the time of publication.

Leon O. Chua (S'60–M'62–SM'70–F'74) is currently a Professor of electrical engineering and computer sciences at the University of California, Berkeley. His research interests are in the areas of general nonlinear network and system theory. He has been a consultant to various electronic industries in the areas of nonlinear network analysis, modeling, and computer-aided design. He is the author of *Introduction to Nonlinear Network Theory* (New York: McGraw-Hill, 1969) and *CNN: A Paradigm for Complexity* (Singapore: World Scientific, 1998), and a co-author of the books *Computer Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques* (Englewood Cliffs, NJ: Prentice-Hall, 1975), *Linear and Nonlinear Circuits* (New York: McGraw-Hill, 1987), *Practical Numerical Algorithms for Chaotic Systems* (New York: Springer-Verlag, 1989), and *Methods of Qualitative Theory of Nonlinear Dynamics* (Singapore: World Scientific, 1998). He has published many papers in the area of nonlinear networks and systems. He served as Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS from 1973 to 1975 and as President of the IEEE Circuits and Systems Society in 1976. He is presently the Editor of the *International Journal of Bifurcation and Chaos* and a Deputy Editor of the *International Journal of Circuit Theory and Applications.*

Prof. Chua is the holder of seven U.S. patents. He is also the recipient of several awards and prizes, including the 1967 IEEE Browder J. Thompson Memorial Prize Award, the 1973 IEEE W. R. G. Baker Prize Award, the 1974 Frederick Emmons Terman Award, the 1976 Miller Research Professorship, the 1982 Senior Visiting Fellowship at Cambridge University, the 1982/1983 Alexander von Humboldt Senior U.S. Scientist Award at the Technical University of Munich, the 1983/1984 Visiting U.S. Scientist Award at Waseda University, Tokyo, the IEEE Centennial Medal in 1985, the 1985 Myril B. Reed Best Paper Prize, the 1985 and 1989 IEEE Guillemin–Cauer Prizes, and the 1995 M. E. Van Valkenburg Award. In 1986, he was awarded a *Professor Invité* International Award at the University of Paris-Sud from the French Ministry of Education. He was also awarded a *Doctor Honoris Causa* from the Ecolé Polytechnique Fédérale-Lausanne, Switzerland, in 1983, and Honorary Doctorate from the University of Tokushima, Japan, in 1984, and Honorary Doctorate from the Technische Universität Dresden in 1992, a *Doctor Honoris Causa* from the Technical University of Budapest, Hungary, in 1994, a *Doctor Honoris Causa* from the University of Santiago de Compostela, Spain, in 1995, a *Doctor Honoris Causa* from the University of Frankfurt, Germany, in 1996, and a *Doctor Honoris Causa* from the Technical University of Iasa, Romania, in 1997. He was elected a foreign member of the European Academy of Sciences (Academia Europaea) in 1997.