An 1 GHz Class E LDMOS Power Amplifier

Andreas Ådahl, Herbert Zirath

Microwave Electronics Laboratory, Chalmers University of Technology, Sweden
Phone: +46-(0)-31-772 50 48, Fax: +46-(0)-31-16 45 13
E-mail: adahl@ep.chalmers.se

Abstract--A class E power amplifier working at 1 GHz and with an LDMOS transistor as switching element has been developed. The circuit is implemented with lumped and distributed elements. An output power of 6.2 W at 69 % drain efficiency with a gain of 11 dB was obtained at 1 GHz. Both simulations and measurements of the amplifier are presented within this paper. This is to our knowledge the highest efficiency and output power reported for a class E amplifier at 1 GHz.

I. Introduction

Both in the civilian and military industry there is a need for power amplifiers with high efficiency. Increasing the efficiency of power amplifiers will decrease size and power consumption and increase output power. Decreased power consumption will also lead to better reliability and lifetime.
Theoretical drain efficiencies of 100 % can be achieved with switching mode amplifier like Class E. The principle was first described by Ewing in 1964 [1], who demonstrated an amplifier with 20 W output power and 94 % efficiency at 500 KHz. In the mid seventies the Sokals [2] developed this technique and reported an amplifier with an output power of 26 W at 96 % efficiency in the MHz range.

In recent years Class E amplifiers have been made successfully up to about 5 GHz with transistor technologies like MESFET and HBT. Unfortunately these technologies often have low breakdown voltage, which limits the output power.
Other interesting transistor technologies is MOS transistors with high breakdown voltages, which can be as high as 60 V. This technology makes it possible to design Class E amplifiers with high output power and high efficiency.
One example of a high efficient Class E amplifier implemented with an LDMOS transistor as switching element has been reported in [3]. The amplifier achieved an output power of 54 W with 70 % efficiency at 144 MHz.

In this paper a Class E amplifier with an LDMOS transistor as switching element has been developed. The amplifier is implemented with both lumped and distributed elements. Variable capacitors are used in the amplifier in order to tune for maximum efficiency at 1 GHz.

II. Class E amplifier

The ideal Class E circuit is shown in fig. 1. This circuit is composed of a parallel capacitor C_p, which is shunted with the switch. This capacitance will minimize the overlap between the current and the voltage waveforms. The output matching network consists of a simple series resonance circuit with the RF-load included. Another important part in the Class E circuit is the RF-choke, which can be treated as a current source.
As the transistor turns off, the current flows into the resonance network and causes a transient voltage at the drain of the transistor to rise and fall. If the matching network is properly designed, the voltage will return to zero when the transistor turns on.

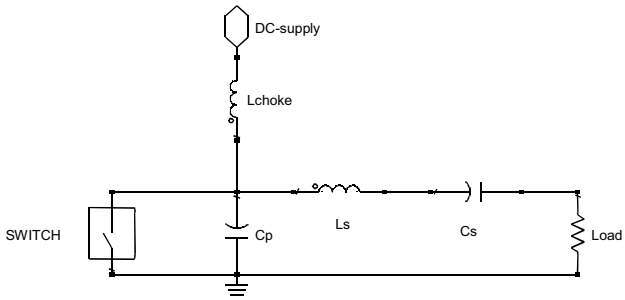


Fig. 1. Ideal Class E circuit.

At the design frequency the transistor and passive components cannot be regarded as ideal and the analytical expression [4] cannot be used. The improvements in circuit simulations and modeling of active devices has made it possible to use programs like ADS to simulate Class E amplifiers with good accuracy.
The LDMOS transistor used in this work is a MRF282SR1 from Motorola. This transistor is capable to deliver 10 W with 40 % efficiency at 2 GHz in class A mode. The transistor model is based on the "Root" model and is available from Motorola's web-site.

The real Class E circuit is slightly different compared to the circuit in fig. 1. First the parallel capacitor C_p is completely absorbed by the output capacitance of the transistor. Secondly the RF-load is transformed to 50 Ω by a parallel capacitor and a series inductor. The input match of the amplifier was implemented with a series

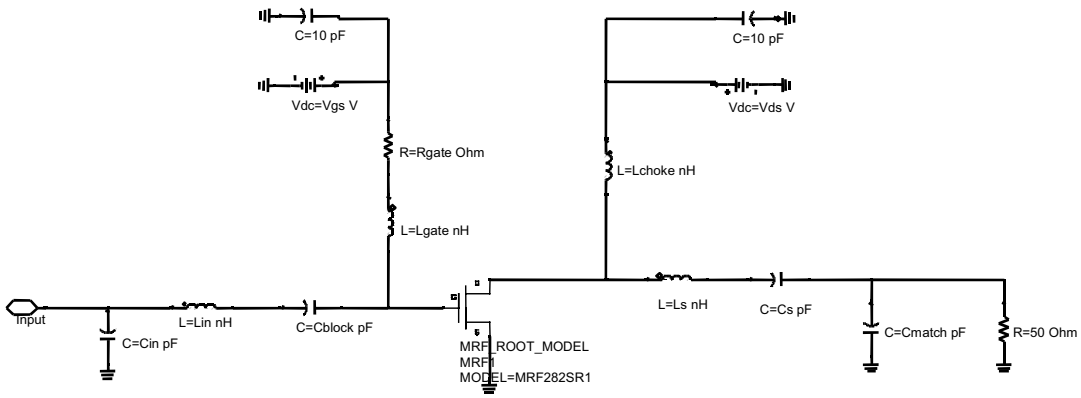


Fig. 2. Complete circuit layout the amplifier.

Table 1. Optimized component values @ 1 GHz.

C_{in} [pF]	L_{in} [nH]	C_{block} [pF]	L_{gate} [nH]	R_{gate} [kΩ]	L_{choke} [nH]	L_s [nH]	C_s [pF]	C_{match} [pF]
22	2.65	30	20	10	20	7.9	5.5	9.3

inductor and a parallel capacitor. Finally the Q_L-value of the series resonant network was chosen to be low, of the order 5, in order to have low sensitivity of the circuit to the series resonator values. The complete Class E circuit can be seen in fig. 2. Note that the inductive elements at the output matching network and the input matching network are implemented with transmission-line elements.

III. Simulations

All the simulations were performed with Agilent's ADS harmonic balance simulator. The circuit layout in fig. 2 was inserted into ADS and the output matching network was then optimized for highest drain efficiency and output power. In table 1 we can see the component values obtained from this optimization. The input matching network was designed from large signal s-parameters simulations in ADS. Most of the capacitors and inductors were then substituted by accurate models, which were derived from measurements made by the manufacturer.

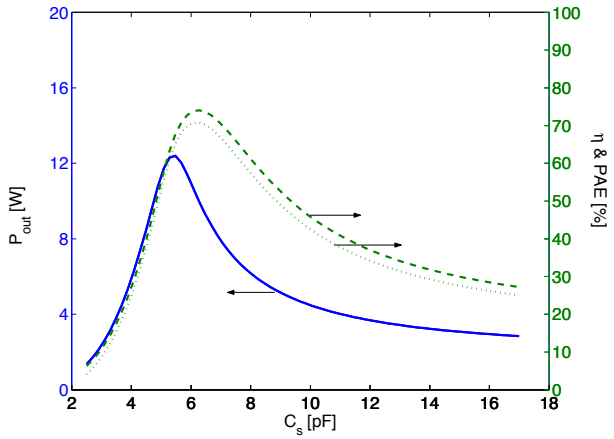


Fig. 3 Output power, drain efficiency and PAE as a function of the capacitance C_s.

The output power and efficiency are quite sensitive to variations in the resonance network. The output power, drain efficiency and PAE are plotted in fig. 3 for different values of the capacitance C_s in the resonance network.

The maximum efficiency is not obtained for the same value of C_s as gives the highest output power. This also means that the resonance network is slightly mistuned compared to the input frequency.
The simulations predicted a drain efficiency of about 74 % at an output power of 10 W and 66 % drain efficiency at an output power of 12.4 W.

In fig. 4 we can see the drain current through and drain voltage over the transistor when the amplifier is tuned to maximum drain efficiency.

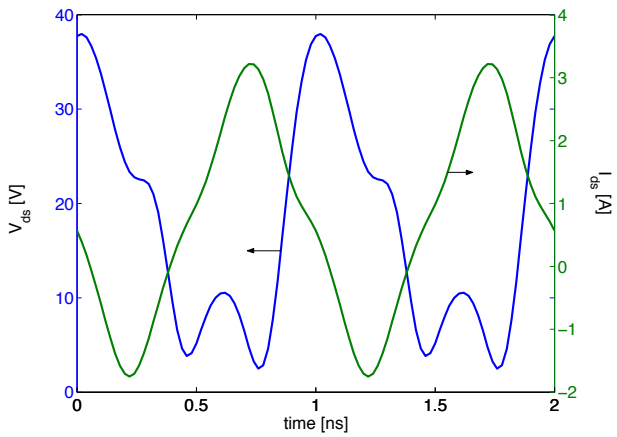


Fig. 4. Drain to source voltage and drain to source current. (C_s is tuned for maximum efficiency)

The drain to source current I_{ds} is nearly sinusoidal, see fig. 4. This can be explained by the fact that the parallel capacitance, Cp, is completely absorbed by the output capacitance of the transistor.

IV. Layout and Assembly

The inductors in the bias network are air core inductors from Coilcraft and most of the capacitors in the amplifier are of the type ATC100B. The variable capacitors used in the circuit are from Johanson technologies, they were characterized with a HP8510c VNA. In fig. 5 we can see how the tunable capacitors varies with frequency for three different positions.

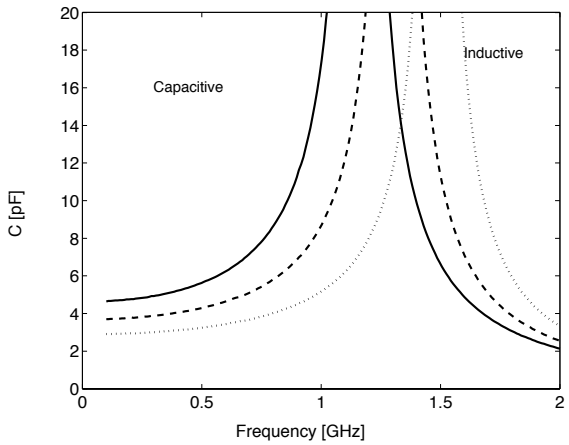


Fig. 5. Johanson's Gigatrim variable capacitors as a function of frequency for three different tuning positions.

The tunable range at 1 GHz is approximately from 0 to 17 pF. The drawback with these capacitors is the low resonance frequency, which means that the capacitances are inductive at higher harmonics.

In fig. 6 we can see the complete layout of the amplifier. The substrate on which the circuit is implemented has the following properties: $\varepsilon_r = 2.75$, H = 0.8 mm, T = 35 µm and Tanδ = 0.0030 @ 10 GHz.

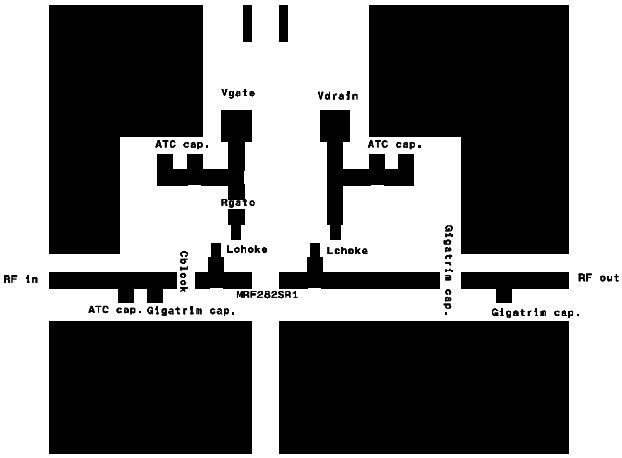


Fig. 6. Complete layout of the Class E circuit. (Scale not 1:1)

The substrate, the passive components and the transistor were then mounted on a heat sink in order to cool the amplifier. The fully mounted Class E amplifier is shown in fig. 7.

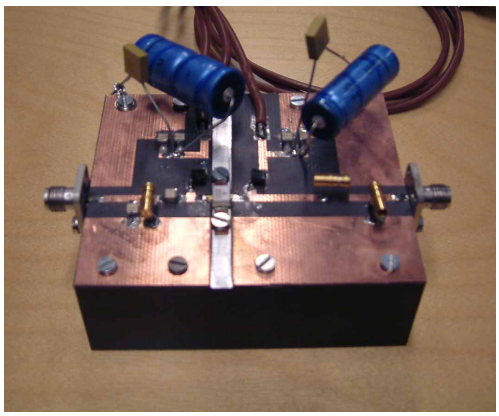


Fig. 7. Fully mounted Class E amplifier.

V. Characterization of the Amplifier

The amplifier was characterized with respect to output power, drain efficiency and PAE. To monitor the output power a Boonton power meter was used and a HP83650B Swept signal generator was used to generate the input power.

The output power and efficiency can be tuned with the variable capacitor in the series resonance network. In fig. 8 we can see how those parameters changes when the capacitance is varied.

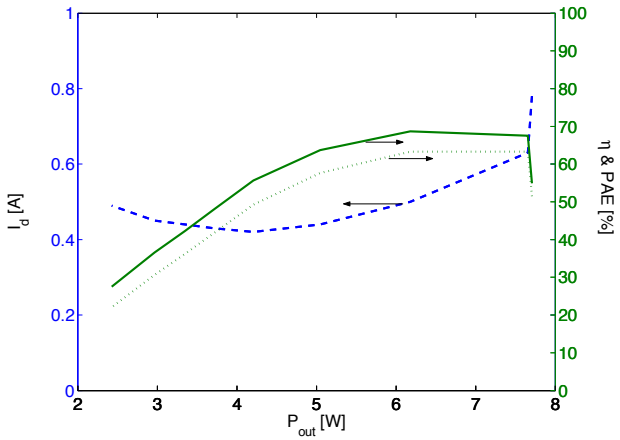
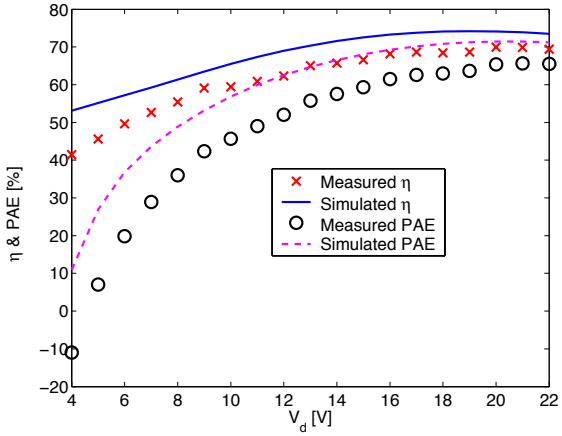


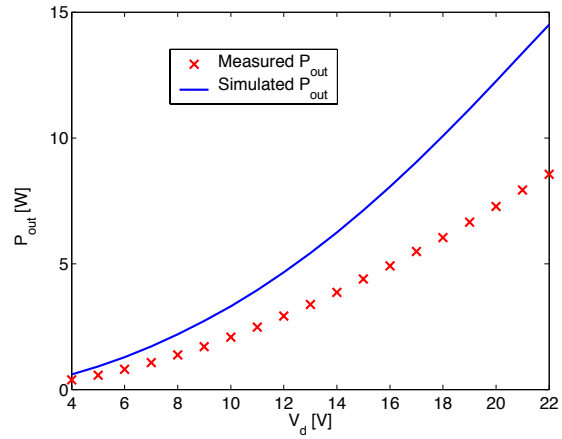
Fig. 8. Drain current, drain efficiency and PAE vs output power (when the variable capacitor in the resonance network is tuned). Vg = 3.5 V, Vd = 18 V and Pin = 0.48 W.

The figure shows a maximum drain efficiency of 69 % at 6.2 W and a drain efficiency of 55 % at 7.7 W. This result agrees quite well with the simulations. However, there are some differences. The simulations predict a slightly higher efficiency and output power, which is due to metal losses and parasitics in the tunable capacitors. Mismatch at the input port can also contribute to the lower value obtained from the measurements.

The typical quadratic behavior of the output power as function of drain supply voltage is shown in fig. 9.



(a)



(b)

Fig. 9. (a) Drain efficiency and PAE vs DC supply voltage. (b) Output power vs DC supply voltage. Vg = 3.5 V and Pin = 0.48 W. (C_s tuned for maximum efficiency)

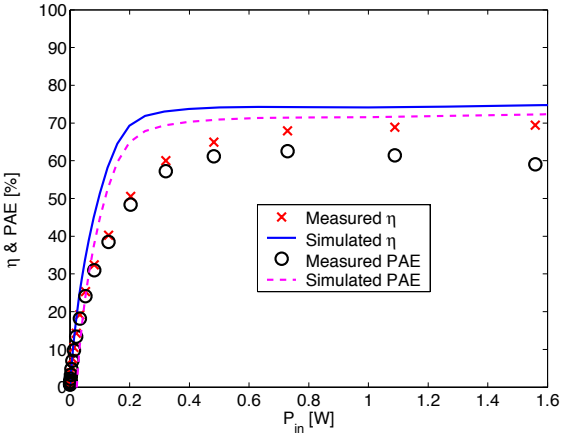
We can see that the drain efficiency is constant over a wide rage of dc supply voltages, which means that amplitude modulation is an efficient method for this type of amplifier.

In fig. 10 the output power, drain efficiency and PAE vs input power is shown. It is clear from this figure that an input power of about 0.5 W or higher is needed in order to achieve saturated operation.

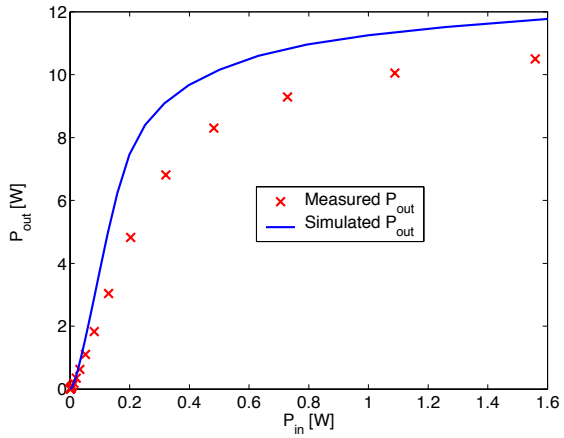
The second harmonic is approximately 20 dB below the fundamental. In a typical Class E amplifier, the second harmonic is expected to be about 30 – 50 dB below the fundamental. A low Q-value of the resonance network can be one explanation to the insufficient reduction of harmonics in the amplifier circuit.

VI. Conclusions

A Class E amplifier working at 1 GHz has been implemented and with an LDMOS transistor as switching element. The implemented circuit topology gave a maximum drain efficiency of 69 % at 6.2 W with 0.48 W of input power. It was found that the output power could be tuned from 6.2 W to 7.7 W with the variable capacitor in the resonance network. The correspondence between simulations and measurements is quite good, but there is room for improvements. Accurate models of the tunable capacitors are one of the improvements that could be made in the future.



(a)



(b)

Fig. 10. (a) Drain efficiency and PAE vs input power. (b) Output power vs input power. Vg = 3.5 V and Vd = 18 V.

References

[1] G. G Ewing, “High –Efficiency Radio-frequency Power Amplifiers”, Corvallis Oregon, USA, Oregon State University, 1964.

[2] N. O. Sokal and A. D. Sokal, “Class E a new class of high-efficiency tuned single-ended switching power amplifiers”, IEEE J. Soild-State Circuits, vol. SC-10, No. 3, pp. 168-176, June 1975.

[3] H. Zirath and D. B. Rutledge, “An LDMOS VHF Class-E power Amplifier Using a High-Q Novel Variable Inductor”, IEEE Transactions on Microwave Theory and Techniques, Vol. 47, No. 12, pp. 2534-2538, December 1999.

[4] S. C. Cripps, “RF Power Amplifiers for Wireless Communications”, Artech House, Boston, 1999.

[5] A. J. Wilkinsin and J. K. A. Everard, “Transmission-Line Load-Network Topology for Class-E Power Amplifier”, IEEE Transactions on Microwave Theory and Techniques, Vol. 49, No. 6, pp. 1202-1204, June 2001.

[6] S. Kee, “The Class E/F Family of Harmonic-Tuned Switching Power amplifiers”, Ph.D. Dissertation, Department of Electrical Engineering, Caltech – Pasadena, 2002.

[7] F. H. Raab, “Idealized Operation of the Class E Tuned Power Amplifier”, IEEE Transactions on Circuits and Systems, Vol. CAS-24, No. 12, pp. 725-735, December 1977.