An 11-bit, 12.5-MHz, Low-Power, Low-Voltage, Continuous-Time Sigma-Delta Modulator in 0.13 µm CMOS Technology

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Abstract

The trend of the last years in the industry of integrated circuits has shifted more and more from the analog toward the digital world. Thanks to the CMOS technology an impressive miniaturization of the electronic active elements has been made possible, which allows for low cost and mass production of complex circuits on a single chip. The natural candidates for very large-scale integration (VLSI) technologies are digital circuits since these can be relatively easily scaled down with large improvements in the operating speed. On the other hand virtually all natural signals are of analog nature, requiring dedicated circuits converting these signals in the digital form, in order to process them with the digital circuitry. Such circuits are named analog-to-digital converters (ADC) and find wide diffusion in all devices dealing with natural signals like images, sound, temperature, radio signals, etc. In order to reduce the equipment cost the integration of the ADC on the same chip containing the digital circuits is highly desirable. Actually, modern highly miniaturized CMOS technologies are not very suitable for analog circuits, as they feature rather poor analog electrical properties. To cope with this, particular ADC topologies are required which are robust enough to be implemented in CMOS technology with a feature size in the order of 100 nanometers. One of the most promising architecture for CMOS processes is the continuous-time sigma-delta (ΣΔ) modulator. This achieves very large accuracy and performance by optimally using the main advantage of the modern CMOS technology: high speed. In this work a study of low-power, high-speed continuous time ΣΔ modulators is presented. A possible application of this class of modulators is represented by high-speed portable communication devices of the next generation. The author focuses on design strategies at architectural and transistor level in order to keep to power consumption to a very low amount without sacrificing the modulator resolution.

The modulator proposed in this work is based on a 0.13 μm CMOS process and achieves an effective resolution of 11 bits at a signal bandwidth of 12.5 MHz dissipating 11.4 mW of power. It is shown how to compensate for the unavoidable excess loop delay which degrades the performance achievable, applying this technique to a resonator-based continuous-time loop filter. A model is illustrated enabling the design of RC-integrators based on two-stage Miller compensated operational amplifiers. Furthermore a resistor-based feed-forward loop filter topology is implemented to reduce the power consumption of the filter. Another low-power benefit is achieved by merging two DAC into a single DAC without altering the functionality of the modulator.

The proposed modulator obtains a very good figure of merit according to post-layout simulation results when compared to the literature state-of-the-art.

Zusammenfassung

Der Trend der letzten Jahre in der Industrie der integrierten Schaltungen hat sich immer mehr von der analogen zur digitalen Welt verschoben. Dank der CMOS Technologie ist eine beeindruckende Miniaturisierung der aktiven elektronischen Bauelemente möglich gewesen, welche eine Reduzierung der Herstellungskosten sowie die Massenproduktion von komplexen Schaltungen auf einem einzigen Chip ermöglicht. Die natürlichen Kandidaten für Technologien mit sehr hohem Integrationsgrad (VLSI) sind Digital-Schaltungen, da diese relativ einfach verkleinert werden können mit erheblicher Erhöhung der Betriebsgeschwindigkeit. Andererseits sind geradezu alle natürlichen Signale analog und benötigen dedizierte Schaltungen für deren Umwandlung in die digitale Form, um diese Signale mit Digital-Schaltungen weiter verarbeiten zu können. Diese Schaltungen werden Analog-Digital-Umwandler genannt (ADC) und finden in praktisch allen Geräten Anwendung, welche sich mit natürlichen Signalen wie Bildern, Ton, Temperatur, Radiofrequenz-Signalen, etc. befassen. Um die Kosten der Geräte zu minimieren, ist die Integration der ADC auf demselben Chip, welcher die Digital-Schaltungen enthält, höchst wünschenswert. Moderne hochminiaturisierte CMOS-Technologien sind aber nicht sehr geeignet für Analogschaltungen, da sie bescheidene analoge elektrische Eigenschaften aufweisen. Um dies zu meistern, werden besondere ADC-Topologien benötigt, welche genügend robust sind, um in einer CMOS-Technologie mit einer Strukturgröße von ca. 100 Nanometern implementiert zu werden. Eine vielversprechende Architektur für CMOS-Prozesse ist der zeitkontinuierliche Sigma-Delta-Modulator ($\Sigma\Delta$). Diese Architektur erzielt große Genauigkeit und Performance, indem der Hauptvorteil moderner CMOS-Technologien ausgenutzt wird: die hohe Geschwindigkeit. In dieser Arbeit wird eine Studie über leistungsarme zeitkontinuierliche $\Sigma\Delta$-Modulatoren mit hoher Geschwindigkeit präsentiert. Diese Klasse von Modulatoren findet eine mögliche Anwendung in tragbaren breitbandfähigen Mobilfunkgeräten der nächsten Generation. Der Autor konzentriert sich auf die Design-Strategien auf Architektur- und Transistorebene mit dem Ziel, die Verlustleistung des Modulators ohne Beeinträchtigung dessen Auflösung zu reduzieren.

Der in dieser Arbeit präsentierte Modulator basiert auf einem 0.13 µm CMOS-Prozess und erzielt eine effektive Auflösung von 11 Bits bei einer Signal-Bandbreite von 12.5 MHz und einer Verlustleistung von 11.4 mW. Es wird gezeigt, wie das unvermeidbare Excess-Loop-Delay, welches die erzielbare Performance verschlechtert, kompensiert werden kann. Diese Technik wird auf ein resonator-basiertes, zeitkontinuierliches Schleifenfilter angewendet. Ein Modell für das Design von RC-Integratoren, welche auf zweistufigen Miller-kompensierten Operationsverstärkern basieren, wird erläutert. Ferner wird eine widerstandsbasierte Feed-Forward Filterarchitektur implementiert, um die Verlustleistung des Schleifenfilters zu reduzieren. Ein zusätzlicher Vorteil bezüglich der Verlustleistung ist erzielt worden, indem zwei verschiedene DAC-Stufen, welche Bestandteile des Modulators sind, in einem einzelnen DAC zusammengefasst werden ohne die Funktionalität des Modulators zu verändern.

Der vorgeschlagene Modulator erzielt gemäß Post-Layout-Simulationen im Vergleich mit dem heutigen Stand der Technik einen sehr guten Gütefaktor.

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Chapter 1

Introduction

1.1. Motivation

The trend of the last decades clearly shows that the implementation of devices for signal processing in every possible field, such as telecommunications, video, audio, medical equipment is moving toward the digital world. This is because of the large number of advantages, which digital devices offer: high integration, simple size scaling, robustness toward noise and other sources of disturbance, programmability. Hence the famous motto "the world goes digital". Nevertheless the world is analog in all its aspects, therefore devices are needed, which allow an interface between the analog world and the digital devices. This interface consists in the analog-to-digital converters and their counterpart, the digital-to-analog converters. The domination of digital circuits in the semiconductor market has led to a technology optimization primarily toward this sort of circuits. Because of its good suitability for digital circuits the CMOS technology has nowadays the largest market share. This technology provides considerable advantages toward other technologies, such as MOS self-alignment, which enables the fabrication of extremely small components and low static power dissipation, a precondition for the implementation of low-power devices. The most important aspect taken into consideration from the industry so far is the miniaturization of the transistors, maximizing the number of components on the same area hence minimizing the cost of the equipment. On the other size the continuous scaling of the dimensions of the transistors has led to a worsening of the analog electrical properties of these fundamental elements. Going into detail, we can observe that the progressive reduction of the transistor channel length has led to a reduction of the maximum available gain, the so called transistor self-gain g_m/g_{ds}, i.e. the ratio of the transconductance to the output conductance. Furthermore, the continuous reduction of the oxide thickness has put stringent limits on the maximum available supply voltage. This reduces in turn the maximum available signal amplitude, hence limiting, considering the circuit thermal noise constant, the maximum achievable SNR. To counteract this trend, the thermal noise must be reduced, which is obtained increasing the power consumption.

Another issue of modern sub-µm CMOS technologies is represented by the difficulty in reducing the threshold voltage V_T at the same rate as the supply voltage [Ito08]. This is desirable to enable low-voltage analog circuits to generate large signal swing. A bound in the scaling of the threshold voltage is represented by the leakage currents of transistors which are supposed to be in the off-state, which rise exponentially when reducing V_T, hence increasing the power consumption. The trend of the most important analog parameters for different technology nodes is depicted in Fig. 1.1 [Pek04].

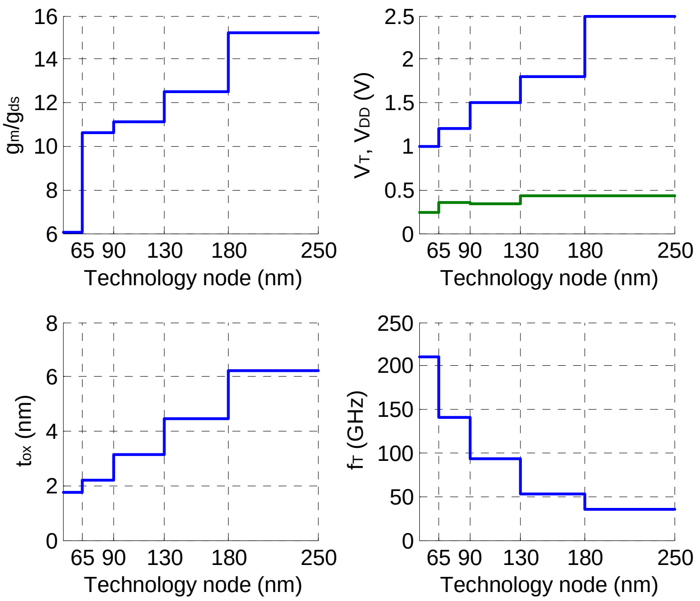


Fig. 1.1. Trend of the most important analog parameters for different technology nodes [Pek04]

1.2. Objective and outline of this work

The objective of this research work is to show the feasibility of a low-voltage, low-power, high-speed Sigma-Delta analog-to-digital converter (ADC) for portable telecommunication devices. The proposed ADC could be employed in devices based on the mobile wireless standard WiMAX [Wim06] or for video or medical imaging. The priority is given to a low-cost device, which should be achieved using a standard CMOS technology. This writing focuses on solutions at both architectural and transistor level to reduce the power consumption without sacrificing speed and performance.

The work is articulated as in the following: chapter 2 introduces the basics of the A/D conversion and analyzes the Sigma-Delta family in particular; chapter 3 concentrates on system level considerations and on the high-level architecture of the proposed ΣΔ modulator; chapter 4 describes into detail the blocks of the proposed modulator up to the layout and shows the simulation results; finally chapter 5 summarizes the achieved results comparing them with the state of the art.

Chapter 2

Basics of analog-to-digital conversion

2.1. Analog-to-digital conversion

The analog to digital conversion is the process of converting an analog signal into a time-discrete, amplitude-discrete digital signal. The operation is performed in two steps: the sampling and the quantization. The device realizing these two operations is called analog-to-digital converter (ADC).

Consider a continuous-time signal $x(t)$ as shown in Fig. 2.1a. This signal is sampled at constant time instants which are multiple of T_s. A time discrete signal is obtained $x[k]=x(nT_s)$. The process of ideal sampling can be mathematically seen as the product of the continuous-time signal $x(t)$ with a Dirac comb signal $p(t)$ with period T_s. We obtain:

$$x(nT_s) = x(t) \cdot p(t) = \sum_{n=-\infty}^{\infty} x(nT_s) \cdot \delta(t - nT_s) \tag{2.1}$$

Transforming this signal in the frequency domain by means of the Fourier transform we find:

$$X_d(\omega) = \frac{1}{2\pi} X(\omega) * P(\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X(\omega) \cdot \delta\left(\omega - \frac{2\pi k}{T_s}\right) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X\left(\omega - \frac{2\pi k}{T_s}\right) \tag{2.2}$$

Equation (2.2) clearly shows that the spectrum $X_d(\omega)$ of the time-discrete signal is periodic. An important consequence of this is that, as stated by the Nyquist-Shannon sampling theorem, the minimum sampling frequency f_s allowing a perfect reconstruction of a low-pass signal with a limited bandwidth f_B is $f_s=2f_B$. This limitation avoids the unwanted effect of aliasing, namely the superposition of "replicas" of the signal in the frequency domain which would cause signal deterioration and information loss. In order to satisfy this condition the analog signal must be bandlimited by means of a so called anti-aliasing filter.

Fig. 2.1a-b and Fig.2.2a-b show the process of sampling both in the time and in the frequency domain.

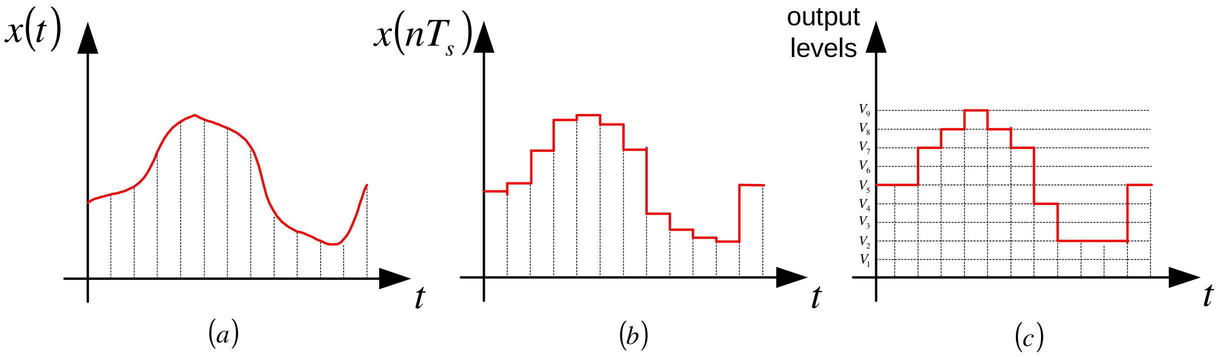


Fig. 2.1. Sampling and quantization in the time domain

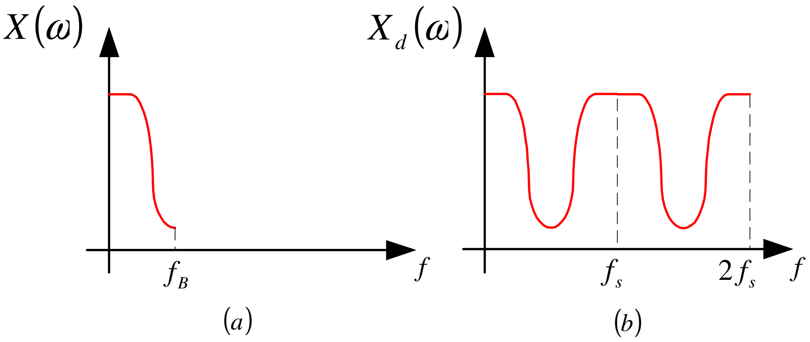


Fig. 2.2. Sampling in the frequency domain

The quantization process consists in mapping the infinite possible amplitude values of the input signal into a finite set of discrete values (Fig. 2.2c). This is done by comparing the signal with a finite set of equidistant threshold values and associating the signal to the nearest threshold. This process is unavoidably associated with information loss, which is depending on the deterministic error introduced by the quantization. Assuming an N-bit quantization, hence 2^N quantization levels and a signal with limited amplitude, such that the quantizer is not overloaded, the introduced quantization error ε_Q will be limited to:

$$-\frac{\Delta U}{2} \leq \varepsilon_Q \leq \frac{\Delta U}{2} \tag{2.3}$$

where ΔU is the width of the quantization interval, that is the distance between two consecutives thresholds. This is equal to:

$$\Delta U = \frac{V_{FS}}{2^{N-1}} \tag{2.4}$$

V_{FS} is the full-scale input signal and N again is the resolution of the quantizer in bits. Fig.2.3 depicts the input-output static characteristic of a three-bit (eight level) quantizer and the signal depending quantization error.

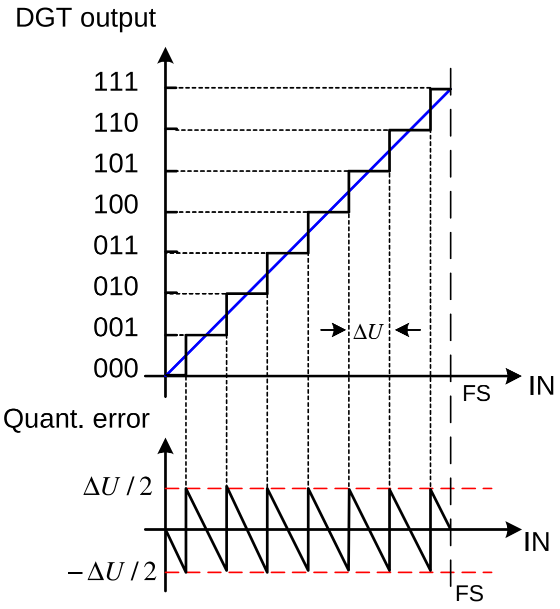


Fig. 2.3. Ideal ADC characteristic (above) and quantization error (below)

2.2. Performance metrics

For the characterization of an analog-to-digital converter we can distinguish two categories of performance metrics: static and dynamic.

2.2.1. Static metrics

All static metrics can be determined by comparison of the input-output characteristic of the ADC under test (real ADC) with that of the ideal ADC. In the following the main static parameters are described.

Linear errors

- The offset error (Fig 2.4a), defined as the intercept of the line interpolating the input-output characteristic with the horizontal axis. This error typically arises because of a shift of all reference voltages used as thresholds for the ADC, i.e. because the ground voltage is larger than zero.

- The gain error (Fig 2.5b), given by the ratio between the slope of the line interpolating the input-output characteristic of the real ADC and the slope of the ideal ADC. This error typically arises because all reference voltages are larger (or smaller) than the nominal value of the same relative amount, that is, all quantization steps are larger (or smaller) but still identical. For instance, this is the case when the threshold voltages of the ADC are generated by dividing a reference voltage by means of a resistive voltage divider and the reference voltage is larger (or smaller) than the nominal value.

Non-linear errors

These parameters are measured after removal of the two linear errors listed above and typically arise because of mismatch of the elements used in the A/D conversion, which are supposed to be identical (i.e. resistors or capacitors).

- Differential non-linearity (DNL) (Fig 2.5c), defined for each quantization step as the difference between the step width of the real ADC and the ideal quantization step *ΔU* normalized to the *ΔU*

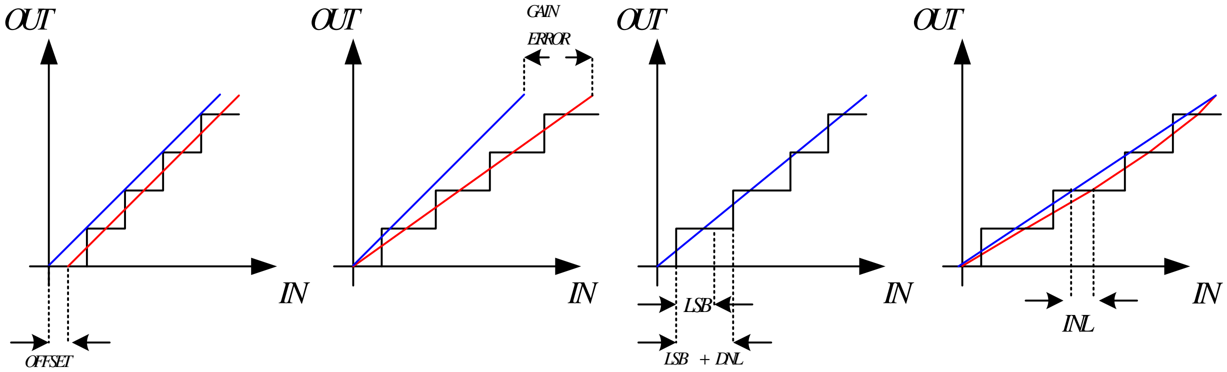
$$DNL(n)=\frac{V(n)-V(n-1)-\Delta U}{\Delta U} \tag{2.5}$$

  DNL typically arises in presence of *random* mismatch of the elements used for the conversion and provides information about the *local* deviation of one step toward the ideal one.

- Integral non-linearity (INL) (Fig 2.d) is defined as the sum of the DNL of the real ADC over the whole input-output characteristic.

$$INL(n)=\sum_{1}^{k} DNL(k) \tag{2.6}$$

  INL is the *accumulated* mismatch of the elements used in the conversion and provides information about the *maximum* (global) deviation of the real ADC characteristic toward the real one. It is also interesting to note that, while the DNL has a high-frequency spatial content, the INL has low-frequency spatial content because of the accumulation as in Eq. (2.6).



(a) (b) (c) (d)

Fig. 2.4. Static errors in the ADC characteristic: a) offset, b) gain, c) DNL, d) INL

2.2.2. Dynamic metrics

Dynamic metrics refer to the dynamic behavior of the ADC and are determined by examining the output spectrum of the ADC. The most important dynamic metrics are listed in the following:

- Signal-to-noise ratio (SNR) is the ratio of the signal power to the noise power in the signal band, expressed in dB

$$SNR = 10\log\frac{P_S}{P_N} \tag{2.7}$$

- Signal-to-noise-and-distortion ratio (SNDR) is the ratio of the signal power to the noise power in the signal band and the power of all signal harmonics in the signal band, expressed in dB

$$SNDR = 10\log\frac{P_S}{P_N + P_D} \tag{2.8}$$

- Spurious free dynamic range (SFDR) is defined as the difference in dB between the signal amplitude and the amplitude of the largest spurious signal in the signal band

$$SFDR = 10\log\frac{P_S}{P_{D,\max}} = P_{S,dB} - P_{D,\max,dB} \tag{2.9}$$

- Total harmonic distortion (THD) is defined has the ratio of the total power of the harmonics to the signal power, expressed in dB

$$THD = 10\log\frac{\sum_i P_{D,i}}{P_S} \tag{2.10}$$

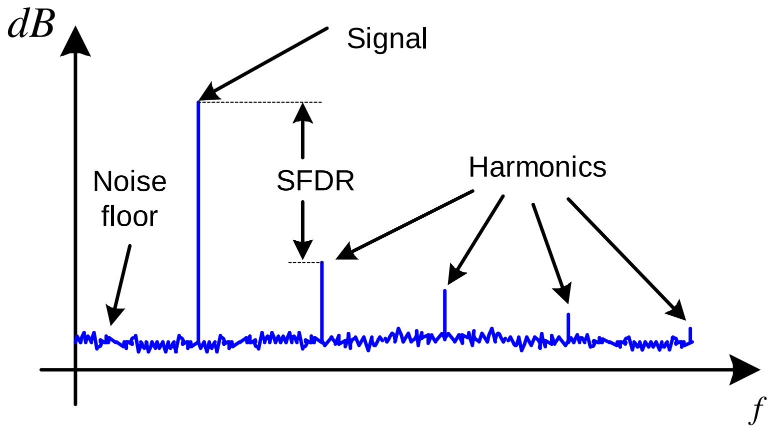


Fig.2.5. ADC output spectrum. Signal, harmonics and noise floor are highlighted

2.3. Linearized model

It is difficult to mathematically model the deterministic error introduced by the quantization process, since we have to cope with a nonlinear element: the quantizer. The problem can be simplified by making following assumptions:

1) the number of quantization levels is large;
2) the quantizer is not overloaded;
3) the input signal changes “rapidly”, in such a way that successive output values are not correlated.

While the first two conditions are not difficult to be satisfied, the third one is hardly realized. For example just consider a constant input signal: in this case also the output will be constant and the output values are fully correlated. Nevertheless these assumptions lead to an approximate but in the reality good working model which is a very powerful instrument for designing an ADC. It can be shown that, if all three assumptions hold, the introduced quantization error presents white noise properties. We can then simplify the problem by replacing the quantizer, a strongly nonlinear block, by a linear amplifier with gain k_q and by adding white noise at its output (Fig. 2.6). The gain is given by the slope of the line interpolating the static input-output characteristic of the quantizer.

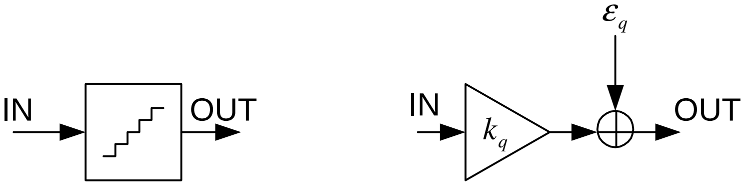


Fig. 2.6. Left: nonlinear quantizer. Right: linear model with added white noise

By replacing the quantization *error* by quantization *noise*, a purely deterministic process is modeled as a stochastic process. To quantify the equivalent white noise we need to calculate its variance. If condition 3) is valid, that is, the input signal changes continuously and in a non-regular way, we can assume that the probability that the signal lays somewhere between two thresholds is uniformly distributed, i.e. the probability $p(\varepsilon_Q)$ of the quantization error is uniformly distributed in the interval [-$\Delta U/2$; $\Delta U/2$] (Fig. 2.7).

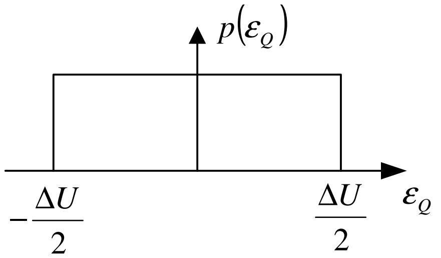


Fig. 2.7. Probability distribution of the quantization error

If assumption 2) applies no overloading of the quantizer takes place, hence the error is certainly limited to the interval [-$\Delta U/2$; $\Delta U/2$]. This means that:

$$\int_{-\frac{\Delta U}{2}}^{\frac{\Delta U}{2}} p(\varepsilon_Q)d\varepsilon_Q = 1 \tag{2.11}$$

From (2.11) and considering a uniform distribution it follows that:

$$p \cdot \Delta U = 1 \Rightarrow p = \frac{1}{\Delta U} \tag{2.12}$$

The variance of the zero mean random variable ε_Q is given by:

$$\sigma^2 = \int_{-\infty}^{+\infty} p(\varepsilon_Q)\varepsilon_Q^2 d\varepsilon_Q = \frac{1}{\Delta U}\int_{-\frac{\Delta U}{2}}^{\frac{\Delta U}{2}} \varepsilon_Q^2 d\varepsilon_Q = \frac{1}{\Delta U}\left(\frac{1}{3}\varepsilon_Q^3\right)\Bigg|_{-\frac{\Delta U}{2}}^{\frac{\Delta U}{2}} = \frac{\Delta U^2}{12} \tag{2.13}$$

that is, the variance of the quantization noise is proportional to the square of the quantization interval. This result agrees with the intuition: a larger *ΔU* means a larger quantization error, hence more “noise”.

The power of the stochastic zero-mean variable ε_Q is its variance σ^2. Because the quantized signal is also sampled (time-discrete), the whole quantization noise power will be aliased in the frequency range $[-f_s/2; f_s/2]$ leading to a power spectral density (PSD):

$$W(f) = \frac{\sigma^2}{f_s} = \frac{\Delta U^2}{12 f_s} \tag{2.14}$$

Since the quantization noise is white, the spectral power density will be constant in the frequency range $[-f_s/2; f_s/2]$ as depicted in Fig. 2.8.

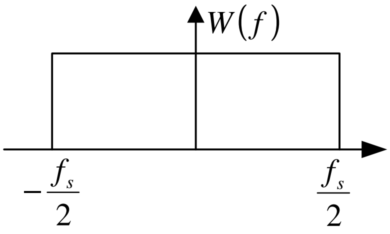


Fig. 2.8. Power spectral density of the sampled quantization error

The signal-to-quantization noise ratio (SQNR) is defined as the SNR of the modulator when the only noise present is quantization noise, that is, all other noise sources (i.e. thermal noise, other disturbances) are assumed to be zero. The maximum SQNR is achieved with a full scale input signal because the quantization noise power is, according to the linearized model, constant and not depending on the signal. Assuming a full-scale sine input signal

$$x(t) = 2^{N-1}\Delta U \sin(\omega t) \tag{2.15}$$

the signal power is

$$P_S = \frac{1}{2} \cdot 2^{2(N-1)} \Delta U^2 \tag{2.16}$$

Hence the SQNR in dB is:

$$SQNR = 10\log\frac{P_S}{P_N} = 10\log\frac{\frac{1}{2}\cdot 2^{2(N-1)}\Delta U^2}{\frac{\Delta U^2}{12}} = 10\log\left(\frac{3}{2}\cdot 2^{2N}\right) = 1.76 + 6.02N \tag{2.17}$$

Eq. (2.17) shows that an SQNR improvement of 6dB is achieved by incrementing the resolution of the ADC of one bit.

Once we know the SQNR of a certain ADC we can define its effective number of bits (ENOB) as the number of bits of an ideal ADC which would have the same SQNR as the ADC we are considering. By simply rewriting (2.17) we get:

$$ENOB = \frac{SQNR - 1.76}{6.02} \tag{2.18}$$

2.4. Oversampling

As previously seen, the minimal required sampling frequency in order to avoid aliasing is, according to the Nyquist-Shannon sampling theorem, twice the maximum signal frequency. In order to limit the signal bandwidth, a low-pass filter is required, called anti-aliasing filter. A low-pass filter has a transition frequency range between its pass-band and its stop-band, the width of this range depends on the order of the filter, that is, on the number of its poles. More precisely, the slope of the frequency response of the filter in the stop-band is equal to $M\cdot 20$ dB/dec, where M is the filter order. In order to relax the requirements on the filter order it is useful to increase the sampling frequency f_s beyond the minimum required value. As shown in Fig. 2.9, the greater f_s, the simpler the anti-aliasing filter that can be used to limit the signal bandwidth. Aliasing will be negligible if the filter is designed to have large attenuation for larger frequencies than $f_s/2$, while it is not of concern if the attenuation is moderate between f_B and $f_s/2$.

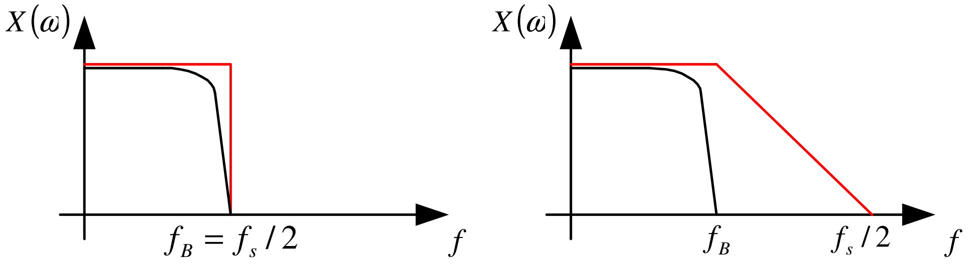


Fig. 2.9. Amplitude response of anti-aliasing filters for $f_s/2=f_B$ (left) and $f_s/2>f_B$ (right)

A sampling process at frequencies above the Nyquist frequency is called oversampling. Apart from the benefits described before, oversampling has another important advantage. To analyze this we will make use of the already described linear model for an ADC. Again, considering a clocked N-bit quantizer and modelling the quantization error as white noise, we get following PSD for the quantization noise:

$$W(f)=\frac{\sigma^2}{f_s}=\frac{\Delta U^2}{12f_s} \tag{2.19}$$

As expected, the whole noise power will be aliased into the frequency range [-f_s/2; f_s/2] because of sampling. A substantial difference towards the Nyquist converter case can be observed: in order to calculate the SQNR of the converter we need to integrate the noise PSD in the signal band, that is, in the frequency interval [-f_B;f_B].

This leads to a noise power

$$P_N=\frac{\Delta U^2}{12f_s}2f_B=\frac{\Delta U^2}{12\cdot OSR} \tag{2.20}$$

where we defined the factor

$$OSR=\frac{f_s}{2f_B} \tag{2.21}$$

This factor is called Oversampling Ratio (OSR). Note that in a Nyquist converter OSR=1 since f_s=2f_B. Following SQNR is obtained.

$$SQNR=10\log\frac{P_S}{P_N}=10\log\frac{\frac{1}{2}\cdot 2^{2(N-1)}\Delta U^2}{\frac{\Delta U^2}{12\cdot OSR}}=1.76+6.02N+10\log OSR \tag{2.22}$$

Comparing equation (2.22) with the equation (2.17), valid for Nyquist converters, a 3-db SQNR improvement can be achieved by doubling the OSR, that is, the sampling frequency. Applying (2.18) this means an improvement of 0.5 bits of ENOB, hence we can achieve a better resolution by simply sampling faster. In other words we can trade off speed for accuracy. This result is particularly important when dealing with modern CMOS technologies: on the one side these offer, thanks to miniaturization, very high working frequencies, on the other size they allow only moderate precision of the analog parts. For this reason oversampled ADC are becoming very popular in the modern CMOS industry.

2.5. Sigma-Delta ADC

In order to further improve the resolution of the oversampled AD conversion architectural changes of the converter can be introduced. This is done by means of a Sigma-Delta modulator. The Sigma-Delta architecture joins the advantages of oversampling with those of feedback. In Fig. 2.10 we can see the general topology of such a modulator. This consists of three main blocks: a filter, called loop filter because of its position inside a loop; a clocked quantizer which is typically a comparator or an *N*-bit flash ADC; a Digital-to-Analog converter (DAC), usually a bank of switched capacitors or an array of identical current sources.

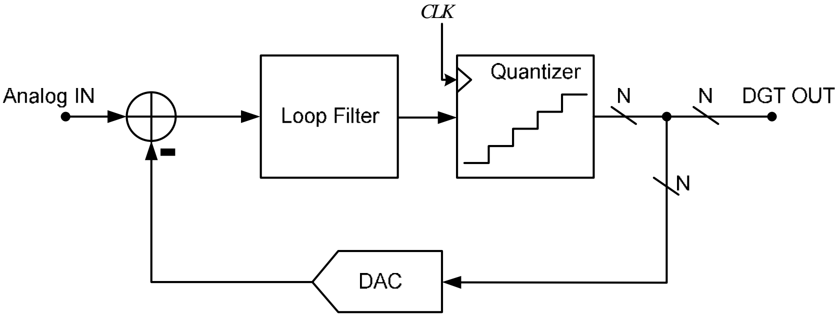


Fig. 2.10. Scheme of principle of a generic ΣΔ modulator

The loop filter is constituted by one or many cascaded integrators, connected by a series of feed-forward and/or feedback paths. A strongly non-linear element is present, the quantizer, making it difficult to analyze the modulator with an exact analytical model. To understand the way this architecture works we can describe it by means of the linear model.

2.5.1. Linear model

At first we will consider the DAC as ideal, namely perfectly linear and delay-free. The filter is also assumed to be linear and time invariant (LTI) and can thus be modeled by means of its transfer function $H(z)$. At this point we assume the filter is discrete-time (DT), typically realized with switched capacitor techniques, since this allows an easier mathematical modeling. Finally, the quantizer is replaced by a gain element followed by an adder in order to take the quantization noise into account. The gain k_Q is the slope of the line interpolating the quantizer characteristic. Fig 2.11 shows the linear model of a generic Sigma-Delta modulator.

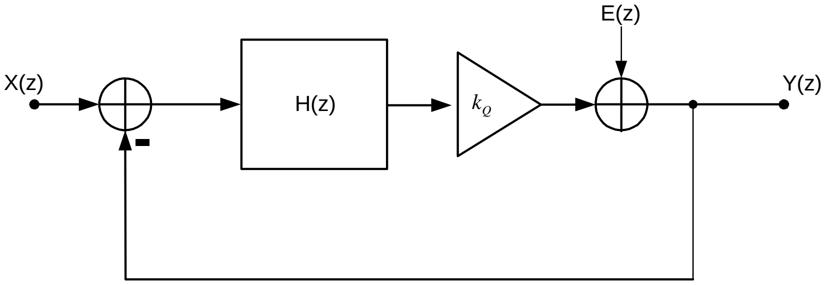


Fig. 2.11. Linear model of a generic ΣΔ modulator

This linear time-invariant system has two inputs, $X(z)$ and $E(z)$ and one output. Assuming k_Q=1, we can calculate two transfer functions:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \tag{2.23}$$

and

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.24}$$

STF is called Signal Transfer Function, NTF is the Noise Transfer Function. Equations (2.23) and (2.24) show that two different filter functions are obtained, depending on $H(z)$, for the input signal and for the unwanted quantization noise. Using the superposition principle the output of the linear model is:

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E(z) \tag{2.25}$$

In order to see the frequency response of *STF* and *NTF* we replace the variable z as following:

$$STF(j\omega) = STF(z)\Big|_{z=e^{j\omega T_s}} = \frac{H\left(e^{j\omega T_s}\right)}{1 + H\left(e^{j\omega T_s}\right)} \tag{2.26}$$

and

$$NTF(j\omega) = NTF(z)\Big|_{z=e^{j\omega T_s}} = \frac{1}{1 + H\left(e^{j\omega T_s}\right)} \tag{2.27}$$

where T_s is the sampling frequency of the system. For all frequencies where

$$\left|H\left(e^{j\omega T_s}\right)\right| >> 1 \tag{2.28}$$

we get:

$$STF(j\omega) \cong 1 \text{ and } NTF(j\omega) \cong \frac{1}{H\left(e^{j\omega T_s}\right)} \tag{2.29}$$

By inserting (2.29) in (2.25):

$$Y(j\omega) \cong X(j\omega) + \frac{E(j\omega)}{H(j\omega)} \tag{2.30}$$

Therefore, if $H(j\omega)$ is designed to have a high gain at frequencies in the signal band, the modulator output contains a replica of the non-attenuated input signal and largely attenuated quantization noise in that band.

The transfer function (TF) of the loop filter can be expressed as:

$$H(z) = \frac{N(z)}{D(z)} \tag{2.31}$$

where $N(z)$ and $D(z)$ are the numerator and the denominator of $H(z)$ respectively. Both are polynomial functions of z.

By substituting (2.31) in (2.24) we obtain:

$$NTF(z) = \frac{1}{1 + H(z)} = \frac{D(z)}{D(z) + N(z)} \tag{2.32}$$

This equation shows that the **zeros of the NTF are the poles of the loop filter**.

The loop filter contains one or more integrators; the number of the integrators is called *order* of the modulator. In the following some basic topologies are shortly analyzed.

2.5.2. 1st order modulator

Assuming the loop filter is a forward Euler DT-integrator, that is:

$$H(z)=\frac{z^{-1}}{1-z^{-1}} \tag{2.33}$$

following STF and NTF can be derived:

$$STF(z)=\frac{H(z)}{1+H(z)}=z^{-1} \qquad NTF(z)=\frac{1}{1+H(z)}=1-z^{-1}=\frac{z-1}{z} \tag{2.34}$$

The STF is a simple delay of one clock period, while the NTF is a differentiator. A sigma-delta modulator using a single integrator as loop filter is called 1st order modulator. The NTF obtained has a zero for $z=1$ that is at DC ($f=0$) and a slope of +20dB/dec. The maximum of the NTF is achieved for $z=-1$, that is for $f=f_s/2$ and is equal to 2 (6 dB). The frequency response of NTF is shown in green in Fig. 2.12.

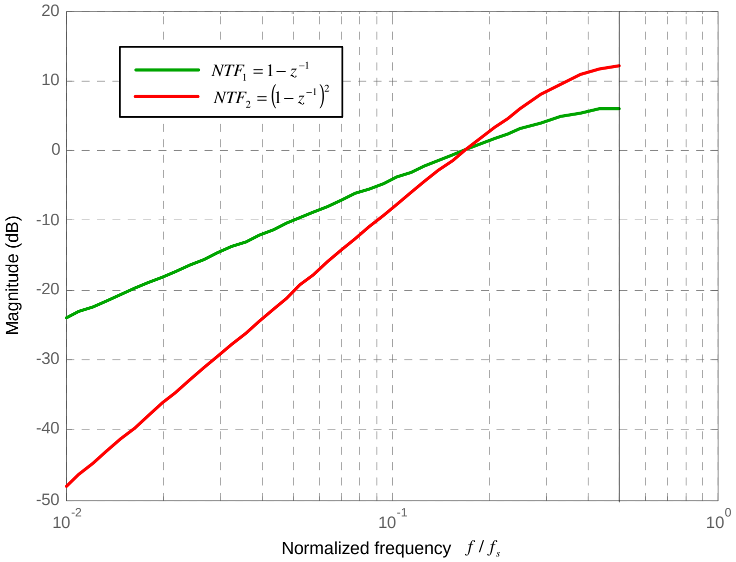


Fig. 2.12. NTF of a 1st order (green) and 2nd order (red) modulator.

The main advantage of the sigma-delta architecture is now evident: the quantization noise is frequency *shaped*, i.e. high-pass filtered. Therefore we expect a better resolution than that of a simple oversampled ADC. To calculate the SQNR of the 1st order sigma-delta modulator we need to calculate the output noise power P_N together with the signal power P_S. Assuming a purely delaying STF, the latter is simply equal to the signal power at the input, namely, as shown in section 2.3, eq. (2.16):

$$P_S=\frac{1}{2}\cdot 2^{2(N-1)}\Delta U^2 \tag{2.35}$$

Considering an N-bit quantizer, following input noise power spectral density (PSD) is added by the quantizer:

$$W(f) = \frac{\sigma^2}{f_s} = \frac{\Delta U^2}{12 f_s} \tag{2.36}$$

the PSD at the output is:

$$\begin{aligned} W_{out}(f) &= W(f)\left|NTF(f)\right|^2 = \frac{\Delta U^2}{12 f_s}\left|\left(1 - z^{-1}\right)_{z=e^{j2\pi f T_s}}\right|^2 = \frac{\Delta U^2}{12 f_s}\left|1 - e^{-j2\pi f T_s}\right|^2 \\ &= \frac{\Delta U^2}{12 f_s}\left|e^{-j\pi f T_s}\left(e^{j\pi f T_s} - e^{-j\pi f T_s}\right)\right|^2 = \frac{\Delta U^2}{12 f_s}\left|\left(e^{j\pi f T_s} - e^{-j\pi f T_s}\right)\right|^2 \end{aligned} \tag{2.37}$$

By using Euler’s formula:

$$\frac{e^{j\pi f T_s} - e^{-j\pi f T_s}}{2j} = \sin\left(\pi f T_s\right) \tag{2.38}$$

$$W_{out}(f) = \frac{\Delta U^2}{12 f_s}\left[2\sin\left(\pi f T_s\right)\right]^2 \tag{2.39}$$

By integrating the PSD of the quantization noise at the modulator output in the signal band we obtain:

$$P_N = \int_{-f_B}^{f_B} \frac{\Delta U^2}{12 f_s}\left[2\sin\left(\pi f T_s\right)\right]^2 df \cong \frac{\Delta U^2}{12}\frac{\pi^2}{3}\left(2 f_B T_s\right)^3 = \frac{\Delta U^2}{12}\frac{\pi^2}{3} OSR^{-3} \tag{2.40}$$

This result is obtained adopting the approximation:

$$\sin\left(\pi f T_s\right) \cong \pi f T_s \tag{2.41}$$

which is valid for $fT_S << 1$, that is, for frequencies which are much smaller than the sampling frequency. This is normally the case by oversampled ADCs. Looking at (2.40), the first term of the final product is the input quantization noise, the second term is a constant while the third one shows that the output noise power is inversely proportional to the 3rd power of the OSR.

The SQNR of a 1st order modulator is:

$$SQNR = 10\log\frac{P_S}{P_N} = 10\log\frac{\frac{1}{2}\cdot 2^{2(N-1)}\Delta U^2}{\frac{\Delta U^2}{12}\frac{\pi^2}{3}OSR^{-3}} = 1.76 + 6.02N - 10\log\frac{\pi^2}{3} + 10\log OSR^3 \tag{2.42}$$

Equation (2.42) shows that 9-dB SQNR improvement can be achieved by doubling the OSR, that is, an improvement of 1.5 bits of ENOB.

2.5.3. 2nd order modulator

A 2nd order sigma-delta modulator makes use of two integrators in the loop. Since each integrator causes a phase shift of -90 degrees because of its pole at DC, this structure is unsuitable for a system with feedback because of stability issues. In this case the phase margin of the modulator would be zero. An additional negative zero is required in order to improve the phase margin. As known, a negative zero causes a phase shift of +90 degrees. The zero can be introduced by means of an additional feed-forward (FF) or feedback (FB) path. Fig 2.13 shows for instance a 2nd order modulator with an additional feedback path. The 1st integrator is a backward Euler non-delaying integrator and its TF is:

$$H_1(z) = \frac{1}{1-z^{-1}} \tag{2.43}$$

the 2nd integrator is a forward Euler delaying integrator with TF

$$H_2(z) = \frac{z^{-1}}{1-z^{-1}} \tag{2.44}$$

The loop filter transfer function of the modulator in Fig. 2.13 is:

$$H(z) = \frac{V(z)}{Y(z)} = -\frac{z^{-1}}{\left(1-z^{-1}\right)^2} - \frac{z^{-1}}{\left(1-z^{-1}\right)} = \frac{-2z+1}{(z-1)^2} \tag{2.45}$$

where $V(z)$ is the quantizer input. Eq. (2.45) shows the presence of a zero z_n=−1/2, which arises from the additional feedback path.

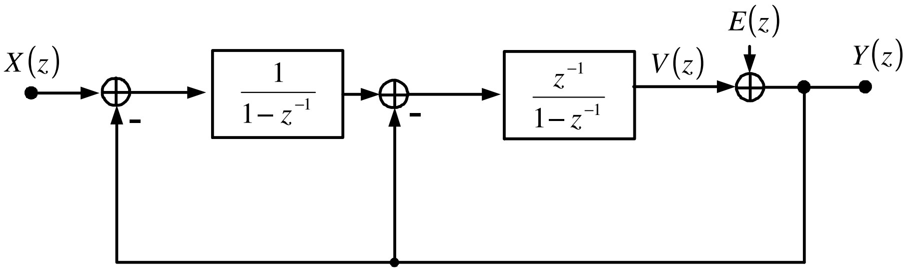


Fig. 2.13. 2nd order ΣΔ modulator with additional feedback

By calculating the STF and the NTF we obtain now:

$$STF(z) = \frac{Y(z)}{X(z)} = z^{-1} \tag{2.46}$$

and

$$NTF(z) = \frac{Y(z)}{E(z)} = \left(1-z^{-1}\right)^2 = \frac{(z-1)^2}{z^2} \tag{2.47}$$

As in the 1st order case, the STF is simply a delay of one clock period T_s. The NTF is now a differentiator of 2nd order, i.e. it has two zeros at DC. Its frequency response is shown in red in Fig. 2.12. The slope of the curve is now +40dB/dec while the maximum of NTF is again for $z=-1$ ($f=f_s/2$) and equals to 4 (12 dB).

To calculate the SQNR we recognize that the signal power is the same as in the 1st order case, since we deal with a simply delaying STF. The output noise PSD is, by taking into account the new NTF (2.47):

$$W_{out}(f)=W(f)|NTF(f)|^2=\frac{\Delta U^2}{12f_s}\left|\left(1-z^{-1}\right)^2_{z=e^{j2\pi fT_s}}\right|^2=\frac{\Delta U^2}{12f_s}\left|\left(1-e^{-j2\pi fT_s}\right)^2\right|^2$$

$$=\frac{\Delta U^2}{12f_s}\left|\left[e^{-j\pi fT_s}\left(e^{j\pi fT_s}-e^{-j\pi fT_s}\right)\right]^2\right|^2=\frac{\Delta U^2}{12f_s}\left|e^{-j2\pi fT_s}\left(e^{j\pi fT_s}-e^{-j\pi fT_s}\right)^2\right|^2 \tag{2.48}$$

$$=\frac{\Delta U^2}{12f_s}\left|\left[2j\sin(\pi fT_s)\right]^2\right|^2=\frac{\Delta U^2}{12f_s}16\sin^4(\pi fT_s)$$

By integrating the PSD of the quantization noise at the modulator output in the signal band we obtain:

$$P_N=\int_{-f_B}^{f_B}\frac{\Delta U^2}{12f_s}16\sin^4(\pi fT_s)df\cong\frac{\Delta U^2}{12}\frac{\pi^4}{5}(2f_BT_s)^5=\frac{\Delta U^2}{12}\frac{\pi^4}{5}OSR^{-5} \tag{2.49}$$

Again, the result is approximated and valid only for $f<<f_s$. In this case the output noise power is inversely proportional to the 5th power of the OSR.

The SQNR of a 2nd order modulator is:

$$SQNR=10\log\frac{P_S}{P_N}=10\log\frac{\frac{1}{2}\cdot 2^{2(N-1)}\Delta U^2}{\frac{\Delta U^2}{12}\frac{\pi^4}{5}OSR^{-4}}=1.76+6.02N-10\log\frac{\pi^4}{5}+10\log OSR^5 \tag{2.50}$$

Equation (2.50) shows that 15-dB SQNR improvement can be achieved by doubling the OSR, that is, an improvement of 2.5 bits of ENOB.

2.5.4. *L*-th order modulator

A loop filter of L-th order is constituted by L cascaded integrators. By generalizing the calculation for a modulator of L-th order with a pure differentiating NTF in the form:

$$NTF=\left(1-z^{-1}\right)^L=\frac{(z-1)^L}{z^L} \tag{2.51}$$

This NTF has L zeros at DC and a maximum of 2^L for $f=f_s/2$. By calculating the output quantization noise power in the signal band solving the integral:

$$P_N = \int_{-f_B}^{f_B} \frac{\Delta U^2}{12 f_s} \left| NTF(f) \right|^2 df \tag{2.52}$$

we obtain, similarly to the previous cases:

$$SQNR = 1.76 + 6.02N - 10\log\frac{\pi^{2L}}{2L+1} + 10\log OSR^{2L+1} \tag{2.53}$$

This means a (2L+1)·3 dB SQNR increase for each doubling of the OSR, that is, an improvement of (2L+1)·0.5 bits of ENOB. Fig. 2.14 plots the theoretically achievable SQNR as a function of the OSR and the modulator order L. The number of bits of the quantizer is assumed to be 1. For each additional bit the plotted lines are simply shifted upwards by 6.02 dB (eq. 2.53).

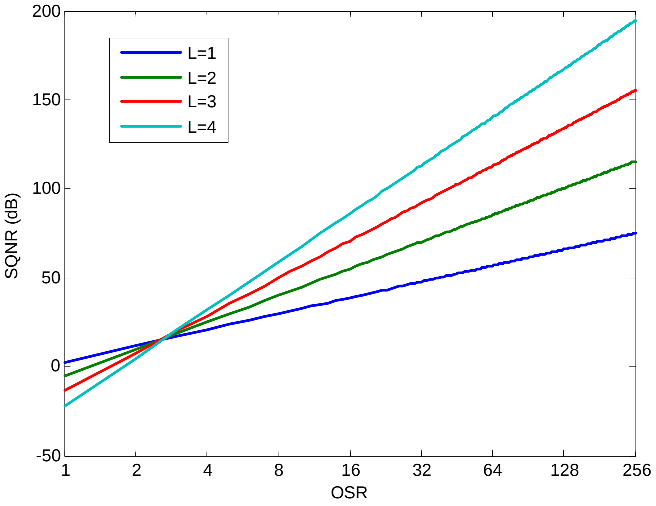


Fig. 2.14. Achievable SQNR with 1-bit comparator for purely differentiating NTF=(1-z^{-1})^L

As explained later, it is not possible to realize a pure differentiating NTF of arbitrary order L, since instability issues occur. The graph above simply plots the theoretical achievable resolution.

2.5.5. Stability analysis

Although the linear model proves very useful to estimate the achievable resolution of the modulator depending on the sampling frequency, the modulator order and the resolution of the quantizer, it gives not much information about the stability of the modulator.

One criterion to estimate the stability is the analysis of the root locus, that is, the position of the filter poles on the z-plane. Even if the filter is designed to be stable, i.e. all poles are inside the unit circle, the modulator can get instable, depending on the amplitude of the signal at the quantizer input. Here we distinguish two cases:

a) one-bit quantizer (i.e. a single comparator); it is not straightforward to define the gain of the quantizer in the linear model, as the straight lines interpolating the comparator characteristic are infinite (Fig. 2.15). Moreover the instantaneous gain depends on the amplitude of the input signal, since the output is limited to only two values ±V.

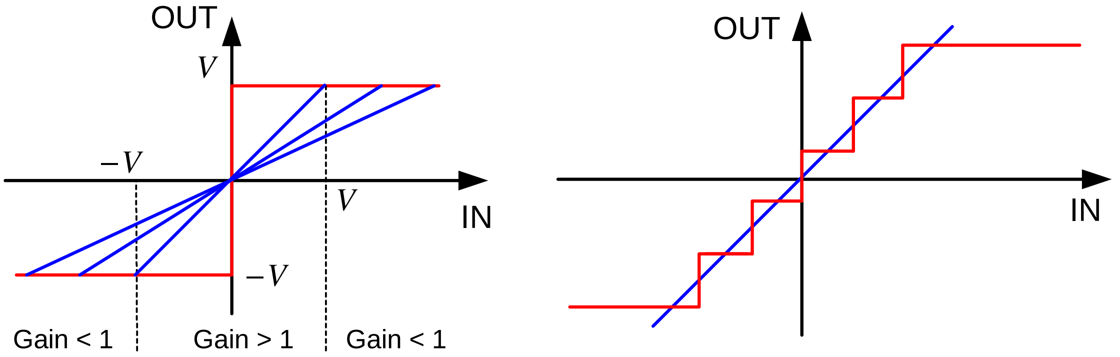


Fig. 2.15. Gain of a 1-bit (left) and multibit (right) quantizer

As depicted in Fig. 2.15, when the input signal is bounded in the interval [-*V*,*V*] a gain larger than one is obtained, otherwise the gain is smaller than one (the comparator is overloaded).

[Ris94] defines the gain of the comparator as:

$$k_q = \frac{\operatorname{cov}(v, y)}{\sigma^2(v)} \tag{2.54}$$

This is the value which minimizes the power of the quantization error sequence [Sch05]. To demonstrate this, consider the linear model of the quantizer (Fig. 2.16). The output is:

$$y = k_q v + \varepsilon \tag{2.55}$$

where v is the comparator input, y its output and ε the quantization error. Assuming a zero-mean quantization error ε, the error power is equal to its variance, namely:

$$\sigma^2(\varepsilon) = \sigma^2(y - k_q v) = \sigma^2(y) - 2k_q \operatorname{cov}(v, y) + k_q^2 \sigma^2(v) \tag{2.56}$$

Differentiating (2.56) with respect to k_q the value of k_q minimizing the error variance is found to be the same as proposed by [Ris94] in (2.54). Equation (2.54) shows that the gain k_q can only be defined if the statistical properties of the quantizer input v are known.

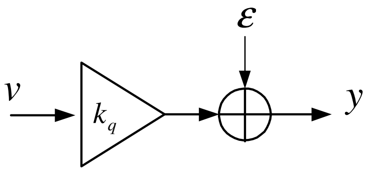


Fig. 2.16. Linear model of the quantizer

b) multibit quantizer: in this case it is possible to define the gain as the slope of the straight line interpolating the input-output characteristic (Fig. 2.15). The larger the number of quantization levels, the better the approximation made. This model works correctly as long as the quantizer is not overloaded. If this happens, the output amplitude remains constant even when the input increases (clipping), leading to a reduction of the effective gain.

The linear model can be enhanced by taking into account a variable gain for the quantizer. We can define the point at which instability occurs, as the point where the closed loop poles, i.e. the poles of the NTF, move outside the unit circle. This can be made by plotting the closed loop poles for different gains of the amplifier which models the quantizer in the linear model. For example, Fig. 2.17 plots the root locus of a 3rd order NTF with three zeros and three poles against the quantizer gain k_Q. By decreasing k_Q the poles eventually move outside the unit circle, leading to instability of the modulator. This analysis is useful to get an insight, how far the system is from instability.

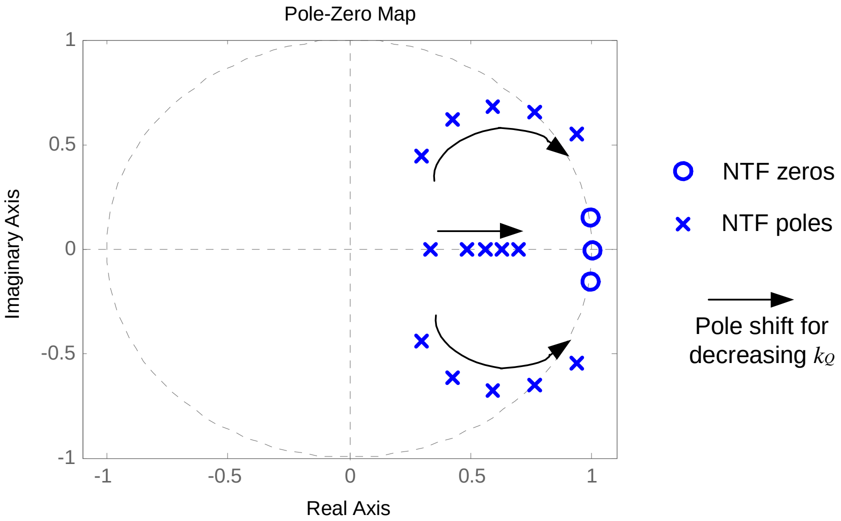


Fig. 2.17. Root locus of the NTF singularities as function of the quantizer gain

Intuitively, a smaller k_Q leads to instability and, as seen previously, this occurs if the quantizer input becomes too large, such that the quantizer is overloaded. Assuming a non overloaded multibit quantizer with unity gain as in Fig. 2.18, we can estimate the amplitude of the quantizer input, by calculating the TF between the input signal $X(z)$ and the quantizer input $V(z)$ and between the "quantization noise source" $E(z)$ and $V(z)$. Using the superposition principle we can express $V(z)$ as the sum, of a signal and a noise contribution.

$$V(z) = V(z)_{signal} + V(z)_{noise} = STF \cdot X(z) + NTF \cdot E(z) - E(z) \tag{2.57}$$

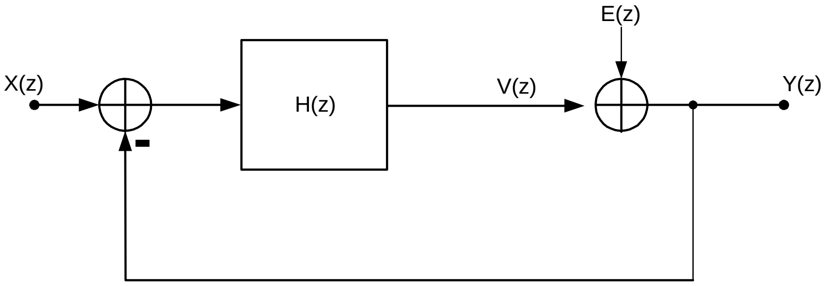


Fig. 2.18. Linear model with unit quantizer gain

Typically the STF is one in the signal band and smaller than one for higher frequencies. From Eq. 2.57 we can see that $V(z)$ contains a replica of the input signal $X(z)$ plus high-pass filtered quantization noise. Qualitatively, two factors contribute to saturate the quantizer: the amplitude of $X(z)$ which is replicated by $V(z)$ and the amount of high-filtered noise which is fed back to $V(z)$. These considerations suggest the introduction of two parameters to get a measure of the modulator stability: a) NTF_{MAX}, the maximum of $|NTF(z)|$, gives information about the high-frequency gain of the NTF; b) the maximum stable amplitude (MSA) defines the maximum amplitude of the input signal, so that the modulator remains stable.

An empirical criterion based on experience and observation states that a modulator is likely to be stable for $\mathrm{NTF_{MAX}}<1.5$[1] [Sch05], although this condition is neither necessary nor sufficient.
From this point of view it becomes clear that higher order purely differentiating NTFs necessarily lead to instability, since their maximum gain increases exponentially with the order L ($\mathrm{NTF_{MAX}}=2^L$). A countermeasure consists in deliberately reducing the maximum of the NTF by introducing poles in its TF [Sch05].

$$NTF_D = \frac{(z-1)^L}{D_N(z)} \tag{2.58}$$

$D_N(z)$ is a polynomial in z in the form:

$$D_N(z) = z^L + a_{L-1}z^{L-1} + \ldots + a_1 z + 1 \tag{2.59}$$

the poles of NTF_D are usually chosen so that the NTF is a Chebyschev or Butterworth high-pass maximally flat filter. The result of this operation is, as depicted in Fig. 2.19, a reduction of the high-frequency gain at the expense of an increased low-frequency gain, that is, an increase of the noise floor in the signal band. The price for a better stability is thus a worse noise suppression, hence a lower SQNR of the modulator. Since the numerator of $\mathrm{NTF_D}$ is the same as that of the purely differentiating NTF we can calculate the increase α of the noise floor, assuming the NTF poles are at much higher frequencies than f_B, as:

$$\alpha = \left.\frac{NTF_D(z)}{NTF(z)}\right|_{z=1} = \frac{1}{D_N(z=1)} = \frac{1}{1+a_{L-1}+\ldots+a_1+1} \tag{2.60}$$

The assumption that the poles are at much higher frequencies than f_B means a constant in-band increase of NTF, which is evident in Fig. 2.19, where both curves are parallel in the lower frequency range.

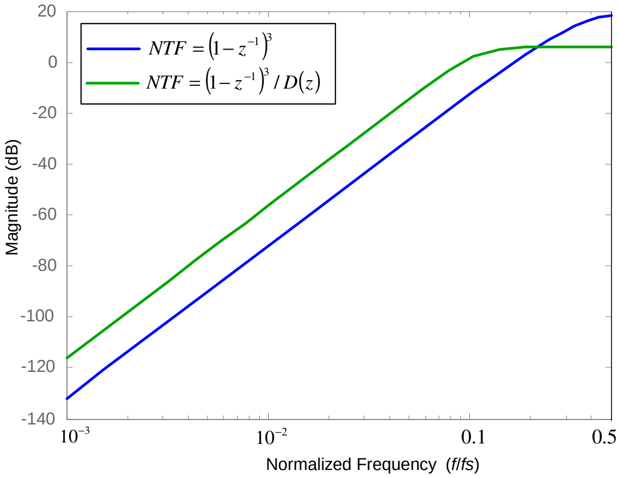


Fig. 2.19. Example of reduction of $\mathrm{NTF_{MAX}}$ by introducing new poles for NTF

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[1] This condition is applied to modulators with binary (one-bit) comparators. Multibit modulators are more robust against instability and tolerate higher values of $\mathrm{NTF_{MAX}}$.

2.5.6. Zero spreading

So far only a purely differentiating NTF was assumed, obtained with a loop filter constituted of one or more cascaded integrators. This kind of NTF does not ensure an optimal noise shaping. For a given modulator order *L* the optimal NTF can be found by minimizing the quantization noise power in the signal band, that is, by finding the minimum of the integral:

$$P_N = \int_{-f_B}^{f_B} \frac{\Delta U^2}{12 f_s} \left| NTF(f) \right|^2 df \tag{2.61}$$

Once the poles are chosen based on stability considerations, the solution of the problem consists in finding:

$$\min \left[\int_{-f_B}^{f_B} \left| N(z) \right|^2_{e^{j2\pi f}} df \right] \tag{2.62}$$

where $N(z)$ is the numerator of the NTF in form of a polynomial of z of order L.

By solving (2.62) numerically, the frequency of the zeros which minimize the in-band noise and the SQNR improvement can be calculated [Nor97]. The results of the numerical calculations are shown in Tab. 2.1. The optimal NTF zeros are always located on the unit circle ($|z_n|=1$), that is, the damping factor is zero. They are either at DC or complex-conjugate and cause the NTF frequency response to have a notch at the frequencies of the zeros.

Order *L* of NTF	**Freq. of the zeros normalized to f_B**	**Location of the zeros on the z-plane**	**SQNR improvement (dB)**
1	0	1	0
2	±0.577	0.994±0.113j	3.5
3	0, ±0.775	1, 0.988±0.152j	8
4	±0.34, ±0.861	0.998±0.067j, 0.986±0.168j	13
5	0, ±0.538, ±0.906	1, 0.994±0.106j, 0,984±0.177j	18

Tab. 2.1. Location of the NTF zeros for optimal suppression of the quantization noise (zero spreading)

Complex-conjugate NTF zeros on the unit circle are obtained with a local feedback path across two consecutive integrators of the loop filter, forming a circuit called resonator (Fig. 2.20) with transfer function:

$$H_{res}(z) = \frac{Y(z)}{X(z)} = \frac{z^{-1}}{1-(2-\gamma)z^{-1}+z^{-2}} \tag{2.63}$$

where γ is the feedback coefficient.

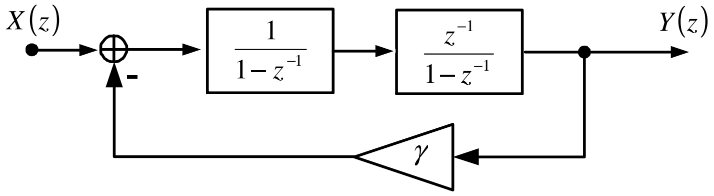


Fig. 2.20. Resonator for generation of complex-conjugate NTF zeros (filter poles) on the unit circle.

Fig 2.21 shows exemplary a NTF of 5th order with (in red) and without zero spreading (in blue). The notches are introduced by two pairs of complex-conjugate zeros on the unit circle.

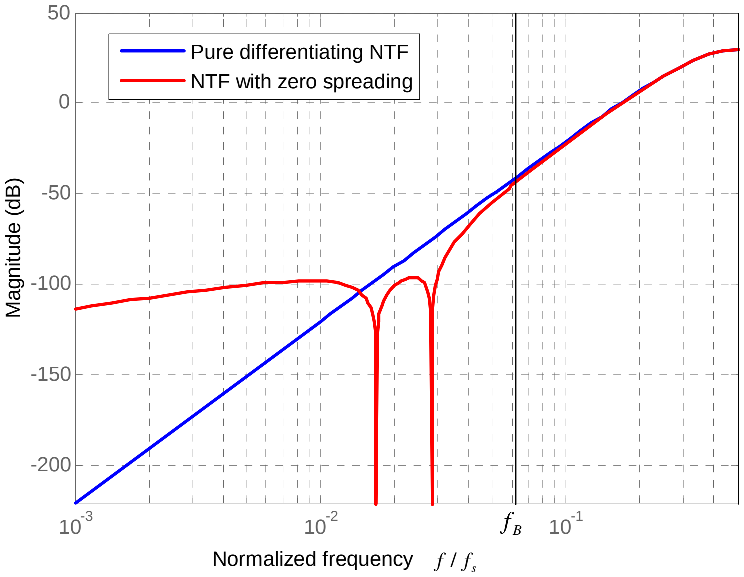


Fig. 2.21. Gain response of a 5th order NTF: pure differentiating (blue) and with zero spreading (red)

The zero spreading allows stronger noise suppression in the higher signal band at the expense of lower suppression at very low frequencies. The total in-band noise power is nevertheless smaller than in the purely differential NTF.

2.6. Quasi-linear model

All previous calculations of the performance of sigma-delta modulators were based on linearized models. Although these models are very simple and powerful, they are not exact and base on assumptions, which are not always true (such as the non-correlation of the input samples). Starting from these considerations, some authors have developed non-linear or quasi-linear models. These models are very complicated to apply and often become unsuitable for practical design implementations. For example [Ris94] models a 1-bit sigma-delta modulator with a technique which is known from the circuit simulation. The problem is split in two parts: a DC operating point and an AC model. Three approximations are made:

- the input signal has zero frequency (DC). This assumption is valid if the sampling frequency is much higher than the signal frequency, that is, if OSR>>1
- the mean output value of the modulator is supposed to be the same as the constant input signal. This assumption is correct if the loop gain of the modulator is very large at low frequencies, so that the output (which is fed back) can track the input. This constant output value can be seen as the operating point of the comparator, which determine its AC (small signal) parameters
- the quantization error is modeled as noise, like in the well-known linear model. The comparator is replaced by a gain element which is applied only to the AC noise and not to the DC signal

In summary the output binary flow is the sum of two components:

- the mean value is a replica of the (constant) input signal of the modulator

– the variance, i.e. the AC power of the output, is the high-pass filtered noise according to the formula

$$\sigma^2(y) = \frac{\Delta U^2}{12} \int_0^{f_B} NTF_K(f)\,df = \frac{\Delta U^2}{12} A(k_q) \tag{2.64}$$

Here NTF_K denotes the NTF of the modulator as a function of the quantizer AC-gain k_q:

$$NTF_K = \frac{1}{1 + k_q H} \tag{2.65}$$

where k_q is the comparator gain defined as in (2.54).

This quasi-linear modeling allows to get information about the stability of the modulator and to predict non-linear phenomena like limit cycles but will not be used in the present work.

2.7. Single loop / Cascaded

It was shown that the maximum of the NTF gives an indication about the stability behavior. In particular, larger values of NTF_{MAX} denote a modulator which is more prone to instability. Apart from the technique already shown, consisting in the introduction of poles in the NTF to lower the maximum NTF gain at the expense of less noise suppression, another solution is possible. The idea is to process the quantization noise in more than one loop, making a more aggressive noise shaping possible without sacrificing the stability of the modulator. Fig. 2.22 shows the main blocks of such architecture. Two ore more loops are cascaded: the first loop processes the input signal while the latter threat the quantization noise introduced by the first loop. The digital outputs of the single stages are processed by a digital block called Error Correction Logic (ECL). This logic block filters the digital inputs with appropriate transfer functions.

In the following an example of a 2-2 cascaded modulator (Fig. 2.2) is explained: the modulator consists of two identical DT 2nd order sigma delta modulators. The digital outputs of the modulators are:

$$\begin{aligned} OUT_1 &= STF_1 \cdot X + NTF_1 \cdot E_1 \\ OUT_2 &= STF_2 \cdot E_1 + NTF_2 \cdot E_2 \end{aligned} \tag{2.66}$$

where STF_1, STF_2 are the signal transfer functions, NTF_1, NTF_2 the noise transfer functions and E_1, E_2 the quantization noise of the 1st and 2nd stage respectively. Digitally filtering both OUT_1 and OUT_2 and summing them, following output signal is provided by the ECL:

$$OUT = OUT_1 STF_{2d} - OUT_2 NTF_{1d} \tag{2.67}$$

Substituting (2.66) in (2.67) the digital output is:

$$OUT = STF_1 STF_{2d} X + NTF_1 STF_{2d} E_1 - STF_2 NTF_{1d} E_1 - NTF_2 NTF_{1d} E_2 \tag{2.68}$$

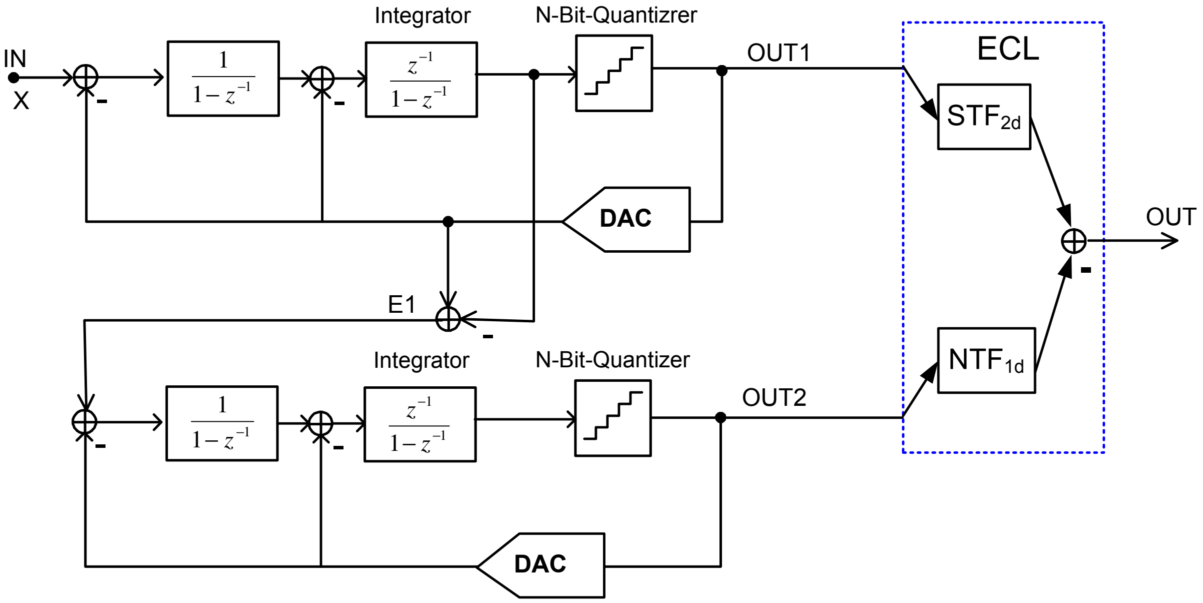


Fig. 2.22. A 2-2 cascaded DT sigma-delta modulator

By choosing:

$$STF_{2d} = STF_2 = z^{-1} \tag{2.69}$$

and

$$NTF_{1d} = NTF_1 = \left(1 - z^{-1}\right)^2 \tag{2.70}$$

we obtain:

$$OUT = STF_1 STF_{2d} X - NTF_2 NTF_{1d} E_2 = z^{-2} X - \left(1 - z^{-1}\right)^4 E_2 \tag{2.71}$$

We see that the digital output is the sum of the input signal delayed by two clock periods plus the 4th order shaped quantization noise of the 2nd stage. The quantization noise of the 1st stage has been completely canceled. In general the noise contained at the output is the quantization noise of the last stage, the order of noise shaping is the sum of the orders of the single stages. The other noise terms from all other stages are cancelled by the ECL. The advantage of a cascaded architecture is that we can *theoretically* achieve a noise shaping of very large order by simply cascading many stages of lower order. Moreover, we can get very stable modulators by keeping the order of the single stages low (typically ≤2).

On the other hand this architecture suffers from a major issue: mismatch between analog and digital part of the modulator. In fact, we need a perfect cancelling of the analog generated TF with the digitally generated ones. This is not possible in a real implementation of the circuit: while the digital filters behave ideally, the analog NTF and STF of the analog loop depend on circuit non-idealities like integrator gain, bandwidth, settling error, etc. and therefore deviate from the ideal form. In the 2-2 modulator, for example, a residuum $\alpha \cdot E_1$ of the unwanted noise of the first stage leaks to the output worsening the modulator resolution (SQNR):

$$OUT = STF_1 STF_{2d} X + \alpha E_1 - NTF_2 NTF_{1d} E_2 \tag{2.72}$$

For this reason seldom more than two stages are cascaded, since the leakage noise eventually dominates the other noise terms and further cascading would have no more benefits.

2.8. Discrete time / continuous time loop filter

Another important distinction in the family of sigma-delta modulators concerns the implementation of the loop filter. There are basically two categories of loop filers: discrete time (DT) and continuous time (CT) filters.

2.8.1. Discrete time filter

Discrete time filters are implemented by means of switched capacitor (SC) circuits. These circuits are constituted by operational amplifiers (opamp), capacitors and switches. Additionally, two clock phases are necessary to switch the capacitors. A typical SC integrator is depicted in Fig. 2.23.

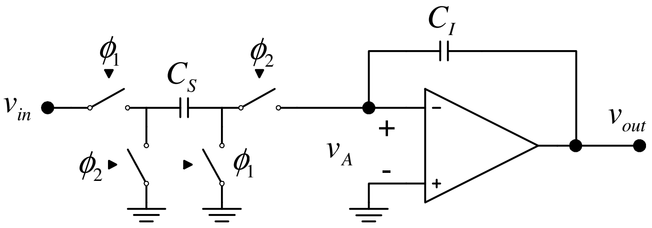


Fig. 2.23. Discrete time, switched capacitor integrator

We can distinguish two operation phases: a sampling phase, when φ_1 is high and φ_2 is low, where the input voltage is sampled on the capacitor C_S; an integration phase when φ_2 is high and φ_1 is low, where the charge stored in C_S is transferred into C_I. The ideal opamp forces the voltage v_A to stay at zero (virtual ground). The output voltage in the time domain is:

$$v_{out}[n] = v_{out}[n-1] + v_{in}[n-1]\frac{C_S}{C_I} \tag{2.73}$$

By z-transforming both terms of equation (2.73):

$$V_{out} = V_{out} z^{-1} + V_{in} z^{-1} \frac{C_S}{C_I} \tag{2.74}$$

that is:

$$H(z) = \frac{V_{out}}{V_{in}} = \frac{z^{-1}}{1-z^{-1}} \frac{C_S}{C_I} \tag{2.75}$$

namely the TF of a forward Euler integrator. The gain coefficient of the integrator is the ratio C_S/C_I. The most important advantage of SC circuits is that sensitive circuit parameters can be made dependant on capacitor ratios. This peculiarity proves useful in integrated circuits were large process-related variations affect the *absolute* values of the components. In contrast to this, the *relative* variations of elements of the same type, which are physically contiguous on the chip are relatively small. Hence, even a large variation of the absolute value of the capacitors C_S and C_I in (2.75) has a very small influence on the capacitor ratio. SC-based integrated circuits can achieve a precision of up to 0.1% despite fluctuations of the absolute values in the order of ±20%.

2.8.1.1. Errors in the TF because of non-idealities

Deviations from the ideal TF are caused by non-idealities of the analog circuit realizing the DT integrator:

- mismatch of the capacitors C_S and C_I
- finite DC-gain of the opamp
- finite bandwidth of the opamp
- slew rate of the opamp

The effect of capacitor mismatch is straightforward and, according to (2.75), a gain error in the integrator TF is introduced. This error is limited, thanks to the good matching properties of capacitors which are contiguous on the layout and is typically on the order of 0.1%.

Let us consider an opamp with finite DC-gain A_{DC}. Now a non-zero voltage v_A is present at the opamp inputs (Fig. 2.23):

$$v_A = -\frac{v_{out}}{A_{DC}} \tag{2.76}$$

Analyzing the DT-integrator in the time domain we can calculate the total charge Q in the capacitors according to the polarity shown in Fig. 2.24. When φ_1 is high (Fig. 2.24a):

$$Q[n-1] = v_{in}[n-1]C_S + (v_{out}[n-1] - v_A[n-1])C_I = v_{in}[n-1]C_S + v_{out}[n-1]\left(1+\frac{1}{A_{DC}}\right)C_I \tag{2.77}$$

where n denotes the discrete time point considered. When φ_2 is high (Fig. 2.24b), noting that capacitor C_S is turned upside down because of the switching, the time-domain equation is:

$$Q[n] = -v_A[n]C_S + (v_{out}[n] - v_A[n])C_I = v_{out}[n]\frac{C_S}{A_{DC}} + v_{out}[n]\left(1+\frac{1}{A_{DC}}\right)C_I \tag{2.78}$$

Rearranging the terms:

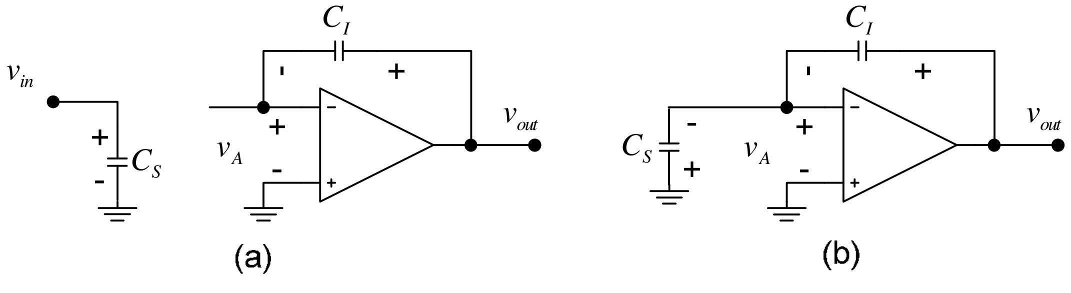


Fig. 2.24. Switched capacitor integrator: sampling phase (a) and integration phase (b)

$$Q[n] = v_{out}[n] \cdot \left[\left(1 + \frac{1}{A_{DC}}\right) C_I + \frac{C_S}{A_{DC}} \right] \tag{2.79}$$

Equating (2.77) and (2.79), according to the principle of charge conservation:

$$Q[n-1] = Q[n] \Rightarrow v_{in}[n-1]C_S + v_{out}[n-1]\left(1 + \frac{1}{A_{DC}}\right) C_I = v_{out}[n] \cdot \left[\left(1 + \frac{1}{A_{DC}}\right) C_I + \frac{C_S}{A_{DC}} \right] \tag{2.80}$$

Transforming this time-domain equation into the *z*-domain:

$$V_{in} z^{-1} C_S + V_{out} z^{-1} \left(1 + \frac{1}{A_{DC}}\right) C_I = V_{out} \left[\left(1 + \frac{1}{A_{DC}}\right) C_I + \frac{C_S}{A_{DC}} \right] \tag{2.81}$$

Hence, the TF of the integrator will be:

$$H(z) = \frac{V_{out}}{V_{in}} = \frac{z^{-1} C_S}{\left(1 + \frac{1}{A_{DC}}\right) C_I + \frac{C_S}{A_{DC}} - z^{-1} \left(1 + \frac{1}{A_{DC}}\right) C_I} \tag{2.82}$$

The DC-gain of the integrator is:

$$H(z)\big|_{z=1} = A_{DC} \tag{2.83}$$

which is, as expected, the same as the DC-gain of the operational amplifier used for the integrator. Furthermore, a pole shift can be observed by equating the denominator of (2.82) to zero:

$$\left(1 + \frac{1}{A_{DC}}\right) C_I + \frac{C_S}{A_{DC}} - z^{-1} \left(1 + \frac{1}{A_{DC}}\right) C_I = 0 \tag{2.84}$$

$$z_P = \frac{\left(1 + \frac{1}{A_{DC}}\right) C_I}{\left[\left(1 + \frac{1}{A_{DC}}\right) C_I + \frac{C_S}{A_{DC}} \right]} = \frac{C_I}{C_I + \frac{C_S}{\left(1 + \frac{1}{A_{DC}}\right) A_{DC}}} \tag{2.85}$$

$$z_P \cong \frac{1}{1 + \frac{C_S}{C_I A_{DC}}} \cong 1 - \frac{C_S}{C_I A_{DC}} = 1 - \Delta_P \tag{2.86}$$

where the last approximation holds for large values of A_{DC}. While the pole of the ideal integrator is at DC (z=1), its location is shifted inside the unit circle by an amount Δ_P in case of finite opamp gain.

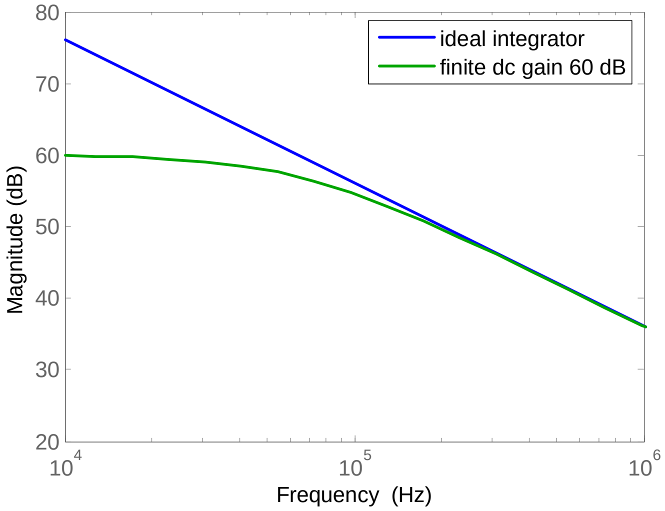


Fig. 2.25. Bode diagram of a DT-integrator with finite DC gain. The pole is not at DC like in the ideal case (blue)

This pole shift has directly an effect on the NTF of the modulator and hence on the quantization noise suppression. Remembering that the zeros of the NTF are the poles of the loop filter (sect. 2.5.1), we can deduce that a pole shift of the integrator causes a worsening of the noise suppression by shifting the zero of the NTF.

Also other opamp non-idealities modify the TF of the integrator and, in turn, worsen the suppression of the quantization noise. The finite bandwidth of the opamp, for example, slows down the process of charge transfer in the integration phase, thus causing an error on the final voltage across the integration capacitance C_I. The same happens in case of finite slew rate of the opamp with the important difference that the opamp does not work as a linear amplifier. These errors will not be examined in the present work, for an extensive explanation the reader can refer to [Fer06].

The non-idealities of the analog devices described so far directly affect the noise transfer function of the modulator introducing error terms and affecting the suppression of the quantization noise. In particular, cascaded modulators are very sensitive to the mismatch between the analog and digital TF and great attention must be paid when designing opamp for cascaded topologies.

2.8.1.2. Switches

A critical aspect of DT modulators in modern sub-μm technologies is the relatively poor quality of switches, which are realized with MOS transistors. The trend of the last years [Pek04] shows that the reduction of the threshold voltage for new technology nodes has been slower than that of the supply voltage. As a consequence, the overdrive voltage which can be applied to the switches is becoming smaller, making it difficult to bias conducting switches in strong inversion. This means a progressive increase in the on-resistance of the conducting switches, hence slower sampling and also non-linearities because of the dependence of the resistance on the input signal. In order to make the on-resistance less dependent on the signal, transmission gates can be used, realized with an nmos and a pmos transistor in parallel as shown in Fig. 2.26.

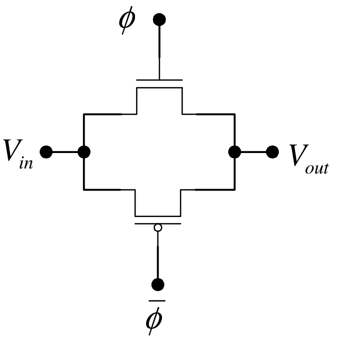


Fig. 2.26. Transmission gate schematic

Ideally, when the gate is switched on, for every possible input voltage at least one transistor must be in the inversion region (Fig. 2.27a). This condition is satisfied if one transistor starts to conduct before the complementary transistor switches off, namely if:

$$V_{Tn} \le V_{DD} - |V_{Tp}| \quad \Rightarrow \quad V_{DD} \ge V_{Tn} + |V_{Tp}| \cong 2V_T \tag{2.87}$$

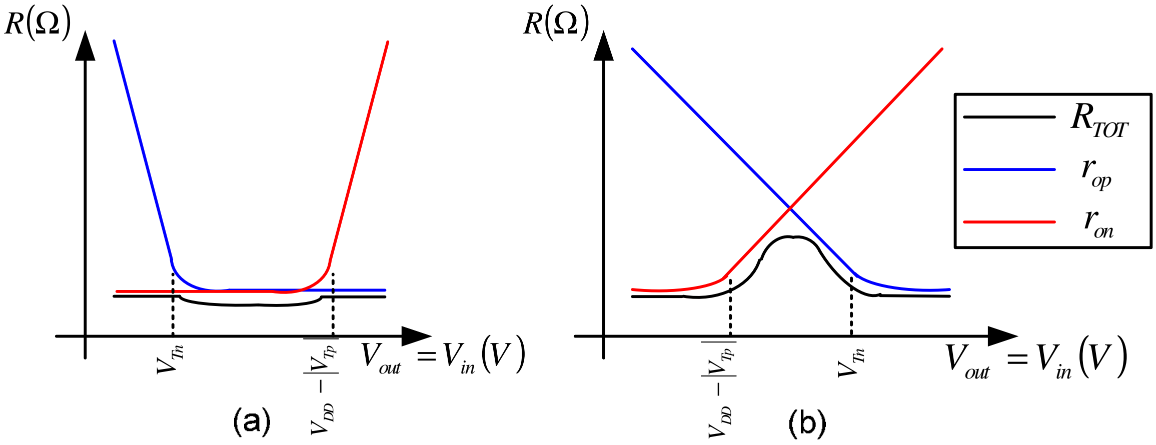


Fig. 2.27. Qualitative characteristics of the on-resistance for V_{DD}-$|V_{tp}|$>V_{tn} (a) and V_{DD}-$|V_{tp}|$<V_{tn} (b)

This means that the supply voltage should be at least two times larger than one threshold voltage, which is not the case in Fig. 2.27b. In the latter case it is evident that an input voltage range exists, situated approximately in the middle of the characteristic, in which both switches are in the off-state (more correctly they work in the sub-threshold region) hence providing a high resistance path.

Fig. 2.28 shows the simulated on-resistance of the nmos r_{on}, that of the pmos r_{op} and the total resistance R_{tot} of a typical transmission gate in the UMC 0.13µm CMOS process used in our work. The total resistance R_{tot} is larger in the middle of the range increasing the charging time for voltages in that range. Moreover, the dependency of R_{tot} on the input voltage $V_{in}= V_{out}$ causes non linear errors since the time constant $\tau=R_{tot}(V_{in})\cdot C$ is signal dependant.
Bootstrap techniques mitigate these issues by biasing the transistor gates at voltages higher than V_{DD} and by keeping the gate-source voltage of the switching transistors constant. This can be accomplished by using switched capacitors [Abo99]. On the other hand the required additional circuit increases the power consumption and the area requirement of the circuit. This problem is not present in CT modulators, since they do not use sampling switches, except in front of the quantizer. However, in this case the sampling switches are located inside the loop, where all non-idealities are strongly shaped by the preceding integrators, thus relaxing the requirements on the linearity and conductance of the switches.

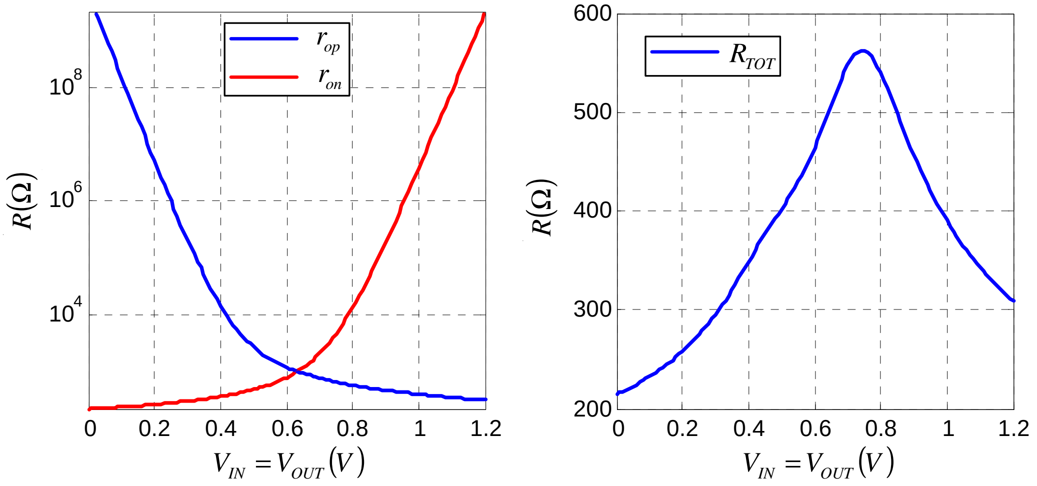


Fig. 2.28. Simulated on-resistance of a transmission gate in UMC 0.13µm CMOS. Transistor sizing: W_p=6µm, W_n=2µm, L_p=L_n=L_{min}=120nm. V_{gn}=1.2 V, V_{gp}=0 V

2.8.2. Continuous time filter

It was shown that DT modulators suffer from poor quality of the switches in low-voltage CMOS sub-µm technologies. Another peculiar aspect is the settling behavior of SC filters used in DT modulators. Since these are clocked systems, they must handle a charge packet in a defined time window, typically in half the clock period. As clearly visible in a time-domain analysis, the voltages of the circuit nodes change abruptly when a switching operation takes place. These "staircase" signals require fast and power-hungry active circuits, which are able to manage fast and short signal changes. An alternative to SC filters is represented by continuous time modulators. A generic modulator with a CT filter is depicted in Fig. 2.29.

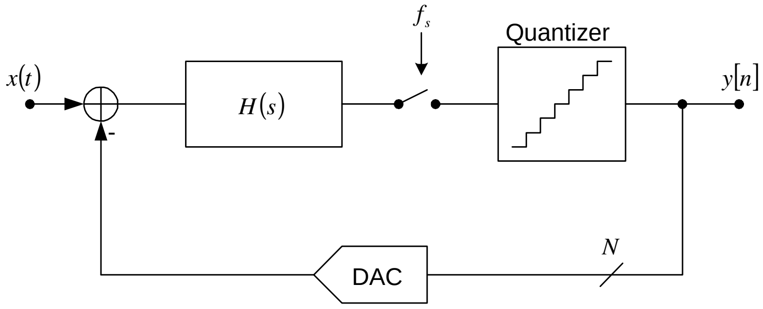


Fig. 2.29. Generic continuous-time sigma-delta modulator

The input signal $x(t)$ is processed by the CT loop filter $H(s)$ and is sampled only just before the quantizer. Hence, smooth internal signals without abrupt amplitude variations are obtained with positive effects on the speed requirements of the analog blocks. On the other hand, all signals processed are allowed to contain only a small error all the time, that is, the whole waveform is important. An additional advantage is given by the location of the sampler after the loop filter: all errors introduced by the sampler, such as settling error and nonlinearities, are suppressed by the gain of the preceding filter. CT filters are constituted by opamps, resistors and capacitors.

The basic block of a CT filter is the integrator, realizing a transfer function k/s. Many implementation ways are possible:

- g_m/C integrator: a voltage controlled current produced by a transistor is fed into a capacitor (Fig. 2.30a). This type of integrator allows low-power operation as no opamp is required and provides good adjustability of the integrator gain by calibration of the transistor transconductance g_m. Nevertheless the linearity is poor, as no feedback regulation is provided.
- Active g_m/C integrator: the current is generated by a transistor and fed to a capacitor, which is located in the feedback path of an opamp (Fig. 2.30b). The advantage is a better linearity, while the current is fed into the virtual ground of an opamp, i.e. to a node with constant potential. An additional advantage of the active topology is the suppression of the parasitic capacitance at the output of the V/I converter (transistor), since the voltage across it is constant. However some non-linearity persists, as the current is generated by an active element with non-linear V/I characteristic, i.e. a MOS transistor.
- Active RC-integrator: this topology provides the best linearity, as the V/I conversion is done by a resistor located between the input and the virtual ground of an opamp (Fig. 2.30c). Assuming the opamp as ideal, the transfer function of the active RC-integrator is:

$$H(s) = -\frac{1}{RCs} = \frac{k_I}{s} \tag{2.88}$$

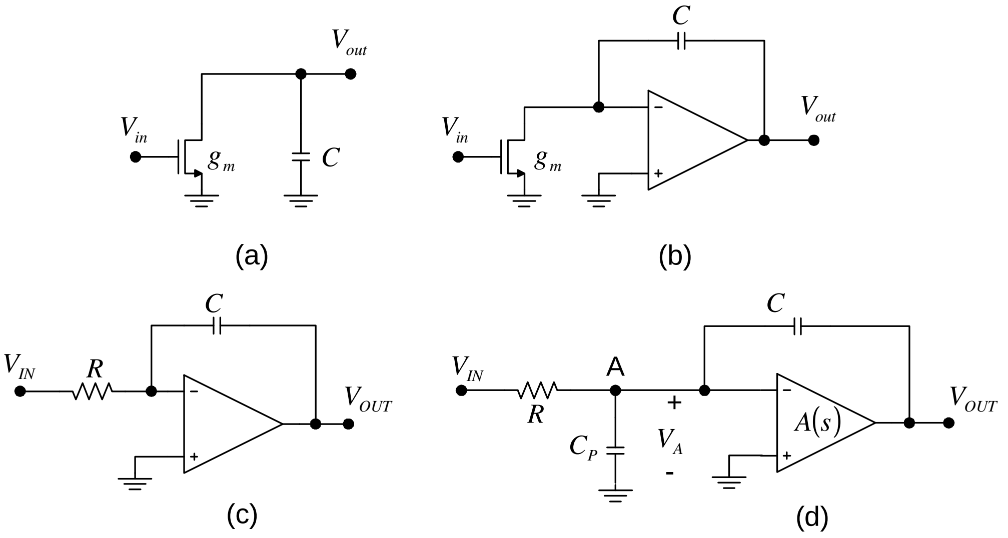


Fig. 2.30. CT integrators, schematic diagram: a) gm/C, b) active gm/C, c) active RC, d) active RC with non-idealities

where k_I is the integrator gain. The most significant problem of CT integrators is here evident: the gain coefficient is the product of a capacitor value with a resistor value. The accuracy of this product is poor when the integrator is realized with integrated components, since it depends on the value of two different components (R and C) which underlie large process variations. In a typical CMOS process the RC time constants have a variation of ±30%. This large variability can be counteracted with specific calibration circuits: after chip fabrication the RC time constant of the integrator is measured and the value of the resistor or of the capacitor is corrected. A possible way of on-chip measurement and calibration is described in sec. 4.3.1.1. Despite this drawback this solution was chosen for the proposed work thanks to the very good linearity achievable.

2.8.2.1. Errors in the TF because of non-idealities

This section analyzes the effect of the non-idealities of the opamp on an active *RC*-integrator. A more realistic model for the opamp is that of a one-pole system with finite DC gain A_{DC} and includes the parasitic capacitance C_P at the virtual ground node (Fig 2.30d). The opamp transfer function is modeled as:

$$A(s) = \frac{A_{DC}}{1 + s/s_P} \tag{2.89}$$

By applying Kirchhoff's current law at node A in Fig 2.30d we obtain:

$$\frac{V_{IN} - V_A}{R} = V_A C_P s + (V_A - V_{OUT}) \cdot Cs \tag{2.90}$$

where V_A is the opamp input voltage, namely:

$$V_A = -\frac{V_{OUT}}{A(s)} \tag{2.91}$$

Inserting (2.91) in (2.90) and solving for V_{OUT}/V_{IN}:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{A(s)}{1 + RC_P s + R[1 + A(s)] \cdot Cs} \tag{2.92}$$

By inserting the opamp transfer function $A(s)$ with one pole (2.89) into (2.92) the integrator TF becomes:

$$H(s) = -\frac{A_{DC}}{[(RC + RC_P)/s_P]s^2 + (1/s_P + A_{DC}RC + RC + RC_P)s + 1} \tag{2.93}$$

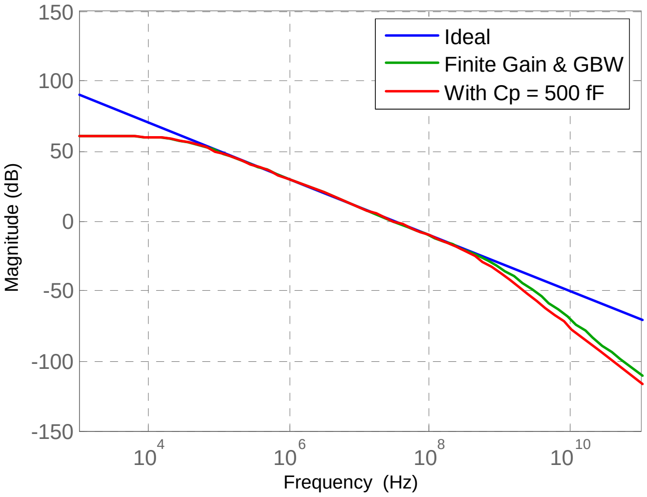


Fig. 2.31. TF of an ideal integrator (blue), an integrator with finite DC-gain and GBW (green) and an integrator with finite DC-gain, GBW and parasitic capacitance C_P.

Eq. 2.93 shows that the DC gain of the integrator is A_{DC} and the presence of two poles. Fig. 2.31 compares the ideal TF with those including the finite opamp gain and GBW with and without the parasitic capacitance C_P.

By assuming that the gain-bandwidth product of the opamp GBW=$s_p \cdot A_{DC}$ is much larger than $1/RC$ the TF can be simplified:

$$H(s) \cong -\frac{A_{DC}}{\left[(RC + RC_P)/s_P\right]s^2 + A_{DC}RCs + 1} \tag{2.94}$$

A generic low-pass TF of 2nd order is:

$$H(s) = -\frac{A_{DC}}{\left(\frac{s}{s_{p1}} + 1\right)\left(\frac{s}{s_{p2}} + 1\right)} \tag{2.95}$$

Assuming $s_{p1} << s_{p2}$ and equating the denominator of (2.95) with that of (2.93) the poles of the RC-integrator can be estimated:

$$s_{p1} \cong -\frac{1}{A_{DC}RC} \qquad s_{p2} \cong -\frac{A_{DC}s_P}{1 + C_P/C} = -\frac{GBW}{1 + C_P/C} \tag{2.96}$$

Hence, a smaller DC-gain shifts the dominant pole away from DC toward larger frequencies while a smaller GBW of the opamp as well as a larger C_P shift the non-dominant pole toward lower frequencies. The location of s_{p1} and s_{p2} influences the TF of the filter and consequently the NTF of the modulator which is based on this filter. Furthermore, the non-dominant pole s_{p2} worsen the phase margin of the filter because of an additional phase shift of –90 degrees. Its position is fundamental to avoid instability of the whole modulator.

2.8.3. DT-CT equivalence

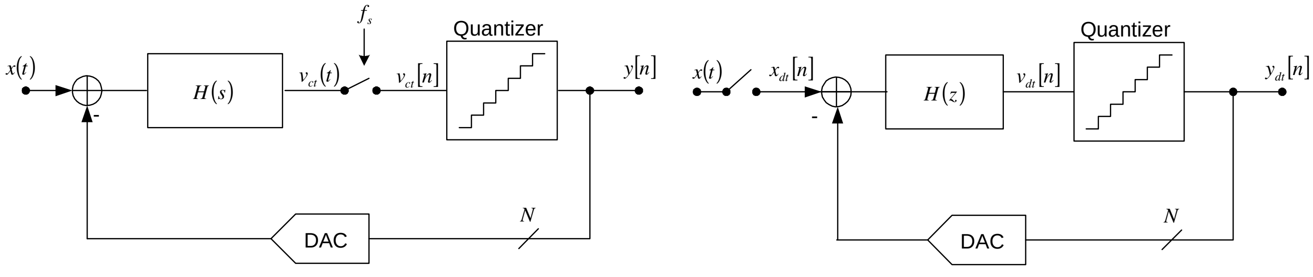
For historical reasons, most of the sigma-delta modulators found in the literature are discrete time. Only in recent years the advantages of CT solutions (in particular, the high speed achievable) toward DT are starting to overwhelm the disadvantages. To facilitate a comparison of the achievable performance of CT and DT modulators, some mathematical instruments are needed. The objective of these instruments is to transform a continuous-time modulator into a discrete-time equivalent and back, both having the same dynamic behavior. For simulation purposes it is also convenient to transform a CT modulator in the equivalent DT, saving much computing power as DT simulations are much faster. Moreover, the analytical modeling of a DT modulator is easier and simpler than that of a CT one, since the latter is a mixed system CT/DT. Last but not least, the modulator design is facilitated by reiterated CT-to-DT transformations and vice versa. For instance, it is usual to start the design with a given NTF, which is a discrete time TF, calculating the relative DT loop filter and then transforming it into a CT equivalent. The non-idealities of the CT are then added and their effect is simulated by transforming the modulator back to a DT equivalent.

One instrument for a CT-to-DT transformation and back is the Impulse Invariant Transformation (IIT). This transformation is based on following definition: two modulators are equivalent if they provide the same output samples for the same input signals [Che02].

This is the case if both quantizer inputs are identical at all sampling instants, that is:

$$v_{ct}(t)\big|_{t=nT_s} = v_{dt}[n] \tag{2.97}$$

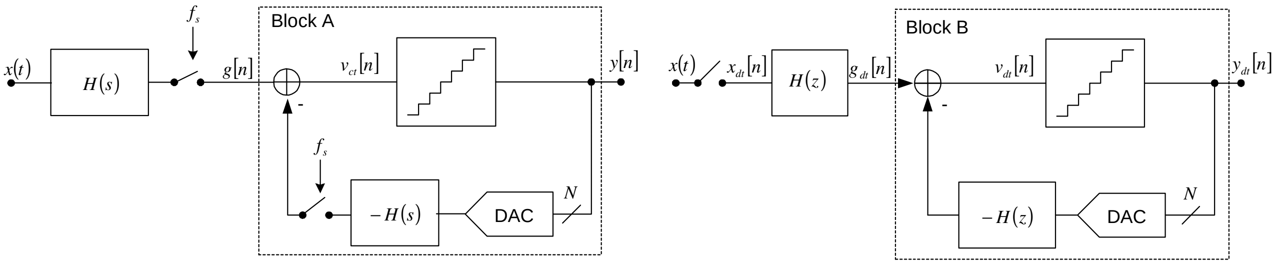
where v_{ct} denotes the quantizer input of the CT modulator and v_{dt} the discrete time one. Fig. 2.32. shows the scheme of a generic CT and that of a DT modulator.



(a) (b)

Fig. 2.32. Continuous-time sigma-delta modulator, b) discrete-time sigma-delta modulator

We can redraw both modulators as depicted in Fig. 2.33 [Tao99], namely by moving the filter and the sampler of the CT modulator or just the filter of the DT modulator to a different location. The so obtained systems are totally equivalent to the original systems in Fig. 2.32, that is, for the same input they provide exactly the same output of the original modulators.



(a) (b)

Fig. 2.33. Different representation of the same modulators as in Fig. 2.32

The advantage of this representation is that both blocks A and B, as illustrated in Fig. 2.33, have discrete-time inputs and outputs making it possible to find a condition that makes both parts equivalent.

By setting the input signal to zero, opening the loops and eliminating the quantizers we obtain the schematics in Fig. 2.34. The outputs of these sub-circuits are the quantizer inputs of the respective modulators. The discrete time DAC can be eliminated, since this ideally does not modify the signal; it must simply provide an analog representation of its input at constant time intervals nT_s. The continuous-time DAC on the contrary can not be eliminated: its output waveform must be exactly known because it directly affects the internal signals of the CT modulators.

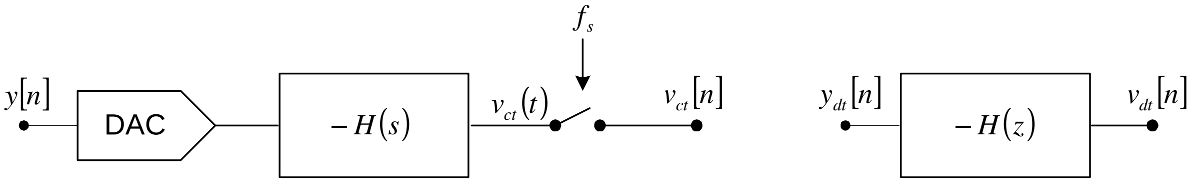


Fig. 2.34. Subcircuits of the CT and DT modulators, to be equalized by means of the IIT

The two sub-circuits in Fig. 2.34 are equivalent if (2.97) applies. This is the case if the sampled impulse responses of both circuits (CT and DT) are identical:

$$h_{ct}(t)\Big|_{t=nT_s} = h_{DAC}(t)\otimes h_{f,ct}(t)\Big|_{t=nT_s} = h_{dt}[n] \tag{2.98}$$

where $h_{DAC}(t)$, $h_{f,ct}(t)$ and $h_{dt}[n]$ are the impulse responses of the CT DAC, the CT filter and the DT filter respectively and $\otimes$ is the convolution operator.

If (2.98) holds both blocks A and B in Fig. 2.33 have the same input-output behavior, i.e. the same transfer function, although they are internally different. Applying the linear model:

$$\frac{Y[z]}{G[z]} = \frac{Y_{dt}[z]}{G_{dt}[z]} = \frac{1}{1+H(z)} \equiv NTF(z) \tag{2.99}$$

where $Y(z)$, $G(z)$, $Y_{dt}(z)$ and $G_{dt}(z)$ are the z-transformed of $y[n]$, $g[n]$, $y_{dt}[n]$ and $g_{dt}[n]$ respectively (Fig. 2.33).

This means that both modulators have the same NTF if (2.98) applies. In fact, they have identical outputs when the input is zero, that is, when only quantization noise circulates through the loops.

Nevertheless they have different STF. Looking at Fig. 2.33 it becomes clear that the input signal is processed differently: the CT modulator first filters *x(t)* with *H(s)*, than samples it and finally filters it again with the TF of block A (Fig. 2.33a); the DT modulator at first samples the signal, then filters it with *H(z)* and finally processes it with block B (Fig. 2.33b). The fundamental difference consists in the *position of the sampler* in the modified schemas: the CT samples the signal *after* low-pass filtering it, that is, an intrinsic anti-aliasing filtering is provided, without additional costs. This is one of the main advantages of CT modulators over DT ones, enabling low-power applications, since often no additional power-hungry anti-aliasing filters are required.

Again, applying the linear model to the modified modulator of Fig. 2.33b, the STF of the DT modulator is:

$$STF_{dt}(z) = H(z)NTF(z) \tag{2.100}$$

The STF of the CT modulator can not be expressed in the z or s-domain since the system realizing this function is mixed CT/DT. Therefore, according to [Sho95] only the frequency response will be given. This is:

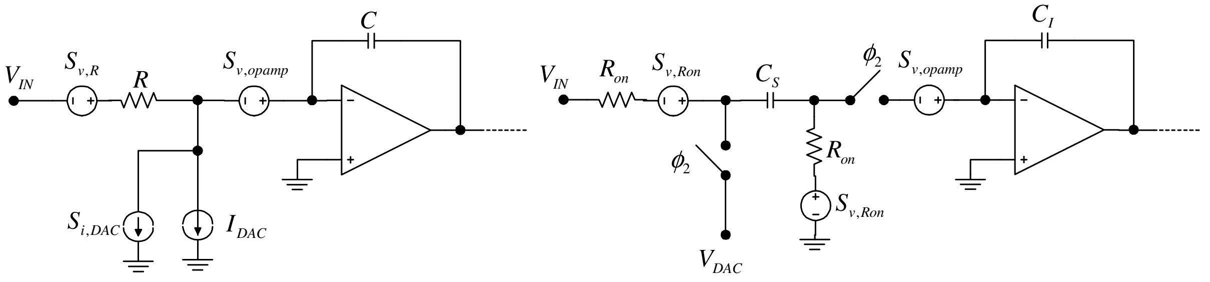
$$STF_{ct}(\omega) = H(j\omega)\cdot e^{-j\omega T_s/2}\cdot\frac{\sin(\omega T_s/2)}{\omega T_s/2}\cdot NTF(z)\Big|_{z=e^{j\omega T_s}} \tag{2.101}$$

that is, the product of the TF of the CT loop filter $H(s)$, a $T_s/2$ delay term, a sinc-function and the DT NTF. The delay term and the sinc filtering are originated by the sampling operation after the CT filtering. This can be better understood by looking at the differently drawn CT modulator in Fig. 2.33a.

It is also possible to convert a CT modulator to a DT equivalent and back with other mathematical instruments, such as the modified z-Transformation ([Jur64], [Gao97]) or using the state-space time-domain representation. These techniques will not be covered in the present work.

2.8.4. Circuit noise

The SNR achievable by a modulator is significantly affected by the noise of the electronic components of the circuit, typically thermal white noise of resistors and MOS transistors and Flicker (1/*f*) noise of MOS transistors. The most sensitive nodes are situated at the input of the modulator: while disturbances such as noise or non-linearities inside the modulator loop are suppressed by the gain of the preceding blocks (noise shaping) and can thus mostly be neglected, this is not the case of disturbances at the modulator input. In the following the most important noise sources at the input of a CT and DT modulator are briefly analyzed.



(a) (b)

Fig. 2.35. Main circuit noise sources of a Sigma-Delta modulator: a) CT, b) DT. The phase φ_1=1 is shown

2.8.4.1. Circuit noise in CT modulators

Basically three circuit noise sources are present at the input of a CT modulator: the input resistor noise, the DAC thermal noise and the opamp input referred noise (Fig. 2.35a).

The PSD of the resistor thermal noise, expressed in V^2/Hz, is:

$$S_{v,R}(f) = 4kTR \tag{2.102}$$

where k is the Boltzmann constant, T the absolute temperature and R the resistor value.

A multibit CT-DAC is a bank of n identical unit current sources connected in parallel, which can be switched on and off. The current sources are made by MOS transistors biased in saturation with a reference gate voltage. The noise of *each* source is essentially thermal noise generated in the transistor channel and Flicker noise caused by random trapping of electrons at the oxide-silicon interface [Raz99]. The noise spectral density of *one* unit current source expressed in A^2/Hz is:

$$S_{i,u}(f) = 4kT\gamma g_{mDAC} + \frac{k_f}{C_{ox}WL}\frac{1}{f}g_{mDAC}^2 \tag{2.103}$$

where C_{ox} is the specific oxide capacitance, W, L and g_{mDAC} the width, length and transconductance of the transistor, f the frequency, k_f a technology depending constant and γ is about 2/3 for long channel transistors or larger for short channel transistors. The latter term of (2.103), accounting for Flicker noise, can be reduced by choosing a large area for the DAC current sources. Assuming all noise sources are uncorrelated, the total DAC noise is the sum of all single noise contributions:

$$S_{i,DAC}(f)=\sum_{i=1}^{n}S_{i,u}(f)=n\cdot S_{i,u}(f) \tag{2.104}$$

where n is the number of current sources in the DAC, that is, the number of quantization levels used in the modulator. To calculate the DAC noise the switches were eliminated, that is, the DAC is assumed to be always connected. Actually, not all DAC elements are switched on during a clock period since the switches are controlled by the bit sequence coming from the quantizer; hence this evaluation is a rather pessimistic estimation.

The opamp input-referred noise is calculated assuming a CMOS differential topology. Fig. 2.36 depicts a typical input stage of a low-voltage opamp. The noise of possible further stages can be neglected if the gain of the input stage is large. Moreover, the equivalent input noise current is neglected, since this is significant only at high frequencies.
Using the small-signal equivalent circuit the total input-referred noise PSD, expressed in V^2/Hz, is obtained:

$$S_{v,opamp}(f)=\frac{8kT\gamma}{g_{m,in}}\left(1+\frac{g_{m,load}}{g_{m,in}}\right)+\frac{2k_f}{C_{ox}f}\left(\frac{1}{W_{in}L_{in}}+\frac{g_{m,load}^{2}}{g_{m,in}^{2}W_{load}L_{load}}\right) \tag{2.105}$$

where the subscripts *in* and *load* refer to the input and load transistors respectively. The first term accounts for the white thermal noise, the latter for Flicker noise.

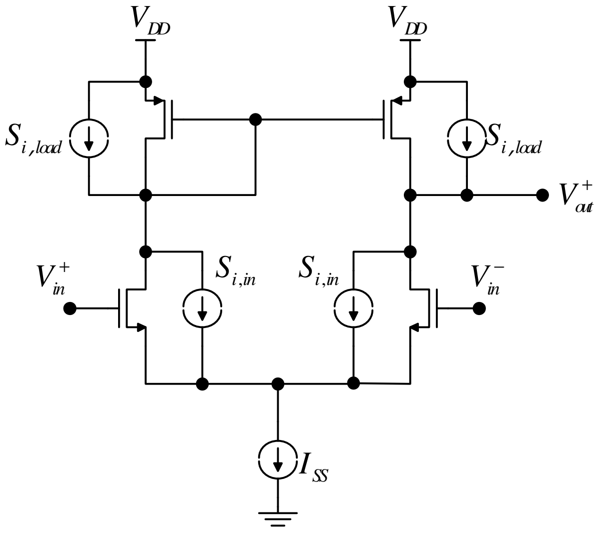


Fig. 2.36. Input stage of a typical low-voltage CMOS opamp

The total circuit noise PSD referred to the input of the modulator is then (Fig. 2.35a):

$$S_{v,in}(f)=S_{v,R}(f)+S_{v,opamp}(f)+S_{i,DAC}(f)\cdot R^{2} \tag{2.106}$$

In order to calculate the SNR due to circuit noise, (2.106) must be integrated in the signal band:

$$SNR_{circuit\,noise}=10\log\frac{P_s}{\int_0^{f_B}S_{v,in}(f)df} \tag{2.107}$$

where P_s is the signal power.

2.8.4.2. Circuit noise in DT modulators

The input sampling capacitor of a multi-bit DT modulator is a bank of n identical unit capacitors C_u connected in parallel. These capacitors sample the input signal and the DAC voltage by means of noisy switches (Fig. 2.35b), realized by means of MOS transistors biased in the triode region. The main noise source is the thermal noise generated in the channel of the switching transistors, which is sampled by the capacitor, causing a charge error. Modeling the closed switches with the on-resistance R_{on} of the transistor, the noise power is, for each unit capacitor, that of a RC member [Nor97]:

$$P_{n,switch} = \frac{kT}{C_u} \tag{2.108}$$

This power is aliased in the frequency band $[0, f_s/2]$, where f_s is the sampling frequency of the switches, leading to the one-sided PSD:

$$S_{v,switch}(f) = \frac{2kT}{C_u f_s} \tag{2.109}$$

Considering two sampling per clock cycle (two phases φ_1 and φ_2) two random uncorrelated charge errors are given, hence the noise power density is doubled:

$$S_{v,switch}(f) = \frac{4kT}{C_u f_s} \tag{2.110}$$

The *total* noise power introduced by all n switches is then:

$$S_{v,switch,tot}(f) = n\frac{4kT}{C_u f_s} \tag{2.111}$$

The other noise source is the input-referred opamp noise of (2.105) as depicted in Fig. 2.35b. The total opamp noise power is:

$$P_{n,opamp} = S_{v,opamp} \cdot B_n \tag{2.112}$$

where B_n is the noise bandwidth of the opamp [Nor97]. This power is aliased in the signal band $[0, f_s/2]$ because of sampling, leading to the one-sided PSD:

$$S_{v,op,sampled}(f) = \frac{2P_{n,opamp}}{f_s} \tag{2.113}$$

In conclusion, the total in-band noise power is:

$$P_{n,tot} = \int_0^{f_B} \left(S_{v,switch,tot} + S_{v,op,sampled}\right) df \tag{2.114}$$

A more detailed description of the circuit noise of a DT integrator can be found in [Fer04].

2.8.5. Jitter error

Jitter error is caused by an uncertainty Δt in the sampling time, that is the time at which the clock edge occurs. This uncertainty is caused by noise in the circuitry for clock generation, i.e. phase noise of the PLL and thermal noise. The most jitter-sensitive points of a sigma-delta modulator are the output of the DAC and, only in DT modulators, the input sample-and-hold circuit. This is because all other internal nodes where sampling occurs are located inside the loop where all errors are suppressed by the high gain of the preceding blocks in the loop [Tao99]. In the following the effect of the clock jitter in both CT and DT DAC will be described. The DAC converts the digital output of the quantizer into an electrical analog signal (a current in CT modulators or a charge in a capacitor in DT modulators, Fig. 2.37) and feeds it back to the the 1st integrator of the loop filter.

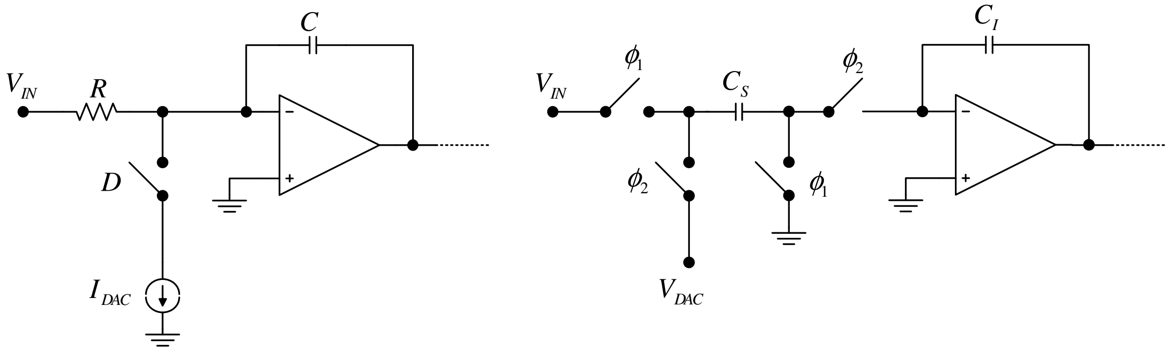


Fig. 2.37. Conceptual scheme of a DAC in a sigma-delta modulator. Left: continuous-time, right: discrete time

The qualitative current waveforms of both DAC types are depicted in Fig. 2.38.

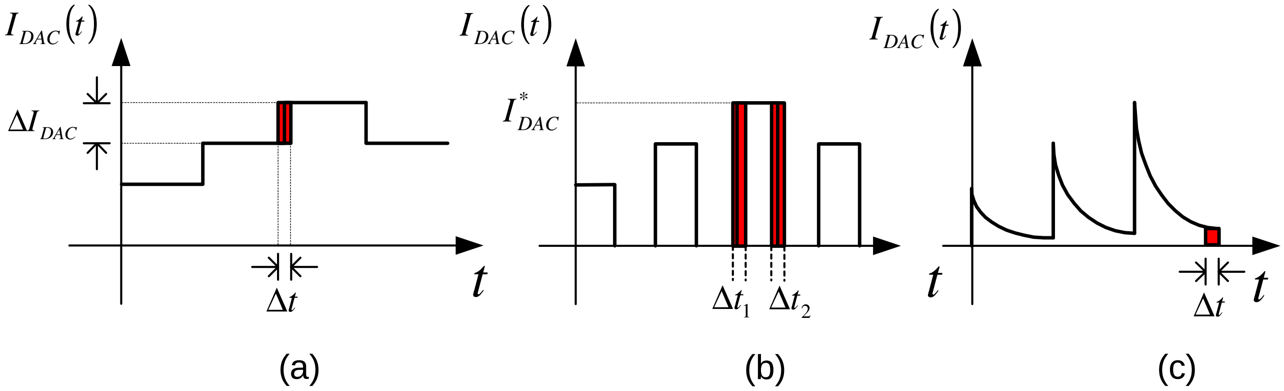


Fig. 2.38. Qualitative waveforms of DAC currents. a) NRZ continuous-time, b) RZ continuous-time, c) SC discrete time

2.8.5.1. NRZ DAC jitter

Fig. 2.38a shows a jittered, rectangular, non-return-to-zero (NRZ) DAC current, typical for continuous-time modulators. Since the DAC output will be integrated by the 1st integrator of the loop filter, the uncertainty in the sampling time introduces a charge error Q_j:

$$Q_j = \int_{T_s}^{T_s+\Delta t} \Delta I_{DAC}(t)dt \tag{2.115}$$

where T_s is the nominal sampling time, ΔI_{DAC} the difference between the actual DAC current and the current at the previous clock cycle (Fig. 2.38a) and Δt the time error because of clock jitter. In multibit modulators the current variation ΔI_{DAC} is an integer multiple k of the unit current I_{LSB}:

$$\Delta I_{DAC} = \pm k I_{LSB} \tag{2.116}$$

The unit current I_{LSB} is equal to the full-scale DAC current I_{FS} divided by 2^N:

$$I_{LSB} = \frac{I_{FS}}{2^N} \tag{2.117}$$

where N is the DAC resolution in bits. Inserting (2.117) in (2.116) we obtain:

$$\Delta I_{DAC} = \pm k \frac{I_{FS}}{2^N} \tag{2.118}$$

In case of an NRZ DAC with rectangular pulse form the integral (2.115) can be simplified, since ΔI_{DAC} is constant within a clock period. We obtain:

$$Q_j = \Delta I_{DAC} \Delta t = \pm k \frac{I_{FS}}{2^N} \Delta t \tag{2.119}$$

Δt is a stochastic variable, usually with Gaussian PSD, zero mean and standard deviation $\sigma(\Delta t)$. According to (2.119) the charge error introduced by the same time uncertainty Δt is halved for each additional bit. It follows that **multibit modulators are less sensitive to jitter noise**.

Furthermore it should be noted that the amplitude of the DAC current variation, ΔI_{DAC}, depends on the output signal of the modulator, which drives the DAC. For example, if the modulator output is constant no charge error is introduced, even if clock jitter is present, since the DAC output does not change, that is k=0 in (2.119). On the other hand if the DAC is driven by a sigma-delta modulated digital signal transitions of up to two or three times the unit current I_{LSB} are possible, as confirmed by simulations. This is due to the large high-frequency content of sigma-delta modulated signals because of the high-pass filtered quantization noise and is reflected in fast transitions in the time domain. Since the amplitude of the DAC current variation at each clock cycle is not known a priory, we can model this by means of its standard deviation $\sigma(\Delta I_{DAC})$. Therefore, we can calculate the standard deviation of the jitter noise *current*, namely the charge error over one clock period as follows:

$$\sigma_{i,jitter} = \frac{\sigma(Q_j)}{T_s} = \frac{\sigma(\Delta t) \cdot \sigma(\Delta I_{DAC})}{T_s} \tag{2.120}$$

Assuming the jitter noise is white, the whole noise power will be aliased in the frequency range $[-f_s/2, f_s/2]$, f_s denoting the clock frequency of the modulator. Hence the PSD of the jitter noise current is:

$$S_{i,jitter}(f)=\frac{\sigma_j^2}{f_s} \tag{2.121}$$

The total in-band jitter noise power is:

$$P_j = \int_{-f_B}^{f_B} S_{i,jitter}(f)df = \frac{2f_B}{f_s}\sigma_j^2 = \frac{\sigma_j^2}{OSR} = \frac{\sigma^2(\Delta t)\cdot\sigma^2(\Delta I_{DAC})}{OSR\cdot T_s^2} \tag{2.122}$$

and the SNR for a modulator affected only by jitter noise is:

$$SNR_j = 10\log\frac{P_S}{P_j} = 10\log\frac{V_{IN}^2/(2R^2)}{\frac{\sigma^2(\Delta t)\cdot\sigma^2(\Delta I_{DAC})}{OSR\cdot T_s^2}} \tag{2.123}$$

where P_S is the signal power and P_j is the jitter power. Since the SNR is dimensionless, the signal power must also be expressed as squared current. The input signal power is obtained assuming a sine signal with amplitude V_{IN} applied to the input resistor R of the modulator.

Alternatively, the standard deviation of the jitter current can be expressed as [Ris94]:

$$\sigma_j = \frac{\sigma(\Delta t)\Delta I_{DAC}A_F}{T_s} \tag{2.124}$$

where an empirical signal activity factor A_F was introduced, which accounts for the average number of signal transitions per clock cycle, based on simulations. Hence we can also express the jitter caused SNR as:

$$SNR_j = 10\log\frac{V_{IN}^2/(2R^2)}{\frac{\sigma_j^2}{OSR}} = 10\log\frac{V_{IN}^2/(2R^2)}{\frac{\sigma^2(\Delta t)\Delta I_{DAC}^2A_F^2}{OSR\cdot T_s^2}} \tag{2.125}$$

2.8.5.2. RZ DAC jitter

Another common DAC pulse in CT modulators is the return-to-zero (RZ) pulse (Fig. 2.38b). The DAC current is nonzero only in a time interval, which is shorter than a clock period. Usually the time at which the signal is active is 50% of T_s. In order to provide the same charge as a NRZ-DAC in half the time, the current value must be doubled.

RZ DAC are very sensitive to jitter noise. Assuming a non-zero signal, the RZ-DAC output has always two edges per clock period, while the NRZ DAC has zero (constant signal) or one edge per clock (if the signal changes)

Additionally, while the NRZ current typically changes of one or two steps, the RZ current must be zeroed at each clock period, hence, the current variation is large increasing the charge error (2.115). Also consider that the current doubling to compensate for the reduced activity time further doubles the charge error induced by jitter.

Because of their considerable jitter sensitivity, RZ-DAC are seldom employed as main DAC in sigma-delta modulators. Nevertheless they prove useful as auxiliary DAC for stability improvement, as shown later in this work.

2.8.5.3. SC DAC jitter

Switched-capacitor DAC are typically employed in DT modulators. Capacitors are charged by means of switches to a reference voltage, hence the current waveforms changes exponentially in time with time constant $\tau = R_{on}C$, where R_{on} is the on-resistance of the switches and C the charged capacitor (Fig. 2.38c).

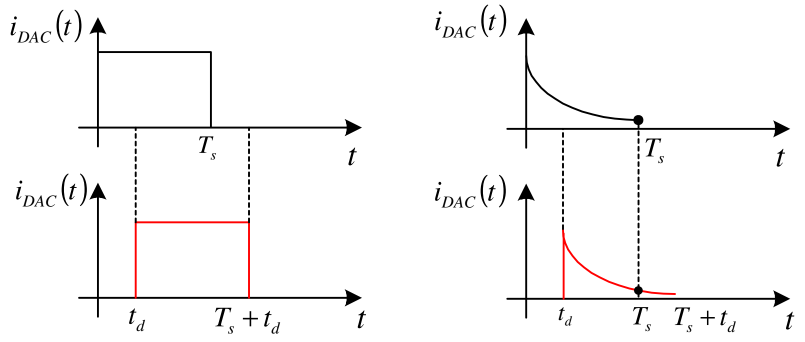
The current waveform has its maximum value at the beginning of the pulse and a very small value at its end (Fig. 2.38c). The edge uncertainty at the beginning of the pulse is not problematic, since this simply represents a (small) time shift of the pulse. The charge error occurs at the end of the pulse where the current is very low, therefore the error is negligible if $\tau \ll T_s$. By a timing error Δt the charge error is:

$$Q_j = \int_{T_s}^{T_s+\Delta t} I_{DAC}(t)dt = \int_{T_s}^{T_s+\Delta t} I_o e^{-R_{on}C/t} dt \qquad (2.126)$$

Because of their robustness against jitter error some attempts have been made to employ SC DAC in CT modulators [Ort02]. Nevertheless SC DAC suffer from a major problem: the current value at the beginning of the pulse is very large and very fast opamps are required to integrate it. The consequence is a large power dissipation of the 1st integrator of the modulator.

2.8.6. Excess Loop Delay

Excess loop delay (ELD) is defined as the delay which elapses between the time when the quantizer output changes and the actual change in the DAC output. This delay occurs in CT modulators because of the nonzero response time of the DAC plus the delay caused by parasitic resistances and capacitances of the metal interconnections. Fig. 2.39a shows an ideal rectangular DAC waveform and its delayed version.



(a) (b)

Fig. 2.39. Ideal DAC waveforms (black) and delayed DAC waveforms (red). Left: CT, right: DT

ELD is detrimental for CT modulators, as it reduces the stability margin of the loop and eventually leads to instability. DT modulators are affected by ELD only in a limited amount. In fact, a DT DAC consists in a reference voltage applied to one or more capacitors by means of switches, which are controlled by the quantizer output. Fig. 2.39b shows the current of a DT DAC charging a capacitor characterized by an exponential waveform. At the instants $n \cdot T_s$ the DAC is disconnected from the capacitors. ELD simply shifts the starting point of the capacitor charging process by an amount t_d causing a small error because of incomplete settling. Since the current is relatively small at the end of the pulse (the capacitor is almost completely charged), the error is usually negligible, similarly to the jitter error in DT modulators.

In order to quantify the effects of ELD on CT modulators the impulse-invariant transformation (IIT) proves very useful [Che02]. In order to obtain a certain NTF a DT prototype loop filter is designed. After defining the impulse response of the CT DAC to be used, the DT filter is transformed into an equivalent CT with the IIF. An additional delay t_d placed before the DAC shifts the impulse response of the CT system composed of the DAC in series with the loop filter (Fig. 2.40). Here $h_{dac}(t)$ and $h(t)$ denote the impulse response of the DAC and of the loop filter respectively.

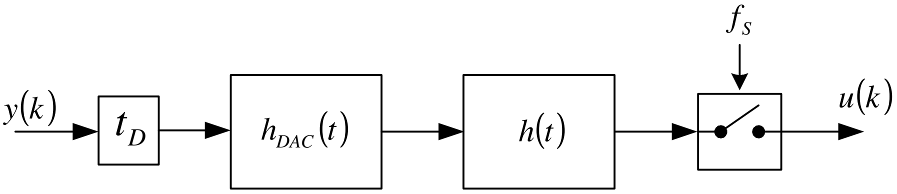


Fig. 2.40. Subcircuit with ELD of the CT modulator which must be equivalent to the DT prototype

As a result the sampled impulse response is now different from that of the prototype modulator. Transforming the sampled delayed impulse response back into the z-domain a new $H(z)$ is obtained, which is different from the original one. In particular, according to [Che02]:

- A delay which shifts the DAC pulse *without exceeding* the clock period T_s, typical for RZ DAC with pulse length of 50% of the clock period, causes a variation of the coefficients of the equivalent $H(z)$ and hence of $NTF(z)$. Therefore, the noise performance is degraded, since the new equivalent NTF is not optimal. This degradation can be compensated by adjusting the filter coefficients in order to restore the original $H(z)$.
- A shift of the DAC pulse *beyond* T_s causes not only noise degradation but also possible instability of the loop. When this case occurs, the order of the DT equivalent modulator is increased by one. This is always the case when using NRZ DAC, as the pulse length is equal to a full clock period. Intuitively, a rectangular DAC pulse $h(t)$ exceeding T_s can be seen as the sum of two rectangular pulses $h_1(t)$ and $h_2(t)$ (Fig. 2.41): one pulse inside the time window between 0 and T_s, the second one inside the next time window from T_s to $2T_s$. Since the second pulse starts at T_s it can be regarded as a rectangular pulse delayed by one clock period. This delayed pulse generates a z^{-1} term in the DT equivalent modulator, obtained with the IIT, and is responsible for the order increase of the equivalent modulator. In order to compensate for ELD in such a case an additional feedback branch must be provided to the CT filter to gain one more degree of freedom [Che99].

2.8.7. Summary of pros and cons of CT and DT modulators

In the following pros and cons of CT and DT are summarized:

- **Mismatch sensitivity**: DT modulators are very robust against process-related variations because they rely on precise capacitor ratios. CT modulators underlie large variations of the filter coefficients and need additional calibration circuitry
- **Speed**: DT filters work with fast changing, abrupt signals, putting stringent requirements on the speed of the operational amplifiers. CT modulators process smooth, relatively slow changing signals, enabling the use of slower, low-power opamps.

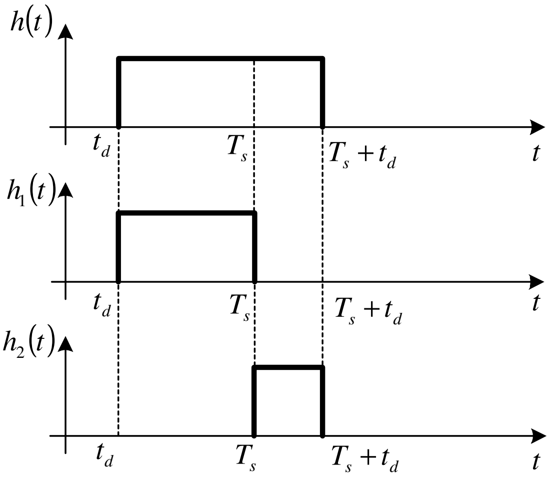


Fig. 2.41. Decomposition of a delayed NRZ DAC pulse in two components

- **Anti-aliasing**: DT modulators require an anti-aliasing (A/A) filter directly at the input increasing the total power consumption. In CT modulators the sample-and-hold block is located after the loop filter. Since this has already a low-pass behavior, no A/A filter is usually required, enabling low-power solutions.
- **Sample-and-hold** (S/H). This circuit is located directly at the input of DT modulators, that is, on the most sensitive location of the modulator. This means that the S/H must feature very good linearity properties and limited errors. On the contrary, CT modulators perform the sampling just before the quantizer, that is, after the loop filter, largely relaxing the requirement on the S/H circuit.
- **Circuit noise**: the overall circuit noise of a DT modulator is contributed in large part by the thermal noise of the input switches, which is sampled on the input capacitors. This puts a limit on the minimum size of these capacitors. This limitation is not present in CT modulators, as sampling occurs solely before the quantizer, where any noise contribution is largely suppressed. Furthermore, the white noise terms are aliased because of sampling in DT modulators, while in a CT modulator this takes place only after filtering. Hence, CT modulators are expected to exhibit less noise.
- **Jitter noise**: CT modulators are more sensitive to jitter noise than DT modulators because of rectangular instead of exponential DAC waveforms. Nevertheless, this error source can be strongly attenuated by increasing the number of quantization levels.
- **Excess Loop Delay**: DT modulators are, in a similar manner as for jitter error, very robust against ELD because of the exponential waveforms of the DAC. CT modulators are instead sensitive to ELD. Compensation is required to avoid performance drop and/or instability issues.

2.9. Single-Bit / Multibit

The resolution achievable with a sigma-delta modulator was calculated in (2.53). We can simply enhance the resolution by one bit, that is, we can improve the SNR of 6 dB, by adding one bit to the quantizer. When increasing the number of quantizer bits also the DAC resolution must be increased of the same factor. These architectural enhancement have pros and cons, which will be examined in the following:

- **Power consumption**: each additional bit of the quantizer, typically a flash-ADC, means a doubling of the circuitry for the A/D conversion, basically comparators and latches for synchronization. The total power consumption of the quantizer therefore approximately doubles for each additional bit.
- **Chip area**: for the same reason also the quantizer area doubles for each additional bit.
- **Jitter sensitivity**: as seen previously, the jitter error is proportional to the amplitude of the DAC output variation. Each additional bit halves the amplitude of a step of this electrical signal, hence halving the charge error introduced by the jitter.
- **Slew rate**: Each additional bit halves the amplitude of a step of the output DAC, therefore reducing the required slew-rate of the opamp of the 1st integrator.
- **DAC linearity**: a one-bit DAC is intrinsically linear because of its two-level input-output characteristic, that is, it can only be affected by gain error or offset. On the other hand multi-bit DAC suffer from non-linearities because of mismatch of the DAC elements (usually capacitors in the DT case, current sources or resistors in the CT case).
- **Modulator stability**: multibit modulators are more robust toward instability. Each additional bit halves the quantization interval ΔU, that is, the quantization noise power circulating in the loop is also halved. Thanks to this, a more aggressive noise shaping with higher values of $\mathrm{NTF}_{\mathrm{MAX}}$ can be tolerated when using more bits.

The most important pros and cons are summarized in the following table.

	Single-bit modulator	**Multibit modulator**
Power consumption	low	high
Chip area	low	high
Jitter sensitivity	high	low
Slew rate required	high	low
DAC linearity required	low	high
Stability	low	high

Tab. 2.2. Pro and cons of single-bit and multibit modulators

The choice of the most appropriate architecture for the proposed work is discussed in the following chapter.

Chapter 3

Low-power high-speed CT ΣΔ modulator: system level design

This chapter illustrates the system specifications of the modulator and the high level approach in order to define the circuit properties fulfilling the specifications. Target of this work is the realization of a high-speed, low-power Sigma-Delta (ΣΔ) modulator. The modulator is intended to be used in high-speed portable broadband communication devices, such as mobile telephony of the next generation, enabling data rates up to some tenth of Megabit per second. In order to reduce fabrication costs, a mainstream standard CMOS process is used.

3.1. Specifications

The table below summarizes the specifications of the modulator:

Resolution (ENOB)	11 bit
Signal Bandwidth	12.5 MHz
Power dissipation	< 15 mW
Technology	CMOS

Tab 3.1. Modulator specifications

Hence, the modulator should provide a resolution of 11-bit at high sampling rate when converting an input signal with a bandwidth of 12.5 MHz. The total power dissipation should not exceed 15 mW, which is a fairly stringent specification for the required bandwidth and resolution. The very low power requirement should enable the employment of the modulator in portable devices. The bandwidth and speed requirements are compatible with the specifications of the wireless broadband WiMAX standard [Wim06], which uses a scalable channel width from 1.25 MHz to 20 MHz [Kim09].

3.2. Architecture choice and loop filter synthesis

The first decision to be taken concerns the modulator family: CT or DT? As the total power consumption must be kept as low as 15 mW CT modulators appear to be the natural choice. As explained in chapter 2 this family of modulators is very promising in the low-power field, enabling the use of slower operational amplifiers in the loop filter. Therefore, a CT modulator was chosen.

The second step concerns the choice of a single-loop or multi-loop (cascaded) architecture. The only publication to date known to the author implementing an on-chip CT cascaded modulator is [Bre04]. Cascading requires good matching between the analog transfer function of the loop filters and that of the digital error correction logic in order to avoid quantization noise leakage from the first stage. This technique is thus more convenient in DT modulators, where the integrator coefficients depend on capacitor ratios and allow therefore good accuracy. On the contrary, CT filter coefficients rely on *RC* time constants which are subject to large variations due to process variations. According to this, we decided to employ a single-loop architecture.
Starting from a generic CT single-loop modulator and taking into account the speed and resolution specifications, we have some degrees of freedom regarding the modulator architecture. In particular three parameters still need to be defined: the modulator order, the oversampling ratio (OSR) and the number of bits of the quantizer. In fact, more solutions exist satisfying the specifications.

Obviously these parameters can not be increased arbitrarily. The maximum OSR is limited by the transit frequency of the transistors of the available technology and by the power consumption of the circuit blocks. Increasing n, the quantizer bits, improves the stability and also reduces the necessary slew-rate of the opamps (the width of a single DAC step halves for each additional bit); nevertheless, each additional bit doubles the quantizer area and its power consumption. Furthermore a larger n impacts the complexity of the DAC and that of the circuit appointed for the DAC linearization. For this reason most of the CT modulators published so far do not exceed 5 bit in the quantizer. A one-bit solution was excluded because of the poor resolution achievable. Finally, increasing the order L of the modulator reduces the stability of the loop and increases linearly the power consumption of the loop filter. In practice, more than 5 integrators are seldom used, as the reduced stability must be compensated at expense of a less aggressive noise shaping (s. Sect. 2.5.5), so that the resolution improvement because of the order increase vanishes.

With these considerations in mind following parameter set was chosen:

- Modulator order L=3
- Oversampling ratio OSR=16
- Number of bits of the quantizer n=4.

The OSR selected implies, assuming a signal band f_B=12.5 MHz, a clock frequency of the modulator of:

$$f_s = 2 \cdot OSR \cdot f_B = 400\,\text{MHz} \tag{3.1}$$

This clock frequency is adequate for the 0.13 μm CMOS technology at our disposal.

The optimal NTF is calculated with the aid of the Schreier's algorithm [Sch05, chapter 8]. This algorithm places the zeros of the NTF according to Tab. 2.1 in chapter 2, in order to minimize the quantization noise power in the signal band. Moreover, the location of the poles of the NTF is determined iteratively in order to limit the maximum of the NTF (NTF_{max}) to a value selected by the user. Since a multibit quantizer with n=4 was chosen, a more aggressive noise shaping with larger NTF_{max} is allowed. For the proposed modulator NTF_{max}=3.1623=10dB was selected. The transfer function of the prototype NTF calculated by the algorithm is:

$$NTF = \frac{(z-1)(z^2-1.977z+1)}{(z-0.3387)(z^2-0.5965z+0.2823)} = \frac{(z-1)(z^2-2z\cos\omega_0+1)}{(z-0.3387)(z^2-0.5965z+0.2823)} \tag{3.2}$$

where ω_0 is the resonating frequency (notch) of NTF(z) normalized to f_s. The notch frequency f_n is thus located at:

$$f_n = \frac{\omega_0 \cdot f_s}{2\pi} = 9.664\,MHz \tag{3.3}$$

The Bode diagram and the location of the poles and zeros on the complex z-plane are plotted in Fig. 3.1. The TF has one zero at DC and two complex-conjugate zeros on the unit circle, realizing a notch in the frequency response, one real pole and two complex conjugate poles. The expected resolution is, according the formula of the linear model with the selected parameters:

$$SQNR = 1.76 + 6.02N - 10\log\frac{\pi^{2L}}{2L+1} + 10\log OSR^{2L+1} + ZS = 88 + 8 = 96dB \tag{3.4}$$

where the term ZS accounts for the SQNR improvement with zero spreading (Tab. 2.1, chapter 2).

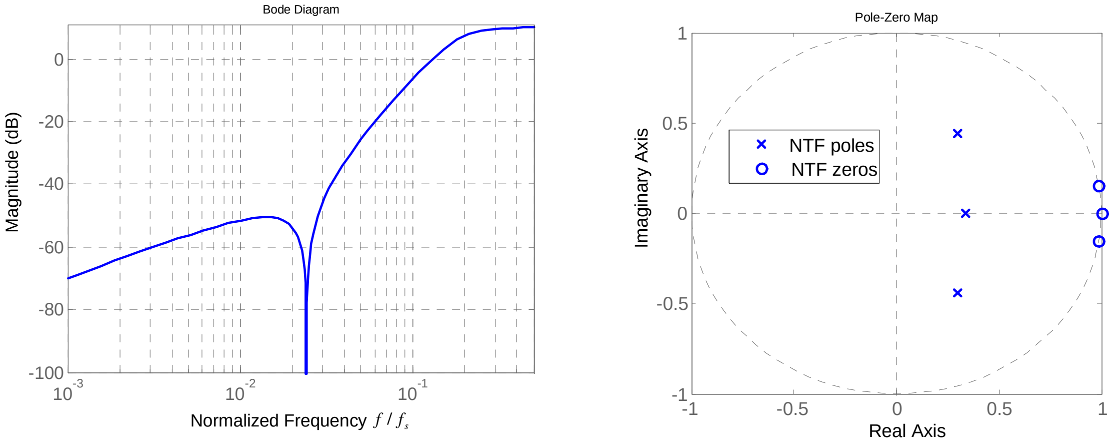


Fig. 3.1. Bode diagram and pole-zero diagram of the NTF of the DT prototype modulator

3.3. High level simulations of the prototype DT modulator

The subsequent design steps include:

- generation of a prototype DT modulator with the calculated NTF
- high-level simulations of the DT modulator
- generation of the equivalent CT loop filter by means of the IIT

The discrete-time loop filter realizing the proposed NTF is, rewriting (eq. 2.24):

$$H(z) = \frac{1}{NTF} - 1 \tag{3.5}$$

Substituting (3.2) in (3.5) we obtain:

$$H(z)=\frac{2.042z^2-2.493z+0.9044}{(z-1)(z^2-1.977z+1)}=\frac{2.042z^2-2.493z+0.9044}{(z-1)(z^2-2z\cos\omega_0+1)} \tag{3.6}$$

As expected, the poles of the filter are the zeros of the NTF in (3.2) The Bode diagram of the TF of the DT prototype filter is plotted in Fig. 3.2

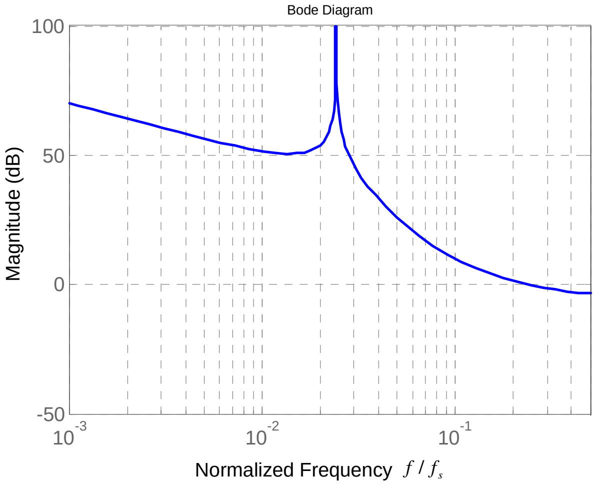


Fig. 3.2. Bode diagram of the DT prototype filter

So far a prototype NTF and the relative DT loop filter H(z) were calculated by means of considerations which are based on the linear model. In order to get more realistic simulation results a high-level numerical simulation of the modulator is required. This was done by means of the simulation tool Simulink® included in the software Matlab®. The simulation bench for the DT 3rd order modulator is depicted in Fig. 3.3 and includes: an input sine signal, a zero order hold, the DT loop filter modeled with its TF and a 4-bit quantizer. A Matlab® function calculates the FFT and the SNR of the digital output flow.

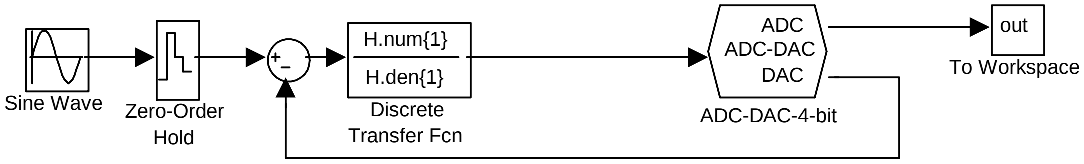


Fig. 3.3. High-level simulation bench of DT prototype modulator

The maximum stable amplitude (MSA) of the input signal is at about -1 dB_{FS} (one dB below the full-scale input) and the maximum achievable SQNR amounts to 91 dB, namely 14.8 bit. This result is in good accordance with the value foreseen by the linear model (3.4), which was calculated for a full scale input signal. For an input signal of -1 dB_{FS} 95 dB are expected from the linear analysis. Although the SNR specification amounts to 11 bit, a large margin is needed, since circuit noise and other circuit non-idealities significantly lower the achievable SNR. Fig. 3.4 plots the SQNR of the DT prototype modulator versus the input signal amplitude in dB_{FS}.

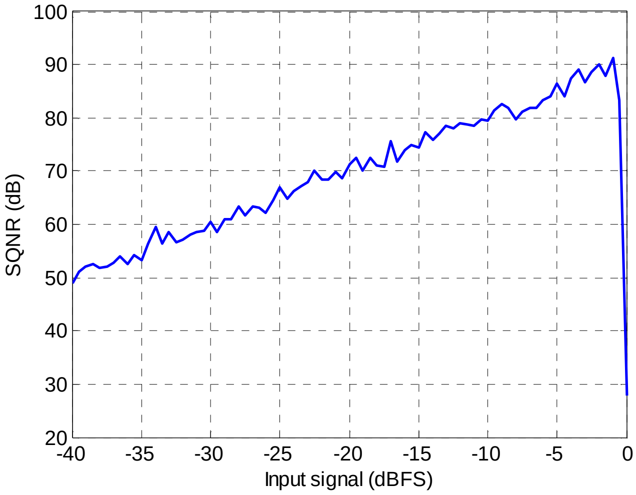


Fig. 3.4. SQNR of the DT prototype modulator against input signal amplitude

3.4. Calculation of the transfer function of the CT filter with the IIT

The next step consists in transforming the DT prototype into a CT equivalent loop filter. The mathematical instrument used for the equivalence is the Impulse Invariance Transformation (IIT). The DT filter TF is expanded in partial fractions and then each term is transformed in the CT equivalent on the basis of conversion tables found in the literature ([Che02],[Sho94]). A generic DT transfer function $H(z)$ has i zeros and j poles with $i \leq j$ because of causality and physical realizability. The numerator and denominator polynomials can be factorized:

$$H(z) = \frac{(z - z_{n1})(z - z_{n2})\ldots(z - z_{ni})}{(z - z_{p1})(z - z_{p2})\ldots(z - z_{pj})} \tag{3.7}$$

where z_{ni} and z_{pj} are respectively the zeros and the poles of the DT loop filter and can be real or complex.

The partial expansion consists in rewriting (3.7) in the form:

$$H(z) = \frac{R_1}{z - z_{p1}} + \frac{R_2}{z - z_{p2}} + \ldots + \frac{R_j}{z - z_{pj}} + k(z) \tag{3.8}$$

R_j are called residues and are real or complex numbers, the direct term $k(z)$ is nonzero only if $i=j$.

The partial fractions in (3.8) are converted through the impulse invariant transformation (IIT) into CT equivalent terms, considering the CT DAC pulse form. For the proposed CT modulator a NRZ-DAC is chosen, due to its low jitter sensitivity and lower slew rate requirements on the 1st integrator.

For NRZ pulse forms the equivalence for the partial fractions is [Che02]:

$$\frac{R_i}{z - 1} \Leftrightarrow f_s \frac{R_i}{s} \tag{3.9}$$

if $z_{pi}=1$ (that is, the pole is at DC), otherwise

$$\frac{R_i}{z-z_{pi}} \Leftrightarrow \frac{R_i f_s \ln z_{pi}}{\left(z_{pi}-1\right)\left(s-f_s \ln z_{pi}\right)} \tag{3.10}$$

where f_s is the clock frequency of the modulator, in our case f_s=400 MHz. The IIT maps the complex-conjugate DT poles located on the unit circle into purely imaginary poles located on on the $j\omega$-axis according to the relation:

$$z_{pi}=e^{j\omega_{dt}T_s} \Leftrightarrow s_{pi}=f_s \ln z_{pi}=f_s j\omega T_s=j\omega_{ct} \tag{3.11}$$

where ω_{dt} and ω_{ct} are the DT and CT frequency respectively.

The CT equivalent loop filter is the sum of all partial fractions in the s-domain. The prototype function $H(z)$ has one pole in DC and a pair of complex-conjugate poles. Expanding (3.6) in partial fractions we obtain:

$$H(z)=\frac{R_1}{z-1}+\frac{R_2}{z-z_p}+\frac{R_2^*}{z-z_p^*} \tag{3.12}$$

Where (*) denotes the complex conjugate operation. The residues and the poles of (3.12) are indicated in Tab. 3.2.

R_1	19.7182
R_2	$-8.8382-j\,4.4329$
R_2^*	$-8.8382+j\,4.4329$
z_p	$0.9885+j\,0.1512$
z_p^*	$0.9885-j\,0.1512$

Tab 3.2 Residues and poles of the partial fraction expansion of the prototype filter

When using a NRZ-DAC the TF of the CT equivalent filter is:

$$H(s)=f_s\frac{R_1}{s}+\frac{R_2\cdot f_s \ln z_p}{\left(z_p-1\right)\left(s-f_s \ln z_p\right)}+\frac{R_2^*\cdot f_s \ln z_p^*}{\left(z_p^*-1\right)\left(s-f_s \ln z_p^*\right)} \tag{3.13}$$

Replacing the coefficients in Tab. 3.2 and adding up the partial fractions we get:

$$H(s)=\frac{5.61\cdot 10^{8}s^{2}+1.82\cdot 10^{17}s+2.91\cdot 10^{25}}{s\left(s^{2}+3.69\cdot 10^{15}\right)} \tag{3.14}$$

Fig. 3.5 plots the Bode diagram and the step response of the DT prototype and CT equivalent filter. The step response instead of the impulse response is shown for convenience, as it is difficult to simulate an ideal pulse generator. The plots show that the *sampled* step response of the DT filter and that of the system composed by the series of a NRZ-DAC and the equivalent CT filter are identical.

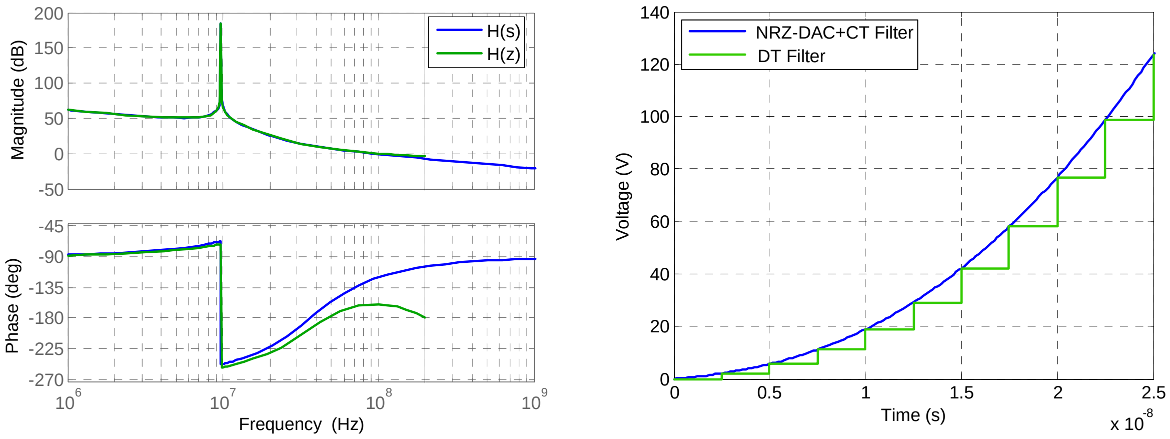


Fig. 3.5. Left: Bode diagram of the DT filter and of the CT equivalent filter. Right: step response of the DT filter and of the NRZ-DAC+CT filter system.

The filter stability margins are plotted in Fig. 3.6 together with the location of the singularities (poles and zeros) on the s-plane. The poles of the prototype DT filter are located on the unit circle and mapped by the IIT. The CT filter has, according to (3.9) and (3.11) one pole at DC and two purely imaginary poles. Furthermore, two complex-conjugate zeros guarantee the stability improving the phase margin (PM) of the loop filter.

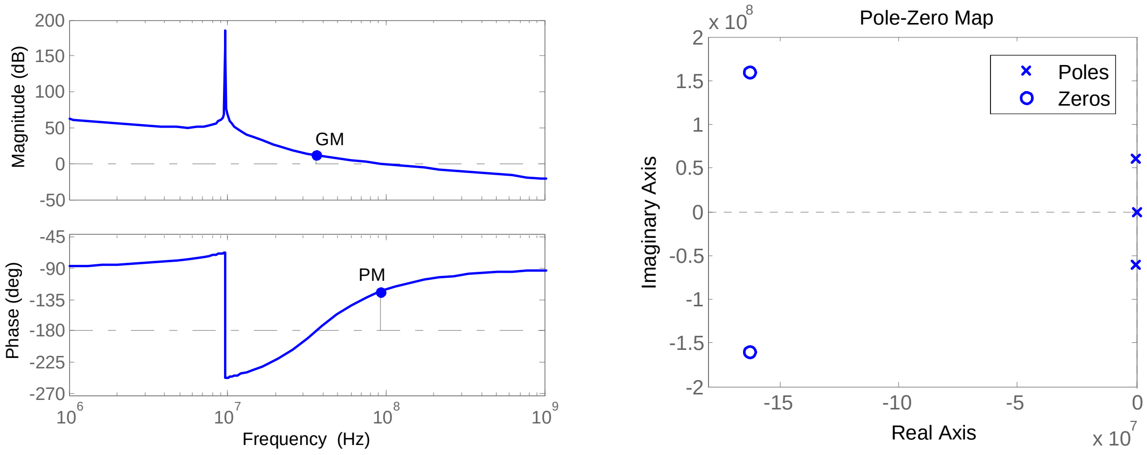


Fig. 3.6. Equivalent CT loop filter. Left: stability margins, right: singularities on the *s*-plane

The main filter parameters are described in Tab 3.3.

Phase margin (PM)	56.2°
Gain margin (GM)	11.6 dB
Unity gain frequency	91.7 MHz
Pole frequencies	0, 9.66 MHz (double)
Zero frequencies	36.2 MHz (double)

Tab 3.3. Main parameters of the CT loop filters

3.5. CT loop filter architecture

3.5.1. CIFF and CIFB topologies

The next step of the modulator synthesis consists in the implementation of the CT filter with an appropriate architecture. At this point the filter is described at high level as a system composed of L integrators, where L is the filter order (L=3 in our case) connected together by means of feed-forward (FF) and feedback (FB) paths. Basically two main filter topologies exist:

- **Chain of integrators with feed-forward paths (CIFF)**. Fig. 3.7 shows a modulator with a CIFF loop filter. The filter is characterized by only one feedback path and L-1 FF paths, which converge in an adder block located after the last integrator. The filter transfer function is:

$$H_{CIFF}(s)=\frac{V(s)}{X(s)}=-\frac{V(s)}{Y(s)}=\frac{A_1k_1s^{L-1}+A_1A_2k_2s^{L-2}+\ldots+A_1A_2\ldots A_Lk_L}{s^L} \tag{3.15}$$

  where L is the filter order, A_i are the integrator coefficients and k_i the FF coefficients. Eq. (3.15) shows that this filter has L poles at DC and L-1 zeros. The zeros are needed to ensure the stability of the loop, increasing the phase margin. To estimate the frequency response of the STF of the modulator we can remove the sampler and the quantizer, replace them with a short and calculate the closed loop TF of the filter:

$$H_{CIFF,CL}(s)=\frac{Y(s)}{X(s)}=\frac{H_{CIFF}(s)}{1+H_{CIFF}(s)}=+\frac{A_1k_1s^{L-1}+A_1A_2k_2s^{L-2}+\ldots+A_1A_2\ldots A_Lk_L}{s^L+A_1k_1s^{L-1}+A_1A_2k_2s^{L-2}\ldots+A_1A_2\ldots A_Lk_L} \tag{3.16}$$

  this filter has the disadvantage that the closed loop frequency response has a peaking at high frequencies because of the zeros in the signal path (cp. [Phi04]). In some cases pre-filtering of the input signal could be required. Nevertheless CIFF filters are the best solution when implementing low-power modulators. At first, only one feedback path is provided, that is, only one DAC is theoretically required to convert the quantizer output to an analog signal. Secondly, if the loop gain is large, only the quantization noise flows through the integrators because of the subtraction $X(s)$-$Y(s)$ at the very input of the filter. In fact, the output $Y(s)$ contains both the quantization noise and the input signal; the latter component is cancelled out by the subtractor at the modulator input. As the quantization noise power is typically much smaller than the signal power, larger integrator coefficients can be selected without saturation of the integrator outputs. This allows the use of smaller, power saving integrator capacitors. Because of its low-power advantages this solution with some major modifications was preferred for this work.

- **Chain of integrators with feedback paths (CIFB)**. Fig. 3.8 shows a modulator with a CIFB loop filter. The filter exhibits L feedback paths and no FF paths. Two filter transfer functions can be defined, one for the signal and one for the output of the modulator which is fed back:

$$H_{CIFB,X}(s)=\frac{V(s)}{X(s)}=\frac{A_1A_2\ldots A_L}{s^L} \tag{3.17}$$

  and

$$H_{CIFB,Y}(s)=\frac{V(s)}{Y(s)}=\frac{A_Lk_Ls^{L-1}+A_{L-1}A_Lk_{L-1}s^{L-2}+\ldots+A_1A_2\ldots A_Lk_1}{s^L} \tag{3.18}$$

Again, the frequency response of the STF can be estimated by replacing sampler and quantizer with a short. The closed loop TF of the filter is, considering the input $X(s)$:

$$H_{CIFB,CL}(s)=\frac{Y(s)}{X(s)}=\frac{A_1A_2...A_L}{s^L+A_Lk_Ls^{L-1}+A_{L-1}A_Lk_{L-1}s^{L-2}+...A_1A_2...A_Lk_1} \tag{3.19}$$

The frequency response of $H_{CIFB,CL}(s)$ is monotonic and has no frequency peaking since no zeros exist in the signal path. The main disadvantage is that a scaled replica of the input signal appears at each integrator output. To understand this let us assume that all integrators have large gain in the signal band, that is, at low frequencies. Each adder of the filter has two inputs, the first one is the output of the preceding integrator, the second one is a scaled version of the quantizer output. The large loop gain will force both inputs to be nearly the same at low frequencies, that is each integrator output provides a signal $v_i(t)\cong k_iy(t)\cong k_ix(t)$, where $v_i(t)$, $y(t)$, $x(t)$ and k_i are the output of the i-th integrator, the quantizer output, the input signal and the coefficient feedback respectively. Since all loop integrator must provide large amplitude signals, larger integration capacitors are needed to prevent saturation of the integrator outputs, increasing the power consumption. Moreover, each feedback path requires an additional DAC. For this reason we discarded the CIFB as not suitable for low-power solutions.

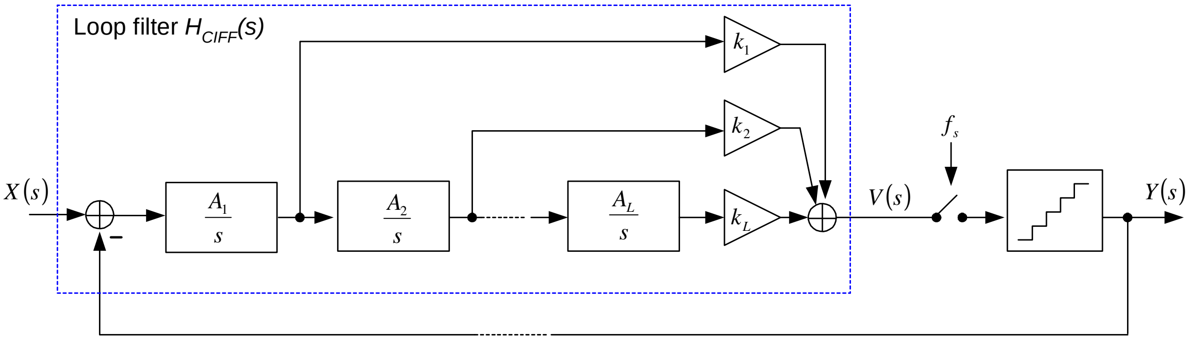


Fig. 3.7. Generic CIFF modulator

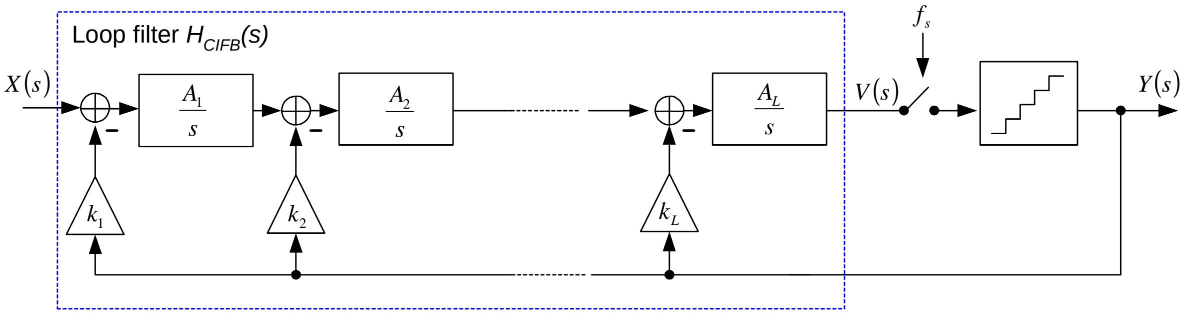


Fig. 3.8. Generic CIFB modulator

Both topologies in Fig. 3.7 and 3.8 can be modified by adding a direct feed-forward path from the modulator input $X(s)$ to the quantizer input $V(s)$. This is particularly useful in the case of a CIFB modulator, as the additional FF-path avoids that the input signal is processed by all the integrators but the last one, hence relaxing their operation. On the other hand an all-pass, unit STF without filtering is obtained[2], which is detrimental if high-frequency interferers are present at the input of the modulator.

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[2] This can be easily verified with the help of the linear model. With the additional FF-path STF=1 is obtained.

3.5.2. Adder removal

As explained in the previous section CIFF loop filters are superior in terms of low power consumption. One issue of this technology is the presence of an adder after the last integrator. This adder can be implemented with a summing amplifier, that is, an opamp with input resistors and a feedback resistor which converts the signals from the FF paths in currents, sum them up, and converts them again to a voltage [Red08]. This choice is unavoidably associated with additional power consumption (because of the opamp) and delay, thus worsening the stability behavior of the loop. In the literature also solutions exist with current mode quantizers ([Dör04], [Pat04], [Phi04], [Yan04]). The disadvantage of this solution is the high linearity required in the transconductance amplifiers converting the integrator output voltages into currents. A third possibility consists in reusing the virtual ground node of the last integrator to implement the addition, saving the additional summing amplifier [Sch04]. Since the feedback impedance of the last opamp is a capacitor, the integrator output voltages must be converted into currents by means of FF capacitors in order to get a frequency independent coefficient (Fig. 3.9). Considering an ideal opamp, the output voltage of the last integrator is then:

$$V_{oL} = -\left[V_{o1}\frac{C_{f1}}{C_L} + V_{o2}\frac{C_{f2}}{C_L} + \ldots + V_{oL-1}\frac{C_{oL-1}}{C_L} + \frac{V_{oL-1}}{sR_L C_L} \right] = -\sum_{i=1}^{L-1} k_i V_{oi} - \frac{A_L}{s} V_{oL-1} \tag{3.20}$$

where C_{fi} are the capacitors in the FF paths, V_{oi} is the output of the i-th integrator and A_L is the coefficient of the last integrator. Hence, all terms in the sum of Eq. (3.20) except the last one implement the frequency-independent FF-coefficients while the last term, obtained with the resistor R_L, realizes the integration coefficient of the last integrator. This architecture provides also a good linearity, as the voltage-to-current conversion is done through passive, linear capacitances. Thanks to its advantages in terms of linearity and low-power consumption, an adder-free solution was chosen for the proposed modulator. The final implementation will make use of resistors instead of capacitors for the signal FF paths, as explained later in this work.

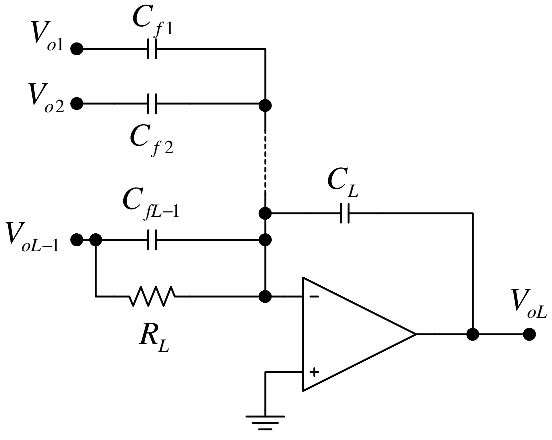
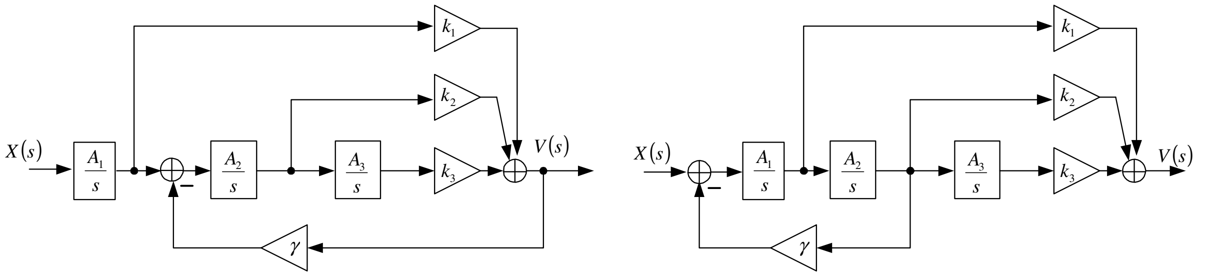


Fig. 3.9. Sum of the FF-paths through feed-forward capacitors

3.5.3. Resonator for zero spreading and architectural modification

In order to improve the modulator resolution we need to introduce complex-conjugate zeros in the NTF, which are located on the unit circle (zero spreading). As previously shown, this results in purely imaginary poles in the CT equivalent loop filter. These poles are generated by means of resonators. Limiting the analysis to a 3rd order modulator the local feedback path required for the resonator can be placed either across the last two integrators (Fig. 3.10a) or across the first two (Fig. 3.10b). At this point it should be noted that the schematic diagrams in Fig. 3.10 are high-level representations of the filter blocks in the *voltage* domain. Therefore, the adder located *after* the last integrator is merely symbolic, as the addition is actually performed in the current domain at its virtual ground node. Hence, in the real circuit the integrator output voltage can only be tapped at the node $V(s)$, i.e. after the adder in Fig. 3.10.



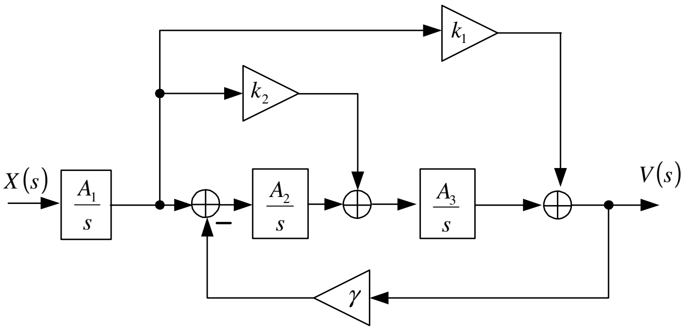
(a) (b)

Fig. 3.10. Filter type a) and b)

The transfer functions of filter of type a) and b) are, respectively:

$$H_a(s) = \frac{A_1}{s} \cdot \frac{k_1 s^2 + A_2 k_2 s + A_2 A_3 k_3}{s^2 + \gamma A_2 k_2 s + \gamma A_2 A_3 k_3} \tag{3.21}$$

$$H_b(s) = \frac{A_1}{s} \cdot \frac{k_1 s^2 + A_2 k_2 s + A_2 A_3 k_3}{s^2 + \gamma A_1 A_2} \tag{3.22}$$



(c)

Fig. 3.11. Filter type c) [Dig10]

Filter of type a) has a damping factor in the denominator because of the non-zero coefficient of the s-term. The reason for this is that the proportional path k_2 starts and ends inside the feedback loop. This topology will be discarded, since it realizes poles which are not purely imaginary, associated with less effective noise suppression. Topology b) enables the generation of purely imaginary poles. On the other hand the feedback path γ, typically realized with a large resistor, directly affects the input-referred thermal noise. Furthermore the large capacitance associated with the resistive feedback path γ loads the virtual ground node of the 1st integrator, affecting its transfer function. Because of its position at the modulator input, the 1st integrator must have a possibly ideal behavior regarding noise, frequency response and linearity. We prefer therefore to put the feedback path across the last two integrators. In order to get an ideal resonator without damping factor an architectural change is needed. The architecture chosen is shown in Fig. 3.11 and has no FF paths which start inside the resonating loop [Dig10]. The FF path k_2 feeds the output of the 1st integrator to the output of the 2nd integrator. The coefficient k_3 was incorporated in the integrator gain A_3.

The transfer function of the 3rd order filter in Fig. 3.11 is:

$$H_c(s) = \frac{A_1}{s}\frac{k_1 s^2 + A_3 k_2 s + A_2 A_3}{s^2 + \gamma A_2 A_3} = \frac{A_1}{s}\frac{k_1 s^2 + A_3 k_2 s + A_2 A_3}{s^2 + \omega_0^2} \tag{3.23}$$

This topology allows the generation of purely imaginary poles and has reduced input noise compared to H_b(s), since the feedback path is moved after the 1st integrator. The value of the filter coefficients, A_i, k_i, γ in (3.23) can be obtained equating them to the CT filter TF obtained with the IIT (3.14):

$$H(s) = \frac{5.61 \cdot 10^8 s^2 + 1.82 \cdot 10^{17} s + 2.91 \cdot 10^{25}}{s\left(s^2 + 3.69 \cdot 10^{15}\right)} \tag{3.24}$$

A linear equation system with 4 equations and 6 unknown is obtained:

$$\begin{aligned} A_1 k_1 &= 5.61 \cdot 10^8 \\ A_1 A_3 k_2 &= 1.82 \cdot 10^{17} \\ A_1 A_2 A_3 &= 2.91 \cdot 10^{25} \\ \gamma A_2 A_3 &= 3.69 \cdot 10^{15} \end{aligned} \tag{3.25}$$

As the system is over-determined, we select the values of the FF coefficients arbitrarily as:

$$k_1 = k_2 = 1 \tag{3.26}$$

With this choice all other unknown A_i and γ can be determined:

$$A_1 = 5.61 \cdot 10^8,\ A_2 = 1.60 \cdot 10^8,\ A_3 = 3.24 \cdot 10^8,\ \gamma = 0.071 \tag{3.27}$$

3.6. Excess Loop Delay compensation

As explained in section 2.8.6, CT modulators suffer from excess loop delay (ELD) which influences the dynamic behavior and the stability of the modulator. In the case of a NRZ DAC with constant delay t_d the rectangular DAC impulse response will start at the time t_d and end at T_s+t_d.

In order to quantify and compensate the effects of ELD the CT modulator with delayed NRZ DAC is transformed back in the DT domain by means of the IIT. Assuming that the coefficients k_i are one, the CT transfer function (3.23) can be simplified:

$$H_1(s) = \frac{A_1}{s}\frac{s^2 + A_3 s + A_2 A_3}{s^2 + \omega_0^2} \tag{3.28}$$

Expanding $H_1(s)$ in partial fractions and transforming the terms taking into account the delayed NRZ DAC waveform, an equivalent DT $H_{NRZ}(z)$ with the same sampled impulse response is obtained [Che02]. For the calculation the reader can refer to Appendix A. The DT equivalent filter of the CT modulator affected by ELD has the form:

$$H_{NRZ}(z,\tau_d)=\frac{N(z,\tau_d)}{z(z-1)\left(z^2-2z\cos\omega_0+1\right)} \tag{3.29}$$

where $N(z, \tau_d)$ is a polynomial in z whose coefficients are function of the normalized delay $\tau_d=t_d/T_s$. Comparing (3.29) with the prototype (3.6) it can be noted that the numerator of the equivalent TF is affected by τ_d: this means that the zeros of the DT equivalent loop filter are shifted because of the delay, which affects the loop stability [Gao97]. On the contrary the *pole* location is the same as in the ideal case apart from the introduction of the term z in the denominator, i.e., a delay of one clock period. This delay arises because the NRZ DAC pulse is partially shifted *after* T_s due to the excess loop delay, as described in Sec. 2.8.6. To fully compensate the effects of ELD, the CT filter coefficients must be adjusted in order to make the transfer function $H_{NRZ}(z)$ identical with the prototype DT filter $H(z)$ (3.6). Since the delayed NRZ DAC ends after T_s, not only coefficient mismatch toward the ideal prototype DT filter results but also the order of the equivalent DT filter is increased [Che02]. Hence a 3rd order CT filter with NRZ DAC and excess loop delay leads to a 4th order DT equivalent filter (3.29).

Although ELD-caused coefficient mismatch can be simply cancelled by correcting the CT filter coefficients, the elimination of the order increase of the DT equivalent filter requires an additional half-return-to-zero (HRZ) DAC for the CT modulator [Ben97]. An HRZ-DAC is characterized by a pulse form starting at $T_s/2$ and ending at T_s. It is advantageous to insert the additional path at the back-end of the filter, where the large gain of the preceding integrators relaxes the requirements on the DAC linearity. Some solutions exist, adding the DAC current directly at the quantizer input ([Red08], [Ben97]), yet this would require an active adder after the filter, increasing the power consumption. An addition in the current domain was thus preferred, feeding the DAC current to the virtual ground node of the last integrator. A similar approach can be found in [Mit06] with the difference, that here the compensation is obtained by moving the DAC from the quantizer input to the input of the last integrator by digitally differentiating the output data flow of the modulator. This is not completely correct: since the last integrator is located in a resonator loop, the TF from the integrator input to the resonator output deviates from a pure integration, this causing a slight error. The approach of this work was the analytical calculation of all coefficients of the modified modulator in Fig. 3.12 in order to make its sampled impulse response the same as that of the prototype DT modulator.

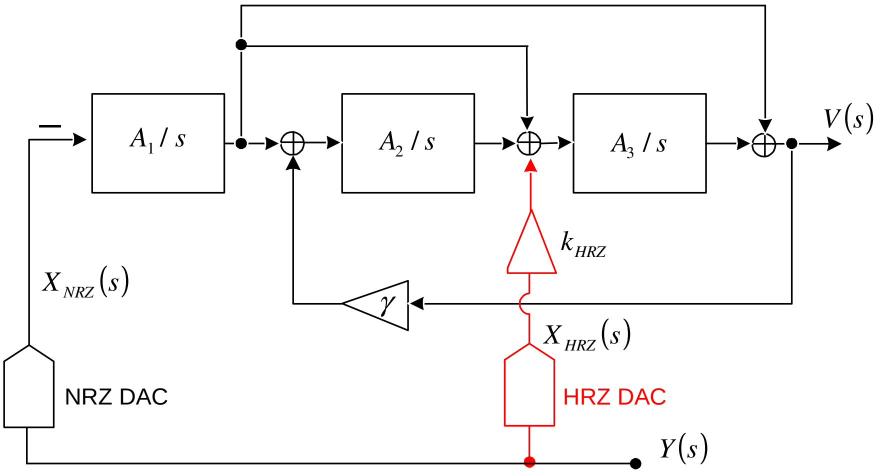


Fig. 3.12. Additional HRZ DAC for ELD compensation (in red)

A description of the symbolic calculation of the coefficients, performed with the aid of the software Maple®, can be found in Appendix A. A new set of coefficients A_i and γ, different from those in (3.27), are found, which together with the additional HRZ DAC fully compensate for the ELD.

To simplify the mathematical calculation both DAC currents are represented by their equivalent voltages. Using the superposition principle the impulse response of the system in Fig. 3.12 can be calculated by superposing the impulse responses of the filter at the node $V(s)$ for each DAC pulse. The transfer function $H_{NRZ}(z,\tau_d)$ of the DT equivalent filter for the system composed by the main NRZ DAC and the loop filter is given in Appendix A (Eq. A.14).

Concerning the auxiliary HRZ DAC (Fig. 3.12), the CT filter transfer function to be considered is:

$$H_{HRZ}(s)=\frac{V(s)}{X_{HRZ}(s)}=\frac{k_{HRZ}A_3 s}{s^2+\omega_0^2} \tag{3.30}$$

where k_{HRZ} is the gain factor of the auxiliary HRZ DAC. Decomposing $H_{HRZ}(s)$ in partial fractions the equivalent discrete time filter is obtained with the IIT. The calculation is explained in Appendix A. Following DT transfer function is obtained:

$$H_{HRZ}(z,\tau_d)=\frac{k_{HRZ}A_3}{\omega_0}\,\frac{\sin\left[\omega_0\left(\frac{1}{2}-\tau_d\right)\right]z^2-\left\{\sin[\omega_0(1-\tau_d)]-\sin\left[\omega_0\left(\frac{1}{2}+\tau_d\right)\right]\right\}z-\sin(\omega_o\tau_d)}{z\left(z^2-2z\cos\omega_0+1\right)} \tag{3.31}$$

Hence, the TF of the equivalent DT filter for the CT modulator affected by ELD with both DAC (Fig. 3.12) is:

$$H_d(z,\tau_d)=H_{NRZ}(z,\tau_d)+H_{HRZ}(z,\tau_d)=\frac{N_H(z,\tau_d)}{z\left(z^2-2z\cos\omega_0+1\right)} \tag{3.32}$$

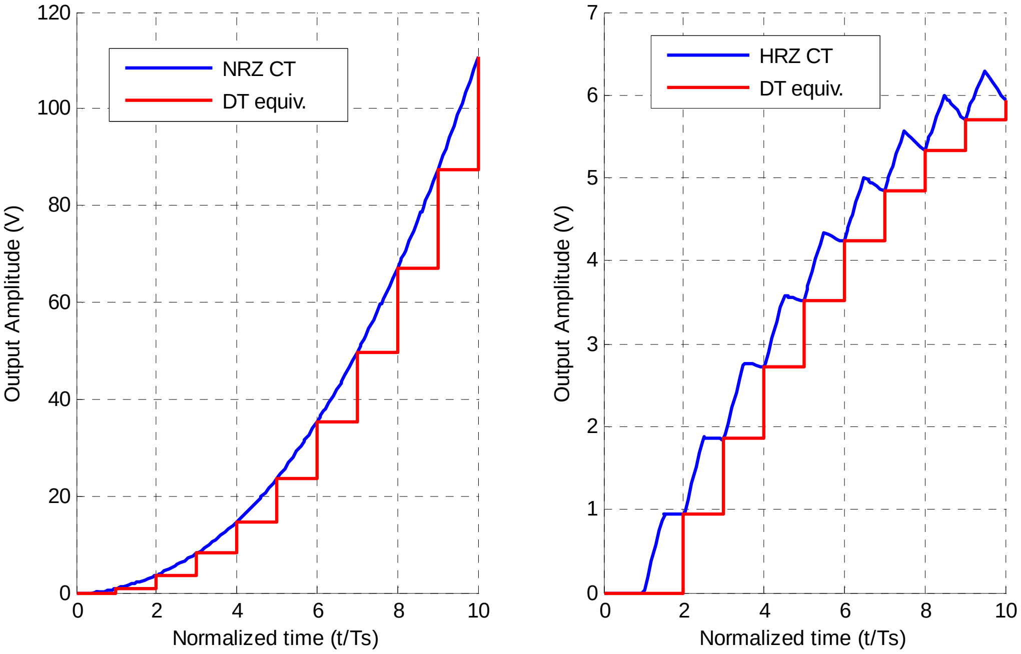


Fig. 3.13. Left: impulse response of the delayed NRZ DAC+filter (blue) and DT equivalent (red). Right: impulse response of the delayed HRZ DAC+filter (blue) and DT equivalent (red)

The ELD is completely compensated if the coefficients are chosen in order to make (3.32) identical to the prototype DT filter (3.6). Since the denominators of both TF are the same except for a factor z, both TF are identical if.

$$\frac{\text{num}\{H_d(z,\tau_d)\}}{z} = \frac{N_H(z,\tau_d)}{z} \equiv \text{num}\{H(z)\} \tag{3.33}$$

(3.33) was solved numerically for a given τ_d with the aid of the symbolic software Maple®. A fixed τ_d=0.5 was chosen, that is, an excess loop delay of half a clock period is assumed. This can be easily realized by latching the quantizer output with a constant delay of $T_s/2$. Equating the coefficients of N_H with the polynomial z·num{$H(z)$} results in a linear system of 4 equations in 4 unknown. A 5th equation fixes the filter resonating frequency:

$$\gamma A_2 A_3 = \omega_0^2 \tag{3.34}$$

Following results were obtained:

A_1	A_2	A_3	γ	k_1	k_2	k_{HRZ}
3.73·f_s	0.33·f_s	0.36·f_s	0.189	1	1	9.37

Tab 3.4. Coefficients for compensation of an ELD $t_d=T_s/2$

3.7. Coefficient scaling

The coefficient set in Tab. 3.4 fully compensates for ELD. Nevertheless the 1st integrator coefficient A_1 is one order of magnitude larger than A_2 and A_3. Large integrator gains are associated with saturation of the integrator output; hence distortion term and clipping are unavoidable in a transistor level realization. Furthermore the coefficient of the HRZ DAC is nearly 10 times larger than that of the main DAC (k_{NRZ}=1), meaning that a large current must be provided by the secondary DAC. To cope with these issues coefficient scaling was accomplished. The scaling does not alter the transfer function of the circuit: it is performed in such a way that consecutive blocks are respectively multiplied and divided by the same scalar, keeping the product of the both TF constant.

The scaled filter is shown in Fig. 3.14, following coefficient scaling was performed:

$$A_1^* = \frac{A_1}{5} \quad A_2^* = \frac{5}{4}A_2 \quad A_3^* = 4A_3 \quad \gamma^* = \frac{\gamma}{5} \quad k_1^* = 5k_1 \quad k_2^* = \frac{5}{4}k_2 \quad k_{HRZ}^* = \frac{k_{HRZ}}{4} \tag{3.35}$$

The new obtained values are indicated in Tab. 3.5.

A_1^*	A_2^*	A_3^*	γ^*	k_1^*	k_2^*	k_{HRZ}^*
0.746·f_s	0.418·f_s	1.456·f_s	0.0378	5	5/4	2.342

Tab 3.5. Scaled coefficients for compensation of an ELD $t_d=T_s/2$

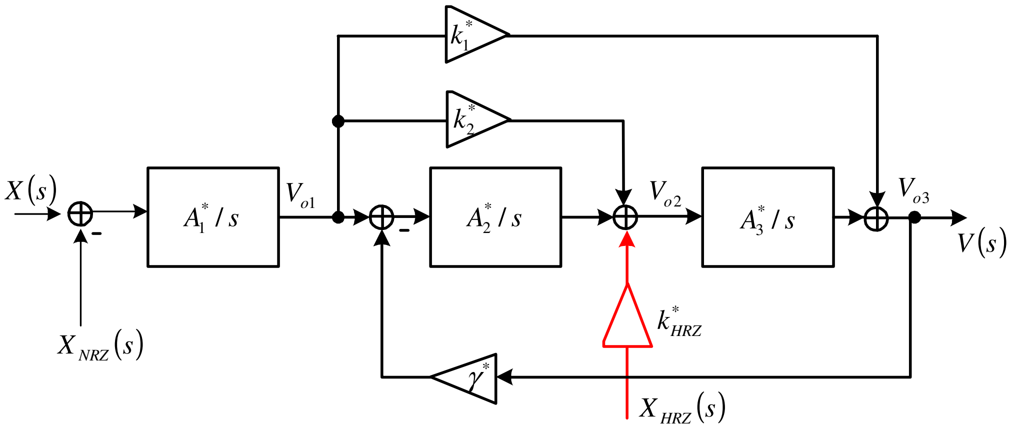


Fig. 3.14. Modulator filter with scaled coefficients for compensation of an ELD t_d=T_s/2 (conceptual drawing)

3.8. Circuit implementation

This section describes the implementation of the loop filter, based on the conceptual drawing in Fig. 3.14, by means of following electrical components: resistors, capacitors and operational amplifiers (opamps). The objective is the realization of a circuit, whose transfer function is identical with that of the conceptual drawing. The single-ended circuit used to realize the loop filter is depicted in Fig. 3.15. It should be noted, that while the conceptual drawing in Fig. 3.14 shows the relation between nodes, which are exclusively in the voltage domain, the real circuit in Fig. 3.15 is based on successive transformations from the voltage to the current domain (V-I) and viceversa (I-V). The first occur from the modulator input or the low-ohmic opamp output or the DAC inputs to the virtual ground nodes of the integrators. The latter occur from the virtual ground nodes to the integrator outputs by means of the integration capacitors.

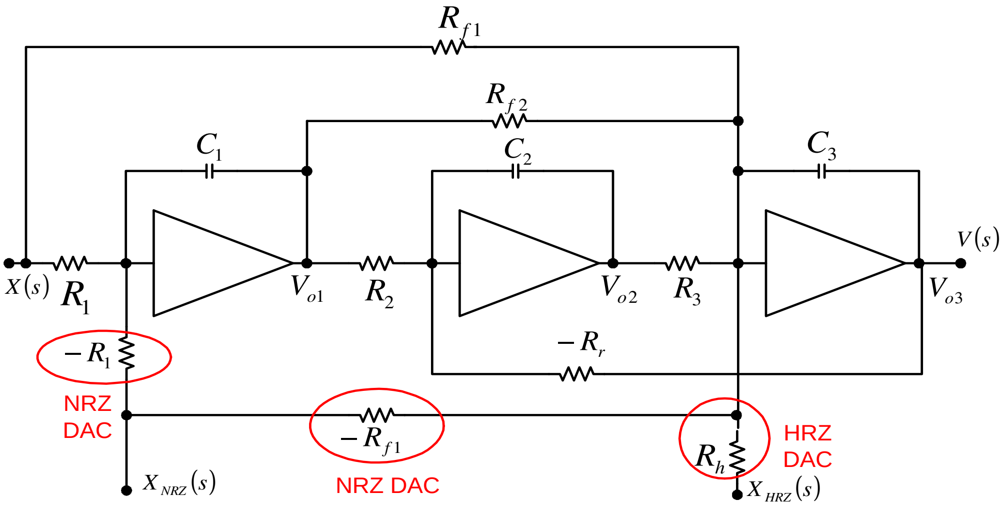


Fig. 3.15. Single-ended schema of the circuit implementation of the loop filter

Assuming at this point all opamps as ideal (i.e. infinite gain and bandwidth), the dimensioning of the passive components (resistors and capacitors) is done by comparing the transfer functions of all signal paths in the conceptual drawing with those of the circuit in Fig. 3.15.

1. **Integrator sizing.** At first the three integrator blocks are realized with an active *RC* topology, leading to following equivalences:

$$\frac{1}{R_1C_1}=A_1^* \qquad \frac{1}{R_2C_2}=A_2^* \qquad \frac{1}{R_3C_3}=A_3^* \tag{3.36}$$

2. **Local feedback path.** Concerning the local feedback path of the resonator γ^*, this multiplies V_{o3}, the output voltage of the 3rd integrator, by γ^* and feeds it back to the input of the 2nd integrator. This in turn integrates the voltage $\gamma^* V_{o3}$ providing:

$$V_{o2}' = -\gamma^* V_{o3}\frac{A_2^*}{s} \tag{3.37}$$

The voltage V_{o2}' in (3.37) is the contribution of the feedback path to the voltage at the output of the 2nd integrator. By looking at the equivalent circuit in Fig. 3.15, the contribution of the feedback path, implemented with the negative resistor $-R_r$ is:

$$V_{o2}' = -\frac{V_{o3}}{R_r}\cdot\frac{1}{C_2 s} \tag{3.38}$$

where the result is obtained[3] by integrating the current $-V_{o3}/R_r$ by means of the integration capacitance C_2. By equating (3.37) with (3.38) we get:

$$-\gamma^* V_{o3}\frac{A_2^*}{s} = -\frac{V_{o3}}{R_r}\cdot\frac{1}{C_2 s} \tag{3.39}$$

that is:

$$R_r = \frac{1}{\gamma^* A_2^* C_2} = \frac{R_2C_2}{\gamma^* C_2} = \frac{R_2}{\gamma^*} \tag{3.40}$$

where the value $A_2^*=1/(R_2C_2)$ as found in (3.36) was inserted.

3. **NRZ DAC and HRZ DAC**. Both DAC are modeled as voltage DAC in the conceptual drawing. To simplify the treatment they are represented as resistors driven by voltage sources in the schematic of Fig. 3.15. In the real implementation they are replaced by fast switched current sources. Nevertheless the ratio between the driving voltage of the DAC and the value of the resistors used to represent the DAC contains the information about the current to be provided by the DAC. Concerning the main NRZ DAC at very input of the modulator, as the feedback coefficient is one, the same current as the that generated by the input signal must be provided. Furthermore, a sign variation is needed, as the feedback must be negative. Hence, a negative resistor $-R_1$ is used to model the main DAC. Concering the auxiliary HRZ DAC for ELD compensation, this is depicted in Fig. 3.14 as a feedback path with gain factor k_{HRZ}^*. The contribution of the feedback path for ELD to the output voltage of the 3rd integrator is then:

$$V_{o3}' = X_{HRZ}(s)\cdot k_{HRZ}^*(s)\cdot\frac{A_3^*}{s} \tag{3.41}$$

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[3] The negative resistor is implemented in the final fully-differential circuit by simply cross-coupling the two differential outputs of the 3rd integrator.

while from the circuit in Fig. 3.15 following is obtained:

$$V_{o3}^{'} = \frac{X_{HRZ}(s)}{R_h} \cdot \frac{1}{C_3 s} \tag{3.42}$$

Equating both equations we can find out the value of R_h:

$$X_{HRZ}(s) \cdot k_{HRZ}^{*}(s) \cdot \frac{A_3^{*}}{s} = \frac{X_{HRZ}(s)}{R_h} \cdot \frac{1}{C_3 s} \tag{3.43}$$

that is:

$$R_h = \frac{1}{C_3 k_{HRZ}^{*} A_3^{*}} = \frac{R_3}{k_{HRZ}^{*}} \tag{3.44}$$

where the last term is obtained by inserting $A_3^{*}=1/(R_3C_3s)$ as in (3.36).

4. **Feed-forward paths.** The feed-forward paths k_1^{*} and k_2^{*} can be realized either with capacitors or with resistors**. The latter solution is the best choice for low-voltage, low-power applications.** The reason for this is that, since no Cascode structures are allowed in low-voltage circuits, all opamps are implemented as two-stage, Miller compensated amplifiers. This topology, when associated with short channel output transistors, has a relatively low R_{out}. Hence, the resistive loading of the opamps because of the resistive FF-paths causes only a negligible DC-gain drop. On the contrary, capacitive FF-paths would load the preceding opamps, reducing the bandwidth and/or increasing the current required in their output stage. To understand this, we can briefly analyze the AC behavior of Miller-compensated two-stage opamps. The two dominant poles, located at the output of the 1st and 2nd stage respectively, are split away by the compensation capacitance. The capacitive load due to the capacitive FF-paths tends to shift the output pole of the 2nd stage, which is at high frequency because of the Miller capacitor, toward lower frequencies, hence reducing the stability phase margin. This can be counteracted by increasing the transconductance of the output stage, i.e. the power consumption. This is highly undesirable in low-power applications. On the other hand the resistive FF-paths increase the circuit noise of the modulator. However, their contribution is negligible since they feed their noise current in the virtual ground of the 3rd integrator. From this node the noise currents flow into C_3 where they are integrated. When referring the output noise voltage of the 3rd integrator to the modulator input, this must be divided by the gain of the preceding integrators. Hence, the input referred noise of the FF resistors in very small. In addition the FF resistors values are kept small to further reduce their thermal noise. In [Mit06] one resistive FF-path in the CT loop filter is also implemented with resistors but no explanation of this choice was published.

The contribution of the FF-paths k_1^{*} and k_2^{*} in the conceptual scheme (Fig. 3.14) to the output voltage of the 3rd integrator is:

$$V_{o3}^{''} = [X(s) - X_{NRZ}(s)]\frac{A_1^{*}}{s}\left(k_1^{*} + k_2^{*}\frac{A_3^{*}}{s}\right) = [X(s) - X_{NRZ}(s)] \cdot \left(\frac{k_1^{*}A_1^{*}}{s} + k_2^{*}\frac{A_3^{*}A_1^{*}}{s^2}\right) \tag{3.45}$$

The two FF paths k_1^* and k_2^* are implemented with the resistors R_{f1}, $-R_{f1}$ and R_{f2}. Their contribution to the output voltage of the 3rd integrator of the circuit implementation (Fig. 3.15) is:

$$V_{o3}^{''} = X(s)\cdot\left(\frac{1}{R_{f1}C_3 s}+\frac{1}{R_1C_1 s}\cdot\frac{1}{R_{f2}C_3 s}\right)+X_{NRZ}(s)\cdot\left(-\frac{1}{R_{f1}C_3 s}-\frac{1}{R_1C_1 s}\cdot\frac{1}{R_{f2}C_3 s}\right) \tag{3.46}$$

Collecting (3.46) with respect to the common terms we obtain:

$$V_{o3}^{''} = \left[X(s)-X_{NRZ}(s)\right]\cdot\left(\frac{1}{R_{f1}C_3 s}+\frac{1}{R_1C_1 s}\cdot\frac{1}{R_{f2}C_3 s}\right) \tag{3.47}$$

Equating (3.45) and (3.47), i.e. equating the coefficients of the 1/s and $1/s^2$ terms, following is obtained:

$$k_1^* A_1^* = \frac{1}{R_{f1}C_3} \qquad \text{and} \qquad k_2^* A_3^* A_1^* = \frac{1}{R_1C_1R_{f2}C_3} \tag{3.48}$$

Replacing the coefficients A_1^* and A_3^*, which are already known from (3.36), we get:

$$\frac{k_1^*}{R_1C_1} = \frac{1}{R_{f1}C_3} \Rightarrow R_{f1} = \frac{R_1C_1}{C_3}k_1^* \quad \text{and} \quad \frac{k_2^*}{R_3C_3R_1C_1} = \frac{1}{R_1C_1R_{f2}C_3} \Rightarrow R_{f2} = \frac{R_3}{k_2^*} \tag{3.49}$$

The feed-forward resistor $-R_{f1}$ provides the signal $X_{NRZ}(s)$ to the virtual ground of the 3rd integrator. In the real implementation it should be replaced by a third current DAC (see Sect. 3.9).

3.8.1. Thermal noise considerations

As the integrator coefficients specify only the R_iC_i products, i.e. the integrator time constants, one additional degree of freedom is given in the choice of the resistor and capacitor value. These values are selected according to two criteria: the maximum resistor value is limited by thermal noise, the minimum capacitance by the parasitic capacitances which limit its controllability. In particular the resistor R_1 is placed directly at the input of the modulator and contributes in large part to the overall noise budget. Reminding the calculation in Chap. 2, Sect. 2.8.4.1, the input-referred *rms* noise voltage of R_1 in the signal band f_B is:

$$\sqrt{\overline{v_{nR1}^2}} = \sqrt{2\cdot 4kTR_1 f_B} \tag{3.50}$$

where the factor two accounts for a differential implementation. For a signal band of 12.5MHz both input resistors R_1 produce an *rms* noise voltage of 35.2µV if their value is 3kΩ. To estimate the limits on the achievable SNR some assumptions have to be made on the power of the input signal. Assuming a supply voltage of 1.2V the input signal will have a DC level of $V_{DD}/2$=0.6V. Even if an input amplitude of 0.6V is theoretically allowed ($V_{FS}=V_{DD}/2$), this is not possible in practice. The reason for this is twofold: the input signal of the modulator is provided by the output stage of a voltage buffer, whose transistors must be operated in the saturation region; furthermore, the input signal of the *quantizer* (after the loop filter) contains the input signal as well as shaped quantization noise. The sum of both components can easily saturate the output of the last integrator of the loop filter. For this reason a full-scale signal amplitude V_{FS}=0.325V was chosen which gives a margin of 0.275V. The single-ended input signal at both input terminals as well as the differential input signal are plotted in Fig. 3.16.

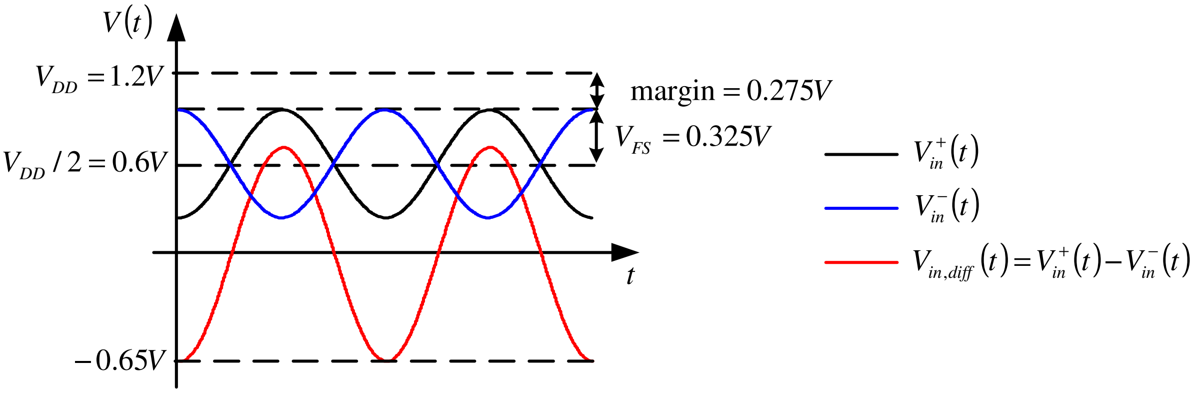

Fig. 3.16. Graphical representation of the single-ended and differential input signals

Assuming the differential input signal is a sine wave with amplitude $2V_{FS}$, the squared *rms* value of the signal is:

$$P_s=\frac{(2V_{FS})^2}{2}=2V_{FS}^2 \tag{3.51}$$

the SNR with the only thermal noise of R_1 will be then:

$$SNR_{th,R1}=10\log\frac{P_s}{\overline{v_{nR1}^2}} \tag{3.52}$$

For the given bandwidth of 12.5 MHz and an R_1 value of 3 kΩ an SNR of 82.3 dB is obtained, corresponding to an ENOB of 13.4 bits. The value of C_1 is then fixed since the reciprocal of the R_1C_1 product is given by the integrator gain A_1^*. The thermal noise of the main DAC and of the 1st integrator will be examined in the next chapter. The thermal noise of the other resistors in the circuit is not problematic, since their noise contribution is suppressed by the large gain of the preceding amplifiers. Hence, the resistors R_2 and R_3 are dimensioned as large as possible, in order to reduce the loading of the preceding stage and to keep the integration capacitors C_2 and C_3 small. A lower limit of 150 fF for each capacitor was selected in order to make them much larger than the parasitic capacitances.
The selected values of the passive components of the CT loop filter are indicated in Tab. 3.6.

R_1	C_1	R_2	C_2	R_3	C_3	R_{f1}	R_{f2}	R_r	R_h[4]
3 kΩ	1.12 pF	20 kΩ	300 fF	9.4 kΩ	183 fF	3.7 kΩ	7.5 kΩ	529 kΩ	4.01 kΩ

Tab 3.6. Values of the passive components of the CT loop filter

The fully differential circuit implementation of the loop filter is depicted in Fig. 3.17, feed-forward paths are in blue, feedback paths in red. The six resistors circled in the figure are actually implemented with three differential current steering DAC.

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[4] This resistor and the resistors $-R_1$ and $-R_{f1}$ are actually implemented with switched current sources.

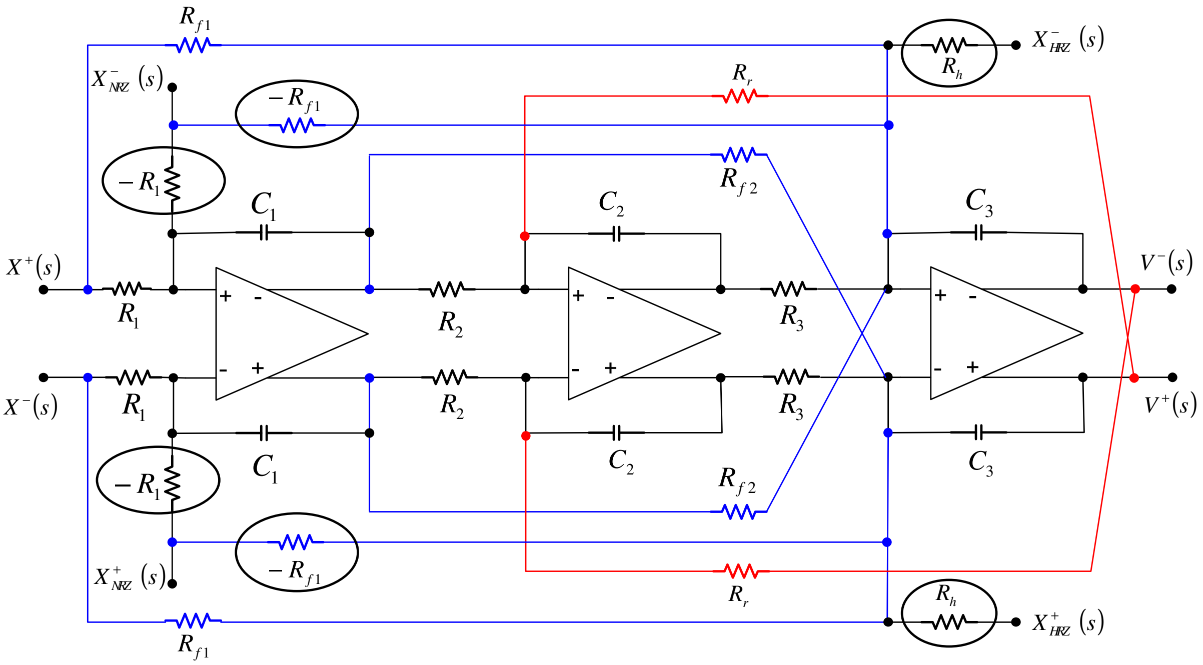


Fig. 3.17. Loop filter: fully differential circuit implementation. FF paths are depicted in blue, FB paths in red. The circled resistors are actually implemented as current steering differential DAC.

3.9. DAC current dimensioning, DAC merging

As already mentioned, the DAC are realized by means of switched current sources. In order to track the input signal, the main DAC must be able to provide a maximum current:

$$I_{NRZ,\max} = \pm\frac{V_{FS}}{R_1} = \pm 108.33\mu A \tag{3.53}$$

where V_{FS}=0.325V is the full scale amplitude of the input signal. Similarly, the HRZ DAC must be capable to provide the current:

$$I_{HRZ,\max} = \mp\frac{V_{FS}}{R_h} = \mp 81.04\mu A \tag{3.54}$$

Finally, an additional NRZ DAC is required to realize the FF-path indicated with the negative resistor $-R_{f1}$ in Fig. 3.17. The current fed by the second NRZ DAC is:

$$I_{NRZ2,\max} = \pm\frac{V_{FS}}{R_{f1}} = \pm 88.56\mu A \tag{3.55}$$

As visible in Fig. 3.17 the current generated by the HRZ DAC (resistor R_h) and that of the NRZ DAC realizing the FF-path k_1 (resistor $-R_{f1}$) are injected in the same virtual ground node of the 3rd integrator with opposite polarities. In addition, both currents have nearly the same absolute value (Eq. (3.54) and (3.55)). We can express the sum of both DAC currents, as plotted in Fig. 3.18, as the sum of two components:

$$i_{NRZ2}(t) + i_{HRZ}(t) = i_{RZ}(t) + i_{\varepsilon}(t) \tag{3.56}$$

The first component $i_{RZ}(t)$ is a RZ data-depending current (Fig. 3.18d) with the same amplitude of $i_{NRZ2}(t)$. Its maximum value amounts to 88.56µA. The second part is a relatively small HRZ data-depending current (Fig. 3.18e) with maximum value 7.52µA. Since these currents are injected in the virtual ground of the last integrator, a 2nd order noise shaping is obtained referring the signals at this node to the input (there are two integrators between the input and this node). The error introduced by replacing the latter current with a zero value is therefore negligible as confirmed by simulation results. For a coarse estimation, considering the current error as a DC current, its input referred value is:

$$i_{\varepsilon,IN} = \frac{i_\varepsilon}{A_{DC1}A_{DC2}} \tag{3.57}$$

where A_{DC1} and A_{DC2} are the DC gain of the 1st and 2nd integrator respectively. Assuming a DC gain of 200 for each integrator an input-referred DC amplitude of merely 0.18 nA is obtained. The full-scale input signal current is:

$$i_{FS,IN} = \frac{V_{FS}}{R_1} = \frac{0.325V}{3k\Omega} = 108.33\mu A \tag{3.58}$$

The latter is $6\cdot 10^5$ times larger then the error, hence the error introduced is far smaller than an LSB by 11 bit resolution. Hence, the combination of the HRZ DAC and the second NRZ DAC realizing the k_1 FF-path is replaced by a single RZ DAC, saving power and circuit complexity.

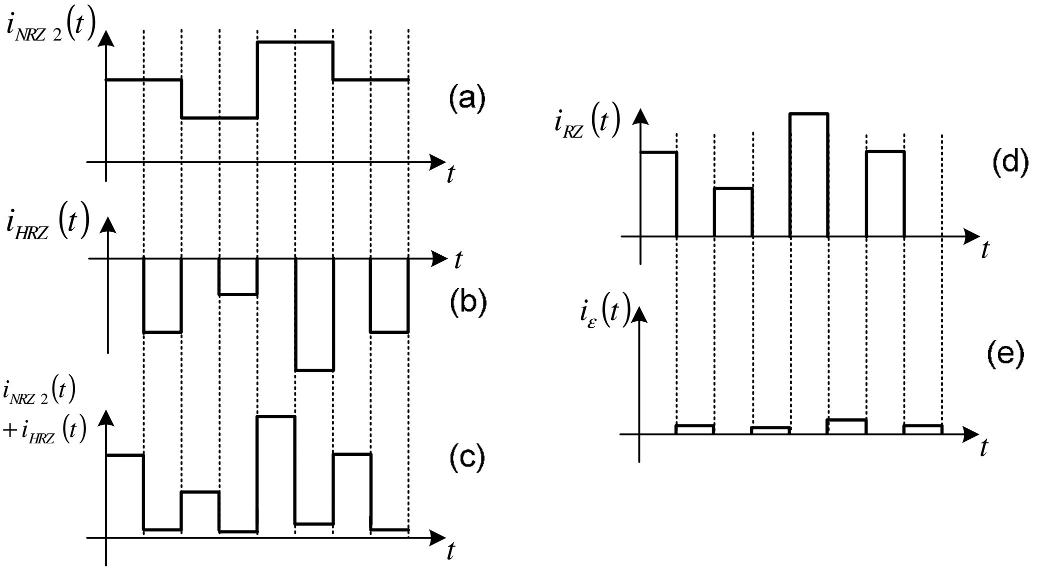


Fig. 3.18. a) NRZ current waveform at the input of the 3rd integrator; b) HRZ current waveform for ELD compensation; c) sum of both currents; d) RZ component of the sum; e) HRZ component of the sum

3.10. High-level simulations

3.10.1. Finite opamp gain

The fully differential CT modulator was simulated at high level with the software suite Cadence® to confirm the architectural approach. The simulated filter topology is that of Fig.

3.17 with the difference that the DAC resistors are implemented with ideal switched current sources. Moreover, all passive elements are assumed to be ideal. The three filter opamps are modeled at this level as differential voltage controlled voltage sources, with frequency independent gain in order to simulate SNR degradation due to non-infinite DC-gain (Fig. 3.19). The quantizer is modeled with a bank of 13 delay-free ideal comparators, that is, only a 14-level quantizer is used instead of a 4-bit, 16 level one. This was done to further save power consumption as simulations show that the first and the last comparator were never used. In the real quantizer implementation a signal-depending delay is unavoidable (s. Chapter 4) which has similar implications as jitter noise. To prevent this, a latch is placed after the quantizer, fixing the delay between the quantizer clock and the time at which its output changes to $T_s/2$.

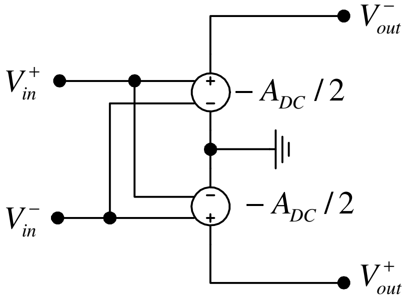


Fig. 3.19. Simple model of a fully differential opamp with DC-gain A_{DC}

The input signal used for this simulation is a sine with a frequency of 1.5625 MHz, its single ended amplitude is V_A=250mV corresponding to $0.77 \cdot V_{FS}$. The SQNR curve as function of the opamp DC gain is plotted in Fig. 3.20. It is deducible that the proposed architecture is adequate for modern sub-μm technology, thanks to its good performance by low gain opamp. The modulator gets eventually unstable for a gain smaller than 30 dB. For the 0.13 μm CMOS technology used an intrinsic gain of about 15 per stage was simulated. Hence, a two-stage opamp can achieve a DC-gain of approximately 45-50 dB, which does not significantly affect the obtainable resolution.

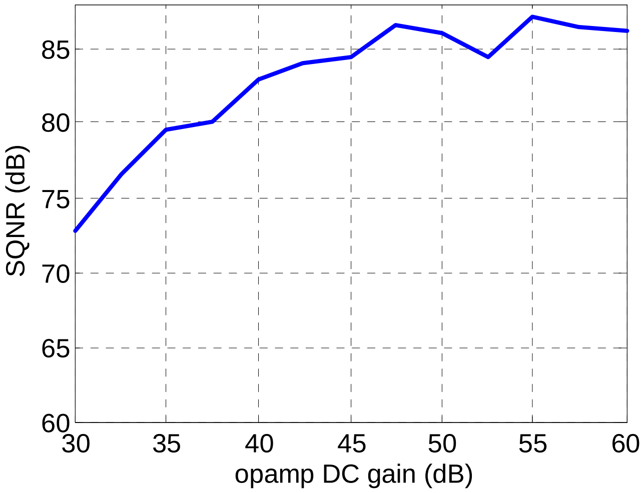


Fig. 3.20. SQNR as function of the opamp DC-gain. f_{in}=1.5625 MHz, V_A=0.77 V_{FS}

The histograms in Fig. 3.21 plot the distribution of the amplitude of the integrator outputs normalized to the full-scale voltage V_{FS}=0.325 V. The gain of the 1st integrator was sized with the objective of keeping the output signal small, i.e. inside an interval $\pm 0.2V_{FS}$. This allows a very good linearity of the 1st integrator, as the output transistors are never driven close to the triode region. On the other hand, large amplitudes are allowed at the output of the 2nd and 3rd integrators, as their non-linearities are respectively 1st and 2nd order shaped when referred to the modulator input. The high-level simulation shows that these vary in an interval $\pm 1.1V_{FS}$.

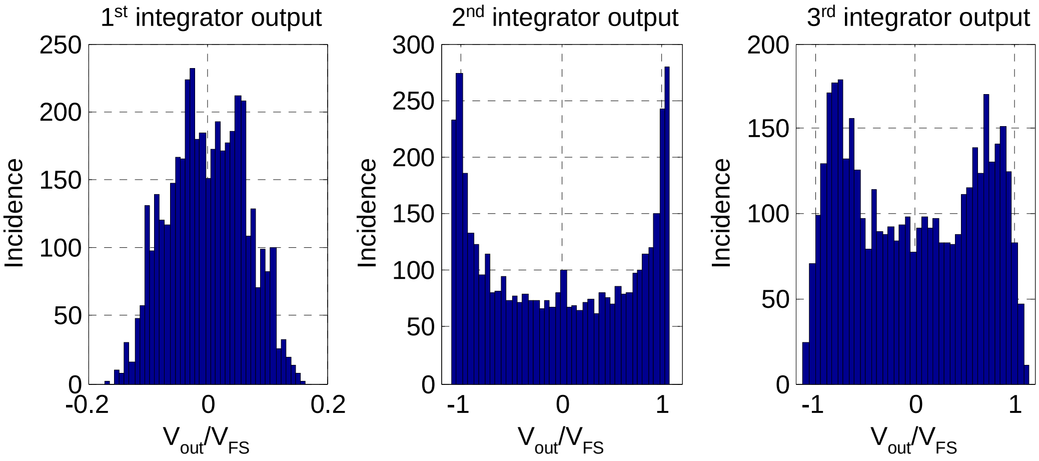


Fig. 3.21. Distribution of the integrator outputs, f_{in}=1.5625 MHz, V_A=0.77 V_{FS}

3.10.2. DAC jitter

The CT modulator with the filter described in the previous section including the additional path for excess loop delay compensation was simulated at high-level with Simulink® to define the maximum tolerable jitter noise. The jitter is assumed to be white with Gaussian distribution [Oli98] and is modeled with a variable delay element, whose value is defined at each clock period by a random number generator (Fig. 3.22), resulting into a data flow from the quantizer output with random varying rising and falling edges. The random number has a normal distribution with mean value $T_s/2$, which models the delay introduced by the latched quantizer and standard deviation $\sigma(\Delta t)$, which models the jitter noise. This kind of simulation is very time consuming, as the maximum simulation step must be of the same order of magnitude of the jitter standard deviation.

A real-life jitter spectrum is not white since it is related to the phase noise of the PLL generating the clock signal [Dad02]. This is usually dominated by the VCO phase noise and depends on the PLL transfer function. As no information was provided about the PLL, the spectral density of the jitter was assumed to be white. Nevertheless this assumption gives a perception of the jitter sensitivity of the proposed modulator.

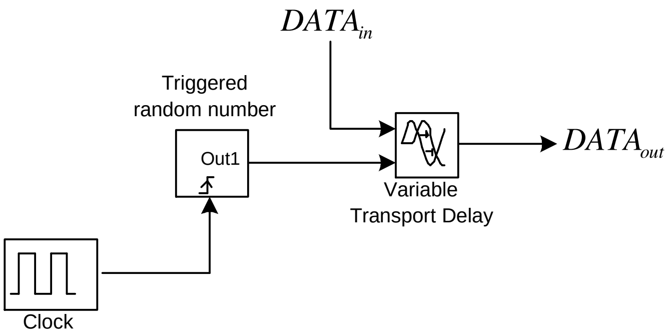


Fig. 3.22. Block schema of the high-level jitter generator

The simulated SNR of the modulator with the jitter generator in Fig. 3.22 is plotted in red in Fig. 3.23 against the jitter standard deviation. The simulations were performed with a sine input signal with half full-scale amplitude and a frequency of 1.5625 MHz.

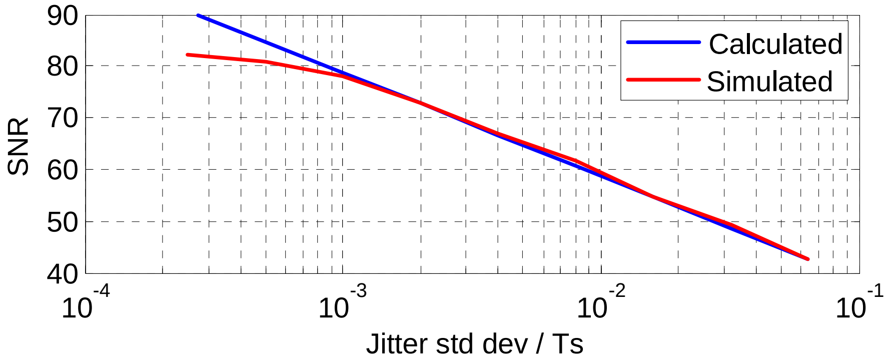


Fig. 3.23. Calculated (blue) and simulated (red) SNR of the modulator against normalized jitter standard deviation

To evaluate the correctness of the results, these were compared with the analytical formula (2.123), reported here for convenience:

$$SNR_j = 10\log\frac{P_S}{P_j} = 10\log\frac{V_{IN}^2/\left(2R^2\right)}{\dfrac{\sigma^2(\Delta t)\cdot\sigma^2(\Delta I_{DAC})}{OSR\cdot T_s^2}} \tag{3.59}$$

Since the main DAC is modeled in Simulink® as a voltage DAC, (3.59) is rewritten as ratio of squared voltages:

$$SNR_j = 10\log\frac{V_{IN}^2/2}{\dfrac{\sigma^2(\Delta t)\sigma^2(\Delta V_{DAC})}{OSR\cdot T_s^2}}\cdot \tag{3.60}$$

ΔV_{DAC} is a discrete-time, discrete-amplitude signal which represents the variation of the DAC output at every clock cycle, expressed in volt. It is a measure of the DAC signal activity. A qualitative plot of a generic multibit sigma-delta modulated signal $y[n]$ together with the corresponding $\Delta V_{DAC}[n]$ is depicted in Fig. 3.24.

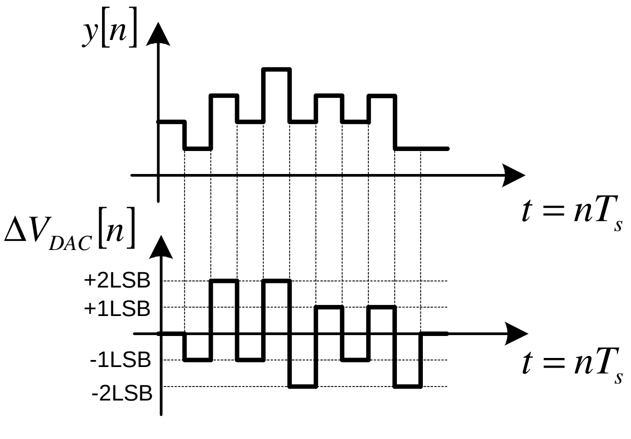


Fig. 3.24. Multibit sigma-delta modulated signal (above) and signal ΔV_{DAC} (below)

In order to characterize statistically the DAC activity the jitter-free CT modulator presented before was simulated with a sine input signal of $0.5V_{FS}$ with a frequency of 1.5625 MHz.

The signal $\Delta V_{DAC}[n]$ was obtained by calculating the finite difference:

$$\Delta V_{DAC}[n] = y[n] - y[n-1] \tag{3.61}$$

where $y[n]$ is the output of the simulated modulator.

Fig. 3.25 depicts the first 1000 simulated samples of $\Delta V_{DAC}[n]$, normalized to the unit step height $\Delta V_{LSB.}$ The variation signal is limited to a maximum of ±3 steps and has a variance $\sigma^2(\Delta V_{DAC})=1.53(\Delta V_{LSB})^2$.

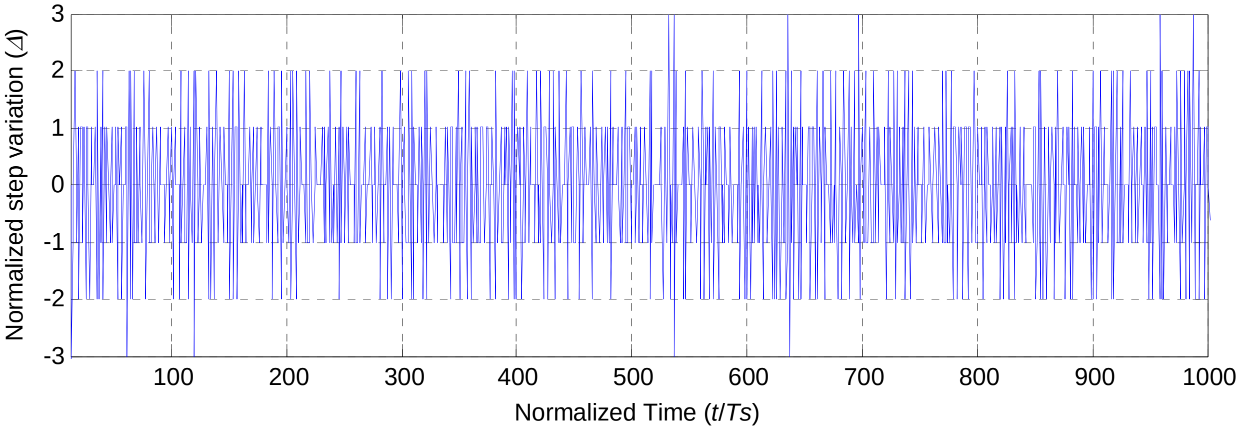


Fig. 3.25. Normalized DAC variations as function of time (simulated)

The SNR values according to eq. (3.60) are plotted in blue in Fig. 3.23. Both simulated and expected curves show good accordance. The discrepancy at very low jitter is due to the rounding error caused by the discrete simulation step. Reducing this step allows the simulation of very low jitter at costs of longer simulation time. Both the analytical formula and the simulation results show that for a jitter standard deviation of $2\cdot10^{-3}T_s$, i.e. 5ps, a SNR of 72.7 dB, namely 11.8 bits, is achieved, which fulfill the modulator specifications.

Chapter 4

Low-power high-speed CT ΣΔ modulator: integrated circuit design

This chapter deals with the design of the integrated circuit realizing the modulator proposed in the previous chapter. After an introduction about the technology used it focuses on the implementation of the main blocks of the modulator: the opamp of the loop filter, the quantizer, the two DAC and the clock generator.

4.1. Used technology and supply voltage

The integrated circuit in this work is based on a UMC CMOS 0.13 μm technology [UMC]. This technology features eight copper metal layers and one polysilicon layer. Nmos and pmos transistors are provided with three different options: high-speed, standard performance and low-leakage. All transistors used in the proposed modulator are of the high-speed type because of their low threshold voltage, which eases low-voltage circuit design. Metal-metal capacitors (MIM) are available with a capacitance density of 1ff/μm^2 as well as high ohmic resistors. All modulator parts are supplied with an operating voltage of 1.2V. The main technology parameters are synthesized in the table below.

Technology	**CMOS 0.13 μm**		
Transistor options	high-speed	std performance	low-leakage
Threshold voltage (V_{Tn}/V_{Tp})	0.38 / -0.33	0.47/-0.42	0.58/-0.52
Layers	1P 8M copper		
High ohmic resistor (Ω/square)	984		
Metal-metal capacitor (fF/μm^2)	1		
Operating voltage	1.2 / 3.3		
Metal thickness M1/M2/M3/M4/M5/M6/M7/M8	0.32 / 0.4 / 0.4 / 0.4 / 0.4 / 0.4 / 0.8 / 0.8		

Tab 4.1. Main technological parameters

4.2. Loop filter operational amplifiers

The following section describes the design steps for the circuit implementation of the operational amplifiers used in the loop filter.

Because of the low supply voltage available of only 1.2V transistor stacking such as in Cascode amplifiers is not allowed, as this would drive the transistors in the triode region.

Folded Cascode should also be avoided when dealing with low V_{DD}, since at least four transistors are stacked. A good solution for low-voltage applications is the use of multi-stage amplifiers to achieve sufficient gain. The first stage is a differential amplifier with tail transistor, the following stages are common source stages with active loads. This choice keeps the number of stacked transistors to a maximum of three. On the other hand, multistage opamps suffer from stability issues and compensation is often difficult and requires particular techniques. In our design we decided for a two-stage CMOS fully differential opamp which is the active part of the active *RC*-integrators of the loop filter (Fig. 3.17). Pmos transistors are used as input transistors thanks to their superior performance in terms of Flicker noise [Jak96, Raz99]. An additional advantage of pmos transistors is that these can be placed in a separate n-well avoiding body effect, hence allowing low-VT operation.

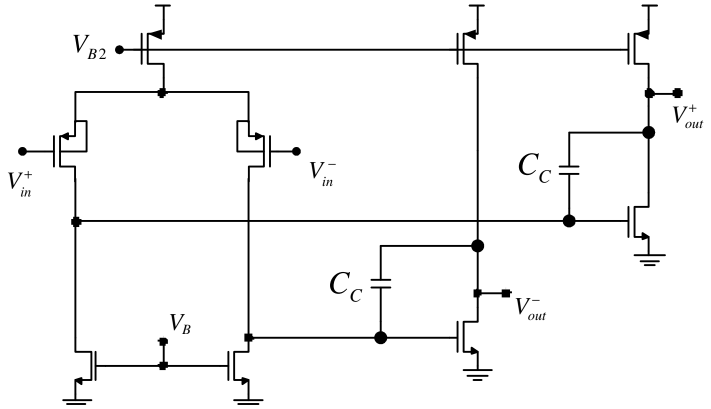


Fig. 4.1. Two stage opamp. Common-mode feedback and bias circuit not shown for simplicity

The proposed architecture has following advantages: same dc level of the input and output voltages; suitability for resistive loads because of the relatively low output resistance; rail-to-rail output swing; low-voltage compliance since no transistor stacking is used.

Our design goal is to design a high performance integrator without increasing the power consumption. To get rid of this problem a good solution is the exact modelling of the opamp in order to get the optimal sizing of the components.

4.2.1. Standard design approach

The *standard* design approach of an RC-Integrator based on the two-stage opamp of Fig. 4.1 is shortly illustrated in this section. The simplified small-signal equivalent circuit is depicted in Fig. 4.2.

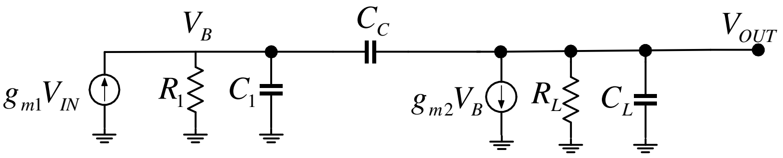


Fig. 4.2. Standard design approach: small-signal equivalent circuit of the loaded opamp

Typically the load capacitance C_L includes also the feedback capacitor of the RC-integrator and is relatively large. Assuming that g_{m1}, the transconductance of the input transistors, is of the same order of the g_m of the load transistors of the 1st stage and neglecting the noise contribution of the 2nd stage[5], we can estimate the total input-referred thermal noise of the opamp as (see also section 2.8.4.1):

---

[5] The noise of the 2nd stage can be neglected if the gain of the 1st stage is much larger than one.

$$S_{v,in}(f) \cong \frac{8}{3} kT \frac{4}{g_{m1}} \tag{4.1}$$

where the factor 4 accounts for the four transistors in the differential input stage. If these assumptions apply, g_{m1} is sized in order to fulfill the noise specifications of the integrator. The compensation capacitors C_C are placed across the input and the output of the 2nd stage, i.e., working as Miller capacitances.

The capacitors C_C are dimensioned in order to fulfill the bandwidth requirement of the opamp:

$$GBW \cong \frac{g_{m1}}{C_C} \tag{4.2}$$

Eq. (4.2) is valid if the opamp is compensated so that the non-dominant poles are located beyond the unity-gain frequency.

After compensation the dominant pole of the opamp is:

$$s_{p1} \cong -\frac{1}{R_1 C_C A_{v2}} \tag{4.3}$$

where R_1 is the output resistance of the 1st stage and $A_{v2}=g_{m2}R_L$ the voltage gain of the 2nd stage. The output capacitance C_1 of the 1st stage was neglected, since this is usually much smaller than the Miller-magnified C_C.

The non dominant pole [Gra01] is approximately located at:

$$s_{p2} \cong -\frac{g_{m2} C_C}{C_L C_1 + C_C C_L + C_C C_1} \tag{4.4}$$

After compensation $|s_{p2}|$ is much larger than $|s_{p1}|$ (pole splitting). To guarantee sufficient phase margin the frequency of s_{p2} must be larger than the unity-gain frequency of the opamp. Typically $|s_{p2}|$=2GBW$\approx 2g_{m1}/C_c$ is selected, giving approximately 63° of phase margin. Replacing this value of $|s_{p2}|$ in (4.4) we obtain:

$$g_{m2} = 2 g_{m1} \frac{C_L C_1 + C_C C_L + C_C C_1}{C_C^2} \tag{4.5}$$

The positive zero which arises because of the feedback path through C_C is usually eliminated either by means of a zero-nulling resistor in series with C_C or with a voltage or current buffer. The function of the buffer is to make the path across the compensation capacitor uni-directional, i.e. the FF direction is blocked, while the feedback is maintained. The method described so far does not lead to the optimal solution, since it causes **over-designing** of the operational amplifier, as we guarantee stability for all kinds of passive feedback networks although the opamp feedback is merely capacitive. Moreover, the load capacitance is typically assumed to include also the integrator feedback capacitance, further increasing the required g_{m2}. In fact, assuming a constant overdrive voltage, the bias current required in the output stage is proportional to the required g_{m2}. Another issue of the standard method is represented by the introduction of an additional zero when using the opamp as RC-integrator. This zero arises from the external feed-forward path through the integration capacitance C and must be taken into account in order to avoid instable behaviour.

4.2.2. New design approach

To overcome the issues with the standard approach an alternative solution is proposed in this section. This consists in designing the whole integrator without separating the opamp from the rest of the integrator. The small-signal equivalent circuit of the RC-Integrator is depicted in Fig. 4.3.

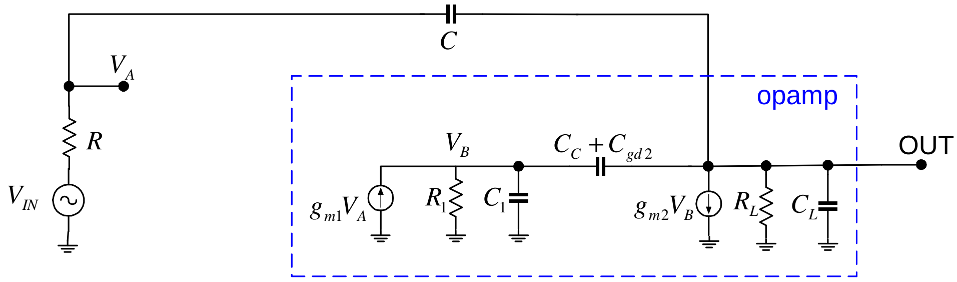


Fig. 4.3. Small-signal equivalent circuit of the active *RC*-integrator with a 2-stage opamp

Applying the Norton equivalence at the input the circuit in Fig. 4.4 is obtained.

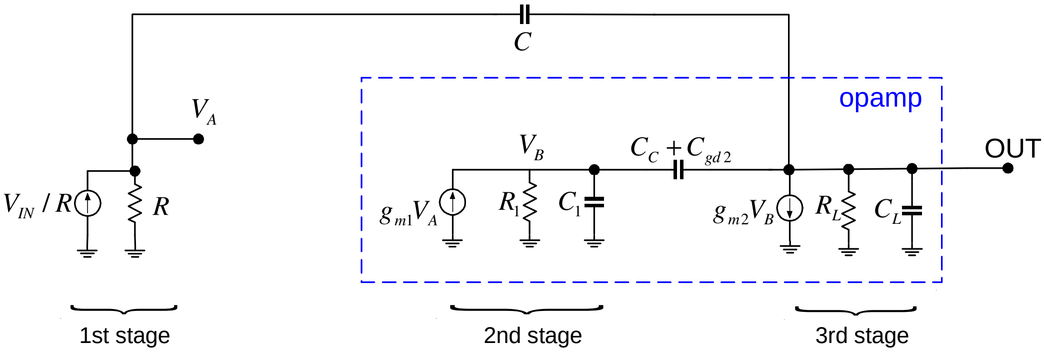


Fig. 4.4. Norton equivalent small-signal circuit of the active *RC*-integrator with a 2-stage opamp

R is the input resistor, C the integration capacitance, g_{m1}, R_1, C_1 and g_{m2}, R_L, C_L are the transconductance, the output resistance and the output capacitance of the first and second stage respectively. C_C is the opamp compensation capacitor and C_{gd2} the gate-drain capacitance of the amplifying transistor of the second stage. Both can be joined together into C_C', since they are in parallel. It should be noted that C_L does *not* include the feedback capacitor C but only the capacitive load of the integrator. C_L of the 1st and 2nd integrator used in the filter topology proposed in this work is small, as only resistive components load the integrators. On the other hand the load capacitance of the 3rd integrator is relatively large, since this drives the input capacitance of the quantizer.

Interestingly this circuit can be seen as a "three-stage amplifier", where the 1st stage of the new amplifier is the Norton equivalent of the signal source and the input resistor and has unit gain. This representation simplifies the analysis of the circuit, since we can make use of the available literature about three-stage amplifiers and their compensation. In particular we can consider the integration capacitor C as the compensation capacitance of the outermost loop of a nested Miller-compensated amplifier. The compensation technique used in this work is that proposed in [Leu99], which employs a common zero-nulling resistor to eliminate the positive zero arising from the FF paths through C and C_C.

With the aid of the symbolic math software Maple® we calculate the transfer function of the small-signal equivalent circuit of the RC-integrator:

$$H(s) = A_{DC} \frac{\frac{C\left(C_1 + C_C^{'}\right)}{g_{m1} g_{m2}} s^2 + \frac{C_C^{'}}{g_{m2}} s - 1}{k_3 s^3 + k_2 s^2 + k_1 s + 1} \tag{4.6}$$

The third order **denominator** has following coefficients:

$$\begin{aligned} k_3 &\cong R_1 R_L RC\left(C_L C_C^{'} + C_L C_1 + C_1 C_C^{'}\right) \\ k_2 &\cong R_1 R_L RCC_C^{'}\left(g_{m2} - g_{m1}\right) \\ k_1 &\cong R_1 R_L g_{m2}\left(RCg_{m1} + C_C^{'}\right) \end{aligned} \tag{4.7}$$

Dominant pole. Since the dominant pole s_{p1} arises at the input node because of the Miller-magnified integration capacitance C and is located at a very low frequency, we can make the assumption $|s_{p1}| << |s_{p2}|, |s_{p3}|$. This leads to following:

$$s_{p1} \cong -\frac{1}{k_1} = -\frac{1}{R_1 R_2 g_{m2}\left(RCg_{m1} + C_C^{'}\right)} = -\frac{1}{A_{DC}\left(RC + \frac{C_C^{'}}{g_{m1}}\right)} \tag{4.8}$$

where A_{DC} is the DC gain of the opamp. The dominant pole s_{p1} is due to the integration capacitance, which appears at the virtual ground node magnified by the opamp DC-gain (Miller effect). Eq. (4.8) shows the frequency shift of s_{p1} because of $C_C{'}$ from the theoretical value $1/(RCA_{DC})$. This directly causes a gain error of the integrator, as the 20-dB-slope range, in which the circuit works as an integrator, starts at an earlier frequency as required. To minimize the pole shift because of $C_C{'}$ following condition must be fulfilled:

$$\frac{C_C^{'}}{g_{m1}} \cong \frac{C_C}{g_{m1}} << RC \tag{4.9}$$

By writing the reciprocals of both size of (4.9) we get:

$$\omega_u = \frac{g_{m1}}{C_C} >> \frac{1}{RC} = \omega_I \tag{4.10}$$

Eq. (4.10) states that the unity-gain frequency ω_u of the opamp must be much larger than the corner frequency ω_I of the integrator.

Non-dominant poles. Two other poles are located at higher frequencies. With the dominant pole approximation they are the solutions of the equation:

$$k_3 s^2 + k_2 s + k_1 = 0 \tag{4.11}$$

If (4.10) applies and we replace the k_i coefficients according to (4.7) equation (4.11) becomes:

$$\left(C_1C_C^{'} + C_1C_L + C_LC_C^{'}\right)s^2 + \left(g_{m2} - g_{m1}\right)C_C^{'}s + g_{m1}g_{m2} = 0 \tag{4.12}$$

The non-dominant poles can be real or complex-conjugate, depending on the circuit parameters. In order to get a stable system all poles must have negative real parts. This is accomplished if:

$$k_2 > 0 \Rightarrow g_{m2} > g_{m1} \tag{4.13}$$

Another important aspect is that these poles do not depend, at a first order approximation, on the output resistance of the individual stages. The poles s_{p2} and s_{p3} can be real and distinct or complex-conjugate depending on the discriminant Δ of the quadratic equation (4.12). The transconductance of the output stage g_{m2} should be large enough to shift the non-dominant poles s_{p2}, s_{p3} at frequencies, where the integrator gain is much lower than one, that is, beyond its corner frequency. This is required to preserve the integrator transfer function, i.e. 90 degree phase shift and an amplitude slope of -20 dB/dec up to the corner frequency.

Zeros. Analyzing the **numerator** we recognize two zeros. These are the roots of the equation:

$$C\left(C_1 + C_C^{'}\right)s^2 + C_C^{'}g_{m1}s - g_{m1}g_{m2} = 0 \tag{4.14}$$

Eq. (4.14) has two positive and one negative coefficient. According to Descartes' rule of signs one solution is negative and one is positive. A positive zero has the same phase behavior as a pole, leading to a worsening of the phase margin. An additional measure against this problem must be taken. Zeros arise from feed-forward paths, possible solutions to eliminate these include: path interruption via current buffers [Ahu83] or voltage buffers [Tsi76]; additional feed-forward transconductance paths [You97]; insertion of zero nulling resistors [Leu99]. The last technique was preferred because of its higher linearity and lower power consumption. This technique includes a common resistor among the two feed-forward paths of the multi-stage amplifier (Fig. 4.5).
The new transfer function becomes quite complex and has the form:

$$H(s) = A_{DC}\frac{n_3s^3 + n_2s^2 + n_1s - 1}{k_4s^4 + k_3s^3 + k_2s^2 + k_1s + 1} \tag{4.15}$$

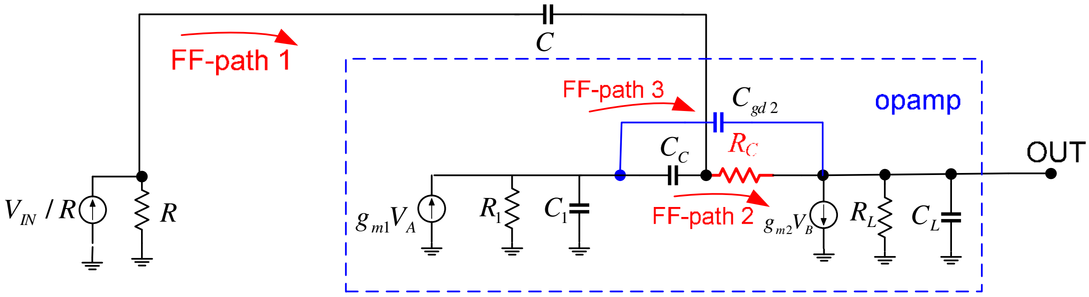


Fig. 4.5. Small-signal equivalent circuit of the active *RC*-integrator with a 2-stage opamp and zero-nulling resistor

indicating the presence of three zeros and four poles. The third zero is introduced by the new FF-path after the insertion of R_C, since C_{gd2} is not in parallel with C_C anymore.
Making following assumptions: $g_{m1}R_1$, $g_{m2}R_L$>>1 (i.e. high stage gain), R_C<<R,R_1,R_L and C_{gd2}<<C_1,C_L,C_C the numerator and denominator coefficients can be calculated, again, with the aid of the symbolic software Maple®:

$$\begin{aligned}
k_4 &\cong R_1 R_L R_C C_C R C\left(C_L C_1 + C_{gd2} C_1 + C_{gd2} C_L\right)\\
k_3 &\cong R_1 R_L R C\left(C_L C_C^{'} + C_L C_1 + C_1 C_C^{'}\right)\\
k_2 &\cong R_1 R_L R C C_C^{'}\left(g_{m2} - g_{m1}\right)\\
k_1 &\cong R_1 R_L g_{m2}\left(R C g_{m1} + C_C^{'}\right)
\end{aligned} \tag{4.16}$$

$$\begin{aligned}
n_3 &\cong \frac{C_{gd2} R_C C_C C}{g_{m1} g_{m2}}\\
n_2 &\cong C\frac{C_1 - C_C g_{m2} R_C + C_C^{'}}{g_{m1} g_{m2}}\\
n_1 &\cong \frac{C_C^{'} - g_{m2} R_C\left(C + C_C\right)}{g_{m2}}
\end{aligned} \tag{4.17}$$

where, again, $C_C^{'}$ is the sum of C_C and C_{gd2}. The denominator coefficients k_1, k_2 and k_3 are the same as in the case without R_C if R_C is “small”. At first it will be assumed that the poles are largely spaced, except for s_{p2} and s_{p3}:

$$\left|s_{p1}\right| << \left|s_{p2}\right|,\left|s_{p3}\right| << \left|s_{p4}\right| \tag{4.18}$$

This assumption states[6] that the integrator has one dominant pole s_{p1}, two “middle frequency” poles s_{p2}, s_{p3} and one high-frequency pole s_{p4}. Hence, we can calculate the poles as following:

$$s_{p1} \cong -\frac{1}{k_1} \tag{4.19}$$

The location of s_{p1} is the same as in (4.8), hence it is independent of R_C. The middle-frequency poles s_{p2} and s_{p3} of the integrator are the roots of the equation:

$$k_3 s^2 + k_2 s + k_1 = 0 \tag{4.20}$$

Since the coefficients k_1, k_2 and k_3 of (4.16) are the same as in (4.7) the location of s_{p2} and s_{p3} remains, at first order, unchanged after the insertion of a low-ohmic R_C.

The high-frequency pole s_{p4} is given by:

$$s_{p4} \cong -\frac{k_3}{k_4} = \frac{\left(C_1 C_C^{'} + C_1 C_L + C_L C_C^{'}\right)}{R_C C_C\left(C_L C_1 + C_{gd2} C_1 + C_{gd2} C_L\right)} \tag{4.21}$$

---

[6] The assumption is valid for realistic values of g_{mi}, R_i, C_i and under the previous assumptions (i.e. large stage-gain, R_C and C_{gd2} “small”). Transistor level simulations of the proposed integrator confirm the correctness of the reasoning.

s_{p4} goes toward infinity if R_C is zero. For realistic, small R_C values, this pole can be neglected.

The **zeros** of the integrator are the roots of the polynomial:

$$n_3 s^3 + n_2 s^2 + n_1 s - 1 = 0 \tag{4.22}$$

Replacing the n_i coefficients the nominator is:

$$C_{gd2} R_C C_C C s^3 + C\left(C_1 + C_C^{'} - C_C g_{m2} R_C\right) s^2 + \left[C_C^{'} - g_{m2} R_C \left(C + C_C\right)\right] g_{m1} s - g_{m1} g_{m2} = 0 \tag{4.23}$$

The three roots of (4.23) are the zeros of the integrator. The sign of the zeros can be determined with the aid of the Decartes' rule stating that the number of positive roots is equal to the number of sign differences between consecutive coefficients.

Following table summarizes the sign of the coefficients and the sign of the zeros for different values of R_C:

R_C value	**Sign of the coefficients**				**Sign of the zeros**
	s^3	**s^2**	**s^1**	**s^0**	
$R_C=0$	0	+	+	–	one positive, one negative
$0<R_C<C_C^{'}/[g_{m2}(C+C_C)]$	+	+	+	–	one positive, two negative
$C_C^{'}/[g_{m2}(C+C_C)]<R_C<(C_1+C_C^{'})/(g_{m2}C_C)$	+	+	–	–	
$R_C>(C_1+C_C^{'})/(g_{m2}C_C)$	+	–	–	–	

Tab 4.2. Sign of the zeros as function of R_C

Clearly the number of sign variations is always one meaning that one positive zero is always present and cannot be eliminated. Still, it can be shifted to higher frequencies, where it is not an issue for the integrator frequency response. The root locus of the zeros as function of R_C is shown in the next section for concrete values of the capacitances and transconductances of the integrator.

The sizing of the circuit was performed in four steps:

1) R and g_{m1} are given by noise specs, since they give the predominant contribution to the input thermal noise of the integrator. Once R is obtained, the integration capacitance is set by the integrator corner frequency $\omega_I=1/RC$.
2) C_C is sized according to (4.10).
3) The transconductance g_{m2} of the output stage is chosen in order to locate the non-dominant poles s_{p2}, s_{p3} far beyond the corner frequency of the integrator $\omega_I=1/RC$. This preserves the frequency response of the integrator. An upper limit of g_{m2} is determined by the power consumption of the output stage. A good compromise consists in placing s_{p2}, s_{p3} at frequencies which are ten times larger than ω_I.
4) The last step is the choice of R_C in order to maximize the phase margin of the integrator by shifting one positive zero toward infinity.

4.2.3. Dimensioning of the 1st integrator

In the following the dimensioning of the components of the 1st integrator is explained. As described in Tab. 3.6, for the 1st integrator following values were chosen:

$$R = 3k\Omega,\ C = 1.12pF \tag{4.24}$$

where R is the input resistor and C the feedback capacitor of the integrator. The noise contribution of the input resistor was calculated in section 3.52. The transconductance g_{m1} of the input p-mos transistors is chosen according to thermal noise considerations. The input-referred opamp thermal noise is, neglecting the Flicker noise:

$$\sqrt{v_{nOTA1}^2} = \sqrt{2\frac{8}{3}\frac{KT}{g_{m1}}\left(1+\frac{g_{m1}}{g_{mn}}\right)f_B} \tag{4.25}$$

where the factor 2 accounts for the differential implementation, f_B is the signal bandwidth and g_{mn} is the transconductance of the load current sources of the opamp input stage. Eq. (4.25) is an approximate formula valid for long channel transistors; nevertheless it is sufficient for an estimation of the noise. Assuming $g_{m1} \cong g_{mn}$=1.2mS and a signal bandwidth of 12.5 MHz, the resulting input-referred *rms* noise voltage amounts to 21.4μV.

The maximum SNR due to the opamp thermal noise is, when an input sine signal with a single-ended amplitude V_{FS}=0.325V is applied:

$$SNR_{th,opamp} = 10\log\frac{2V_{FS}^2}{v_{nOTA1}^2} = 86.6dB = 14.1bit \tag{4.26}$$

Eq. (4.26) shows that the thermal noise introduced by the opamp with the selected g_{m1} is very small for the intended modulator resolution of 11 bit. This choice is dictated in order to let some margin for other noise contributors. In particular, a large contribution to the overall input-referred circuit is produced by the current sources of the main DAC as explained later. A further contribution is given by the Flicker noise of the active elements.

The compensation capacitor is dimensioned according to (4.10) so that the unity-gain frequency of the opamp is a factor 10 larger than the corner frequency of the integrator:

$$C_C = \frac{g_{m1}RC}{10} \tag{4.27}$$

Eq. (4.27) leads to a compensation capacitor of approximately 400 fF.

The transconductance of the opamp output stage g_{m2} is chosen so that the poles s_{p2}, s_{p3} are larger than the unity-gain frequency of the opamp ω_u (i.e., at least ten times larger than ω_I) and exhibit only moderate peaking. Fig. 4.6 shows the root locus of the non-dominant poles as function of g_{m2} according to (4.12).

The capacitances needed for the estimation of the location of the non-dominant poles (C_1, C_L, C_{gd2}) were estimated according to technology data of the oxide capacitance (11 fF/μm^2) and considering the dimension of the transistors required for a given g_m. g_{m1} was fixed to 1.2 mS according to thermal noise requirements as previously explained.

The values of R_1, R_L are not required for the estimation of the zero and pole location, since these terms do not appear in the formulas of the analytical model. The DC-gain of the integrator was assumed to be 225 (47 dB), which is a realistic value for a two-stage amplifier in 0.13 µm CMOS. This value is needed for the determination of the dominant pole s_{p1}. The Bode diagram of the integrator according to the proposed model (4.6) as function of g_{m2} is plotted in Fig. 4.6. A g_{m2} value of 2.4 mS was chosen, this being a good compromise between low frequency-peaking (larger g_m reduces peaking and increases the frequency of s_{p2}, s_{p3}) and low-power (larger g_m means more power consumption).

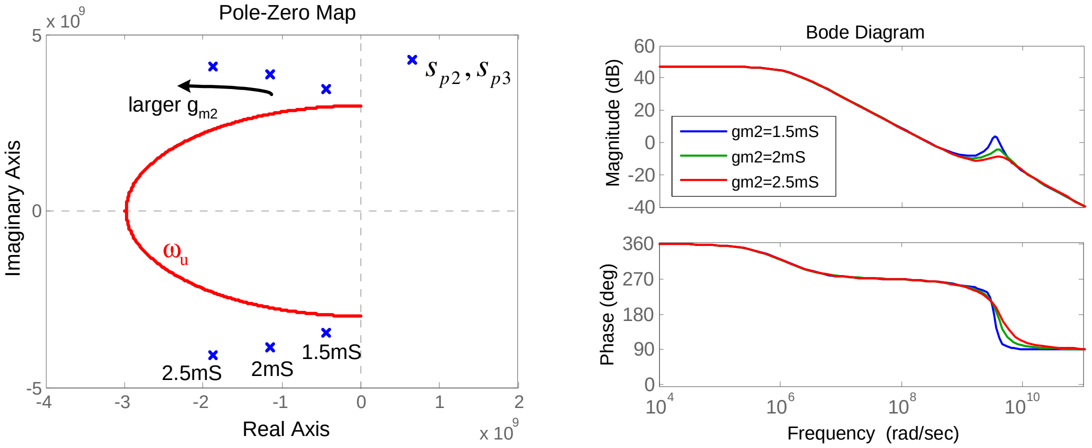


Fig. 4.6. Left: Root locus of s_{p2}, s_{p3} as function of g_{m2}, right: Bode diagram of the integrator as function of g_{m2} according to (4.6).

The last step consists in dimensioning the zero-nulling resistor R_C. Fig. 4.7 shows the zero-locus depending on R_C according to (4.23). While the negative zero s_{n1} remains nearly constant, increasing R_C the positive zero s_{n2} is shifted toward higher frequencies, thus increasing the phase margin. Also s_{n3} is shifted, still its effect remains negligible as long as R_C is small enough (high frequency zero).

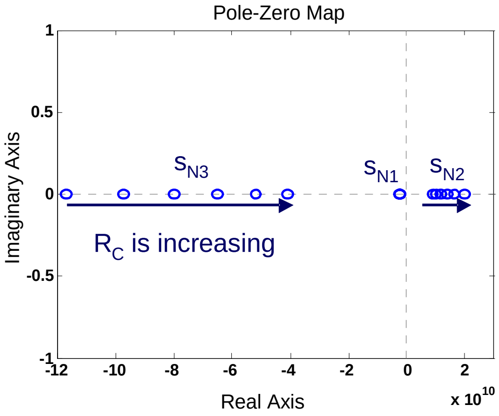


Fig. 4.7. Root locus of the zeros as function of R_C

Fig 4.8 plots the Bode diagram of the 1st integrator for different values of R_C. A value of 300 Ω guarantees a maximally flat phase response, hence a phase margin of 90° as in the ideal integrator.

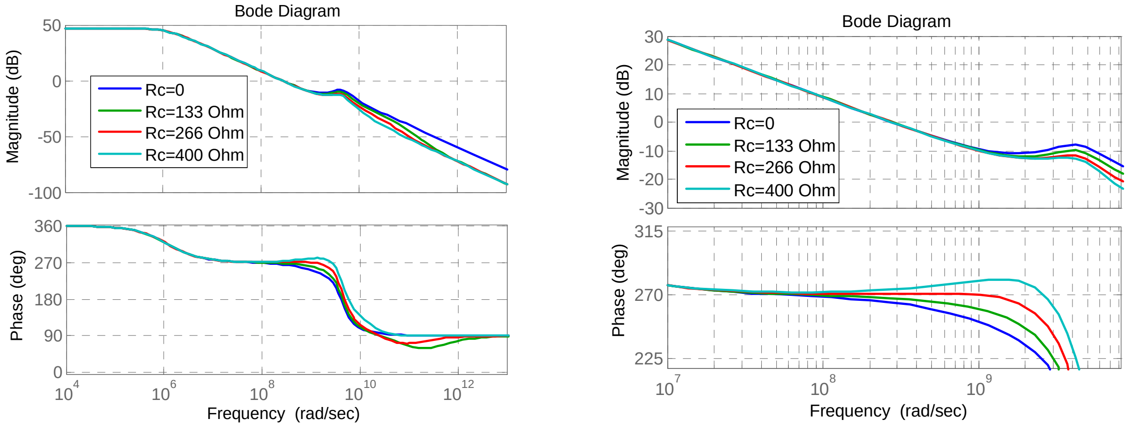


Fig. 4.8. Left: Bode diagram of the TF of the 1st integrator as function of RC. Right: zoom-in

Model verification. An *RC*-integrator was implemented as depicted in Fig. (4.9) and simulated at transistor level. The input resistor *R* and the integrating capacitance *C* are highlighted in blue. The opamp consists in a two-stage topology without stacked transistors for low-voltage compatibility. Input p-mos transistors were chosen in order to minimize Flicker noise [Raz99]. The output stage works in class A in order to guarantee maximum linearity. A common-mode feedback (CMFB) circuit is included, based on a differential amplifier with diode connected loads ([Gra01], p. 824). The common-mode output voltage is sensed by means of two relatively large resistors R_{cm}=30kΩ and compared with a reference voltage $V_{REF}=V_{DD}/2$=0.6V. Two small capacitors C_{cm} (50 fF) are included for improvement of the phase margin of the CM-loop. The nmos transistors loading the input stage are split in two identical parts. One part is biased with a constant gate voltage V_{B2}, the other is controlled by the output voltage V_{ctrl} of the CMFB amplifier (dashed rectangle in Fig. 4.9). This reduces the load capacitance of the CMFB amplifier, thus improving the phase margin of the CMFB loop.

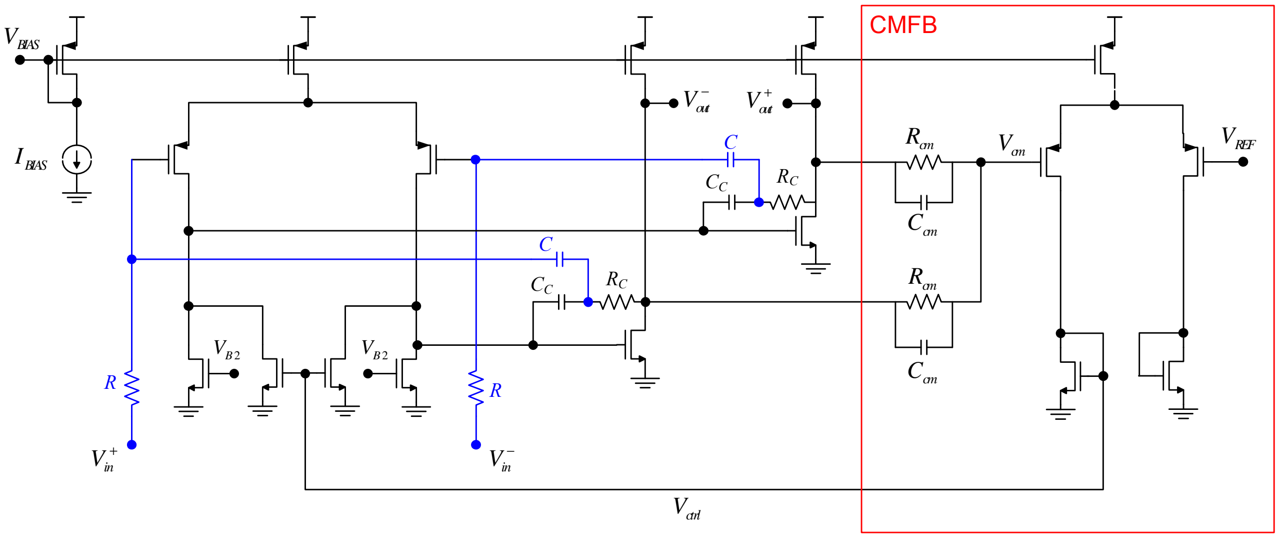


Fig. 4.9. *RC*-integrator based on a two stage opamp with common-mode feedback (CMFB)

Table (4.3) summarizes the transconductance of the amplifying transistors of the 1st and the 2nd stage together with the dimension of the passive components, Table (4.4) indicates the dimension of the main opamp transistors and Fig (4.10) depicts the Bode diagram of the approximated transfer function of the integrator together with the transistor level simulation results. Good accordance between the model and the simulation is obtained up to high frequencies. The deviation of the simulation results from the model at high frequencies is due to the effect of parasitic capacitances which were not included in the model. The 1st integrator consumes 786 μW draining a total current of 655 μA including bias and CMFB.

Circuit parameter	Size	Circuit parameter	Size
g_{m1}	1.2 mS	C_C	400 fF
g_{m2}	2.4 mS	C_L	100 fF
R	3 kΩ	External R_L	5 kΩ
R_C	300 Ω	C_{gd2} (simulated)	22 fF
C	1.12 pF	C_I (simulated)	160 fF

Tab 4.3. Main circuit parameters of the 1st integrator

	1st stage input pmos	1st stage nmos loads	1st stage pmos current tail	2nd stage input nmos	2nd stage pmos loads	CMFB input pmos	CMFB nmos loads	CMFB pmos current tail
W	80 μm	40 μm	40 μm	24 μm	40 μm	40 μm	20μm	20 μm
L	0.24 μm	0.6 μm	1 μm	0.24 μm	1 μm	0.24 μm	0.6 μm	1 μm

Tab 4.4. Size of the main transistors of the opamp in the 1st integrator

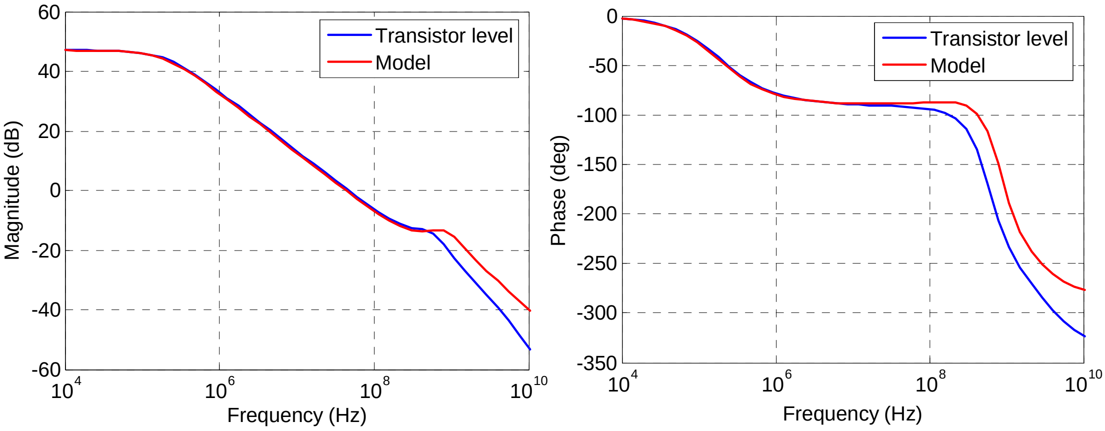


Fig. 4.10. Gain Magnitude (left) and phase of the simulated 1st integrator compared with the analytical model

To confirm the noise estimation the input referred noise of the opamp *input stage* was simulated. The PSD is plotted in Fig. 4.11. From a frequency of about 1 MHz the thermal noise of the input and load transistors dominates over the Flicker noise. The *rms* input noise integrated in the signal band of 12.5 MHz amounts to 20 μV, i.e. a SNR due to circuit noise of 87.2 dB is achieved, which is in accordance with the analytical estimation (4.26).

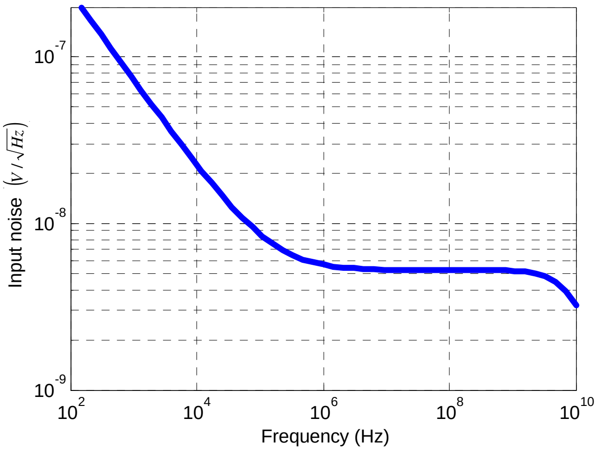


Fig. 4.11. Simulated input referred noise PSD of the opamp input stage (1st integrator)

4.2.4. Dimensioning of the 2nd integrator

The 2nd integrator is realized with the same architecture as the 1st integrator. The integrator circuit noise is shaped by the previous integrator; hence, a larger input resistor R can be chosen for this integrator. To realize the integrator coefficient A_2=0.418·f_s following values of the input resistor and the integrating capacitor were used: R=20kΩ, C= 300fF.

In order to reduce design and layout time the same identical *active* elements are used for the 1st and the 2nd integrator. The only differences are the values of the compensation capacitance and of the zero-nulling resistor. Tab. 4.5 synthesizes the component and transconductance values, while Fig. 4.12 compares the Bode diagram of the analytical model with the results of the transistor level simulation. The power consumption of the 2nd integrator amounts, as in the 1st integrator, to 786 mW.

Circuit parameter	Size	Circuit parameter	Size
g_{m1}	1.2 mS	C_C	300 fF
g_{m2}	2.4 mS	C_L	100 fF
R	20 kΩ	External R_L	5 kΩ
R_C	700 Ω	C_{gd2} (simulated)	22 fF
C	300 fF	C_1 (simulated)	160 fF

Tab 4.5. Main circuit parameters of the 2nd integrator

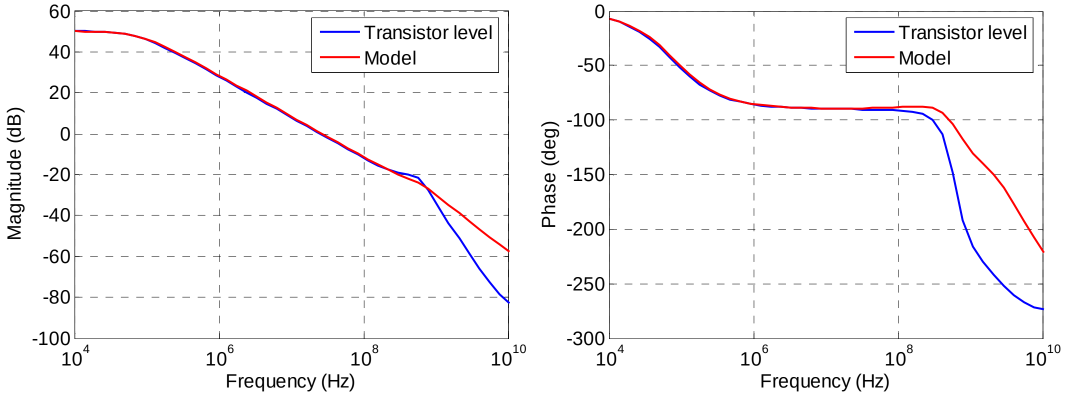


Fig. 4.12. Gain Magnitude (left) and phase of the simulated 1st integrator compared with the analytical model

4.2.5. Dimensioning of the 3rd integrator

The 3rd integrator of the loop filter has different requirements when compared to the preceding integrators. On the one hand the linearity requirements are relaxed because of its position at the end of the loop. On the other hand it must provide good slewing properties since it is fed by a RZ-DAC. In fact, a RZ-DAC is characterized by large current variations from zero to the data-depending current value. Furthermore, all FF paths of the loop filter are connected to the virtual ground of the opamp, feeding a relatively large amount of current. The optimal solution for such demands is a class AB push-pull output stage which joins low quiescent currents with large maximum output currents. The required level shift between the gates of the output transistors for class AB biasing is realized with a transistor coupled feed-forward control [Mon86], which has good quiescent current regulation, low chip area requirements, low-voltage suitability and good high-frequency behavior [Hog96]. The simplified schematic of the opamp used in the 3rd integrator is shown in Fig. 4.13. The function of the level shifter stage is to keep the DC voltage difference between the gates of the output transistors constant. This works as following: if the gate voltage of the output nmos rises, the V_{GS} of the nmos transistor of the level shifter drops, together with its drain current. Since the level shifter is biased with a constant current I_B, a larger portion of this current will flow through the pmos of the level shifter. This causes its source voltage to rise, thus rising the gate voltage of the output pmos transistor. Hence, the difference of the gate voltages of the output transistors remains approximately constant.

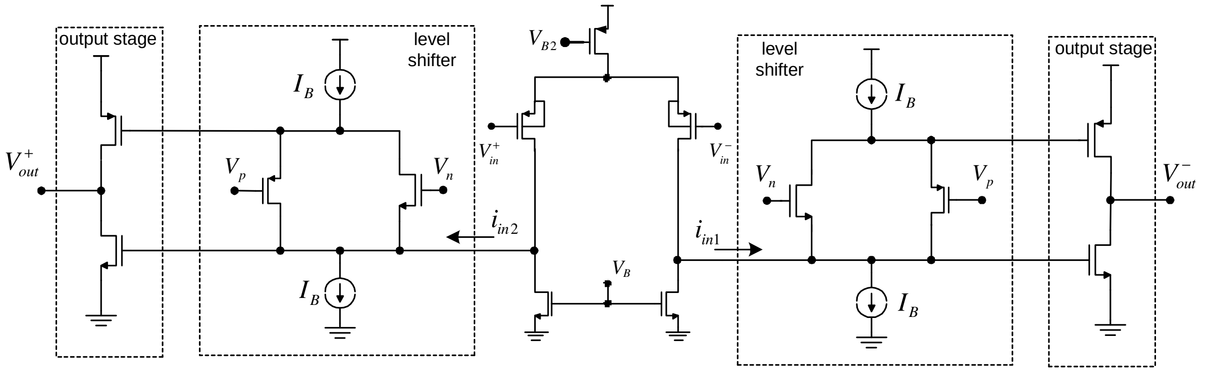


Fig. 4.13. Opamp of the 3rd integrator with class AB output stage [Mon86]. CMFB and compensation capacitors not shown for simplicity

The input stage current is sized so that no slewing occurs according to high-level simulations of the modulator. Concerning the ac behavior of the integrator, no zero-nulling resistor is required, since the output g_m of this opamp is large. The 3rd integrator drains a total current of 1.34 mA in the quiescent state, corresponding to a power consumption of 1.61 mW.

Circuit parameter	Size
g_{m1}	1.6 mS
g_{m2} (quiescent)*	9.8 mS
R	3.7 kΩ
C	300 fF
C_{Cn}	150 fF
C_{Cp}	150 fF
C_L	800 fF

*sum of g_m of both output transistors

Tab 4.6. Main circuit parameters of the 3rd integrator

4.3. Loop filter passive components

The following section describes the implementation of the integrated resistors and capacitors used in the loop filter.

4.3.1. Capacitors

All capacitors are metal-metal capacitors (MIM) with a specific capacitance of 1 fF/µm^2. This ensures high-linearity and low voltage and temperature sensitivity. Since the CT integrator coefficients are given by RC time constants, they are largely inaccurate because of the large process variations of the absolute values of integrated capacitors and resistors in the order of ±30%. To cope with this all integration capacitors are realized as switchable, binary weighted capacitor banks in parallel with a fixed capacitor. The implementation of the integration capacitors of the 1st integrator is depicted in Fig. 4.14. The wanted capacitance value can be tuned by means of a digital calibration word and is equal to:

$$C = C_{fix} + 2\sum_{i=0}^{n-1} b_i C_u \qquad (4.28)$$

where C_u is the unit capacitance. A 4-bit array is used for the integration capacitance of the 1st integrator, 3-bit are used for the 2nd integrator, 2-bit for the 3rd integrator. The values of the unit and fixed capacitors for all three integrators are given in Tab. 4.7.

Integration capacitance of	C_{fix}	C_u
1st integrator	700 fF	40 fF x 30
2nd integrator	75 fF	17 fF x 14
3rd integrator	39 fF	17 fF x 6

Tab 4.7. Composition of the integration capacitances

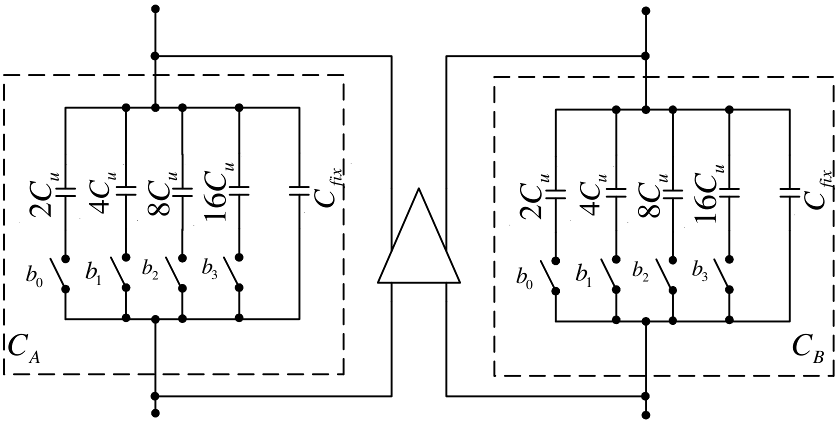
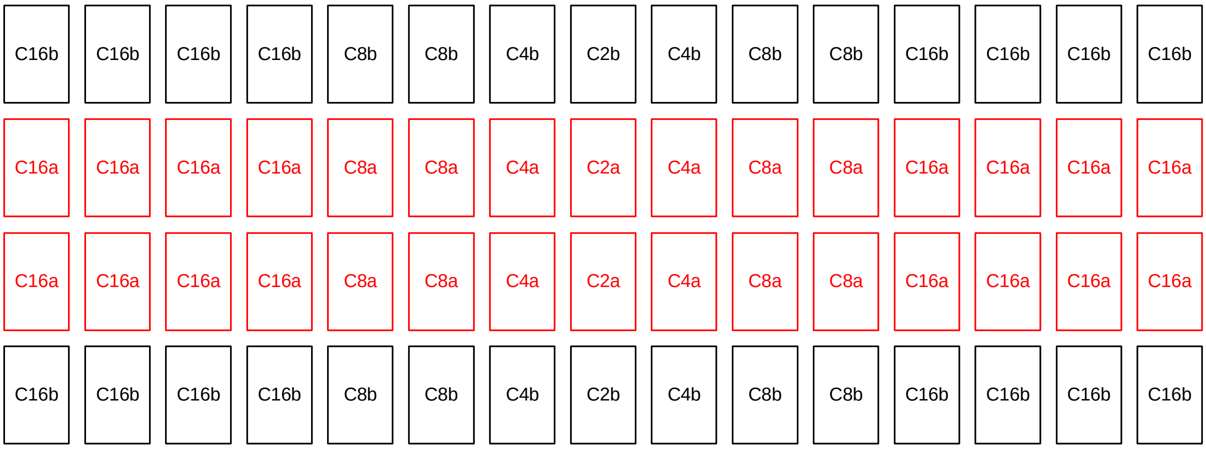


Fig. 4.14. Digitally tunable integrated capacitor of the 1st integrator

A fully symmetrical, common-centroid layout of the unit capacitors in the bank minimizes the systematic mismatch between the binary weighted capacitors. Fig. 4.15 depicts the layout of the variable part of the two integration capacitors (differential implementation) of the 1st integrator. The number denotes the weight of the capacitance to whom the unit capacitors belong, the indexes *a* and *b* denote the integration capacitance of the differential circuit to whom they belong (cp. Fig. 4.14).



C16b	C16b	C16b	C16b	C8b	C8b	C4b	C2b	C4b	C8b	C8b	C16b	C16b	C16b	C16b
C16a	C16a	C16a	C16a	C8a	C8a	C4a	C2a	C4a	C8a	C8a	C16a	C16a	C16a	C16a
C16a	C16a	C16a	C16a	C8a	C8a	C4a	C2a	C4a	C8a	C8a	C16a	C16a	C16a	C16a
C16b	C16b	C16b	C16b	C8b	C8b	C4b	C2b	C4b	C8b	C8b	C16b	C16b	C16b	C16b

Fig. 4.15. Layout of the tunable capacitors of the 1st integrator

4.3.1.1. *RC*-calibration circuit (not implemented)

A possible way for automatic calibration of the *RC* time constants of the integrators is depicted in Fig. 4.16. The circuit works as in the following: one plate of the capacitor under test is separated from the integrator and connected to ground by means of a commuting switch S_1. A constant voltage V_{R1} is applied to the so obtained *RC* member; at the same time a clocked counter is triggered. The voltage V_C across the capacitor rises according to:

$$V_C(t) = V_{R1}\left(1 - e^{-\frac{t}{RC}}\right) \tag{4.29}$$

where C is the capacitance composed by the fixed capacitor C_{fix} and the additional binary weighted capacitors which are currently switched on.

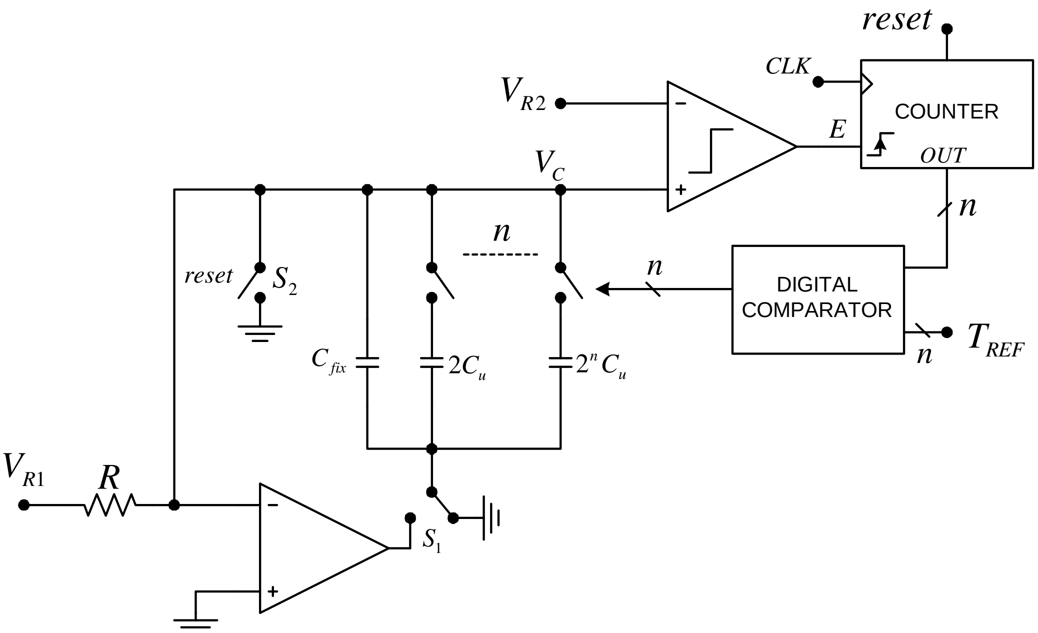


Fig. 4.16. A possible automatic circuit for calibration of the RC products

$V_C(t)$ is compared with a reference voltage V_{R2} by means of a comparator which toggles as soon as V_C reaches V_{R2}. At this point the counter is stopped by the rising voltage at the pin E. The time required by the capacitor to be charged to the reference voltage V_{R2} is proportional to the RC product:

$$t_F = RC \ln \frac{V_{R1}}{V_{R1} - V_{R2}} \tag{4.30}$$

The value stored in the counter at the end of the charge process is the number of clock cycles required by the capacitor to be charged, hence, according to (4.30) is proportional to the *RC* product. A digital comparator can switch additional capacitors on/off depending on the difference between the digital word in the comparator and a reference word T_{REF} which represents the charging time for a nominal *RC*-constant. The so obtained new capacitance is reset with the switch S_2 and charged again. The calibration procedure terminates when the difference between the charge time (represented in the counter at the end of every charge process) and the nominal time T_{REF} is smaller than a minimum value.

A different calibration circuit, which charges the capacitor with a constant reference current is shown in [Mit06].

4.3.2. Resistors

The integrated resistors are implemented with polysilicon non-salicided resistors in two flavors: high-resistance for the large feedback resistors of 529 kΩ to save chip area and reduce the parasitic capacitance, normal type for all other resistors.

4.4. Quantizer

A 14-level flash ADC is used as a quantizer. This consists of a resistor ladder for the generation of the reference voltages and 13 sampled comparators. Each comparator is composed of a switched capacitor sampler, a preamplifier, a cross-coupled bistable element and a D-flip-flop for output synchronization (Fig. 4.17).

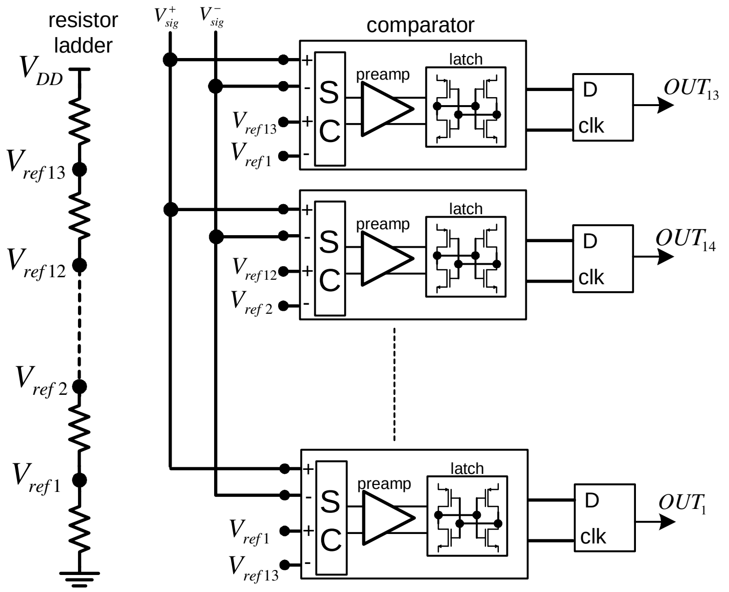


Fig. 4.17. Schematic of the 14-level flash ADC used as quantizer

The offset requirements are not very stringent because of 3rd order noise shaping. Behavioral simulations show that an offset of up to 20 mV is tolerable to achieve the required resolution of the modulator. On the other hand glitches at the comparators' inputs are problematic. These can be reduced by means of a low-ohmic resistor ladder, which nevertheless leads to larger static current consumption. To keep the resistor size at a reasonable level additional preamplifiers are used, which work as buffers between the inputs and the cross-coupled latches of the comparators. Each preamplifier consists of a differential pair with current tail transistors and low-ohmic passive loads (Fig. 4.18). A current of 30 µA flows in each branch of the differential amplifier. The value of the load resistors R_L=20kΩ is chosen according to a trade-off between speed (lower values enhance the cut-off frequency), gain (larger R_L means more gain, i.e., more suppression of mismatch and glitches of the latch stage) and DC output level (the gates of the following stages must be biased in strong inversion). The main preamp parameters are listed in Tab. 4.8. An additional advantage when using a preamp is the reduction of the input offset of the quantizer. In fact, the input offset of the cross-coupled element (latch) is usually large, as the area of its transistors must be kept small to reduce the dynamic power consumption; on the contrary, larger low-offset transistors can be used in the differential pair of the preamp. In this case the preamp gain reduces the contribution of the latch input offset to the total offset. The offset voltage of the preamp was estimated considering only the mismatch of the V_T of the input transistors. According to [Pel89]:

$$\sigma(V_{OS}) \cong \sigma(V_T) \cong \frac{A_{VT}}{\sqrt{W_1 L_1}} \tag{4.31}$$

where A_{VT} is a technology constant, A_{VT}=5.2 mV·μm in the used technology and W_1, L_1 are the width and the length of the preamp input transistors respectively. The calculated input offset V_{OS} amounts to 3.4 mV for each pre-amplifier.

Gain	**I_{DC}**	**W/L_{in}**	**f_{3dB}**	**V_{OS}**	**R_L**
19.7 dB	60 μA	10μm / 0.24 μm	1.17 GHz	4.7 mV	20 kΩ

Tab 4.8. Main parameters of the pre-amplifier

In order to allow nearly rail-to-rail input signals and reference voltages of the comparator, a switched capacitor (SC) input network is provided (Fig. 4.18), which makes the bias voltage of the input transistors of the preamplifiers independent on the signal and reference amplitude; otherwise these would be completely turned off for input signals (or references) approaching the negative supply rail if of n-mos type (positive rail for p-mos inputs) making pre-amplification possible only in a reduced input range. Non-overlapping phases φ_1 and φ_2 (Fig. 4.19) are used for the sampling of the reference voltage difference and of the input signal difference respectively. Channel charge injection from switched off transistors is minimized by using half-sided dummy transistors with opposite control phases connected to the sensitive nodes. The sampling capacitances C_s are sized according to a trade-off: larger capacitances decrease the signal attenuation at the input because of the capacitive divider C_s–C_{in} (Fig. 4.18) and reduce KT/C noise; smaller capacitances are charged faster and reduce loading of the preceding integrator. A value of 60 fF was chosen for C_s.

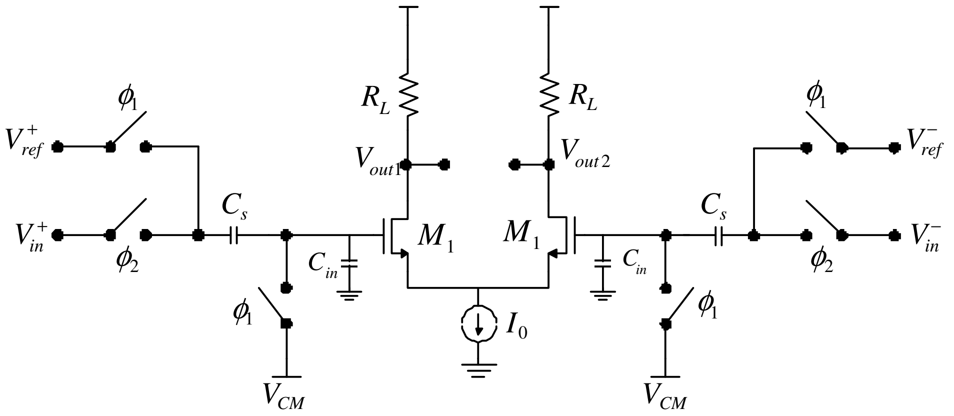


Fig. 4.18. Comparators' input stage: SC network and pre-amplifier

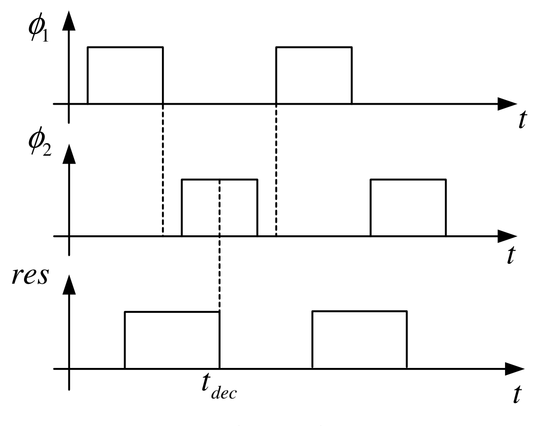


Fig. 4.19. Non-overlapping sampling phases (ϕ_1 and ϕ_2) and reset phase. The decision starts at t_{dec}.

After sampling, the output voltages of the preamp are converted into currents by the common source (CS) transistors M_2 (Fig. 4.20), which are biased by a current of 2.5µA each. The CS transistors M_2 work as a buffer between the latch and the preamp, reducing the capacitive coupling, therefore the kick-back noise at the comparator input. The current difference from the CS transistors is injected into a cross coupled latch which performs the comparator decision. To reduce hysteresis a reset switch controlled by the phase *res* is provided. When *res* is high the reset switch is switched on (reset phase) and both outputs of the cross coupled latch are at approximately half the supply voltage. At the high-low transition of *res* the reset switch is switched off and the decision phase occurs. After a short time the latch toggles to a stable state, where one output reaches V_{DD} and the other one is close to ground. Hence the maximum voltage variation at the output is limited to $V_{DD}/2$ (instead of V_{DD}), further reducing kick-back noise at the comparator input. CMOS inverters with asymmetrical dimensioning of the n-mos and p-mos transistors are used for regeneration of the logic output level. Finally a D-Flip-Flop completes the comparator to avoid signal depending decision time of the comparator. The D-FF is clocked in order to generate a constant delay of $T_s/2$ between the decision time and the time at which the comparator output is updated. Power-off switches are included, saving power by deactivating currently not used circuit parts.

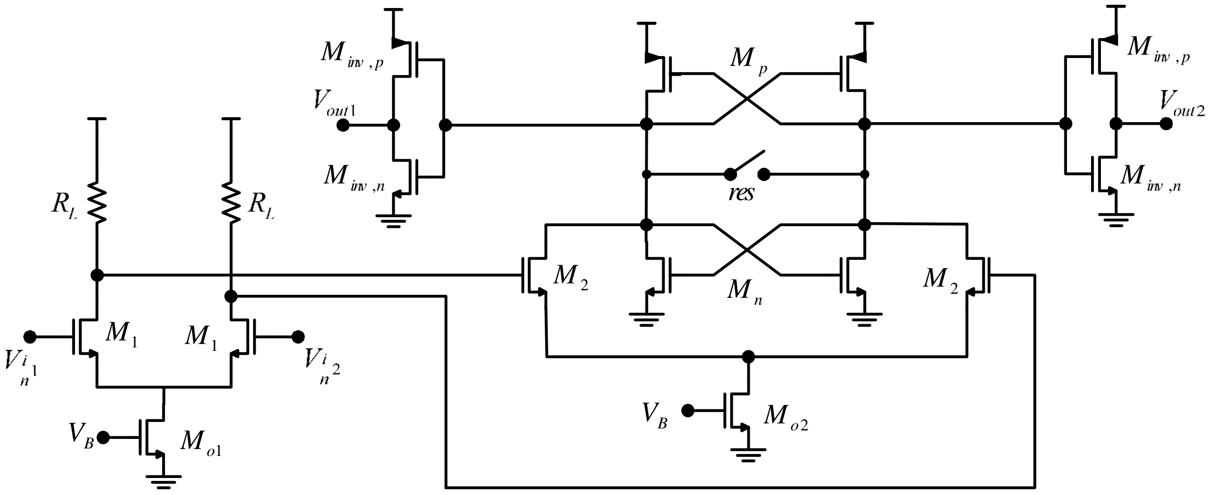


Fig. 4.20. Schematic of the comparator

The table below shows the size of the active components used in the comparator. The comparator layout is depicted in Fig. 4.21.

Transistor	M_1	M_{o1}	M_2	M_{o2}	M_n	M_p	$M_{inv,n}$	$M_{inv,p}$	**Switch**
Width (µm)	10	60	0.6	5	0.6	1	0.5	2	4
Length (µm)	0.24	0.36	0.12	0.36	0.12	0.12	0.12	0.12	0.12

Tab 4.9. Transistor size of the comparator

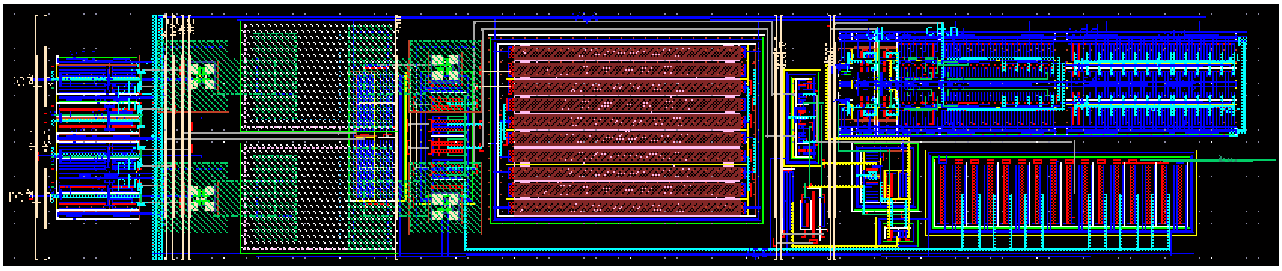


Fig. 4.21. Layout of the comparator

The reference voltages required for the comparator are generated by a resistor ladder which divides the supply voltage. The ladder is composed by 12 resistors of 80 Ω and two terminating resistors of 480 Ω between the largest reference and V_{DD} and between the smallest reference and ground. All 80 Ω-resistors are realized with two 160 Ω-resistors in parallel to increase the layout area in order to reduce the relative variations due to process mismatch.
The resistor ladder drains a total static current of 625 µA and the 13 equally spaced thresholds are between 0.3 and 0.9 V with a spacing of 50 mV. The total power consumption of the quantizer, including bias circuit and resistor ladder amounts to 3.7 mW.

4.5. Main DAC

The main NRZ DAC is an 11-bit-accuracy, differential DAC implemented with 13 identical Cascode current sources I_u (Fig. 4.22a). The *i*-th current is switched to the left or to the right branch according to the sign of the quantizer data D_i, providing fully differential operation. The current summation takes place at the virtual ground node of the 1st integrator. In order to provide bi-directionality, a constant, half full scale current $13 \cdot I_u/2$ feeds current to the virtual ground. This fixed current source consists of a pMOS regulated Cascode with large output resistance. A single-ended schema of the differential implementation together with the 1st integrator is shown in Fig. 4.22b. The current steering topology was chosen due to its advantages in term of fast response time. In fact, any delay in the feedback loop of the modulator increases the excess loop delay, worsening the resolution and eventually leading to instability. As explained in section 3.9 the NRZ DAC must be able to provide a current in the range [-108.33µA; +108.33µA]. After insertion of a fixed current source, which continuously feeds 108.33 µA, the multibit DAC must be able to drain a current in the range [0; +216.66µA]. This is accomplished with a bank of 13 switchable unit currents of:

$$I_u = \frac{216.66\mu A}{13} = 16.66\mu A \tag{4.32}$$

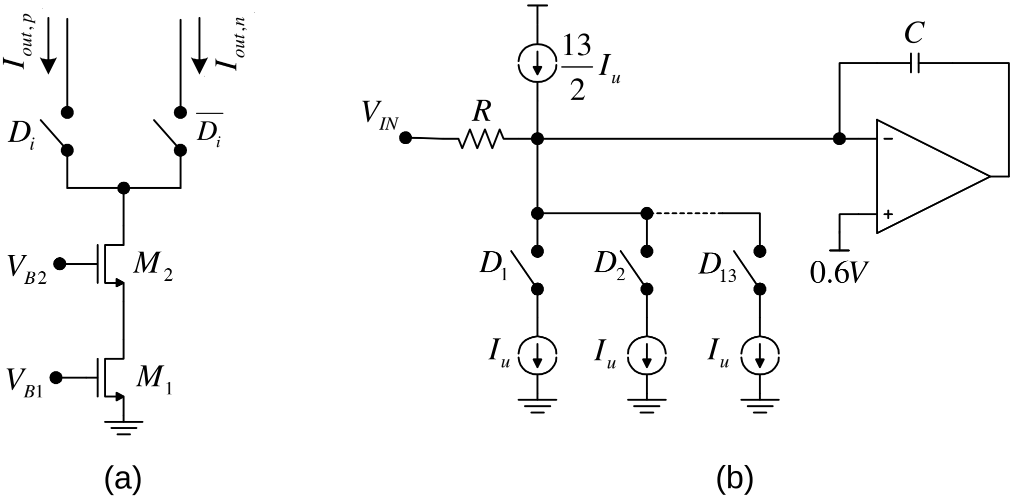


Fig. 4.22. a) Schematic of the unit current source, b) single-ended schematic of the DAC location

4.5.1. Mismatch

The matching of the unit current sources is of great importance for the linearity of the modulator. Because of the DAC location in front of the loop, the DAC non-idealities are not suppressed when referred to the modulator input. Any non-linearity in the DAC will have a direct effect on the SNDR and SFDR of the modulator, limiting its accuracy. In particular, any mismatch in the theoretically identical I_u modifies in a random way the height of a current step in the static DAC characteristic, introducing an integral non-linearity (INL). To quantify the mismatch between the current sources we use the model for the current mismatch of two closely spaced MOS-transistors [Kin96]:

$$\sigma^2\left(\frac{\Delta I_u}{I_u}\right)=\frac{1}{W_1 L_1}\left[A_\beta^2+\frac{4A_{VT}^2}{V_{OV1}{}^2}\right] \tag{4.33}$$

where W_1 and L_1 are the width and the length of the common source (CS) transistor M_1 implementing the unit current source (Fig. 4.22a), V_{OV1} its overdrive voltage and A_β and A_{VT} the technology parameters accounting for the random variation of the current factor $\beta=\mu_n C_{ox} W_1/L_1$ and the threshold voltage V_T respectively. At this point it should be noted that the contribution of the common-gate (CG) transistors M_2 to the current mismatch can be neglected if the output resistance of the CS transistors is large.
Eq. (4.33) shows that the variance of the relative current mismatch of two adjacent MOS transistor can be minimized by enlarging the area of M_1 and/or by increasing the overdrive voltage V_{OV1}. While the first condition increases the chip area (i.e. the chip cost), the upper value of the latter is limited by the fact that M_1 must operate in saturation ($V_{DS1}>V_{OV1}$). A value of 0.4 V for V_{OV1} was chosen as trade-off between low mismatch and operation of M_1 in the saturation region.
Assuming the switches as ideal, i.e. the voltage drop across them is negligible, a total voltage of $V_{DD}/2$=0.6 V is available for the V_{DS} of both the CS and the CG transistors. The larger part of this voltage, 0.45 V, was allocated for the drain-source voltage of the CS transistor. This is required to guarantee a large output resistance of the current source. The residual 0.15 V are used by the CG transistor. The drain-source voltages of M_1 and M_2, V_{DS1} and V_{DS2}, are selected by biasing the gates with an appropriate voltage. M_2 was dimensioned so that the unit current defined in (4.32) and the V_{DS2} of 0.15 V bias the transistor with an overdrive voltage V_{OV2}=0.1V, that is, in saturation. This further enhances the output resistance of the current source. The operating point of the DAC transistor is summed up in Tab. 4.10.

Transistor	V_{OV}	V_{DS}	I_{DS}
M_1	0.4 V	0.45 V	16.66µA
M_2	0.1 V	0.15 V	16.66µA

Tab 4.10. Biasing voltages and currents of the transistors of the current source

The overdrive voltage of 0.4 V for transistor M_1 is small enough to neglect the contribution of the β factor to the current mismatch in (4.33). According to (4.33), for a transistor area $A_1=W_1L_1$ of 1250 µm^2 and assuming A_{VT}=5.2 mV·µm a relative standard deviation of the unit current I_u of 0.073% results. For the technology used, under the bias conditions in Tab. 4.10, a W/L ratio of 0.5 is need for transistor M_1 to provide the required unit current, resulting in following dimensioning of the CS transistor (M_1): W_1=25µm L_1=50µm.

Since the current mismatch leads to an INL which varies randomly, a model is needed to estimate the yield of the DAC, defined as the percentage of the DAC fulfilling a given INL specification. By N-bit accuracy the maximum tolerable INL is:

$$INL_{\max}=\frac{LSB}{2}=2^{-(N+1)} \tag{4.34}$$

Analytical models exist in the literature for the estimation of the yield ([Van00], [Lak86], [Lak88]). However, these models provide only an approximate result of the yield and are not sufficiently accurate. A better way for yield estimation is represented by Monte Carlo simulations. MATLAB® code was written to perform 10.000 simulations for each random generated vector composed of 13 unit current sources. Each current sources has a threshold voltage:

$$V_T = V_{T0} + \Delta V_{T,rand} = V_{T0} + \frac{A_{VT}}{\sqrt{W_1 L_1}} \cdot randn \tag{4.35}$$

where V_{T0} is the nominal threshold voltage (0.22 V for large transistors according to simulations), $\Delta V_{T,rand}$ the random component of V_T and *randn* is a normally distributed random number with zero mean and unit standard deviation. The unit current together with its random variation was calculated with the current equation in saturation:

$$I_u = \mu_n C_{ox} \frac{W_1}{2L_1}\left(V_{GS} - V_T\right)^2 = \mu_n C_{ox} \frac{W_1}{2L_1}\left(V_{OV1} - \Delta V_{T,rand}\right)^2 \tag{4.36}$$

The W_1/L_1 ratio was set to 0.5 according to the required current and overdrive voltage, the product $\mu_n C_{ox}$ was obtained after transistor level simulations of the transistor M_1 under the biasing conditions given in Tab. 4.10.

The Monte Carlo simulation shows a yield of 80% for the required accuracy of 11.5 bit. In other words, 80% of the 10.000 random generated DAC exhibit an INL, which is better than LSB/2, where LSB=1/2$^{11.5}$.

4.5.2. Signal depending DAC non-linearity

A systematic INL error is caused by the signal-depending output resistance of the DAC. The signal-depending INL is, expressed in LSB [Raz95]:

$$INL = \frac{nR_L}{4r_0} 2^N \tag{4.37}$$

where n=13 is the total number of unit current sources, R_L the DAC load resistance seen at the integrator virtual ground, r_0 the output resistance of a unit current source and N the required accuracy of the DAC. The demonstration of (4.37) is reported in Appendix B.

The available voltage of only 600 mV for the Cascode current sources is nevertheless sufficient to bias both the CS and CG transistors in saturation, ensuring an output resistance r_0 of 2 MΩ, which is large enough to suppress any non-linearities due to code-depending output resistance. By substituting a simulated R_L of 13.3 Ω, a value of 0.08 LSB for a required accuracy of 12-bit is obtained.

4.5.3. Dynamic behavior of the DAC

Dynamic errors such as glitches are also of great importance, as these are directly added at the modulator input. These errors are generated by capacitive coupling of the switching square-wave to the output through parasitic capacitance of the switches as well as by low crossing point of the switching scheme [Fal99]. The first issue can be reduced by means of low swing control signals of the DAC switches, generated by an appropriate driver. The latter by synchronizing the switching signals, so that the steering switches are never simultaneously off. The driver circuit used is an all-p-mos driver [Fal99], which allows a relatively process-independent crossing point of the control signals (Fig. 4.23). Thirteen driver stages as that in Fig. 4.23 drive the gates of the switching transistors of the main DAC unit current sources.

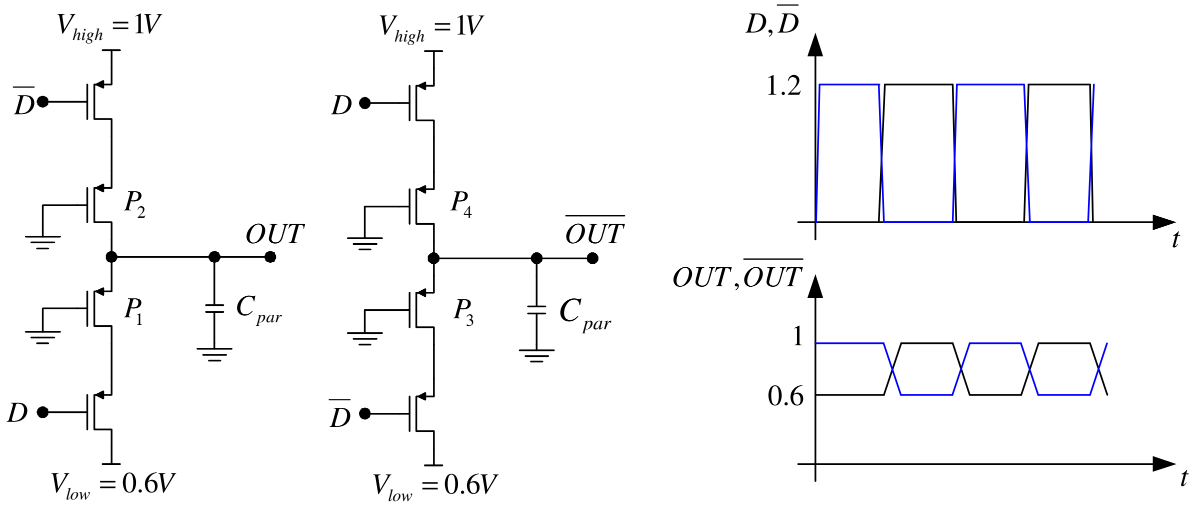


Fig. 4.23. Left: all p-mos driver, right: data and driving signals waveforms

In our implementation all pmos have the same size, hence the crossing point is roughly in the middle between V_{low}=0.6V and V_{high}=1V, that is, at approximately 0.8 V. This voltage is sufficient to keep both switches of the current source in the on state at the transition point. Transistors P_1–P_4 are used to avoid capacitive coupling of the full-swing digital signal to the driver output.

Switches. To improve the dynamic behavior of the DAC the size of the switches is of primary importance. The length is chosen to be minimal in order to reduce the on-resistance and the parasitic capacitance of the switches. In particular, the gate-drain capacitance of the switches is responsible of capacitive coupling of the switching control signal to the DAC output and must be kept as low as possible [Bas98]. The width is selected according to a trade-off: a larger width reduces the on-resistance but increases the parasitic capacitance. Hence, the DAC switches were sized as in the following: W=10µm, L=0.12µm.

Common-gate transistors. The CG transistor M_2 (Fig. 4.22a) is sized according to the required DC-working point (Tab. 4.10) and taking into account the frequency of the pole generated at the drain node of the CS transistor:

$$s_{p2} \cong \frac{g_{m2}}{C_{gs2}} \tag{4.38}$$

where g_{m2} is the transconductance and C_{gs2} the gate-source capacitance of the transistor M_2. If the CG transistor works in saturation, neglecting the channel-length modulation and the body-effect, the W/L ratio is known once its current and overdrive voltage V_{OV2} are defined (Tab. 4.10):

$$\frac{W_2}{L_2} \cong \frac{2I_D}{\mu_n C_{ox} V_{OV2}^2} = const \tag{4.39}$$

Clearly, if W_2 is increased also L_2 must grow proportionally, causing a quadratic growth of the parasitic capacitance C_{gs2} with detrimental effect on s_{p2}:

$$C_{gs2} \propto W_2 L_2 \propto W_2^2 \tag{4.40}$$

On the other hand g_{m2} remains constant:

$$g_{m2} = \frac{\partial I_D}{\partial V_{GS}} \cong \frac{\mu_n C_{ox}}{2} V_{OV2} \frac{W_2}{L_2} = const \tag{4.41}$$

Shortly, the frequency of the pole s_{p2} is maximized if W_2 (and L_2) are minimized. A lower limit for the CG transistor width and length is put by matching considerations. Following values were chosen: W_2=1.5µm, L_2=0.36µm.

4.5.4. Bias circuit

The DAC currents must be matched to the input resistor of the modulator R_1 to avoid gain errors in the A/D conversion. To suppress temperature drifts and mismatches the DAC currents were generated by means of a regulated circuit providing a current proportional to a reference resistance R_{REF} (Fig. 4.24). The opamp is a simple differential pair with input nmos and pmos loads and single-ended output. The resistor R_{REF} has a value of 30 kΩ and is laid out with the input resistor of the modulator in an interdigitated way to maximize the matching and the guarantee the same temperature. The current generated by the biasing circuit is:

$$I_{OUT} = \frac{V_{REF}}{R_{REF}} \tag{4.42}$$

The required DAC currents are obtained by mirroring I_{OUT}. A Miller capacitor C_C of 1 pF was used to guarantee sufficient phase margin of the two stage amplifier in feedback configuration. The second stage of the amplifier is the pMOS transistor in series with R_{REF}.

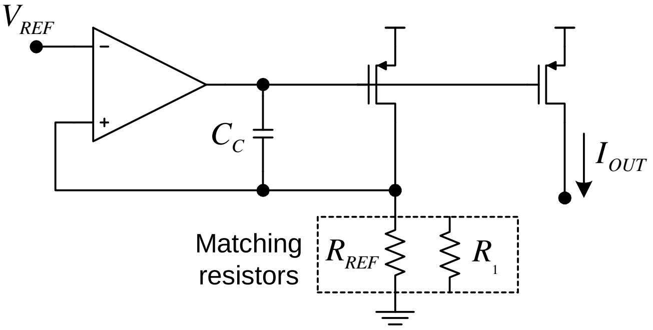
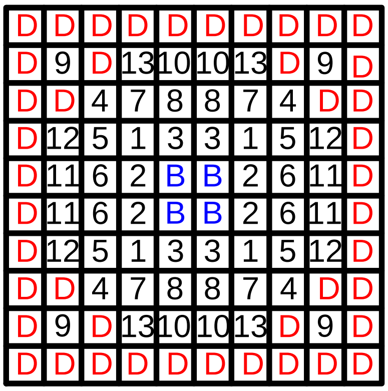


Fig. 4.24. Bias circuit for the generation of the DAC currents

4.5.5. Layout

In order to suppress systematic errors due to the large layout area, such as doping, temperature and stress gradients, a common-centroid structure is used. Each unit current source is split into four parts and laid out with central symmetry (Fig. 4.25). The array of current sources is surrounded by dummy transistors to avoid edge effects. No additional area is needed for the interconnect lines, as these are laid out directly above the current source transistors (Fig 4.26).



D	D	D	D	D	D	D	D	D	D
D	9	D	13	10	10	13	D	9	D
D	D	4	7	8	8	7	4	D	D
D	12	5	1	3	3	1	5	12	D
D	11	6	2	B	B	2	6	11	D
D	11	6	2	B	B	2	6	11	D
D	12	5	1	3	3	1	5	12	D
D	D	4	7	8	8	7	4	D	D
D	9	D	13	10	10	13	D	9	D
D	D	D	D	D	D	D	D	D	D

Fig. 4.25. Layout of the current sources of the main DAC. B=Bias current source, D=dummy transistor, numbers denote current sources

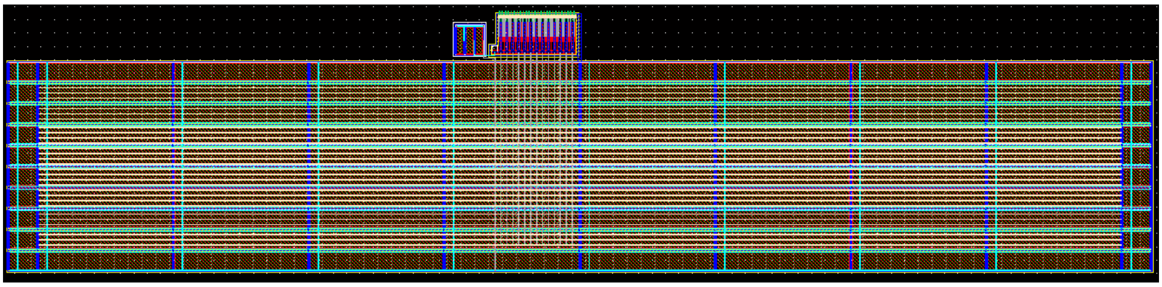


Fig. 4.26. Layout of the main DAC

4.5.6. DAC circuit noise

The DAC circuit noise is added directly at the modulator input without shaping and is thus a large contributor to the total circuit noise of the modulator. The Flicker noise contribution can be neglected, since the area of the common-source transistors is very large. Considering only the thermal noise of the channel, the total DAC output *rms* noise current is:

$$\sqrt{\overline{i_{nDAC}^{2}}} = \sqrt{n \cdot f_B \frac{8}{3} kT g_{mCS}} \tag{4.43}$$

where n is the number of unit current sources, f_B the signal bandwidth and g_{mCS} the transconductance of the common-source transistors generating the DAC unit currents. Replacing n=13, f_B=12.5MHz and the simulated g_{mCS}=71.7µS, an *rms* output noise current of 11.3nA is obtained. Referring this *rms* current to the modulator input the thermal SNR, when only the DAC thermal noise is present, is:

$$SNR_{th,DAC} = 10 \log \frac{2V_{FS}^{2}}{\overline{i_{nDAC}^{2}} \cdot R^{2}} \tag{4.44}$$

where R is the 3kΩ input resistor of the modulator and V_{FS} the amplitude of the full-scale single-ended input signal. Substituting V_{FS}=0.325 a thermal SNR of 82.6 dB, i.e. 13.4 bit is obtained. This value is much lower than the aimed modulator resolution and can therefore be neglected. Also the constant current sources, which are used to get a bi-directional DAC characteristic, contribute to the thermal noise budget. The output noise current is:

$$\sqrt{\overline{i_{nFIX}^2}} = \sqrt{2 f_B \frac{8}{3} kT g_{mFIX}} \tag{4.45}$$

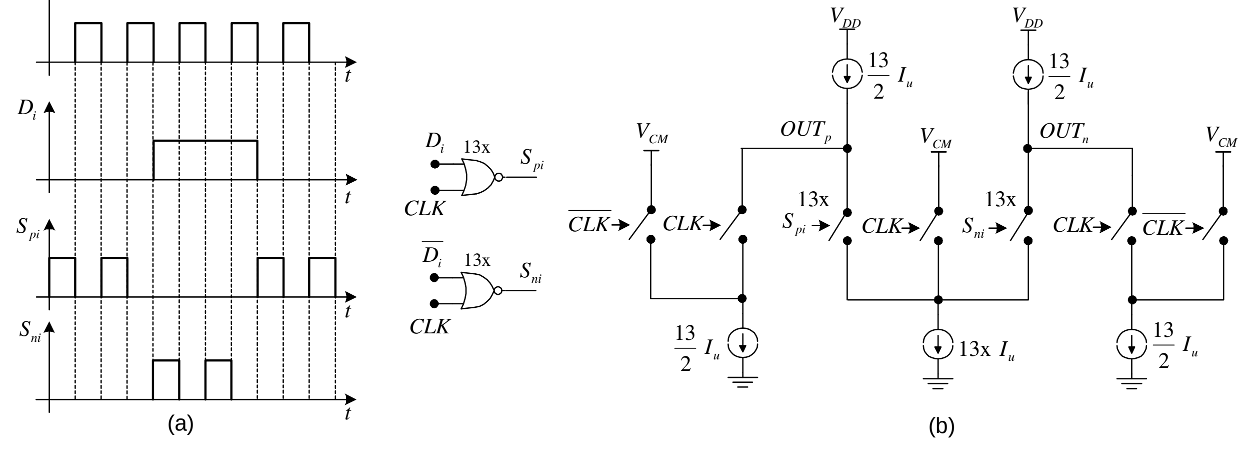
where the factor two accounts for the differential implementation and g_{mFIX} of the transconductance of the CS transistors generating the constant currents. For a simulated g_{mFIX}=1.45 mS an *rms* noise current of 20nA is obtained. Again, referring the noise current to the modulator input the thermal SNR is calculated:

$$SNR_{thFIX} = 10\log\frac{2V_{FS}^2}{\overline{i_{nFIX}^2}\cdot R^2} \tag{4.46}$$

According to (4.46) a thermal SNR of 77.7 dB, i.e. a resolution of 12.6 bit, due to the fixed current sources of the main DAC is achieved.

4.6. Secondary RZ-DAC

The linearity and dynamic requirements of the secondary RZ-DAC are relaxed in comparison with the main DAC. In fact, all errors introduced by the secondary DAC are 2nd order shaped by the first two integrators of the loop filter. This allows saving area, since the tolerable mismatch is some orders of magnitude larger than that of the main DAC, and complexity, as simple CS transistor without cascoding are sufficient to guarantee the required linearity. Furthermore, since the glitches are 2nd order shaped as well, no driver circuit for the generation of the switching signals was provided. The schematic of the secondary RZ-DAC is depicted in Fig. 4.27 together with the timing diagram for a given datum D_i from the quantizer. NOR gates are used for the generation of the RZ switching control signals S_{pi} and S_{ni}. Two fixed current sources feed a constant current of 13/2 times the unit current in order to ensure a bidirectional DAC characteristic. When the clock signal is high no current is drained by the unit current sources; nevertheless these are never switched off to avoid peaking and long rise and fall time of the current output waveform. The unit currents are instead redirected to a constant potential $V_{CM}=V_{DD}/2$. To ensure a zero output current in this phase a constant current equal to $13/2\cdot I_u$ is drained by two additional current sources, which equalizes the current fed by the constant sources.



(a) (b)

Fig. 4.27. Secondary RZ-DAC: a) timing diagram, b) control logic and DAC schematic

The current source transistors have a width of 6.5µm and a length of 13 µm, drain a unit current of 13.6µA and are biased with an overdrive voltage of 0.36V. No Cascode transistors were used for the unit current sources.

4.7. Clock generation

Eight different phases of the main clock are generated with the circuit shown in Fig. 4.28. The non-overlapping phases *φ1* and *φ2* with their inverted replicas are used in the switched capacitor network of the quantizer.

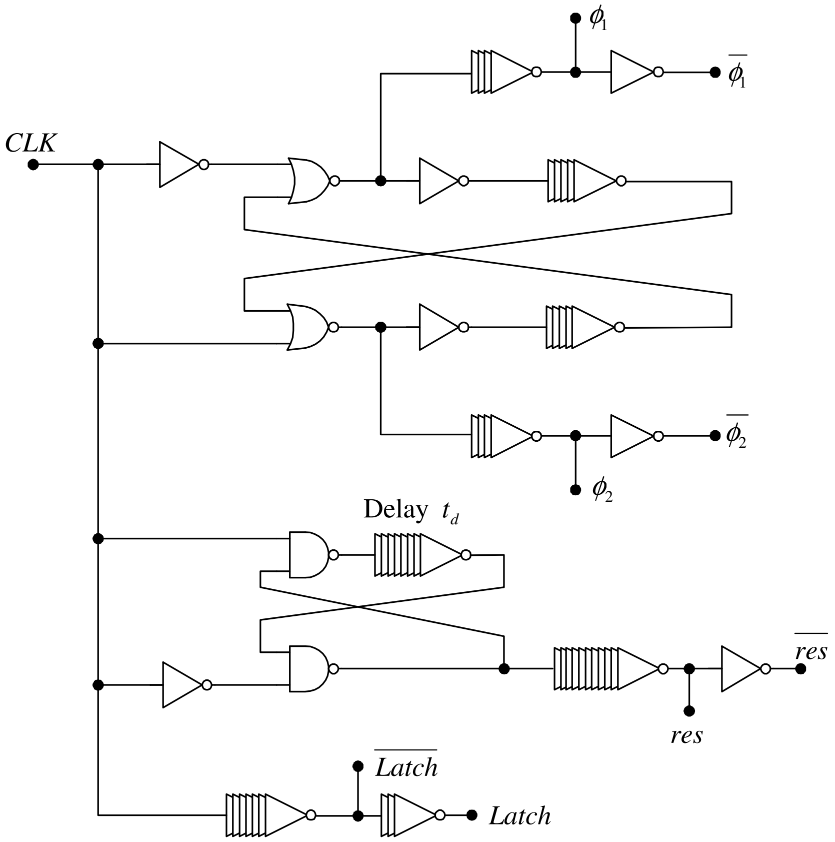


Fig. 4.28. Circuit for clock generation

The quantizer decision is performed when the *res* phase is low. The *res* waveform has a duty-cycle which is larger than 50%. This was obtained by delaying the falling edge of the *res* signal without shifting the rising edge (Fig. 4.29). The reason for this is the following: since the implemented loop filter shows a delay when compared with the ideal filter because of its parasitic capacitances, the decision time (falling edge) was postponed of t_d=500 ps. The time shift was estimated by simulating the step response of the loop filter with extracted parasitic capacitances. In contrast, the reset time of the cross-coupled latch (rising edge) and the time at which the output D-flip flops provide the quantizer output were not shifted. The *res* waveform with delayed falling edge was realized with the cross-coupled circuit in Fig. 4.28 where the delay element consists of eight inverters with different transistor lengths.

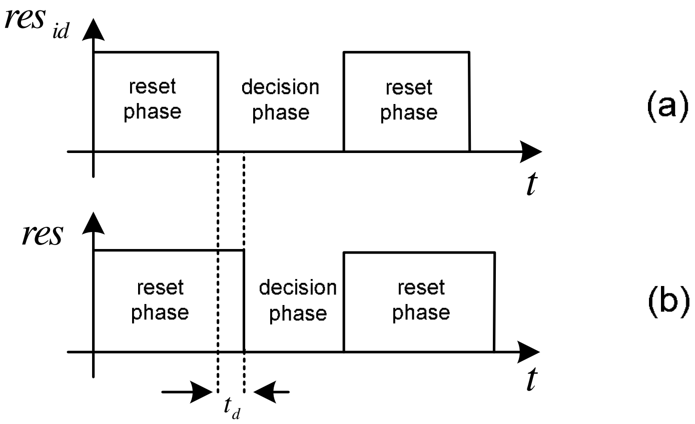


Fig. 4.29. Waveform of the quantizer reset phase: a) ideal phase, b) modified phase with delayed falling edge

Large buffers were used as final stages of the eight clock phases to ensure steep edges of the clock signals and reduce delays.

4.8. Modulator layout

The modulator layout measures 500x470 μm^2 without pads and is depicted in Fig. 4.30. The layout was designed with particular attention to the delay issues. At a clock frequency of 400 MHz the clock period is only $T_s = 2.5$ ns. Hence, a delay of just 250 ps because of parasitic resistances and capacitances of the metal interconnections causes already an excess loop delay of 10% of the clock period, jeopardizing the stability of the modulator. This issue is particularly severe in the path between the quantizer output and the inputs of the main and secondary DAC. In order to cope with this, following approach was adopted: reduction of the parasitic capacitance of the long metal paths by using the top level metal layer; use of large buffers at the output of the quantizer to drive these paths; anticipation of the clock phase of the latches after the comparator to compensate the parasitic induced delay. Furthermore clock skew of the latches at the quantizer output is of primary importance, since this causes signal depending delay. This effect was reduced by using metal interconnections of equalized length for the clock lines.

All differential components (transistors, capacitors and resistors) were split in two or more subparts and laid out using the common-centroid technique to minimize the systematic mismatch. All sensitive components were surrounded by dummy replicas to minimize edge effects.

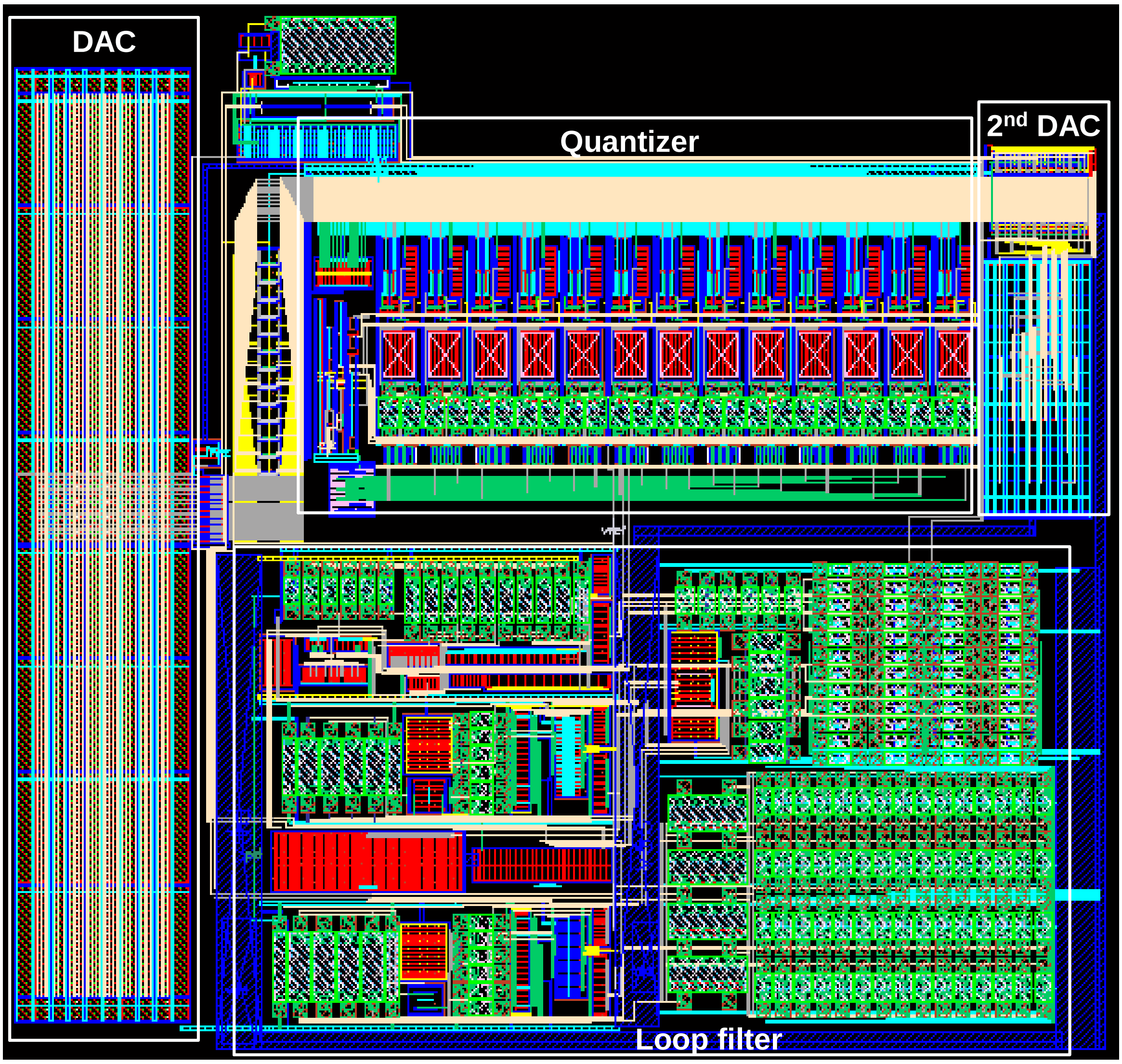


Fig. 4.30. Modulator layout. The main blocks are highlighted.

4.9. Post-layout simulation results

This section summarizes the post-layout simulation results. The parasitic capacitors were extracted from the layout with the Assura® RCX Extraction tool. To reduce the number of the extracted capacitors, i.e. to keep the simulation time to an acceptable level, the filtering option MinC=0.1fF was activated, which suppress all capacitors smaller then 0.1fF. This is a very small value and has a negligible impact on the simulation results.

The modulator was simulated with a differential input sine signal with a frequency of 1.5625 MHz, a single-ended amplitude of 0.25 V, i.e. -2.3dB$_{FS}$, and a DC level of 0.6 V. The output spectrum, obtained by means of the FFT of 32768 output samples, is plotted in Fig. 4.31. An SNDR of 70.4 dB (i.e. en ENOB of 11.4 bits) is achieved in the signal bandwidth of 12.5 MHz.

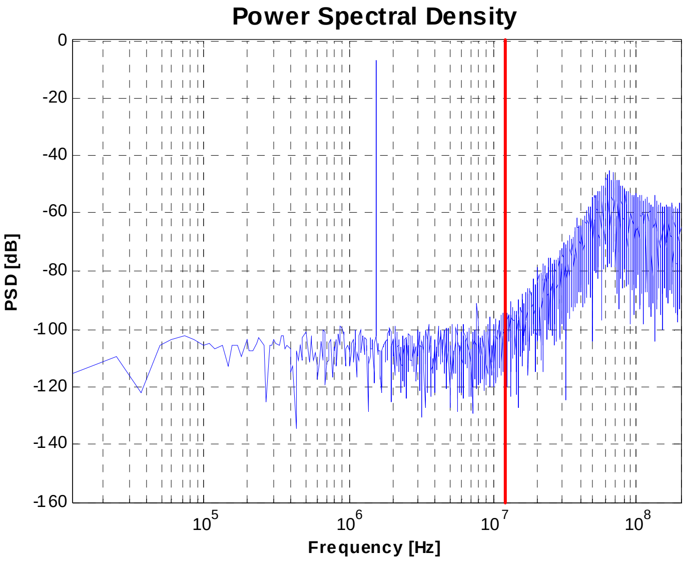


Fig. 4.31. Output spectrum for V_{in}=-2.3dB$_{FS}$ @ 1.5625 MHz according to post-layout simulations

Fig. 4.32 plots the SNR and SNDR against the amplitude of the input signal in dB$_{FS}$. A dynamic range of 71.8 dB is obtained.

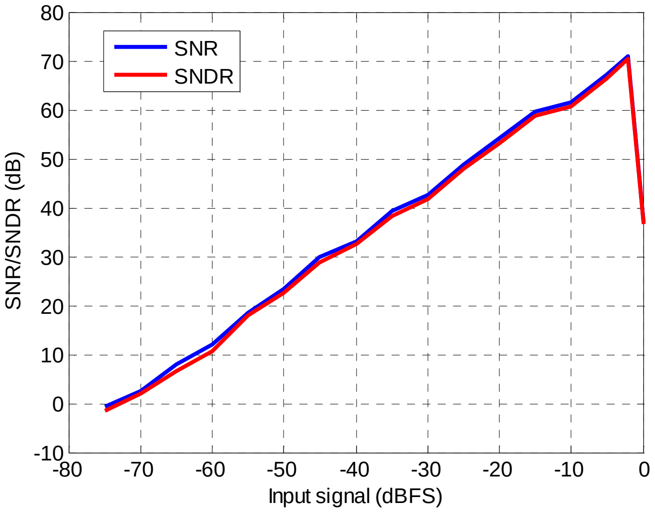


Fig. 4.32. SNR and SNDR as function of the input signal amplitude. The input signal is a sine waveform with a frequency of 1.5625 MHz (post-layout simulation)

The main modulator parameters and post-layout simulation results are summarized in Tab. 4.11.

Parameter	**Value**
Signal bandwidth (f_B)	12.5 MHz
Sampling frequency (f_S)	400 MHz
Oversampling Ratio (OSR)	16
Total power consumption (P)	11.3 mW
Signal-to-noise-and-distortion ratio (SNDR)	70.4 dB
Signal-to-noise ratio (SNR)	70.9 dB
Effective Number Of Bits (ENOB)	11.4 bits
Dynamic range (DR)	71.8 dB
Maximum stable amplitude (MSA)	-2.3 dB$_{FS}$
Process technology	0.13 µm CMOS
Chip area	500 x 470 µm^2

Tab 4.11. Main parameters of the modulator

4.10. Corner simulations

Corner post-layout simulations were performed in order to analyze the modulator behavior in presence of variation of the temperature and the supply voltage. The results are depicted in Tab. 4.12. An ENOB of at least 11.5 bits is achieved in the whole temperature range when using a supply voltage of 1.3V or more. At 1.2V the ENOB is 10.5 bits at a temperature of 80°C. At 1.1V the modulator gets unstable at high operating temperatures and can therefore not be used at this low supply voltage.

	V_{DD}=1.1V		**V_{DD}=1.2V**		**V_{DD}=1.3V**		**V_{DD}=1.4V**	
Temp.	**SNR**	**SNDR**	**SNR**	**SNDR**	**SNR**	**SNDR**	**SNR**	**SNDR**
-40°C	66.7	66.3	75.6	74.8	76.3	76.1	75.1	74.9
27°C	63.1	61.2	70.9	70.4	75.1	74.3	75.8	75.0
80°C	38.0	35.0	66.5	65.1	71.5	70.9	76.0	75.1

Tab 4.12. Corner post-layout simulations

4.11. Estimated total circuit noise

The total circuit noise was estimated by considering the four main contributors to the overall noise: the input resistors, the 1st opamp, the main DAC and the constant current sources of the main DAC. The singular values were calculated previously. Assuming all noise sources are uncorrelated, following total noise results:

$$SNR_{th,tot} = 10\log\frac{2V_{FS}^2}{\left(\overline{i_{nDAC}^2} + \overline{i_{nFIX}^2}\right)R^2 + \overline{v_{nR}^2} + \overline{v_{nOTA1}^2}} \qquad (4.47)$$

Replacing the input-referred noise sources of the four main contributors as in (4.43), (4.45), (3.50) and (4.25) a total thermal SNR of 71.8 dB is obtained, that is, a thermal ENOB of 12.2 bit. This value is about one bit higher than the resolution achieved after post-layout simulations. Hence, no significant worsening of the output spectrum in Fig. 4.31 because of thermal noise is expected.

Chapter 5

Conclusions and future work

5.1. FOM and comparison with state of the art

In order to compare the result of this work with the state of the art present in the literature we introduce following figure of merit (FOM):

$$FOM = \frac{P}{2^{ENOB} 2 f_B} \tag{5.1}$$

where P is the power consumption, $ENOB$ the effective number of bits and f_B the signal bandwidth. Smaller values of FOM mean a better figure of merit.

Inserting the values for the proposed modulators: f_B=12.5 MHz, ENOB=11.4 bit, P=11.3 mW, an excellent FOM of 0.17 pJ per conversion step is obtained, second only to [Mit06].

Tab. 5.1 compares the main parameters, such as clock frequency, signal bandwidth, resolution, power and the FOM of recent wideband continuous-time modulators with a signal bandwidth of at least 2 MHz. It should be highlighted that, while the other modulators in the comparison provide measurement results (except for [Sch05]), post-layout simulation results are used for the proposed modulator. Nevertheless we do not expect a significant worsening of the performance after chip fabrication; firstly, the noisy circuit elements were dimensioned to keep the thermal noise under the quantization noise floor of the simulated spectrum as explained in section 4.11; secondly, the mismatch-caused DAC non-linearity is expected to be lower than the achieved resolutions, as the DAC was dimensioned to fulfill this specification.

Paper	f_S (MHz)	f_B (MHz)	SNDR (dB)	SNR (dB)	DR (dB)	Power (mW)	FOM (pJ/step)	CMOS process
[Mit06]	640	20	74	76	80	20	0.12	130nm
[Shu08]	256	8	70	76	81	50	1.21	65nm
[Str08]	950	10/20	72/67	86/75	N/A	40	0.61/0.55	130nm
[Wen08]	640	10	82	84	87	100	0.49	180nm
[Dha09]	250	20	60	62	68	10.5	0.32	65nm
[Par09]	900	20	78.1	81.2	80	87	0.33	130nm
[Kim09]	250	10	65	68	71	18	0.62	130nm
[Bre07]	340	20	69	71	77	56	0.61	90nm
[Bre04]	160	10	55	63	67	68	7.4	180nm
[Pat04]	300	15	63.7	64.6	67	70	1.85	130nm
[Van02]	154	2	68	70	70	11.5	1.4	180nm
[Dör05]	104	2	71	72	N/A	3	0.26	130nm
[Cal06]	100/200	10/20	57/49	58/50	61/55	87	7.5/9.4	180nm
[Yag05]	276	23	69	70	72.5	46	0.43	180nm
[Sch07]	640	10	66	N/A	72	7.5	0.23	180nm
[Sch05][7]	1000	8	63.4	63.5	N/A	10	0.54	90nm
This work[8]	**400**	**12.5**	**70.4**	**70.9**	**71.8**	**11.4**	**0.17**	**130nm**

Tab 5.1. Main performance parameters of CT high-bandwidth, low-power ΣΔ modulators

A graphical representation of the FOM against the signal bandwidth, the SNDR and the power consumption is plotted in Fig. 5.1 for the modulators of Tab. 5.1.

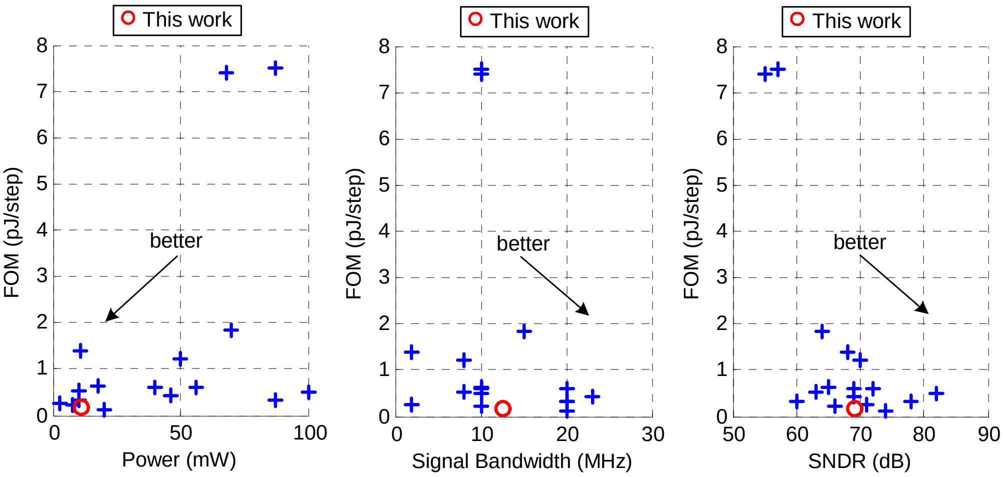


Fig. 5.1. FOM of the modulators in Tab. 5.1 against power, signal bandwidth and SNDR

5.2. Future work: DEM or DAC analog calibration

To reduce the chip area and/or improve the DAC linearity additional circuits could be implemented in the future. Digital Element Matching (DEM) techniques such as Data Weighted Averaging (DWA) or pseudo DWA [Ham04] are usually used for the dynamic selection of the mismatching DAC elements according to special algorithms (rotation of the selected elements or similar). These circuits largely improve the DAC linearity by suppressing the harmonics generated by the DAC INL. The main drawback of such circuits is the additional delay introduced in the path between the quantizer output and the DAC, because of the latency of the switching network selecting the DAC elements. In high speed solutions, such as the modulator proposed in this work, this could lead to system instability; furthermore DEM circuits lose effectiveness at low OSR.

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[7] ELDO™ simulation results

[8] Spectre® Post-layout simulation results

A good alternative to DEM is represented by analog calibration circuits ([Gro89], [Yan04]). They work according to the following principle: each current source is separated from the DAC after a defined time and calibrated with the aid of a reference current. By adding one spare current source to the DAC the calibration can be performed without interruption of the DAC operation, since the current source under calibration is replaced by the additional current source. This type of calibration do not cause additional delay, as the calibration takes place outside the feedback loop of the modulator, and is the ideal solution for high speed, ELD-prone modulators.

5.3. Publications

Following papers were published so far by the author of this work:

- Eugenio Di Gioia and Henrich Klar. *A 11-bit, 12.5 MHz, Low Power Low Voltage Continuous-Time Sigma-Delta Modulator*. Mixed Design of Integrated Circuits and System, IEEE, MIXDES 2010

- Eugenio Di Gioia, Christoph Schwoerer and Heinrich Klar. *A 14-Bit Cascaded 3-2 Sigma-Delta Modulator for VDSL*. 49th IEEE International Midwest Symposium on Circuits and Systems, MWSCAS '06, 6-9 Aug. 2006

- Eugenio Di Gioia, Carsten Hermann and Heinrich Klar. *Design of a LNA in the frequency band 1.8-2.2GHz in 0.13µm CMOS Technology*. Advances in Radio Science, 3, 299–303, 2005

Appendix A

Calculation of the DT equivalent transfer function with the aid of the IIT

In the following the discrete-time equivalent filter of a 3rd order continuous-time filter with a resonator together with an NRZ DAC and a HRZ DAC (Fig. A.1) is calculated against the excess loop delay (ELD), which is normalized to the clock period:

$$\tau_d = \frac{t_d}{T_s} \tag{A.1}$$

Since the CT filter is linear time-invariant the superposition principle can be applied. Hence, the overall impulse response of the system is the sum of two terms:

$$h(t) = h_{NRZ}(t) + h_{HRZ}(t) \tag{A.2}$$

where $h_{NRZ}(t)$ is the impulse response of the system when the HRZ DAC is removed, while $h_{HRZ}(t)$ is the impulse response of the system when the NRZ DAC is removed.

Transforming in the Laplace domain we get:

$$H(s) = H_{NRZ}(s) + H_{HRZ}(s) \tag{A.3}$$

where

$$H_{NRZ}(s) = H_{NRZ,DAC}(s)\frac{V(s)}{X_{NRZ}(s)} \tag{A.3}$$

and

$$H_{HRZ}(s) = H_{HRZ,DAC}(s)\frac{V(s)}{X_{HRZ}(s)} \tag{A.4}$$

The functions $H_{NRZ,DAC}(s)$ and $H_{HRZ,DAC}(s)$ in (A.3) and (A.4) are the Laplace transformations of the impulse responses of the main and the auxiliary DAC respectively. The transfer function of the equivalent DT filter will be calculated by converting (A.3) and (A.4) into the DT equivalents by means of the impulse invariant transformation (IIT) and then summing the discrete-time transfer functions obtained.

To simplify the treatment the integrator coefficients will be normalized to the clock frequency of the modulator. Following substitutions are made:

$$A_1 \to \frac{A_1}{f_s},\ A_2 \to \frac{A_2}{f_s},\ A_3 \to \frac{A_3}{f_s} \tag{A.5}$$

All calculations in the following sections assume that the integrator coefficients are normalized to the clock frequency.

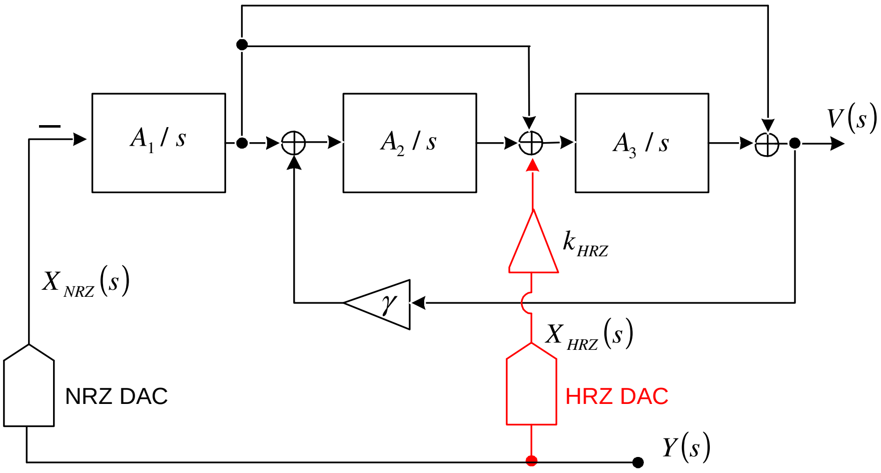

Fig. A.1. CT filter with main DAC and auxiliary DAC for compensation of ELD

A.1 Main DAC

The filter transfer function from the input $X_{NRZ}(s)$ to the output V(s) is:

$$H_1(s) = \frac{A_1}{s}\frac{s^2 + A_3 s + A_2 A_3}{s^2 + \omega_0^2} = \frac{A_1}{s}\frac{s^2 + A_3 s + A_2 A_3}{(s - j\omega_0)(s + j\omega_0)} \tag{A.6}$$

where $\omega_0^2 = \gamma A_2 A_3$ is the resonance frequency of the resonator. Expanding $H_1(s)$ in partial fractions it can be written in the form:

$$H_1(s) = \frac{A}{s} + \frac{B}{s + j\omega_0} + \frac{B^*}{s - j\omega_0} \tag{A.7}$$

The coefficients of the partial fractions are:

$$A = H_1(s)\cdot s\big|_{s=0} = A_1 \frac{A_2 A_3}{\omega_0^2} \tag{A.8}$$

$$B = H_1(s)\cdot(s + j\omega_0)\big|_{s=-j\omega_0} = \frac{A_1}{-j\omega_0}\frac{-\omega_0^2 - jA_3\omega_0 + A_2A_3}{(-2j\omega_0)} = \frac{A_1\left(A_2A_3 - \omega_0^2 - jA_3\omega_0\right)}{-2\omega_0^2} = C_0 - jC_1 \qquad \text{(A.9)}$$

$$B^* = H_1(s)\cdot(s - j\omega_0)\big|_{s=+j\omega_0} = \frac{A_1}{j\omega_0}\frac{-\omega_0^2 + jA_3\omega_0 + A_2A_3}{(2j\omega_0)} = \frac{A_1\left(A_2A_3 - \omega_0^2 + jA_3\omega_0\right)}{-2\omega_0^2} = C_0 + jC_1 \qquad \text{(A.10)}$$

B and B^* are complex and conjugate, C_0 represents their real part $\pm C_1$ their imaginary part. With the aid of the table in [Che02] we can calculate the DT terms having the same sampled impulse response as the partial fractions in (A.7) together with a NRZ DAC with normalized delay τ_d. The delayed NRZ DAC waveform can be conceived as the sum of two pulses: one pulse starts at $t/Ts=\tau_d$ and ends at $t/Ts=1$; the second pulse starts at 1 and ends at $1+\tau_d$ (Fig. A.2a)

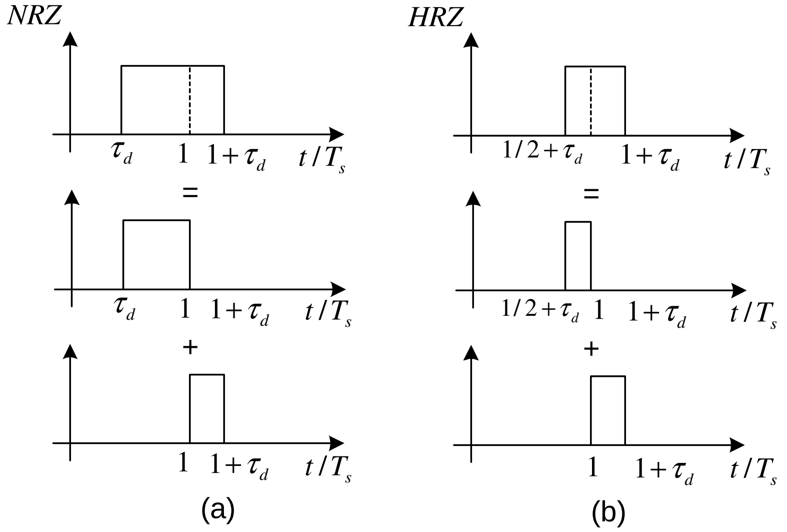

Fig. A.2. Decomposition of the DAC waveforms in two components

$$\frac{A}{s} \Leftrightarrow H_{1,NRZ}(z,\tau_d) = A\left(\frac{1-\tau_d}{z-1} + z^{-1}\frac{\tau_d}{z-1}\right) \qquad \text{(A.11)}$$

$$\frac{B}{s + j\omega_0} \Leftrightarrow H_{2,NRZ}(z,\tau_d) = \frac{B}{-j\omega_0}\left[\frac{e^{-j\omega_0(1-\tau_d)} - 1}{z - e^{-j\omega_0}} + z^{-1}\frac{e^{-j\omega_0} - e^{-j\omega_0(1-\tau_d)}}{z - e^{-j\omega_0}}\right] \qquad \text{(A.12)}$$

$$\frac{B^*}{s - j\omega_0} \Leftrightarrow H_{3,NRZ}(z,\tau_d) = \frac{B^*}{j\omega_0}\left(\frac{e^{j\omega_o(1-\tau_d)} - 1}{z - e^{j\omega_o}} + z^{-1}\frac{e^{j\omega_o} - e^{j\omega_o(1-\tau_d)}}{z - e^{j\omega_o}}\right) \qquad \text{(A.13)}$$

The equivalent discrete time TF for the NRZ input is then:

$$H_{NRZ}(z,\tau_d) = H_{1,NRZ}(z,\tau_d) + H_{2,NRZ}(z,\tau_d) + H_{3,NRZ}(z,\tau_d) \qquad \text{(A.14)}$$

As $H_{1,NRZ}(z,\tau_d)$, $H_{2,NRZ}(z,\tau_d)$ and $H_{3,NRZ}(z,\tau_d)$ do not exhibit the delay term τ_d in the denominator, the same can be stated for $H_{NRZ}(z,\tau_d)$, which is the sum of (A.11), (A.12) and (A.13).

A.2 Auxiliary DAC

The filter TF from the input $X_{HRZ}(s)$ to the output $V(s)$ is:

$$H_2(s)=\frac{V(s)}{X_{HRZ}(s)}=\frac{k_{HRZ}A_3 s}{s^2+\omega_0^2}=\frac{k_{HRZ}A_3 s}{(s-j\omega_0)(s+j\omega_0)} \tag{A.15}$$

Expanding $H_2(s)$ in partial fractions it can be written in the form:

$$H_2(s)=\frac{C_1}{s+j\omega_0}+\frac{C_2}{s-j\omega_0} \tag{A.16}$$

The coefficients of the partial fractions are:

$$C_1=H_2(s)\cdot(s+j\omega_0)\big|_{s=-j\omega_0}=\frac{k_{HRZ}A_3}{2} \tag{A.17}$$

$$C_2=H_2(s)\cdot(s-j\omega_0)\big|_{s=+j\omega_0}=\frac{k_{HRZ}A_3}{2}=C_1=C \tag{A.18}$$

Both residues are identical and were renamed as C. The delayed HRZ DAC is decomposed in two pulses: one pulse starts at $t/T_s=0.5+\tau_d$ and ends at $t/T_s=1$; the second pulse starts at 1 and ends at $1+\tau_d$ (Fig. A.2b). The DT equivalents of the partial fractions are:

$$\frac{C}{s+j\omega_0}\Leftrightarrow H_{1,HRZ}(z,\tau_d)=\frac{C}{-j\omega_0}\left[\frac{e^{-j\omega_0(1/2-t_d)}-1}{z-e^{-j\omega_0}}+z^{-1}\frac{e^{-j\omega_0}-e^{-j\omega_0(1-t_d)}}{z-e^{-j\omega_0}}\right] \tag{A.19}$$

$$\frac{C}{s-j\omega_0}\Leftrightarrow H_{2,HRZ}(z,\tau_d)=\frac{C}{j\omega_0}\left[\frac{e^{j\omega_o(1/2-t_d)}-1}{z-e^{j\omega_o}}+z^{-1}\frac{e^{-j\omega_0}-e^{-j\omega_0(1-t_d)}}{z-e^{j\omega_0}}\right] \tag{A.20}$$

Finally, the DT equivalent of the HRZ DAC and the filter is:

$$H_{HRZ}(z,\tau_d)=H_{1,HRZ}(z,\tau_d)+H_{2,HRZ}(z,\tau_d) \tag{A.21}$$

Adding (A.19) with (A.20) and using Euler's trigonometric formulas following result is obtained:

$$H_{HRZ}(z,\tau_d)=\frac{k_{HRZ}A_3}{\omega_0}\frac{\sin\left[\omega_0\left(\frac{1}{2}-\tau_d\right)\right]z^2-\left\{\sin[\omega_0(1-\tau_d)]-\sin\left[\omega_0\left(\frac{1}{2}+\tau_d\right)\right]\right\}z-\sin(\omega_o\tau_d)}{z\left(z^2-2z\cos\omega_0+1\right)} \tag{A.22}$$

As in the case of $H_{NRZ}(z,\tau_d)$ also $H_{HRZ}(z,\tau_d)$ does not contain any delay term in the denominator, since the discrete-time equivalent transfer functions of the partial fractions have τ_d-independent denominators.

A.3 DT equivalent

The transfer function of the discrete-time equivalent of the system in Fig. A.1 is:

$$H_d(z,\tau_d) = H_{NRZ}(z,\tau_d) + H_{HRZ}(z,\tau_d) \tag{A.23}$$

Since the delay term τ_d has no effect on the denominator except for a delay term z, also $H_d(z,\tau_d)$ will have the form:

$$H_d(z,\tau_d) = \frac{N_H(z,\tau_d)}{z\left(z^2 - 2z\cos\omega_0 + 1\right)} \tag{A.24}$$

The effect of ELD on the system in Fig. A.1 can thus be summarized as follows: coefficient mismatch in the numerator and increase of the order of the equivalent DT filter because of the z term in the denominator.

Appendix B

Calculation of the INL of the DAC

A systematic INL error is due to the signal-depending output resistance of a current-mode DAC [Raz95]:

$$INL = \frac{nR_L}{4R_{OUT}} \tag{B.1}$$

where n is the total number of unit current sources, R_L the DAC load resistance and R_{OUT} the DAC output resistance. To demonstrate this we model each current source with its small-signal equivalent circuit (Fig. B.1).

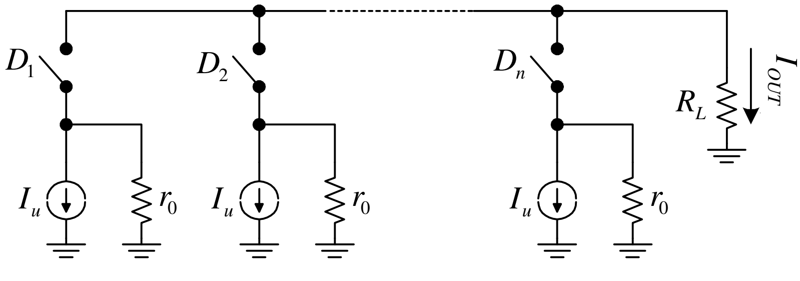

Fig. B.1. Small-signal equivalent circuit of a multi-bit current DAC

The actual value of the DAC output resistance depends on the number of current sources which are switched on (Fig. B.1). The maximum current that can be provided by the DAC to the load is obtained when all sources are switched on:

$$I_{OUT,\max} = \frac{n \cdot I_u \cdot r_0 / n}{R_L + r_0 / n} = \frac{I_u \cdot r_0}{R_L + r_0 / n} \tag{B.2}$$

To calculate the INL we need to plot the output current against the number of sources which are currently switched on. This problem can be analyzed more easily if we consider this number not as discrete but continuously varying between zero and n. For this purpose we introduce an index x, bounded between zero and one, so that the number of switched sources is equal to $n{\cdot}x$. The current flowing across the load is then:

$$I_{OUT,nl}(x)=\frac{nx\cdot I_u\cdot r_0/nx}{R_L+r_0/nx}=\frac{I_u\cdot r_0}{R_L+r_0/nx} \tag{B.3}$$

Eq. (B.3) shows a non-linear dependence of the load current from the number *nx* of unit currents, which are actually switched on and describes the curve of the non-linear DAC characteristic (Fig. B.2). Replacing (B.2) in (B.3) we obtain:

$$I_{OUT,nl}(x)=I_{OUT,\max}\cdot\frac{R_L+r_0/n}{R_L+r_0/nx} \tag{B.4}$$

The ideal, linear output current is the straight line connecting the origin to $I_{OUT,max}$:

$$I_{OUT,id}(x)=x\cdot I_{OUT,\max} \tag{B.5}$$

Hence, the non linear error is:

$$I_\varepsilon(x)=I_{OUT,nl}(x)-I_{OUT,id}(x)=I_{OUT,\max}\left(\frac{R_L+r_0/n}{R_L+r_0/nx}-x\right)=I_{OUT,\max}R_L\left(\frac{1-x}{R_L+r_0/nx}\right) \tag{B.6}$$

The INL is the maximum of $I_\varepsilon(x)$ normalized to $I_{OUT,max}$ and expressed in LSB. Differentiating (B.6) and equating to zero we get:

$$\frac{\partial I_\varepsilon}{\partial x}=0\;\rightarrow\;x'=\frac{r_0\left(-1+\sqrt{1+\dfrac{nR_L}{r_0}}\right)}{nR_L}\cong\frac{r_0}{nR_L}\left(-1+1+\frac{nR_L}{2r_0}\right)=\frac{1}{2} \tag{B.7}$$

where the approximation holds if $R_L<<\dfrac{r_0}{n}$.

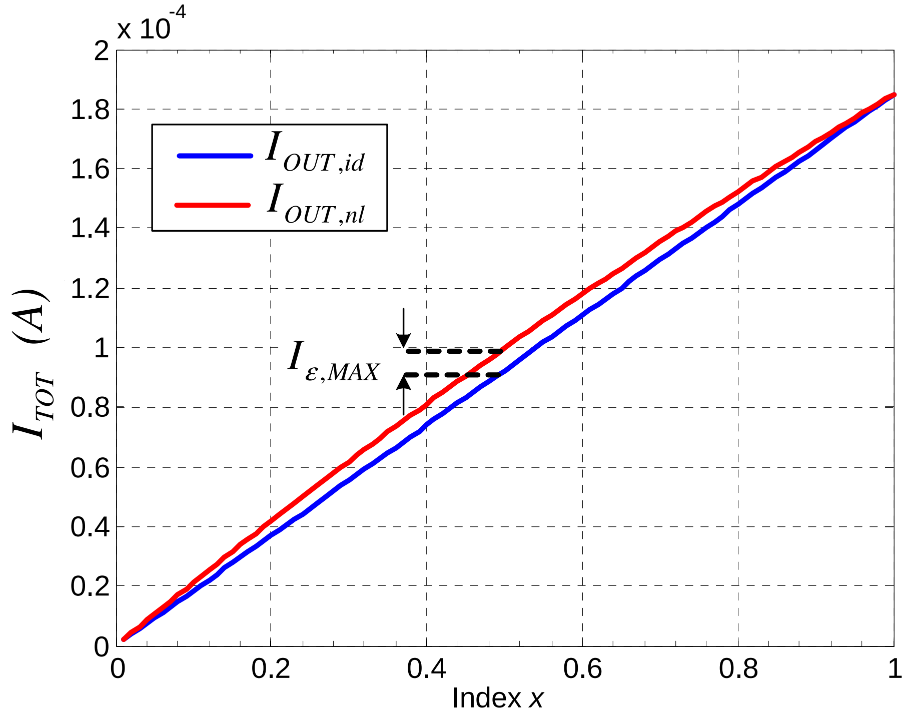

Fig. B.2. Ideal and non-linear static characteristic of a DAC

Replacing the value *x*=1/2 in (B.6) we obtain:

$$I_{\varepsilon,\max} = I_{\varepsilon}(x') \cong I_{\varepsilon}(x)\Big|_{x=1/2} = \frac{1}{2}\frac{nR_L I_{OUT,\max}}{nR_L + 2r_0} \cong \frac{nR_L I_{OUT,\max}}{4r_0} \tag{B.8}$$

By normalizing (B.8) to the maximum current and expressing it in LSB the INL is obtained:

$$INL = \frac{I_{\varepsilon,\max} / I_{OUT,\max}}{LSB} \cong \frac{nR_L 2^N}{4r_0} \tag{B.9}$$

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