An 18-mW 1.175–2-GHz Frequency Synthesizer With Constant Bandwidth for DVB-T Tuners

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***Abstract*—A fully integrated 1.175–2-GHz differentially tuned frequency synthesizer aimed for digital video broadcasting-terrestrial tuners is implemented in a 0.18-μm CMOS process. To maintain phase-noise optimization and loop stability over the entire output frequency range, techniques of constant loop bandwidth are proposed. The voltage-controlled oscillator gain $K_{\rm VCO}$ and band step $f_{\rm res}$ are both maintained by simultaneously adjusting the sizes of switched capacitors and varactors. Charge pump current $I_{\rm CP}$ is programmed to compensate the variation of the division ratio N. The measured results show an in-band phase noise of -97.6 dBc/Hz at a 10-kHz offset and an integrated phase error of 0.63° from 100 Hz to 10 MHz. The measured variations of $K_{\rm VCO}$ and $f_{\rm res}$ are less than 12.5% and 4.5%, respectively. The variations of the measured phase noise at 10-kHz and 1-MHz frequency offsets are less than 1 dB. The measured 3-dB closed-loop bandwidth is 110 kHz and the variation is less than 9%. The chip draws 10-mA current from a 1.8-V supply while occupying a 2.2-mm^2 die area.**

***Index Terms*—Frequency synthesizer, loop bandwidth, loop gain, phase noise, voltage-controlled oscillator (VCO) gain, wideband.**

I. Introduction

THE DIGITAL video broadcasting-terrestrial (DVB-T) standard has ushered in a new era in TV entertainment. Often the DVB-T tuners employ a double-conversion zero-IF (DZIF) architecture, which demands the use of a wideband frequency synthesizer as the first local oscillator (LO) ($\rm LO_1$) to cover the 48–862-MHz-wide frequency range and a fractional-N frequency synthesizer as the second LO ($\rm LO_2$) to support several channel bandwidths (6/7/8 MHz) [1], [2].

There are many challenges in designing a wideband frequency synthesizer $\rm LO_1$. It must achieve a wide frequency tuning range, while providing low phase noise and low integrated phase error. The wideband synthesizer $\rm LO_1$ needs to meet a stringent phase-noise requirement over the entire frequency range, which should be larger than the input range of 814 MHz. An adequate target for the overall phase noise is -87 dBc/Hz at a 10-kHz offset [2]. In addition, because of the very wide frequency range, the synthesizer loop bandwidth, which affects the phase-noise optimization and loop stability, may vary quite significantly due to two reasons. Firstly, to cover such a wideband frequency range and achieve a relatively low voltage-controlled oscillator (VCO) gain ($K_{\rm VCO}$), a switched capacitor array is usually employed in the LC VCO. However, even with a switched capacitor bank, the VCO gain variation is still huge. The phase noise is degraded as the VCO gain increases [3]. Secondly, a large range of division ratio N is required to obtain the wide tuning range of nearly one octave. The N variation also changes the loop bandwidth, thus impacting the phase noise and loop stability.

To achieve a constant loop bandwidth, several methods have been previously proposed [4], [5]. In [4], natural frequency ω_n is used as a definition of the loop bandwidth. To handle the large division ratio range, a sampled loop filter (LPF) network is constructed and an inverse-linear charge pump (CP) is used to keep the natural frequency over reference frequency $(\omega_n/\omega_{\rm ref})$ and the damping factor ζ constant. Though the natural frequency and damping factor are widely used in the analysis of synthesizer loop dynamic, strictly speaking, they are applicable only to second-order loops. The inverse-linear CP also adds design complexity. Reference [5] uses open-loop crossover frequency ω_c as the loop bandwidth and adjusts only the CP current $(I_{\rm CP})$ to compensate the $K_{\rm VCO}$ and N variations. Although the open-loop crossover frequency is often used to define a loop bandwidth, it cannot accurately capture the low-pass corner characteristics of the closed-loop transfer function. In addition, though adjusting $I_{\rm CP}$ alone can achieve a constant loop bandwidth, a multiband VCO with constant and smaller gains is still desired in order to improve the phase-noise performance.

In this paper, the concept of loop gain is used as the loop bandwidth to accurately model the low-pass characteristics of the closed-loop transfer function. Techniques achieving a constant and smaller VCO gain $K_{\rm VCO}$ while obtaining a constant loop bandwidth are proposed [6]. Both a constant $K_{\rm VCO}$ and an equal band step $f_{\rm res}$ are obtained in a multiband VCO. Automatic frequency control (AFC) is used to ensure the operation of VCO in the linear region of the tuning range. The VCO with equal band steps greatly helps to simplify the AFC loop design. Programmable CP current is also adopted to compensate the variation of the division ratio N.

The remainder of this paper is organized as follows. In Section II, design issues of the frequency synthesizer are considered and the loop gain is derived. The $K_{\rm VCO}$ variation in a

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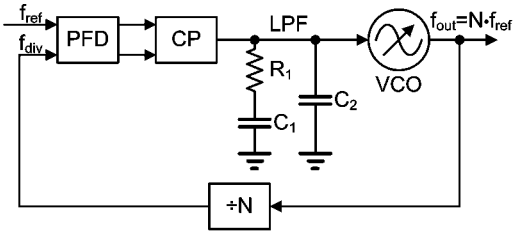


Fig. 1. Block diagram of an integer-N frequency synthesizer with a typical passive LPF.

wideband PLL design is also investigated. Section III proposes techniques to achieve a constant $K_{\rm VCO}$ and loop bandwidth. The circuit implementation is described in Section IV. The experimental results are given in Section V, and finally, Section VI concludes this study.

II. Design Considerations

A. Loop Gain

The phase-locked loop (PLL) loop bandwidth is an important design parameter for minimizing phase-noise variation and guaranteeing loop stability. As mentioned earlier, it is often desired to have a constant loop bandwidth over the entire frequency range.

The block diagram of an integer-N third-order type-II PLL is shown in Fig. 1, which includes a phase-frequency detector (PFD), a CP, a second-order passive LPF, an LC VCO, and a divider. Often the natural frequency ω_n or the open-loop crossover frequency ω_c is used as the loop bandwidth; however, the former is not applicable in third or higher order loops and strongly depends on the damping factor ζ, while the latter cannot capture the low-pass corner characteristics of the closed-loop transfer function. In this paper, the loop gain K is used to model the low-pass corner of the closed-loop transfer function [7], [8]. The open-loop transfer function of a PLL with a general LPF $F_{\rm LPF}(s)$ is expressed as

$$\begin{aligned} G(s) &= \frac{I_{\rm CP}K_{\rm VCO}}{2\pi Ns}F_{\rm LPF}(s) = \frac{I_{\rm CP}K_{\rm VCO}}{2\pi Ns}F_{p+i}(s)F_{\rm hf}(s) \\ &= \frac{I_{\rm CP}K_{\rm VCO}}{2\pi Ns}\left(K_1+\frac{K_2}{s}+\cdots\right)F_{\rm hf}(s) \\ &= \frac{I_{\rm CP}K_{\rm VCO}K_1F_{\rm hf}(0)}{2\pi Ns}\left(1+\frac{K_2}{K_1s}+\cdots\right)\frac{F_{\rm hf}(s)}{F_{\rm hf}(0)} \end{aligned} \quad (1)$$

where $I_{\rm CP}$ is the sink or source current of the CP. The $F_{p+i}(s)$ represents the proportional and integral components of the LPF, and $F_{\rm hf}(s)$ represents the high-frequency components of the LPF. Note that $F_{\rm hf}(0)$ is a finite and nonzero number. Thus, the loop gain K is given by [7]

$$K = \frac{I_{\rm CP}K_{\rm VCO}K_1F_{\rm hf}(0)}{2\pi N} \text{ rad/s}. \quad (2)$$

Note that K has a unit of radians/second.

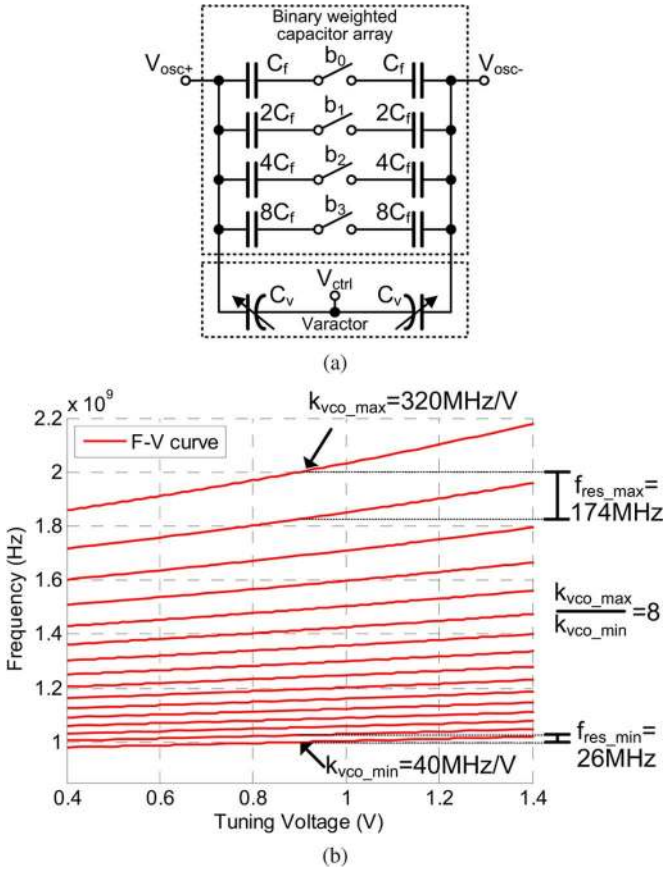


Fig. 2. Conventional topology. (a) Switching capacitor array and one varactor unit. (b) F–V curve with large variations of VCO tuning gain and band step.

For a typical third-order PLL, the transfer function of the LPF is obtained as

$$F_{\rm LPF}(s) = R_1C_1\left(1+\frac{1}{R_1C_1s}\right)\frac{1}{R_1C_1C_2s+C_1+C_2} \quad (3)$$

where K_1 is equal to R_1C_1 and $F_{\rm hf}(0)$ is equal to $1/(C_1+C_2)$. Therefore, the loop gain K of the third-order PLL can be rewritten as

$$K = \frac{I_{\rm CP}K_{\rm VCO}R_1}{2\pi N}\frac{b}{b+1} \quad (4)$$

where b is the ratio of C_1 over C_2. It can be observed that to achieve a constant loop gain without changing the pole and zero positions is to maintain a constant VCO gain $K_{\rm VCO}$ and to make the CP current $I_{\rm CP}$ match N.

B. VCO Gain

Frequency synthesizers for RF receivers usually employ an LC-based VCO due to its superior phase-noise performance. For the DVB-T frequency synthesizer, the targeted 814-MHz frequency range requires a VCO gain of more than 500 MHz/V assuming a 1.6-V tuning range for the CP output voltage. Such a high $K_{\rm VCO}$ may significantly degrade the phase-noise performance. To cover a wideband frequency range with a smaller $K_{\rm VCO}$, a switched capacitor array is usually adopted, as shown in Fig. 2(a). A fixed varactor C_v is tuned by the analog control voltage $V_{\rm ctrl}$ to achieve a continuous VCO frequency tuning,

while a binary weighted capacitor array is controlled digitally to discretely change the frequency band.

Although the switched capacitor array can extend the VCO tuning range while maintaining a smaller $K_{\rm VCO}$, it has two disadvantages. Firstly, equal capacitor is switched in or out of the capacitor bank whenever a lower or higher adjacent tuning band is required. Due to the nonlinear characteristic of frequency versus capacitance, the $K_{\rm VCO}$ will vary by a factor of 8 when the output frequency doubles by reducing the tank capacitance to a quarter [9]. Simulated tuning curves of a wideband VCO from 1 to 2 GHz are shown in Fig. 2(b), where a tank inductance of 4 nH is used. The highest and lowest $K_{\rm VCO}$ is 320 and 40 MHz/V, respectively. Such a large VCO gain variation significantly changes the loop bandwidth. As a result, the phase noise is deteriorated and the PLL loop becomes unstable. Secondly, the highest and lowest band step $f_{\rm res}$ is 174 and 26 MHz, respectively. Such a large band-step difference with a ratio of 6.7 greatly increases the complexity of the AFC loop design.

III. Design Techniques

A. Wideband VCO With Constant VCO Gain and Band Step

The $K_{\rm VCO}$ variation is a severe problem in designing wideband VCOs. Several techniques have been previously reported to reduce $K_{\rm VCO}$ fluctuation [10], [11]. In [10], an additional serial LC-tank with a variable inductor configuration is used to offset the VCO gain variation; however, such a method requires extra inductors and consumes more die area. A switched varactor array in combination with a multibias scheme is used to compensate the $K_{\rm VCO}$ variation in [11]. However, this method requires extra complicated biasing networks. In addition, both techniques cannot solve the variation problem of the band step $f_{\rm res}$. To minimize variations of both the VCO gain $K_{\rm VCO}$ and the band step $f_{\rm res}$, a proposed architecture is shown in Fig. 3(a). The idea behind the proposed architecture is to make both the sizes of switched capacitors and the varactors changeable. Instead of using a fixed analog varactor and a binary-weighted capacitor array, a number of capacitor and varactor units with different sizes are adopted. At lower frequency bands, not only more switched capacitor units are connected into the LC-tank, but also more varactor units are connected to the analog control voltage; the remaining varactor units are connected to a fixed voltage V_B to have a minimum fixed capacitance and the remaining switched capacitor units are disconnected. On the other hand, at higher frequency bands, less switched capacitor units, as well as less varactor units are switched into the LC-tank. Doing so allows a small and a constant $K_{\rm VCO}$, as well as a constant $f_{\rm res}$ to be achieved over the entire frequency range without adding extra design complexity, die area, or power consumption.

In the synthesizer, a digitally controlled capacitor array (DCCA) divides the whole tuning range into 16 sub-bands to keep a relatively low analog tuning gain, while an extra digitally controlled varactor array (DCVA) is inserted to equalize the tuning sensitivity. Assuming α_i $(i = 1, 2, \ldots, 15)$ being the capacitor ratio of DCCA units and β_i $(i = 1, 2, \ldots, 15)$ being the varactor ratio of DCVA units, the total capacitance $C_{{\rm tot},n}$

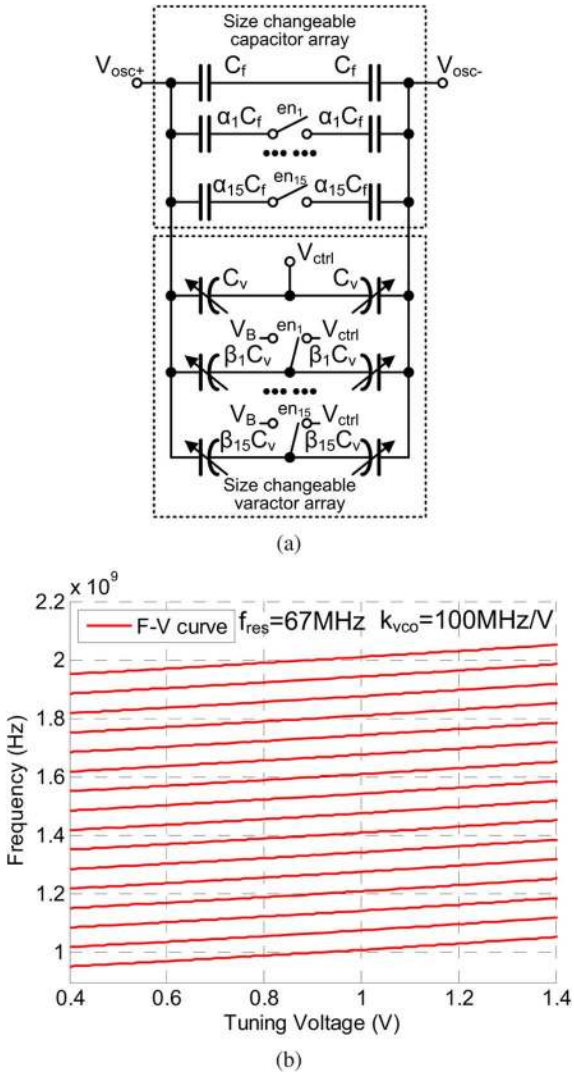


Fig. 3. Proposed LC-tank topology. (a) DCCA with a DCVA. (b) F–V curve with constant VCO tuning gain and band step.

across the tank at the center frequency of the nth sub-band can be expressed as follows:

$$C_{{\rm tot},n} = \begin{cases} C_p + C_f + (\beta_1 + \cdots + \beta_{15}) \cdot C_{v,\min} + C_{v,(0.9)}, \\ \qquad n = 1 \\ C_p + (1 + \alpha_1 + \cdots + \alpha_{n-1}) \cdot C_f + (\beta_n + \cdots + \beta_{15}) \\ \quad \cdot C_{v,\min} + (1 + \beta_1 + \cdots + \beta_{n-1}) \cdot C_{v,(0.9)}, \\ \qquad n = 2, 3, \ldots, 15 \\ C_p + (1 + \alpha_1 + \cdots + \alpha_{15}) \\ \quad \cdot C_f + (1 + \beta_1 + \cdots + \beta_{15}) \cdot C_{v,(0.9)}, \\ \qquad n = 16. \end{cases} \tag{5}$$

where C_p is the parasitic capacitance, C_f is the capacitance of the basic switched capacitor unit, $C_{v,\min}$ is the minimum capacitance of the varactor C_v, and $C_{v,(0.9)}$ is the capacitance of C_v at the center of the control voltage ($V_{DD} = 1.8$ V). Note that $n = 1$ is the highest frequency band. The oscillation frequency $f_{{\rm VCO},n}$ at the center of nth sub-band is expressed as

$$f_{{\rm VCO},n} = \frac{1}{2\pi\sqrt{LC_{{\rm tot},n}}}, \qquad n = 1, 2, \ldots, 16. \tag{6}$$

where L is half the inductance value of the differential tank inductor. Furthermore, the VCO gain $K_{\mathrm{VCO},n}$ at the center of the nth sub-band, which is derived from the partial derivative of control voltage, can be calculated as

$$K_{\mathrm{VCO},n} = \frac{\partial f_{\mathrm{VCO},n}}{\partial V_{\mathrm{ctrl}}} = \begin{cases} -\dfrac{1}{4\pi\sqrt{LC_{\mathrm{tot},n}^3}} \cdot \dfrac{\partial C_v}{\partial V_{\mathrm{ctrl}}}\Bigg|_{V_{\mathrm{ctrl}}=0.9}, & n=1 \\ -\dfrac{1+\beta_1+\cdots\beta_{n-1}}{4\pi\sqrt{LC_{\mathrm{tot},n}^3}} \cdot \dfrac{\partial C_v}{\partial V_{\mathrm{ctrl}}}\Bigg|_{V_{\mathrm{ctrl}}=0.9}, & n=2,3,\ldots,16 \end{cases} \tag{7}$$

where $\partial C_v/\partial V_{\mathrm{ctrl}}\,(V_{\mathrm{ctrl}}=0.9\,\mathrm{V})$ is the slope of the C–V curve of the varactor C_v at the center of control voltage. Note that $\partial C_v/\partial V_{\mathrm{ctrl}}$ is negative, hence, $K_{\mathrm{VCO},n}$ is a positive number.

For a given constant K_{VCO} and f_{res}, as well as the entire frequency range, the procedure to calculate α_i and β_i is as follows. Firstly, the highest frequency band f_H, the lowest frequency band f_L, the number of frequency bands n, and the inductance value L are selected, then the center frequency $K_{\mathrm{VCO},n}$ at each frequency band can be determined according to the frequency range and the number of bands. Substituting $K_{\mathrm{VCO},n}$ into (6), $C_{\mathrm{tot},n}$ can be obtained. Secondly, with the predetermined $K_{\mathrm{VCO},n}$, $C_{\mathrm{tot},n}$ is substituted into (7) to obtain the coefficients β_i. Thirdly, the inherent capacitance of the cross-coupled MOS transistors and the layout parasitic capacitance are estimated to determine the value of C_p. In addition, a varactor unit is simulated to obtain $C_{v,\min}$ and $C_{v,(0.9)}$. Finally, by substituting $C_{\mathrm{tot},n}$, $C_p, C_f, C_{v,\min}$, and $C_{v,(0.9)}$, as well as the coefficient β_i into (5), the coefficients α_i can be obtained.

Therefore, by choosing α_i and β_i properly, the K_{VCO} and the band step f_{res} can be arbitrary and constant. Nevertheless, it should be noted that if MOS transistors are used as the switched capacitors or the varactors, the minimum channel length of the technology may limit the minimum value of the capacitor and varactor sizes and this restricts the K_{VCO} and the band step f_{res} that can be achieved. An example of the coefficients α_i and β_i is summarized in Table I when C_p is 1.4 pF, C_f is 73 fF, $C_{v,(0.9)}$ is 40 fF, and $C_{v,\min}$ is 10 fF. These coefficients should be rounded to the nearest values that the technology permits. It should also be noted that since these coefficients are only ratios, they are insensitive to the process, voltage, and temperature (PVT) variations. The simulated tuning curves of the proposed architecture are shown in Fig. 3(b). Across the entire frequency range from 1 to 2 GHz, f_{res} is 67 MHz uniformly and K_{VCO} is 100 MHz/V for every switching band.

B. AFC

Due to the nonlinearity of the C–V curve of the varactor, the K_{VCO} of each frequency band can only be made equal in the middle of the tuning curve. For each tuning curve, the slope around the middle is linear and maximal. The AFC algorithm senses the VCO output center frequency of each band and compares it with the target value, which is determined by the division ratio N. The AFC loop selects the band whose center frequency is the closest to the target value [12], [13]. As long as the overlapping ratio between any two adjacent bands exceeds 50%, all output frequency points can fall near the middle of the tuning curve thus having linear tuning gains. By doing so, the VCO gain variation is further suppressed.

TABLE I
VALUES OF COEFFICIENTS α_i AND β_i

i	α_i	β_i	i	α_i	β_i	i	α_i	β_i
1	1.47	0.11	6	2.56	0.23	11	5.03	0.56
2	1.63	0.12	7	2.90	0.27	12	5.88	0.69
3	1.82	0.14	8	3.29	0.32	13	6.93	0.87
4	2.03	0.16	9	3.77	0.38	14	8.24	1.10
5	2.27	0.19	10	4.34	0.46	15	9.91	1.41

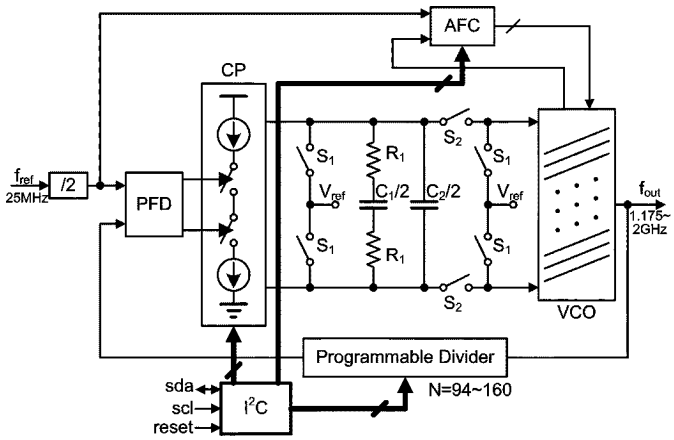


Fig. 4. Block-level diagram of a wideband 1.175–2-GHz frequency synthesizer with differential tuning.

C. CP

The frequency synthesizer varies its output frequency by changing the division ratio N. As can be seen from (4), when N changes, the loop gain is affected. To compensate the N variation, the CP current I_{CP} is programmed to match the division ratio N. A number of current mirrors are paralleled with a reference current source and sink to calibrate the total output charging and discharging current. By adjusting I_{CP}, the term I_{CP}/N can be made unchanged. With a constant I_{CP}/N and K_{VCO}, a constant loop gain K can be achieved across the entire frequency tuning range.

IV. CIRCUIT IMPLEMENTATION

A. System Architecture

A block-level diagram of the wideband 1.175–2-GHz frequency synthesizer is shown in Fig. 4. The synthesizer is fully integrated including a PFD, a rail-to-rail differential CP, a differential passive LPF, a wideband LC VCO, a programmable divider, a low drop-out (LDO) regulator, an AFC block, and an

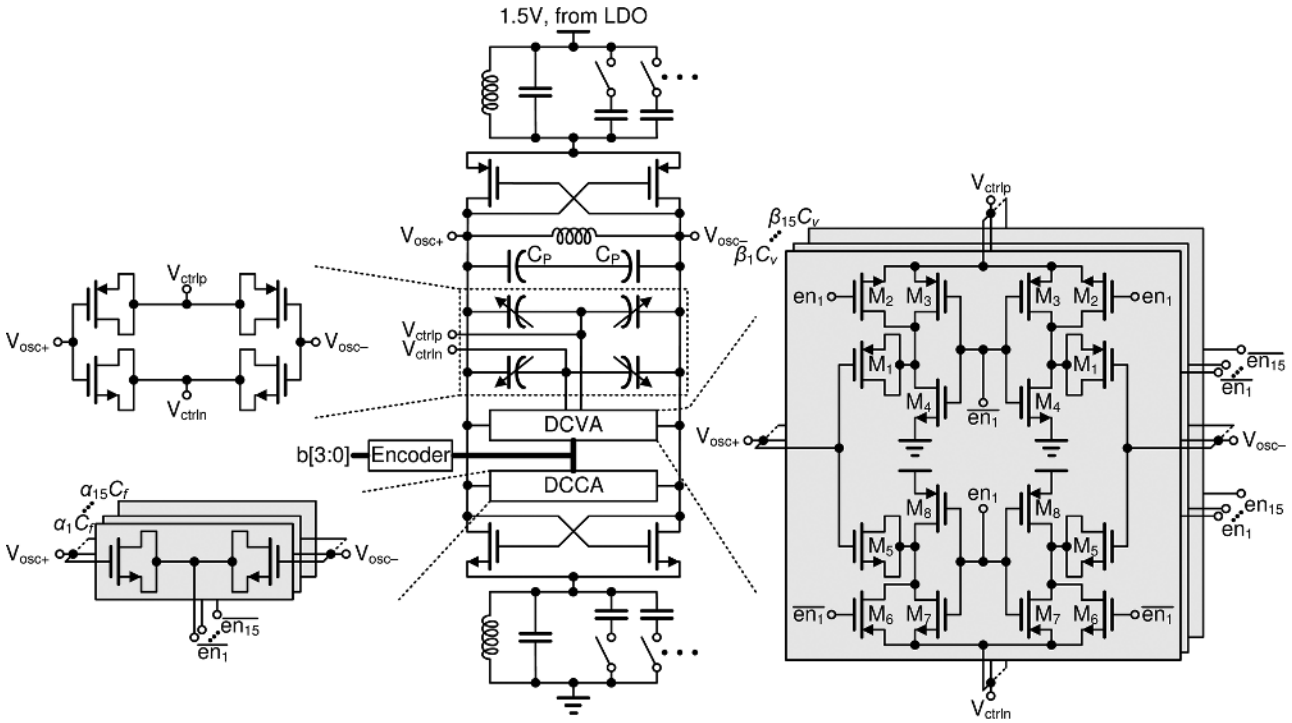


Fig. 5. Circuit diagram of the proposed wideband LC VCO.

I^2C controller. In order to suppress common-mode noise from control lines, power supply, and the substrate, a differentially tuned LC VCO was implemented [14]. Accordingly, the CP of the synthesizer was also implemented as a fully differential structure. When switch S_1 is closed, the differential control voltages $V_{\mathrm{ctrl}p}$ and $V_{\mathrm{ctrl}n}$ are connected to a reference voltage V_{ref}, and the AFC loop counts the clock divided by eight from the VCO output and performs the coarse tuning. After AFC operation, switch S_2 is closed and S_1 is open, and the differential control voltages are connected to the CP output to carry out the analog fine tuning. Internal digital registers are configured by an I^2C controller.

B. Wideband VCO

The schematic of an LC VCO is illustrated in Fig. 5. To reduce supply noise coupling, the VCO core is biased by a 1.5-V power supply from an on-chip LDO. Two complementary cross-coupled NMOS and PMOS transistors are adopted to form the negative transconductance. The LC tank uses a differential inductor to achieve a higher Q factor compared to single-ended inductors. The tail current source has been removed to improve the phase noise in the $1/f^3$ region. Removing the tail current source also maximizes the oscillation amplitude to nearly full swing. A tail LC-tank is used to increase the impedance of the tail nodes at the second harmonic, thus eliminating the thermal noise at twice the oscillation frequency. It also enhances the average loaded Q factor of the resonant LC-tank over one period improving the VCO phase-noise performance [15].

Inversion-mode MOS (I-MOS) varactors are used to perform analog fine tuning [16], [17]. To cover the wide frequency range of more than 814 MHz, four digital control bits are used and a total of 16 sub-bands are achieved. An encoder is used to transform binary codes into thermometer codes to control the digital bits. A basic varactor unit of only I-MOS is used at the highest frequency band. The DCCA using I-NMOS transistors performs coarse tuning. When en_i $(i = 1, \ldots, 15)$ is high, the NMOS transistor operates in the strong inversion region and maximum capacitance is realized. To meet the wideband frequency resonating characteristics, switched capacitor arrays are also added at the tail nodes to compensate the tail capacitance and allow the tail nodes to oscillate at twice the resonant frequency over the entire tuning range.

The detail realization of DCVA is also depicted. When en_1 is high, M_4 and M_8 are off, M_2–M_3 and M_6–M_7 are on to conduct the control voltage $V_{\mathrm{ctrl}p}$ and $V_{\mathrm{ctrl}n}$ to the drain–source of M_1 and M_5, then M_1 and M_5 are analog controlled and act as varactors. On the other hand, when en_1 is low, the drain–source of M_1 is connected to ground and the drain–source of M_5 is connected to V_{DD}, thus the capacitances of the varactor M_1 and M_5 are fixed and set at the minimal value.

The quality factor Q of the resonator tank is mainly limited by the tank inductor. The differential inductor in the tank is modeled using the Agilent full-wave EM simulator Momentum, and the inductor Q factor is between 6–10 from 1 to 2 GHz. All the capacitors and varactors are made using inversion-mode MOS transistors, and their Q factors are optimized between 20–30 across the entire tuning range so as to obtain larger values than that of the inductor.

C. Differential CP

A differential CP is used to achieve a better immunity to common-mode, power supply, and substrate noises. The conventional differential CP topology, despite the use of common-

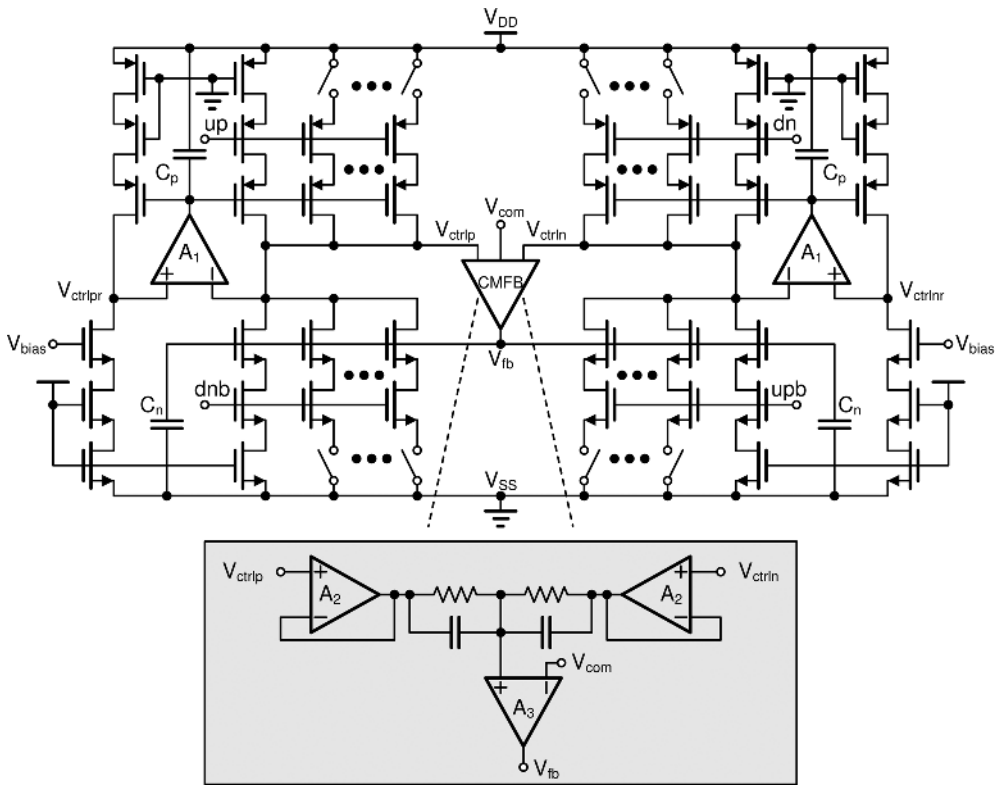


Fig. 6. Circuit diagram of the differential CP.

mode feedback (CMFB) circuitry, can still have mismatch between the differential output currents due to the channel-length modulation effect [18]. In this paper, a differential CP with excellent single-ended current matching is adopted, as shown in Fig. 6. It uses a replica bias circuit to provide good matching between the up and down current sources [19]. Owing to the local feedback opamp A_1, the CP can have near rail-to-rail operation. Capacitors C_p and C_n are large bypass capacitors, which act as voltage sources with low impedance during the onset of the up and down pulses and ensure fast turn-on of the current sources. During the charging period, current is sourced out to the LPF connected to $V_{\mathrm{ctrl}p}$ and sinks from the LPF on $V_{\mathrm{ctrl}n}$, causing the differential voltage to increase. Similarly discharging current will cause the differential output voltage to decrease.

Programmable current banks are added to compensate the N variation from 80 to 160. The CP current is programmed from 62.5 to 125 μA with a step of 1.95 μA and a 5-bit digital control. A CMFB loop is used to ensure the stability of the desired common-mode voltage of $V_{\mathrm{ctrl}p}$ and $V_{\mathrm{ctrl}n}$. Two unit-gain buffers A_2 are inserted to isolate the control voltages and the common-mode sensing point. Rail-to-rail opamps are used to ensure a near V_{DD} swing for $V_{\mathrm{ctrl}p}$ and $V_{\mathrm{ctrl}n}$.

D. On-Chip LPF

The large area of the LPF capacitor makes it difficult to be integrated on chip. Moreover, two LPFs with the same loop bandwidth are required for differential tuning, and this may require twice the area. Although the capacitance multiplier technique can be used, it suffers from the degradation of phase-noise performance [20]. To ensure on-chip integration of the LPF, an impedance transformation method is employed. The LPF schematic is shown in Fig. 7, which illustrates the principle. The capacitor C_1 that is the largest capacitor generates the first pole for the type-II synthesizer. C_1 and R_1 are used to generate a zero for loop stability, and C_2 is used to generate the second pole and

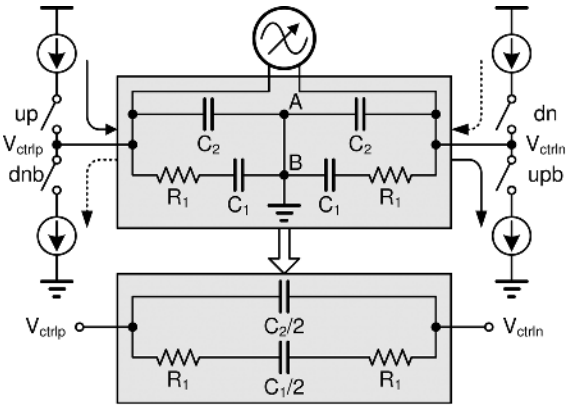


Fig. 7. Circuit diagram of the differential-mode LPF.

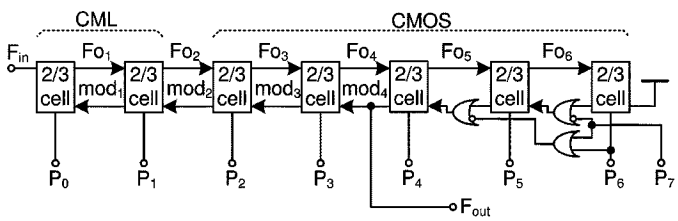
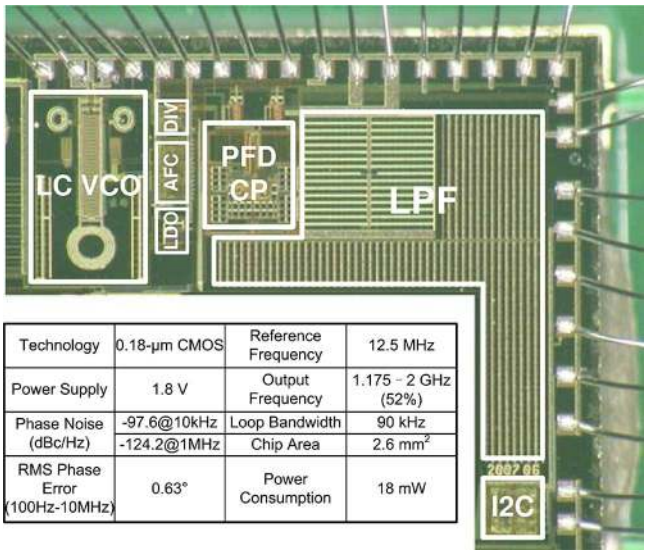


Fig. 8. Circuit diagram of the programmable cascaded divider.



Technology	0.18-μm CMOS	Reference Frequency	12.5 MHz
Power Supply	1.8 V	Output Frequency	1.175 - 2 GHz (52%)
Phase Noise (dBc/Hz)	-97.6@10kHz	Loop Bandwidth	90 kHz
	-124.2@1MHz	Chip Area	2.6 mm^2
RMS Phase Error (100Hz-10MHz)	0.63°	Power Consumption	18 mW

Fig. 9. Die micrograph and performance summary.

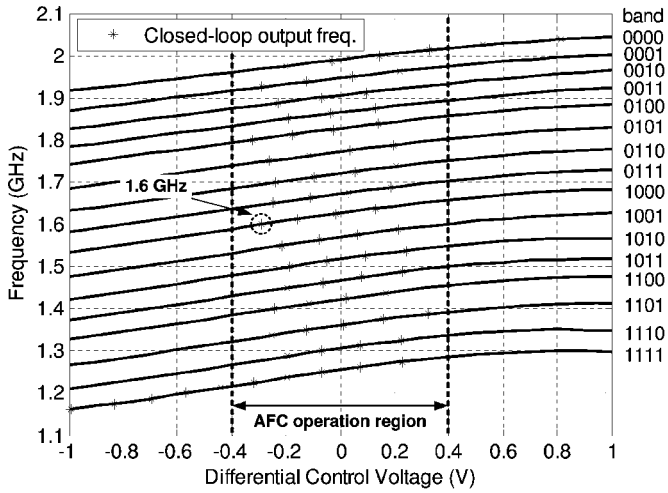


Fig. 10. Measured tuning curves of 16 sub-bands.

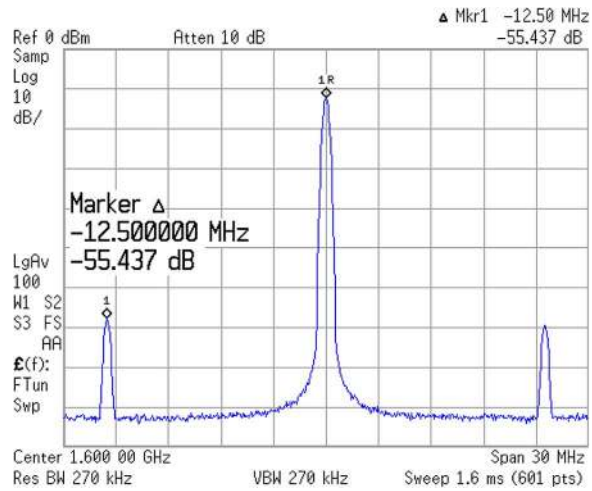


Fig. 11. Measured PSD of the oscillation amplitude at 1.6 GHz.

smooth ripples of the control voltage. Since the VCO is driven by differential control voltages, nodes A and B can be consid-

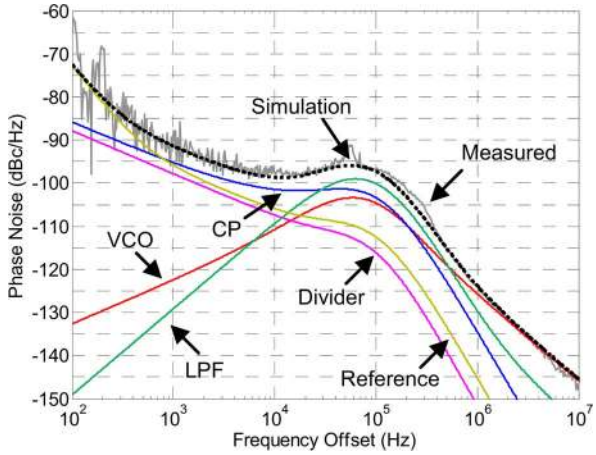


Fig. 12. Comparisons of simulation and measured phase noise at the oscillation frequency of 1.6 GHz.

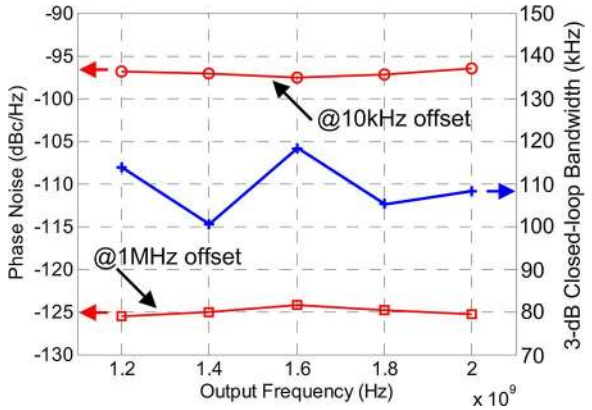


Fig. 13. Measured phase noise and 3-dB closed-loop bandwidth.

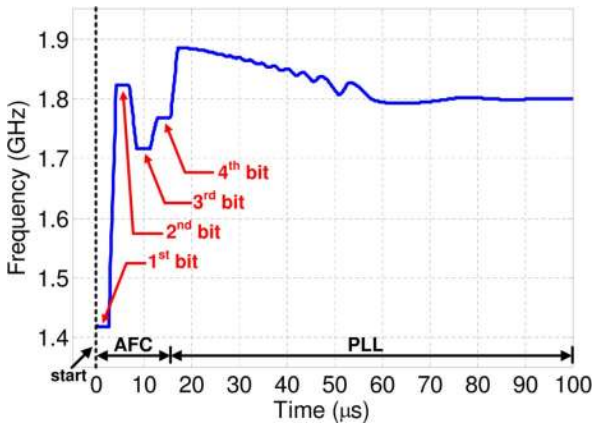


Fig. 14. Measured total locking time.

ered as virtually grounds. The two capacitors C_1 and C_2 can thus be connected in series directly. As a result, only a quarter of the area is needed as compared to the conventional implementation. The LPF parameters are as follows: C_1 is 971 pF, C_2 is 97.1 pF, and R_1 is 5.66 kΩ.

E. Other Blocks

The schematic of the programmable divider is shown in Fig. 8. It uses a cascade of seven 2/3 divider cells [21]. A

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ARTS

Ref.	[22]	[23]	[24]	[25]	This Work
Application	DVB-S	ISDB-T	DVB-H	DVB-T	DVB-T
Integration	Fully-Integrated	Fully-Integrated	Fully-Integrated	Off-Chip LPF	Fully-Integrated
Loop Bandwidth[a]	1 MHz	100 kHz	60 kHz	100 kHz[b]	110 kHz
Output Frequency (Normalized Tuning Range[c])	2.24-4.48 GHz (66.7%)	1.5-3.78 GHz (43.2%)	1.2-1.8 GHz (20%)	1.1-2.2 GHz (22.2%)	1.175-2 GHz (52%)
VCO Core	Ring	Two LCs	Two LCs	Three LCs	Single LC
Tuning Type	Single-Ended	Single-Ended	Single-Ended	Single-Ended	Differential
Phase Noise (dBc/Hz)	–98@100 kHz –100@1 MHz	–88@10 kHz -118@1 MHz	–94@10 kHz –127@1 MHz	–90@10 kHz	–97.6@10 kHz –124.2@1 MHz
RMS Phase Error	0.8°	N.A.	0.5°	1.5°	0.63°
Power Consumption	132 mW	20 mW	N.A.	N.A.	18 mW
Die Area (Exclude PADs)	0.3 mm^2	1.9 mm^2	2.45 mm^2	1.2 mm^2	2.2 mm^2 (Exclude I^2C)
Technology (CMOS)	0.13-μm, 3.3 V	0.11-μm, 1.2 V	0.18-μm, 1.8 V	0.18-μm, 1.8 V	0.18-μm, 1.8 V

[a] 3-dB Closed-Loop.
[b] Does not indicate which kind of bandwidth is used.
[c] The whole tuning range divided by the number of LC-VCOs.

few logic gates are added to extend the division range so the resulting division range is from 32 to 255. To save the power consumption, only the first two stages use the current mode logic (CML), and the following stages adopt CMOS circuits.

The AFC loop uses a binary-search algorithm. Each unit comparison time of AFC is 4 μs and a total of 16 μs is used for performing the AFC operation.

V. EXPERIMENTAL RESULTS

The wideband frequency synthesizer was implemented in a 0.18-μm CMOS process. The die micrograph is shown in Fig. 9 and a summary of the measured chip performance is also included. The die area is 2.2 mm^2, excluding PADs, electronic discharge (ESD) protection circuits, and I^2C controller. The power supply is 1.8 V.

The measured closed-loop output frequency is shown in Fig. 10, which includes a total of 71 points with a division ratio from 93 to 163. The tuning gain varies from 70 to 90 MHz/V. The tuning gain variation is less than 12.5% across the entire wideband frequency range of 825 MHz. One possible reason for this small tuning gain variation is that the oscillation amplitude is not constant across the entire frequency range, as a result, the calculated average capacitance over an oscillation period varies slightly. The measured band step $f_{\rm res}$ is from 50 to 60 MHz. The variation of the band step is less than 4.5%. Due to the adoption of the AFC loop, the differential control voltages fall between $\pm$0.4 V over the entire frequency range, and this ensures the operation of the VCO in the linear tuning region.

Fig. 11 shows the oscillation amplitude power spectral density (PSD) at 1.6 GHz. The reference spur at a 12.5-MHz frequency offset is below -55 dBc/Hz. The measured phase noise at 1.6 GHz is plotted in Fig. 12 and is compared with the simulation result. The spot phase noise is -97.6 dBc/Hz at a 10-kHz offset and -124.2 dBc/Hz at a 1-MHz offset. The integrated phase error from 100 Hz to 10 MHz is $0.63^\circ_{\rm rms}$. The measured and simulated curves agree very well from 100 Hz to 10 MHz. The simulated phase-noise contributions of all the blocks are also depicted. At below 1-kHz offset, the noise from reference clock dominates; the CP contributes most at the in-band frequency offset; the LPF contributes most from 30 to 500 kHz; and the VCO dominates at the far out-of-band frequency offset beyond 500 kHz. Phase-noise plots at frequency offsets of 10 kHz and 1 MHz with the oscillation frequency ranging from 1.2 to 2 GHz are shown in Fig. 13. The phase-noise curves have a flat characteristic across the entire frequency range. The variation is less than 1 dB. It is also shown that the closed loop has an average 3-dB bandwidth of 110 kHz and the bandwidth variation is less than 9%.

The measured locking process is shown in Fig. 14. The AFC operation consumes 16 μs, with 4 μs for each unit comparison time. The remaining time for PLL operation is 84 μs, and the total locking time is less than 100 μs.

Table II presents a performance comparison with recently reported frequency synthesizers designed for DVB applications. This work used a single LC VCO, while the others used multiple (either two or three) LC VCOs. For the synthesizers using LC VCOs, this work achieved the highest normalized tuning range of 52%. The normalized tuning range is defined as the whole tuning range divided by the number of LC VCOs used. Even with a single LC VCO, the wideband frequency synthesizer described in this paper still achieved an excellent phase-noise performance. It consumed the smallest power with a comparable die area (compared with the synthesizers having a fully integrated LPF). In addition, the synthesizer adopted differential tuning modes to suppress the common-mode noise from control lines, power supply, and the substrate. A unique feature of the synthesizer is that it achieved a constant 3-dB closed-loop bandwidth. The VCO is designed to achieve a constant band step $f_{\rm res}$, as well as a small and constant VCO gain $K_{\rm VCO}$. The CP current is adjusted to match the division ratio N.

VI. Conclusion

Having a constant bandwidth is essential for phase-noise optimization and ensuring loop stability for wideband frequency synthesizers. This paper reports a fully integrated 1.175–2-GHz frequency synthesizer with a constant loop bandwidth for DVB-T applications. Techniques for achieving a constant synthesizer loop bandwidth are proposed. To overcome the VCO gain $K_{\rm VCO}$ and the band step $f_{\rm res}$ variations, a technique by simultaneously adjusting both the sizes of switched capacitors and varactors is developed. The procedure for calculating the switching capacitor and varactor sizes at each frequency band is also described. Furthermore, the CP current $I_{\rm CP}$ is programmed to compensate the variation of division ratio N. In addition, an impedance transformation method is employed to reduce the die area of the LPF allowing its on-chip integration. The synthesizer was fabricated and validated in a 0.18-μm CMOS process. It achieved a normalized tuning range of 52% using a single LC VCO, and a less than 12.5% VCO gain $K_{\rm VCO}$ variation, as well as a less than 4.5% band step $f_{\rm res}$ variation. The in-band phase noise at a 10-kHz offset is below -97 dBc/Hz and the integrated phase error from 100 Hz to 10 MHz is $0.63^{\circ}_{\rm rms}$. It has a nearly constant 3-dB closed-loop bandwidth and a flat phase-noise characteristic across the entire wide frequency tuning range. The synthesizer consumes only 18 mW with a 1.8-V supply.

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