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An 18-nA Ultra-Low-Current Resistor-less Bandgap Reference for 2.8 V - 4.5 V High Voltage Supply Li-ion-Battery-Based LSIs

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***Abstract*— This paper presents a resistor-less bandgap reference (BGR) with ultra-low current consumption, which can be applied in energy harvesting systems that use lithium-ion (Li-ion) batteries as intermediate energy storage. The system supply voltage is defined by the output voltage of the Li-ion battery, which is usually from 3 V to 4.2 V. The BGR circuit working in this kind of system needs to withstand a high supply voltage while consuming nano-watt power. In this work, differential pairs are first used in a low-power BGR circuit as a voltage duplicator to achieve duplication of both the proportional-to-absolute-temperature (PTAT) voltage and the trimming network, which can reduce the complexity of the structure and the chip area of the trimming network. The total current consumption of the BGR is around 18 nA for different supply voltages ranging from 2.8 V to 4.5 V. Fabricated in a 0.35-µm CMOS process, the BGR circuit generates a 1.17 V bandgap voltage with an average temperature coefficient of 65 ppm/ºC and a line regulation of 0.112 %/V.**

***Index Terms*—Bandgap reference, resistor-less, low power, nano-watt, high supply voltage.**

I. Introduction

Energy harvesting is an essential technology for Internet-of-things (IoT) application. However, the energy generators used in harvesting energy cannot always provide a consistent power supply voltage to the system. For example, in an energy harvesting system that utilizes a thermoelectric generator (TEG), the differing temperature gradient will result in different TEG voltages. In this case, a Li-ion battery is a common choice as intermediate energy storage to transmit the power from the energy generator to the circuit and provide a stable supply voltage [1][2]. The nominal cell voltage of a Li-ion battery is 3.6 V, and its output voltage level can vary from a typical end-of-charge voltage of 3.0 V to maximum charge voltage of 4.2 V. The output voltage of the battery defines the high supply voltage to the system circuit. In such an energy harvesting system, the core system is sometimes controlled by the duty cycle to achieve low average power consumption. During the turn-off period, the converters and regulators are off. Since an always-on reference voltage is needed for the energy harvesting system with a fast clock to deal with a large power range [1], the bandgap reference circuit will be powered by the battery directly. For this reason, the bandgap reference, which can work under a high supply voltage with a decent line regulation and operate at nano-watt power, is indispensable.

Nano-watt power consumption voltage references are widely used in ultra-low power IoT devices. However, recent low-power voltage reference designs are usually target for the application of low supply voltage which is under 1.8 V [3]-[7]. In [3] & [7], the PTAT voltage is realized by a leakage-current-based topology by shorting the gate to the source terminal ($V_{GS} = 0$). However, the threshold voltage will decrease linearly with an increasing temperature and cause the leakage current to increase exponentially, which will induce significant power consumption at high temperature. Using a switch capacitor circuit as a V_{EB} voltage divider can reduce the supply voltage headroom [4][5]. However, this will induce switching noise in the system. In [11], the BGR can work with high supply voltage from 3.5 V to 5 V. However, the power consumption is larger than 100 µW. In most reference circuits, a resistor is a common choice to generate PTAT current and PTAT voltage [6]-[10]. In order to reduce the current on the resistors, large resistance values are used, which will increase the silicon area. Using a switched capacitor network with low switching frequency [4][5] can also be regarded as a large resistance path, but the switching noise need to be filtered by a large loading capacitor as in [12], which is again area inefficient. The CMOS-only voltage reference that can operate at pico-watt power and consume a very small chip area has attracted increasing attention recently [13]. However, the output voltage is threshold voltage dependent and the accuracy is degraded by the process variation. A resistor-less bandgap reference circuit using a PTAT voltage multiplier is proposed in [14]. However, this method cannot operate in the MOSFET subthreshold region and the total power consumption is at the milli-watt level. Another resistor-less bandgap reference is presented in [15], which utilizes multiple PMOS differential pairs in series and are biased in the subthreshold region to generate a PTAT voltage. However, a trimming network in each differential pair is needed to achieve a large trimming range.

This paper presents a resistor-less BGR consuming nano-watt power under a voltage supply from 2.8 V to 4.5 V. The

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complementary-to-absolute-temperature (CTAT) voltage is generated by V_{EB} of the bipolar transistor with current biasing. The PTAT generator is implemented by two PMOS differential pairs in series, then multiplied four times by the proposed voltage duplicator. A cascode structure is used in the current source to generate a current bias insensitive to supply voltage.

II. Proposed Bandgap Reference

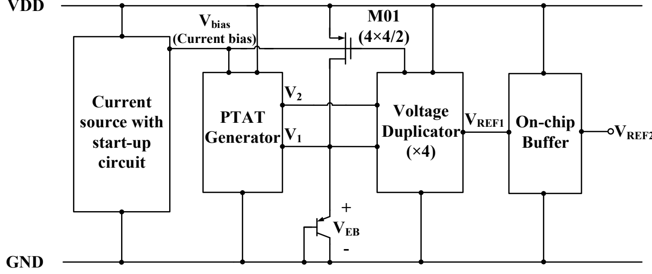

Fig. 1. Diagram of the proposed bandgap reference circuit.

The structure of the proposed bandgap reference circuit is shown in Fig. 1. The current source generates a 1.4 nA output current to bias the PTAT generator, bipolar transistor and voltage duplicator by the PMOS current mirror. The PTAT voltage is the difference between V_2 and V_1, which is generated by the PTAT generator, and is copied four times by the voltage duplicator. The CTAT voltage from V_{EB} of the bipolar transistor is added to the input of the voltage duplicator at node V_1. Then, the output V_{REF1} of the voltage duplicator is equal to (V_{CTAT} + $4V_{PTAT}$), which is 1.17 V. A source-follower is used as an on-chip buffer to improve the driving capability and generate V_{REF2}, which is half V_{REF1}, for testing.

A. PTAT Voltage Generator with Trimming Network

The structure of the PTAT voltage generator is shown in Fig. 2 [15]. The PTAT voltage is generated by the differential V_{GS} of the PMOS transistors in the sub-threshold region. Two differential pairs are used in the PTAT generator, A 3-bit trimming network is applied at M05, and the biasing for the PMOS current mirror in the PTAT generator (M02 and M07) is generated from the current source.

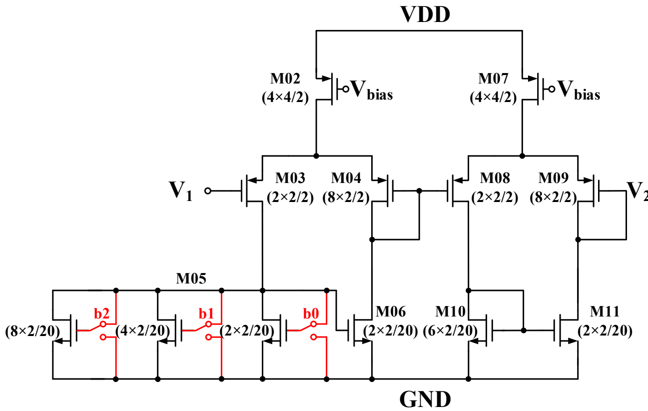

Fig. 2. Schematic of the PTAT voltage generator with trimming network.

The source-drain current in the sub-threshold region of the PMOS transistor can be described in (1), where $|V_{ds}|$ is three times larger than the thermal voltage ($|V_{ds}| > 3V_T$), which is the saturation condition of sub-threshold region:

$$I_{sd} = \mu_p C_{ox}\left(\frac{W}{L}\right)(\eta-1)V_T^2 \, exp\left(\frac{|V_{GS}|-|V_{thp}|}{\eta V_T}\right), \quad (1)$$

where μ_p, C_{ox}, η, V_T and V_{thp} is the hole mobility, gate oxide capacitance per area, inverse of the gate-to-surface coupling coefficient, thermal voltage and P-MOSFET threshold voltage, respectively. By rearranging (1), V_{GS} can be described as

$$|V_{GS}| = \eta V_T \cdot \ln\left(\frac{I_{sd}}{\mu_p C_{ox}\left(\frac{W}{L}\right)(\eta-1)V_T^2}\right) + |V_{thp}|. \quad (2)$$

To cancel the threshold voltage variation, the same finger size in M03, M04, M08 and M09 is used to get $|V_{th,M03}|-|V_{th,M04}| \approx 0$ and $|V_{th,M08}|-|V_{th,M09}| \approx 0$. Thus, the PTAT voltage can be described as in (3):

$$\begin{aligned} V_{PTAT} &= V_2 - V_1 \\ &= |V_{GS,M03}| - |V_{GS,M04}| + |V_{GS,M08}| - |V_{GS,M09}| \\ &= \eta V_T \cdot \ln\left(\frac{I_{sd,M03} I_{sd,M08}}{I_{sd,M04} I_{sd,M09}} \cdot \frac{W_{M04} W_{M09}}{W_{M03} W_{M08}}\right). \end{aligned} \quad (3)$$

The transistor sizes of M03, M04, M08 and M09 are fixed. The current ratio between $I_{sd,M08}$ and $I_{sd,M09}$ is also fixed. Therefore, the PTAT voltage is only defined by the current ratio between $I_{sd,M03}$ and $I_{sd,M04}$. Since (M03, M04) and (M05, M06) share the same current ratio, a proper trimming code of b0, b1 and b2 in M05 can be chosen to adjust the current ratio between $I_{sd,M05}$ and $I_{sd,M06}$. During testing, if the output voltage V_{REF2} behaves as PTAT, which means the output voltage increases with the rising temperature, the trimming bit in the trimming network should be reduced to decrease the PTAT voltage. For a CTAT scenario, the trimming bit should be increased.

B. Proposed Voltage Duplicator

Fig. 3 shows the proposed voltage duplicator, which can copy the PTAT voltage ($V_2 - V_1$) four times. The biasing current generated by the PMOS current mirror (M12, M16, M20 and M24) and the NMOS current mirror (M15, M19, M23 and M27) ensures that the current ratio of each differential PMOS pair in the voltage duplicator is same. This means the differential voltage across each differential PMOS pair is the same. The PTAT voltage ($V_2 - V_1$) is applied on the first differential PMOS pair in the voltage duplicator, and the CTAT voltage generated by the V_{EB} of a bipolar transistor is connected to the input of the voltage duplicator at node V_1. The output voltage V_{REF1} of the voltage duplicator is the sum of V_{EB} and four V_{PTAT}.

The number of the pairs (n_{pair}) in the voltage duplicator is chosen based on the tradeoff between the total current consumption and the minimal tolerable current of the NMOS current mirror (M15, M19, M23 and M27). The relationship between n_{pair} and the PTAT voltage is shown in (4), where the silicon bandgap voltage ($V_{Si,Bandgap}$) is a constant value and should be equal to the bandgap voltage V_{REF1}.

$$V_{EB} + n_{pair} \cdot V_{PTAT} = V_{Si,Bandgap}. \quad (4)$$

A smaller number of n_{pair} will lead to a larger PTAT voltage ($V_2 - V_1$) across each differential pair. This will cause a smaller branch current in M14 and M15. This small current will be

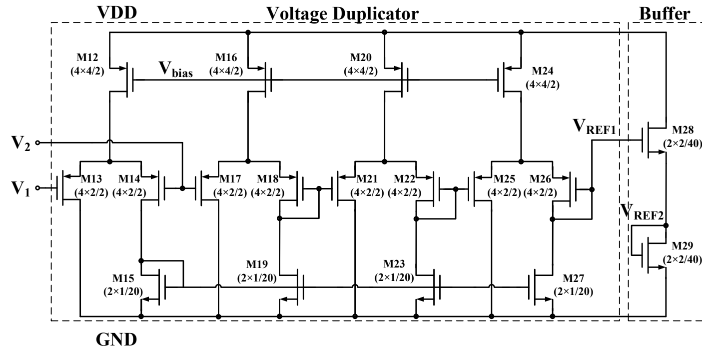

Fig. 3. Schematic of proposed voltage duplicator and on-chip buffer.

mirrored to the other pairs in the voltage duplicator by the NMOS current mirror and will be sensitive to process variation, gate leakage current and source/drain to substrate junction leakage current, and have a poor driving capability of node V_{REF1}. To relieve this problem, a larger number of n_{pair} should be chosen. However, more differential pairs means larger total current consumption. To have both decent total power consumption and reasonable biasing current of M15, the value of n_{pair} should be chosen carefully.

The drain current ratio of M13 and M14 can be expressed as

$$\frac{I_{sd,M13}}{I_{sd,M14}} = \frac{\mu_p C_{ox}\left(\frac{W_{M13}}{L_{M13}}\right)(\eta-1)V_T^2\, exp\left(\frac{|V_{GS,M13}|-|V_{thp}|}{\eta V_T}\right)}{\mu_p C_{ox}\left(\frac{W_{M14}}{L_{M14}}\right)(\eta-1)V_T^2\, exp\left(\frac{|V_{GS,M14}|-|V_{thp}|}{\eta V_T}\right)}. \quad (5)$$

Since M13 and M14 have the same transistor size,

$$\frac{I_{sd,M13}}{I_{sd,M14}} = \exp\left(\frac{|V_{GS,M13}|-|V_{GS,M14}|}{\eta V_T}\right) = \exp\left(\frac{V_{PTAT}}{\eta V_T}\right). \quad (6)$$

Since $I_{sd,\,M15} = I_{sd,\,M14}$, (7) provides the estimation of $I_{sd,\,M15}$:

$$I_{sd,M15} = \frac{I_{sd,M13}}{\exp\left(\frac{V_{PTAT}}{\eta V_T}\right)}. \quad (7)$$

The biasing current in M12 is 1.4 nA from the current source. Since $I_{sd,M14}$ is much smaller than $I_{sd,M13}$, it can be assumed that $I_{sd,M13} \approx 1.4$ nA. V_{EB} is 0.48 V at 1.4 nA biasing current, and $V_{Si,Bandgap} \approx 1.2$ V. If n_{pair} is four, V_{PTAT} will be equal to 0.18 V. Since η is between 1.1 and 1.3 in an advanced CMOS process, the estimated value of $I_{sd,M15}$ is between 2.59 pA and 6.81 pA based on (7). Fig. 4 shows the simulated value of $I_{sd,M15}$ from Cadence. When n_{pair} is four, the simulated $I_{sd,M15}$ is 4.48 nA, which is in the same order of magnitude as the estimated result from (7).

For the NMOS current mirror (e.g. M15), the parasitic diode leakage current from N-diffusion area to p-substrate is about 1 fA based on the datasheet and M15 transistor size. The parasitic diode leakage current will increase exponentially with increasing temperature. Thus, the branch current is designed at pico-ampere level which is about 1000 times larger than the parasitic leakage current. n_{pair}=4 is a reasonable choice for the consideration of both the NMOS branch current margin and the total current consumption. Therefore, the reference voltage can be expressed as

$$V_{REF1} = V_{EB} + 4 \cdot V_{PTAT}. \quad (8)$$

Since the small current of M15 will lead to a low V_{GS}, and V_{DS} is equal to V_{GS} for M15, the low V_{DS} will be insufficient for the saturation condition in the sub-threshold region. A long channel length is therefore used in the NMOS current mirror (M15, M19, M23 and M27) to maintain the V_{DS} of the NMOS in the current mirror larger than $3V_T$, which is the condition of saturation in the sub-threshold region. Since long channel MOSFETs are used in the current mirror and all PMOS differential pairs, the V_{DS} to I_{DS} modulation effect is weak to be ignored. The variation of the reference voltage (V_{REF2}) from Monte Carlo simulations is shown in Fig. 5. σ/μ is 1.23%.

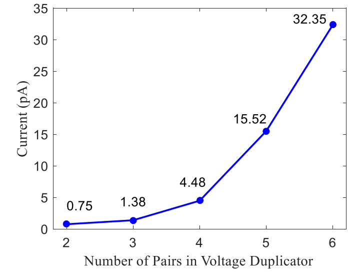

Fig. 4. Simulation results of branch current versus number of pairs in the voltage duplicator.

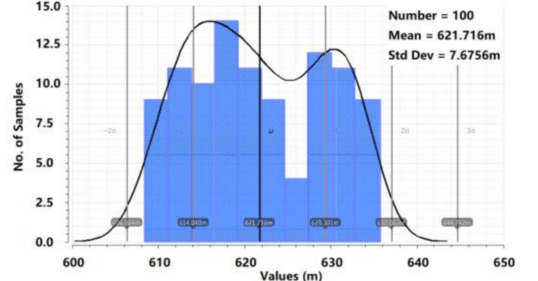

Fig. 5. Monte-Carlo simulation results of reference voltage (100 samples).

C. Current Source

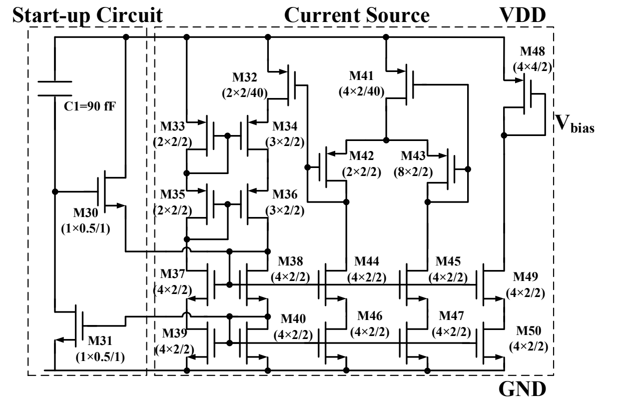

Fig. 6. Schematic of the current source for the bandgap reference circuit.

In this work, the current source is implemented by a resistor-less structure, as shown in Fig. 6 [16]. The output current of M48 is about 1.4 nA. Transistor M32 is operating in the linear region as a resistor. The threshold voltages of three pairs (M32, M41), (M33, M34) and (M42, M43) can cancel each other if the same finger size is used in each pair. Therefore, the current source can tolerate the threshold voltage variation. To achieve a decent line regulation, a cascode structure is used in the current source, which can reduce the output current variation due to the supply voltage changes. For the start-up circuit, the capacitor C1 stacked above M31 is used to avoid the DC current leakage path. When the circuit is powered on, the voltage across the capacitor will not change instantly. M30 will be turned on due to the pulled-up gate voltage, and the current through M30 will power up the current source. When the current source is fully turned-on, M31 will pull down the gate voltage of M30 to ground. The off-state M30 with body effect will have negligible leakage current and will not affect the DC condition of the current source.

D. On-Chip Buffer

As previously discussed, the small drain current of M15 is mirrored to M19, M23 and M27. This means there is poor driving capability at V_{REF1} node, which is difficult to measure during testing since any PCB leakage path will disturb the DC node voltage. If an off-chip buffer is used, the high impedance node V_{REF1} is still exposed to a possible PCB leakage path. Therefore, a source-follower is used as an on-chip buffer to improve the driving capability, as shown in Fig. 3. The source-follower is implemented by the isolated P-well NMOS to eliminate the body effect, which can offer V_{REF2} as a perfect half of V_{REF1}. The current consumed by the on-chip buffer is 2 nA. For application in a system circuit with a voltage regulator, the V_{REF1} node can be directly used as the reference voltage.

III. MEARSURMENT RESULTS

The proposed BGR circuit is fabricated in a standard 0.35-μm CMOS process. The chip micrograph is shown in Fig. 7. The active area is 0.042 mm^2. Fig. 8 (a) and (c) show the untrimmed and trimmed reference voltage versus temperature with a 3-V supply voltage. The average temperature coefficient (TC) is 109.09 ppm/°C before trimming, and 65 ppm/°C after trimming. The distribution of the testing node V_{REF2} is shown in Fig. 8 (b) and (d). σ/μ is 1.66% before trimming, and is 1.21% after trimming. The trimmed average value of V_{REF2} is 585 mV. V_{REF1} is twice the value of the testing node V_{REF2}. Thus, V_{REF1} should be about 1.17 V at room temperature.

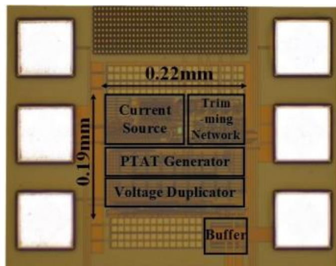

Fig. 7. Chip micrograph.

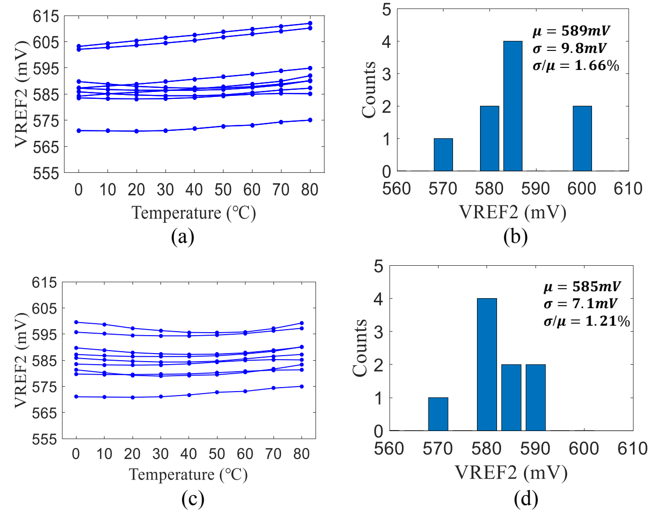

Fig. 8. Measured reference voltage (V_{REF2}) with 9 sample chips. (a) Untrimmed BGR as a function of temperature. (b) Untrimmed distribution at room temperature. (c) Trimmed BGR as a function of temperature. (d) Trimmed distribution at room temperature.

In Fig. 9, the distribution of the TC and the current consumption of the nine samples are given. The current consumption is measured at room temperature at a 3-V supply voltage. The lowest current consumption is 14 nA, the highest current consumption is 22 nA, and the average current consumption of the sample chips is 18 nA. Fig. 10 shows the reference voltage as a function of temperature at different supply voltages: 2.8 V, 3.0 V, 3.6 V and 4.5 V, and the reference voltage values are 579.5 mV, 579.6 mV, 580.4 mV and 580.6 mV, respectively, at room temperature. The line regulation is 0.112 %/V with a supply voltage changing from 2.8 V to 4.5 V. The measured current consumption versus temperature at different supply voltages is plotted in Fig. 11. The total current consumption of the reference circuit is around 18 nA at room temperature and increases to around 30 nA at 80°C.

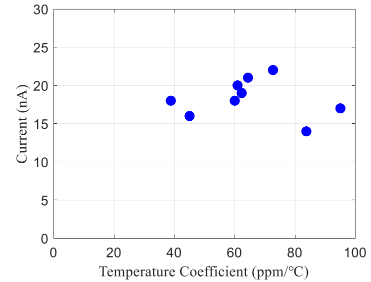

Fig. 9. Distribution of current consumption and TC in nine samples.

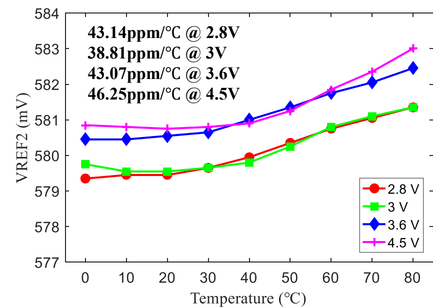

Fig. 10. Measured reference voltage versus temperature at different supply voltages.

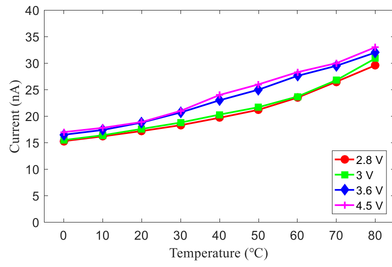

Fig. 11. Current consumption versus temperature at different supply voltages.

The performance comparison is shown in Table I and includes the results of seven low-power BGR designs reported in recent papers. Compared with other works, only this work can achieve an ultra-low-current consumption with a wide range of high supply voltage, from 2.8 V to 4.5 V. Without using a resistor, the active area is relatively small and only slightly larger than another resistor-less BGR [15] implemented by a more advanced 0.18-µm technology. [15] also has a much larger current consumption. The active area of this work is comparable with [3], [4] and [5]. In [3], only one resistor is used to generate current bias. However, this method uses leakage current to generate PTAT voltage, which cannot be used in a high V_{TH} process for high voltage application since the extreme small leakage current in a high V_{TH} process cannot generate PTAT voltage. Further, this method will induce large current consumption at high temperature. In [4] and [5], switch capacitors are used as a V_{EB} voltage divider and only one resistor in the current source is needed. However, this method will induce switching noise in the output voltage, which is not suitable for the systems that need a clean and stable reference voltage. Thus, the proposed BGR can simultaneously achieve low current consumption with a small chip area for high supply voltage application.

IV. Conclusions

This paper presents a resistor-less bandgap reference circuit for an ultra-low-power energy harvesting system with a Li-ion battery as energy storage. The reference allows a high-voltage supply, from 2.8 V to 4.5 V, to meet the output level of the Li-ion battery. The average reference voltage is 1.17 V. The power consumption is 54 nW at a 3-V supply voltage.

TABLE I.
Performance Comparison

	This work	[5] 2017	[3] 2017	[4] 2015	[7] 2015	[15] 2013	[6] 2012	[17] 2010
Process	0.35µm	0.18µm	0.18µm	0.13µm	0.35µm	0.18µm	0.13µm	0.35µm
Type	V_{EB}	V_{EB}	V_{EB}	V_{EB}	V_{EB}	V_{EB}	V_{EB}	V_{EB}
Supply voltage	2.8V-4.5V	0.5V	1.3V-1.8V	0.5V -1.5V	1.4V	1.2V-1.8V	0.75V	1.3V-3.3V
Vref (V)	1.17	0.24	1.238	0.498	1.176	1.09	0.256	1.18
Power (nW)	54	40	9.3	32	28.7	100	170	108
Total current (nA) at room temperature	18	80	7.2	64	20.5	83	227	83
TC (ppm/°C)	65	58	26	75	13	147	40	215
Temperature range	0°C-80°C	−25°C-85°C	0°C-110°C	0°C-80°C	−10°C-110°C	−40°C-120°C	−20°C-85°C	−20°C-80°C
Line Reg. (%/V)	0.112	0.46	0.99	2	0.198	N/A	N/A	0.45
σ/µ	1.21	0.29	0.43	N/A	0.2	1.05	0.5	1.63
Active Area (mm²)	0.042	0.058	0.055	0.03	0.48	0.03	0.07	0.21

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