An 8-Bit, 1-Gsample/s Folding-Interpolating Analog-to-Digital Converter

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Abstract

This thesis deals with the design and implementation of an 8-bit, 1-Gsample/s folding-interpolating analog-to-digital converter using a conventional 0.5 μm self-aligned, double polysilicon bipolar process with maximum unity gain cutoff frequency f_T of 25GHz. The high-speed and high-resolution A/D converter has applications in direct IF sampling receivers for wideband communications systems. The folding-interpolating architecture offers an optimum solution for Gsample/s, high-resolution A/D converters in terms of system complexity, power dissipation and chip area. The use of a silicon bipolar process allows the integration of Gsample/s ADCs with DSP systems usually realized by silicon CMOS or BiCMOS processes.

The 8-bit, 1-Gsample/s A/D converter consists of a reference ladder; four folding blocks for the fine quantizer and one folding block for the coarse quantizer; interpolation resistive strings; a comparator array; a digital encoder including an EXOR array, an error-correction stage, and a 31-to-5 OR ROM; and a coarse quantizer. All circuit blocks are integrated on one chip. The chip area of the circuitry is 2.5mm×3.5mm including bonding pads. The converter exhibits a better than 7-bit ENOB with an input signal frequency of 200MHz and at a sampling rate of 1-Gsample/s. The maximum power dissipation of the ADC is 2.5W using a 5-V power supply

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CHAPTER 1

Introduction

Analog-to-digital (A/D) conversion and digital-to-analog (D/A) conversion lie at the heart of modern signal processing systems where digital circuitry performs the bulk of the complex signal manipulation. As digital signal processing (DSP) integrated circuits become increasingly sophisticated and attain higher operating speeds, more and more processing functions are performed in the digital domain. Driven by the enhanced capability of DSP circuits, A/D converters (ADCs) must operate at ever-increasing frequencies while maintaining accuracy previously obtainable only at moderate speeds.

Digital systems offer significant advantages in terms of functionality, flexibility, and immunity against external influences compared to their analog counterparts, and as such are becoming pervasive in electronic systems. Fig. 1.1 illustrates the evolution of communications systems towards relying upon DSP hardware with a concomitant reduction in analog circuit content. This shift indicates that only Radio Frequency (RF) processing and data conversion (including anti-aliasing filters) will remain as important niches where analog implementations exhibit advantages over digital approaches. Intermediate Frequency (IF) and RF data conversion will continue to play a significant role in advanced communications systems. However, the characteristics of ADCs frequently limit the

performance of such systems because of the circuit complexity and large power consumption of high-speed A/D converters. The development of improved A/D conversion algorithms and circuitry to meet the need of communications systems represents an important area of research for the foreseeable future.

(a)

(b)

(c)
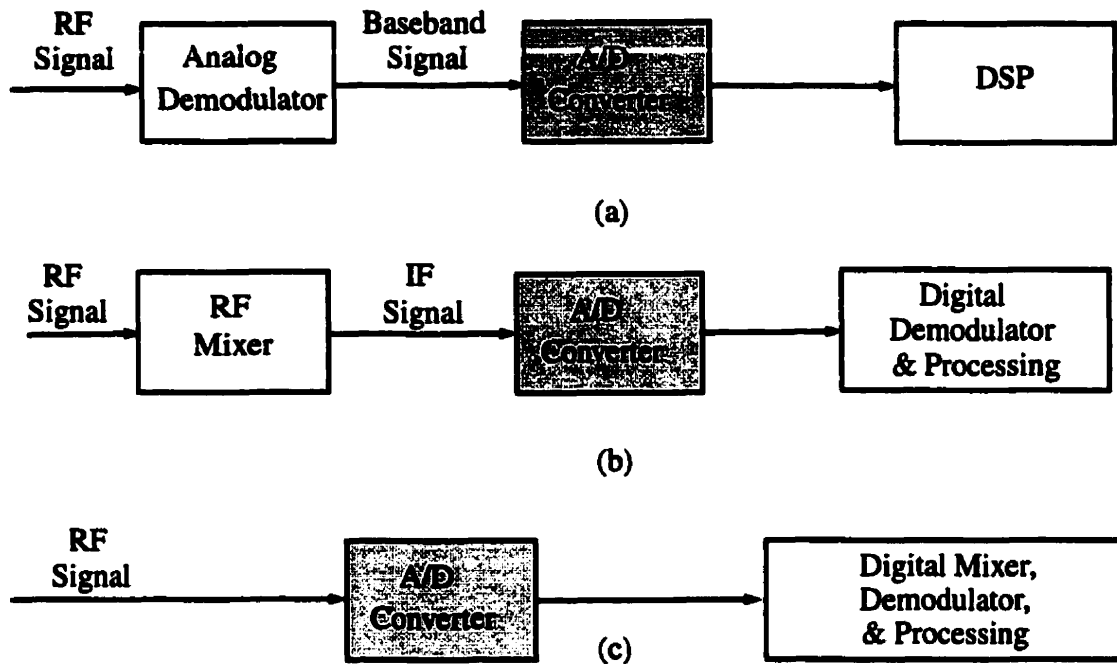
Fig. 1.1. Examples of increasing DSP complexity in communication systems. (a) A classic system with analog demodulator followed by baseband A/D conversion and DSP. (b) An advanced system with IF A/D conversion using digital demodulation and signal processing. (c) An emerging system with RF A/D conversion followed by digital downconversion, demodulation, and basedband signal processing.

A variety of efforts have been made to increase the sampling speed of ADCs over past years, but the evolution of wideband communications systems which take the advantage of the Industrial, Scientific, Medical (ISM) unlicensed frequency bands, especially in the 2.4 GHz band, and possibly in the 5.0GHz band [1], are driving the demands for ADCs with multi-Gsample/s capabilities. However, most ADCs with Gsample/s speed are designed using expensive GaAs-based and InP-based heterojunction bipolar (HBT) processes [2, 3,

4], another drawback of III-V HBT processes is the problematic compatibility with DSP systems realized using silicon CMOS and BiCMOS processes. Further increase in system integration requires that high-speed ADCs be implemented using conventional silicon processes. This thesis is aimed at developing an 8-bit, Gsample/s ADC using a silicon bipolar process.

1.1   A/D Converter Characteristics and Architectures

1.1.1   A/D Converter Characteristics

There are five major characteristics that define the performance of an ADC. The first characteristic is the resolution used to represent the analog signal. A high resolution is desirable since it ensures reduction of noise inherent in the quantization process as illustrated in Fig. 1.2.

V_{FS}: Full Scale Range of the input signal

$V_{FS} = 2^N \Delta$ N: Resolution
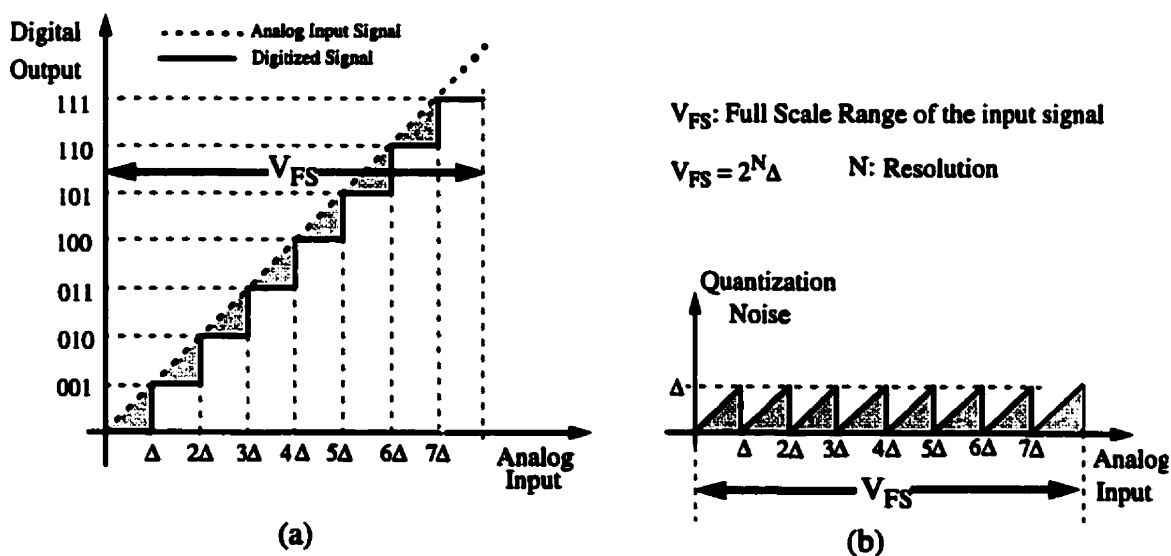
Fig. 1.2. (a) An ideal unipolar quantization operation for a ramp input.
(b) quantization noise

Quantization operation is also characterized by signal to noise ratio (SNR) which is the ratio of the output signal power to the output noise power. The maximum SNR for an N-bit

ideal converter with a sinusoidal input of amplitude equal to $V_{FS}/2$ can be expressed as follows [5]:

$$SNR_{max} = 6.02N + 1.76 \qquad (dB) \qquad\qquad (1\text{-}1)$$

For example, for a 10-bit converter the maximum SNR is 61.97dB. However, in practice, the SNR of most 10-bit A/D converters is not able to reach this number. Using the actual SNR and solving for the equivalent resolution, a figure of merit called the number-of-effective-bits, N_{eff}, can be expressed as:

$$N_{eff} = \frac{SNR_{actual} - 1.76}{6.02} \qquad\qquad (1\text{-}2)$$

The-number-of-effective-bits, sometimes referred to as effective-number-of-bits (ENOB) is a commonly used metric for characterizing the performance of non-ideal quantizers. ENOB or SNR (corresponding to a given ENOB) is the second important characteristic of an A/D converter.

The third characteristic of an ADC is the sampling rate. The sampling rate is the speed at which analog input samples can be continuously converted into a digital word. In most applications the sampling rate of an ADC is determined by the analog signal bandwidth, because the sampling rate has to be at least twice the highest input frequency in accordance with Nyquist's theorem. Power dissipation is the fourth characteristic of an ADC. Typically, high-resolution and high-speed ADCs tend to consume more power than simpler low-resolution designs. Finally, the last characteristic is the chip area which, in general, should be minimum.

1.1.2   A/D Converter Architectures

A variety of architectures exist for implementing ADCs. They are classified as *parallel*, *feedback* and *feedforward* converters [6,]. Each architecture offers specific advantages.

Parallel Converters

Parallel converters such as flash converters are usually used for very high-speed data conversion. Fig. 1.3 presents the architecture of such a converter. In this architecture, an array of comparators simultaneously compares the input voltage with a set of reference voltages. The outputs of the comparators represent the input signal in a set of thermometer codes that can be easily converted into a binary code. Flash converters are inherently fast due to their parallelism. However, this architecture has a significant drawback when a high resolution conversion is desired: namely, the number of comparators grows exponentially with the resolution. In addition, the separation of adjacent reference voltages grows smaller exponentially with the resolution bit. This results in: difficulties in matching components, a very large chip area, a high power dissipation and a large input capacitance that reduces analog input bandwidth. For example, an 8-bit flash ADC with 250 Msample/s sampling rate occupies an area of $31mm^2$ and dissipates 12W of power [7]. Most flash converters available today have less than 8-bit resolution.
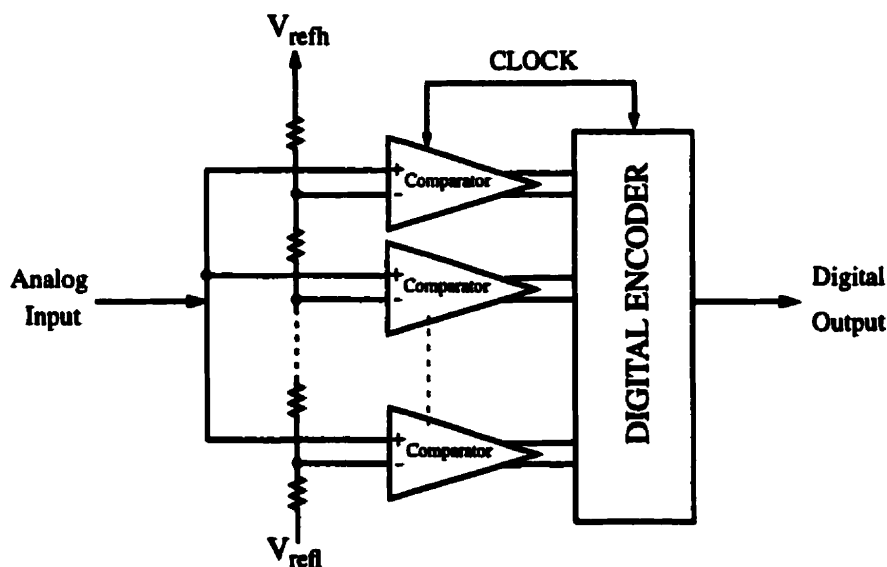
Fig. 1.3. A block diagram of flash converter

Feedback Converters

Feedback converter architectures reduce complexity compared with the parallel approach by utilizing comparators multiple times during each quantization [8-12]. In this architecture as shown in Fig. 1.4, the full N-bit digitizing process is divided into a series of low resolution, m-bit quantizations. Each of these steps begins by amplifying the incoming signal appropriately, followed by a coarse m-bit quantization. The digital result from this operation is applied to a special accumulator called a Successive Approximation Register (SAR), the output of which drives an N-bit D/A converter. The analog output from the DAC subtracts from the input signal to form a residue signal which is ready for the next pass through the feedback loop. The N-bit resolution obtained with this arrangement is governed by N=mp where m is the resolution of the coarse quantizer used, and p is the number of passes around the loop required to produce each N-bit output code. The gain of the amplifier preceding the m-bit quantizer must be increased at each successive pass around the feedback loop to ensure that the coarse quantizer is driven with the proper amplitude. The gain required to meet this condition is:

$$A_V = 2^{m(p-1)} \qquad (1\text{-}3)$$
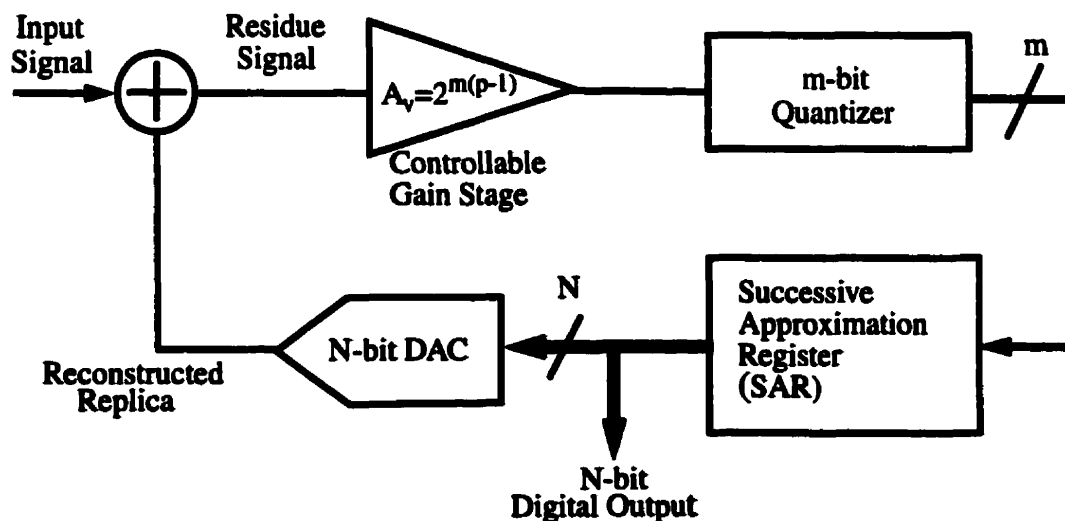
Fig. 1.4. A block diagram of feedback converter

Feedback A/D converters can offer significant hardware savings compared to parallel converters because the coarse quantizer resolution m can be much smaller than the converter resolution N. The severe drawback of the feedback architecture is that it requires p=N/m passes to generate the full N-bit output word, limiting maximum throughput rate, and therefore limiting the speed of conversion. The feedback architecture is an excellent candidate for very high-resolution, low-speed conversions.

Feedforward Converters

Feedforward converters use several stages for one conversion [13, 14]. Each stage consists of an ADC, a DAC and a subtractor, as shown in Fig. 1.5. The ADC converts the input signal and stores the digital value. The digital signal according to this value is reconverted by the DAC and subtracted from the original analog input signal. This residue is again quantized by the following stages. By adding a sample-and-hold (S/H) circuit in the front of each stage, pipelining becomes possible. Using a pipelined approach, only one clock cycle is required for each sample, ensuring a fast sampling rate. The sole disadvantage associated with this approach is the requirement for many S/H circuits. Since analog
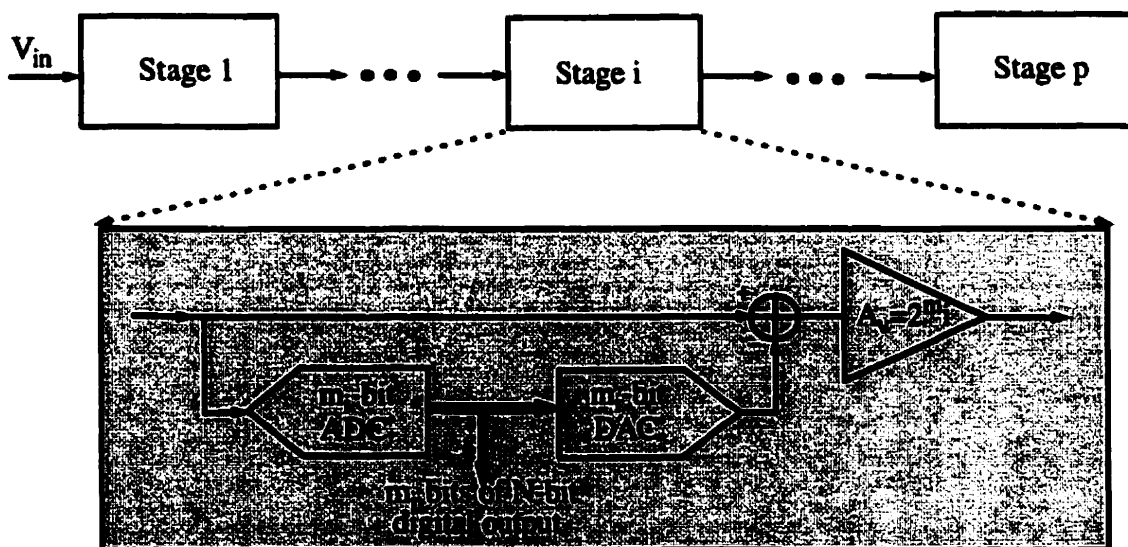
Fig. 1.5. A block diagram of feedforward converter

switches (fundamental to S/H operation) are difficult to implement using bipolar components, most pipelined A/D converters utilize CMOS processes [15-18].

Each of the three converter architectures mentioned above offers a performance trade-off. A designer must choose the appropriate architecture based upon the target specifications and applications. In general, parallel converters are used when low resolution (less than 8-bit) and very high speed is required. Feedback converters are chosen when low speed but very high resolution is required. Feedforward converters are suitable for high speed and high resolution applications.

1.2   Folding-Interpolating A/D Converters

To be used in wideband communications systems, A/D converters must meet very stringent requirements. If the input signal is assumed to lie within the IF/RF band in such applications, sampling rates in the range of 200-Msample/s to multi-Gsample/s are required to satisfy Nyquist's criterion. In addition, a 6 to 10-bit resolution is generally required [2, 19, 20]. However, the resolution and the sampling rate are related. State of the art A/D converters show that the product of the resolution and the sampling rate is roughly a constant for a particular process. The resolution falls off by about 1 bit for every doubling of the sampling rate [21, 22].

The previously mentioned A/D converter architectures are not able to meet the requirements for Gsample/s speed and 8-bit resolution simultaneously. Fortunately, a folding architecture can overcome the drawbacks of parallel converters while retaining the very high speed of parallel converters. A folding A/D converter, shown in Fig.1.6, operates in a similar manner to a feedforward A/D converter by coarsely quantizing the incoming signal and generating a residue signal for further quantization by a lower resolution succeeding stage. However, in a folding converter, the residue signal is formed by a special analog circuit (the Analog Folding Block highlighted in Fig. 1.6) which operates

simultaneously with the coarse quantizer [23-28]. This arrangement obviates the need for a

S/H circuit between the coarse and fine quantizer by forming the residue signal without

going through an A/D-D/A combination with its associated clock delay. The folding

converter, illustrated in Fig. 1.6, corresponds to a 2-stage feedforward implementation with

a $\log_2F$-bit coarse quantizer and an $(N-\log_2F)$-bit fine quantizer, where F is the number of

cycles or defined as the folding rate of the analog folding block. This analog cell, details of

which are described in Chapter 2, performs the function of the DAC and the subtraction

element from the feedforward architecture described previously, but does so without

utilizing a clock, thus enabling simultaneous operation of the coarse and fine quantizers.

Folding can be combined with an interpolating technique to create folding-interpolating

architecture. The architecture offers low complexity along with high-speed operation by

further minimizing the number of folding blocks used in the fine quantizer. The architecture

is an optimum choice for low power dissipation, small chip area and very high speed data

conversions.
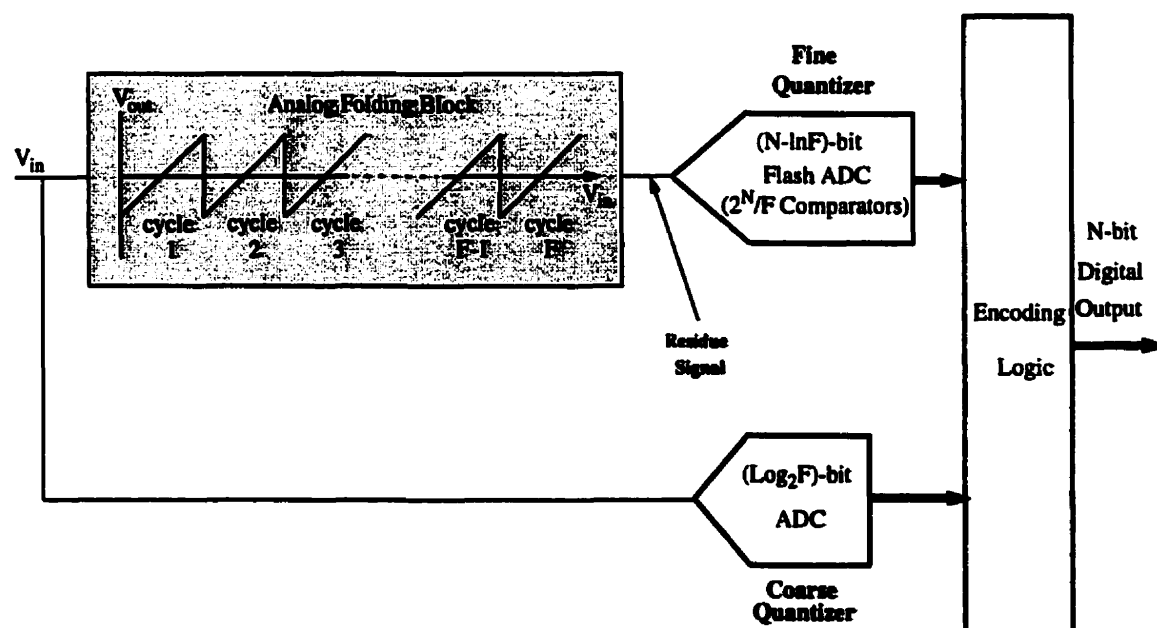
Fig. 1.6. A block diagram of folding converter

1.3 Previous Work on Folding-Interpolating Gsample/s A/D Converters

As discussed in the previous sections, the best option to implement a Gsample/s ADC with 8-bit resolution is the folding-interpolating approach because it retains the very high speed, the characteristic of parallel converters, without penalties on power and area.

A number of folding-interpolating Gsample/s ADCs have been reported and are listed in Table1.1. Most are implemented using expensive GaAs-based or InP-based heterojunction bipolar (HBT) processes, because these processes offer unique characteristics such as a very high cutoff frequency f_T (around 50GHz), low parasitics and good device matching which are all key issues to achieve high-speed and high-resolution ADCs.

Very few Gsample/s ADCs with 8-bit resolution have been implemented on silicon. Van Valburg's [28] design , which is highlighted in Table 1.1, achieves 8-bit resolution and 0.65-Gsample/s speed using a folding-interpolating architecture, but its input bandwidth is limited to 150MHz.

Table 1.1 Reported folding-interpolating monolithic Gsample/s ADCs

Design	Process	Architecture	Resolution (Bit)	Speed (Gsample/s)	Power Consumption (W)	Chip Area (mm^2)
K. Poulton [3]	HBT f_T=50GHz	folding	6	4	5.7	2.7x3.3
H.Kobayashi [4]	HBT f_T=40GHz	folding-interpolating	6	3	4	4.4x4
K.R.Nary [2]	HBT f_T=55GHz	folding-interpolating	8	2	5.3	2.8X3.5

1.4 Thesis Objective and Outline

The main objective of this thesis is to develop an 8-bit, 1-Gsample/s ADC with minimum power dissipation and minimum chip area using the NT25 silicon process. The A/D converter with 8-bit, 1-Gsample/s speed has applications in direct IF sampling receivers for wideband communications systems. Direct sampling receivers offer significant advantages over conventional receivers by digitizing the analog signal at a point closer to the antenna. The receivers offer such advantages as reduced size, weight and power and increased flexibility, functionality and noise immunity [2].

The NT25 process used for this project is provided by Nortel Networks. The process is a 0.5 μm self-aligned, double poly silicon bipolar process with maximum unity gain cutoff frequency f_T of 25GHz*. This process provides NPN transistors, diffused and polysilicon resistors, and triple layer metal interconnection [29].

The target specifications of the converter are listed in Table 1.2. A folding-interpolating architecture was chosen to achieve the desired specifications. Input signal bandwidth was chosen to be greater than 200MHz which covers most of IF frequency band in wideband communications systems.

The thesis is organized as follows. Chapter 2 describes the architecture of the folding-interpolating ADC. It investigates the design of the major building blocks necessary to implement the ADC. Simulation results are presented.

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* The unity gain frequency f_T is 25GHz for a minimum emitter size device ($0.5 \times 1.3 \mu m^2$).

Table 1.2 Target specifications of the A/D converter

ADC	Target Specification
Architecture	Folding-Interpolating
Process	NT25 Si BJT f_T=25GHz
Resolution	8-bit
Sampling Rate	1-Gsample/s
Signal Bandwidth	≥200MHz
Power supply	5V

Chapter 3 presents the layout of the converter implemented using the NT25 process. Some important layout issues are discussed. Experimental results are presented.

Chapter 4 gives a brief summary of what has been achieved and outlines areas for future work.

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CHAPTER 2

8-Bit, 1-Gsample/s Folding-Interpolating A/D Converter Design

2.1 Introduction

As described in Chapter 1, (2^N-1) comparators are required to compare the analog input voltage with (2^N-1) thresholds for an N-bit conversion in a conventional flash ADC. The number of comparators becomes unacceptable when the required resolution is greater than 6. This problem can be overcome by employing a feedforward multi-stage A/D converter which partitions the N-bit quantization into a number of lower-resolution quantizations. In such a converter, shown in Fig. 2.1a, an m-bit coarse quantizer digitizes the input signal with low resolution, and applies the resultant code to a reconstruction DAC. The analog output of the DAC is then subtracted from the original input to form a residue signal, as shown in Fig. 2.1b. This residue is quantized by an n-bit fine quantizer. The advantage of this approach is due to the fact that the combined complexity of the m-bit coarse quantizer and the n-bit fine quantizer can be far less than the complexity of a single (m+n)-bit quantizer. In a folding quantizer, shown in Fig. 2.2, the residue signal is formed with a simple analog circuit, thereby obviating the need for the coarse quantizer, the DAC, and the subtracter components as in Fig. 2.1a. In such an implementation, the low dynamic-range residue signal generated by the analog folding circuit directly drives the fine quantizer.
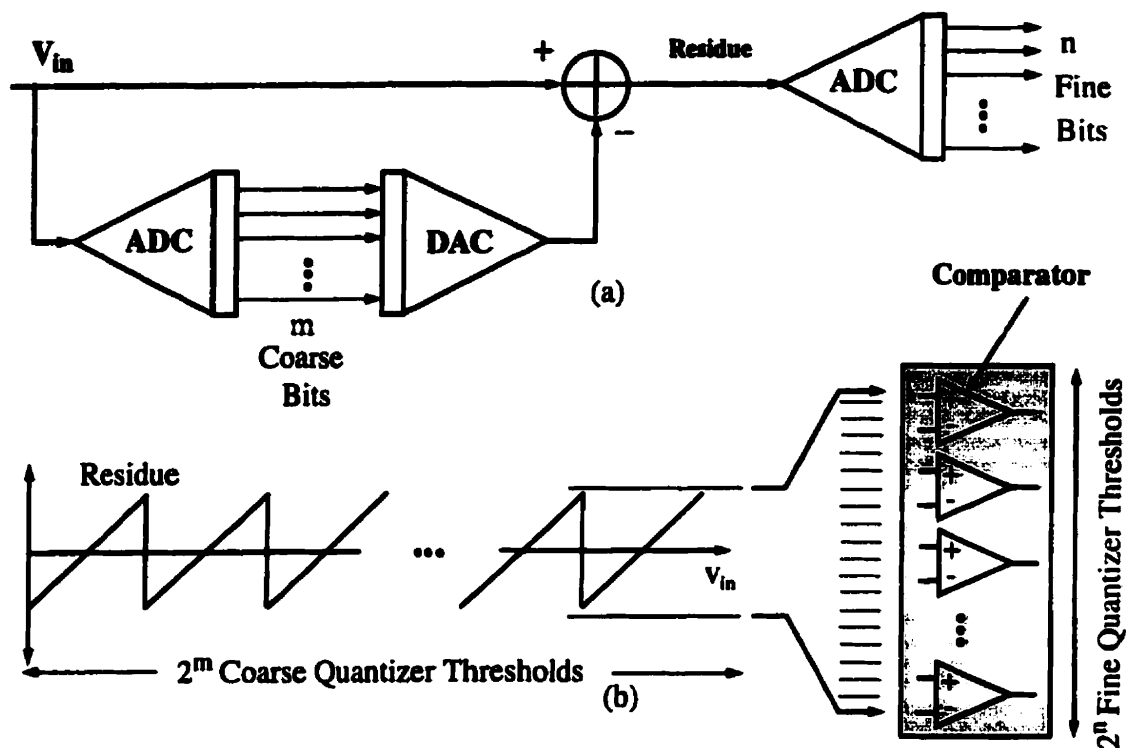
Fig. 2.1: Architecture of a feedforward quantizer
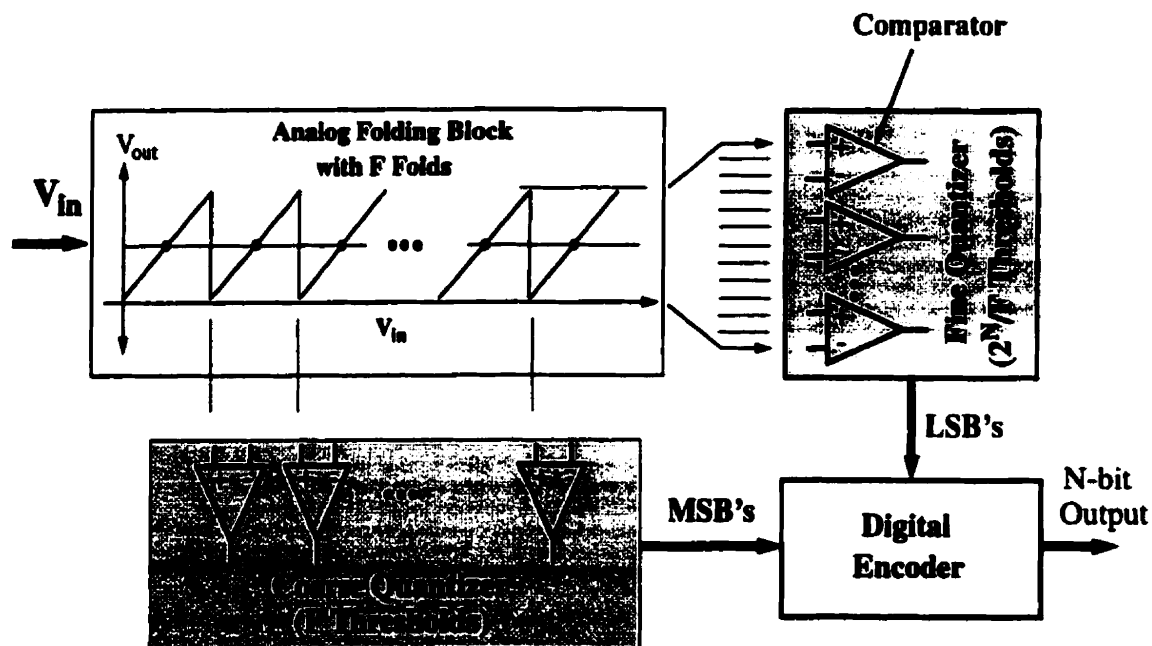
Fig. 2.2. A folding A/D converter architecture. Analog folding with F folds reduces fine quantizer resolution to $\log_2(2^N/F)$

Because of the periodic nature of the residue signal, the digitized output from the fine quantizer is ambiguous, and a coarse converter is still necessary to ascertain in which period the quantizer input signal lies. The input-output characteristics of the analog folding circuit, illustrated in Fig. 2.3, can be parameterized by the number of piece-wise linear segments, or folds; the number of folds or folding rate, denoted as F, determines the resolution of both the coarse and fine quantizers required in a folding A/D converter. Since the coarse quantizer requires F thresholds, its resolution is $m=\log_2 F$ while the fine quantizer requires $2^N/F$ thresholds so that its resolution is $n=\log_2(2^N/F)$. The number of comparators required is therefore reduced by a factor of F. The main disadvantage of folding is the multiple frequency effect inherent in the process.
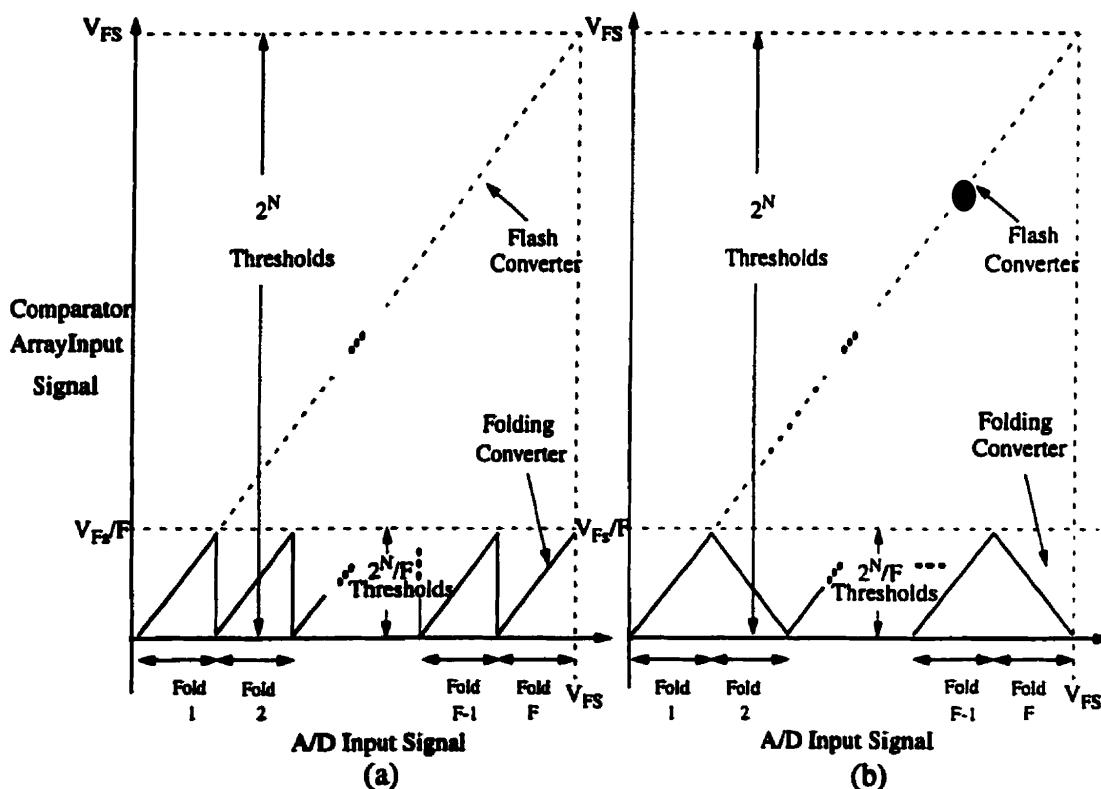
Fig. 2.3. Reduction in dynamic range seen from comparator array
(a) sawtooth folding characteristic, (b) triangle folding characteristic

2.2   Folding and Interpolation Techniques

A folding A/D converter, based on the architecture of Fig. 2.2, would be possible if a simple analog circuit could easily realize the piece-wise linear input-output characteristics indicated in Fig. 2.3. However, because of the discontinuity in the folding transfer function, these types of characteristics are inherently difficult to realize. Several implementations based on the translinear principle have been developed to approximate the triangle wave folding characteristic of Fig. 2.3, but few are used in practice due to the significant drawbacks associated with the very large input swing required for these implementations [1-3]. This voltage swing is unacceptably large for the low-power, high-frequency application considered here.

A folding A/D converter based upon a periodic but not a piece-wise linear folding function can be developed if that non-linear function is periodic and does not saturate. A sinusoidal folding function, shown in Fig. 2.4, serves as an apt example. In this case, the folding characteristic resembles the triangle-wave depicted in Fig. 2.3b; however, the output signal from the folding circuit is not a linear function of the input. Therefore, the fine quantizer must contain thresholds which are not uniformly spaced, but which are located according to an inverse-sine law. This threshold placement is very difficult to achieve in practice, but a simple alternative is to generate many sinusoids uniformly shifted in phase with respect to each other, as shown in Fig. 2.5. In this arrangement, the fine quantizer consists of an array of comparators, each with its reference input grounded so that the quantizer thresholds correspond to the zero-crossings of the sinusoids. Since the sinusoids are equally spaced in phase, their zero-crossings are equally spaced along the analog input range and the quantizer thresholds are located uniformly.
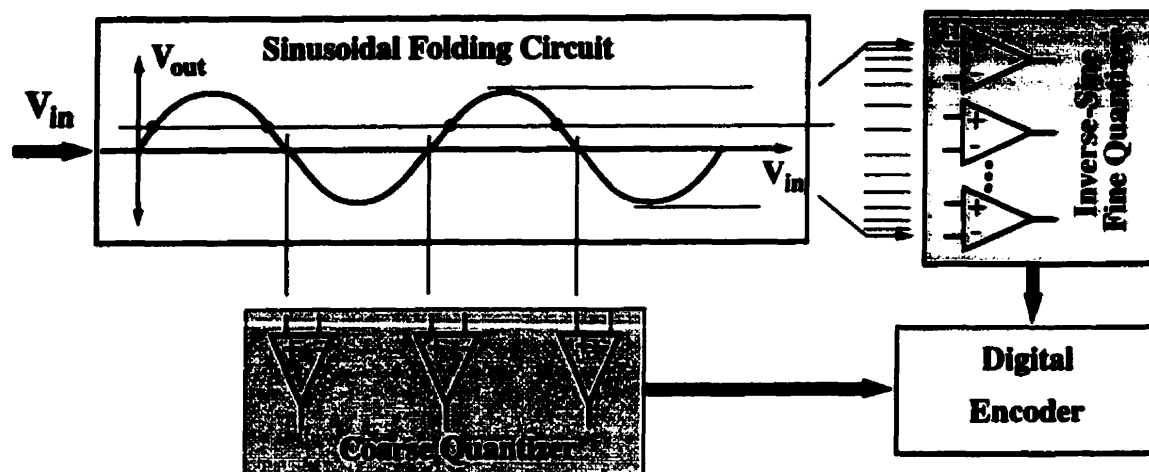
Fig. 2.4. A folding function which is not piece-wise linear
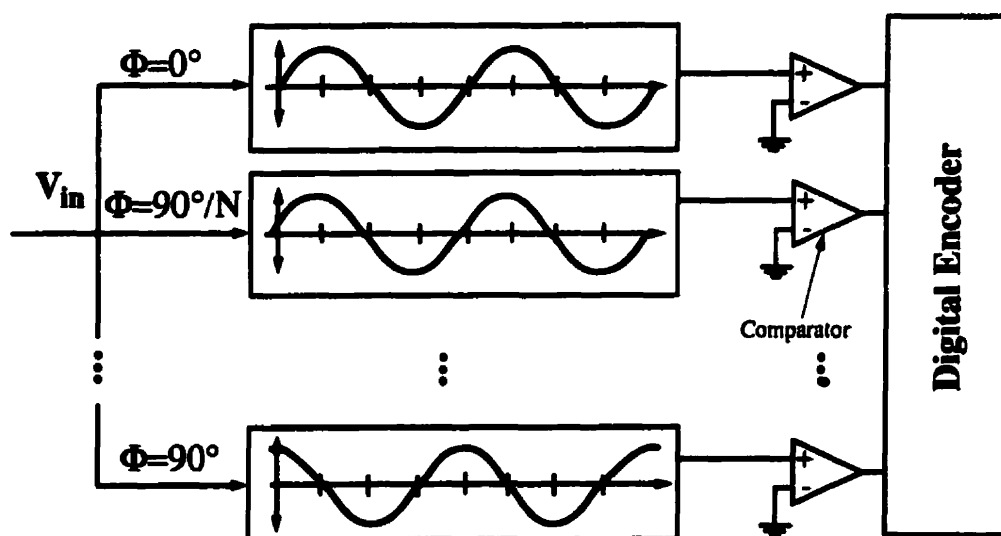
Fig. 2.5. An array of phase-shifted, non-linear folding blocks with
comparators detecting zero-crossings

Generating the phase-shifted waveforms with an array of sinusoidal folding circuits would be very inefficient, but a simplification of the scheme depicted in Fig. 2.5 obviates the need for this type of redundancy. Instead, only two sinusoids are generated, illustrated in Fig. 2.6, and the remaining signals are obtained by linear superposition between them. One technique, illustrated in Fig. 2.6, for achieving the superposition utilizes resistive

interpolation [4]. By appropriately selecting the interpolation resistors, any desirable phase angle can be generated. The folding quantizer architecture presented in Fig. 2.6 is simple and potentially very efficient and is the one used in this work.
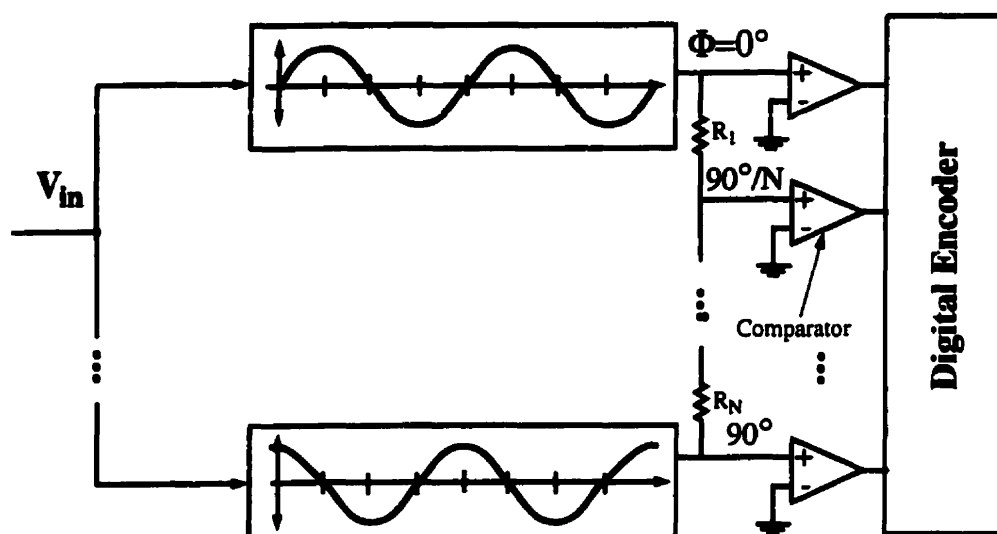
Fig. 2.6. Linear superposition using resistor string to generate multiple sinusoids equally spaced in phase from two quadrature

2.3 Block Diagram of the 8-Bit Folding-Interpolating ADC

Fig. 2.7 shows the block diagram for an 8-bit folding-interpolating converter. The input signal drives 4 folding blocks with a folding rate of 8, and a coarse quantizer. A reference ladder is used to generate a set of reference voltages. The 4 folding blocks governed by the appropriate combination of the reference voltages produce sinusoidal signals phase-shifted by 45°. These sinusoidal signals are applied via buffers across differential interpolation resistive strings to create an array of 32 equally phase-shifted sinusoids. After interpolation, 32 wave patterns are available, and contain all the information to define 5 fine bits and the MSB-2 bit. A comparator array is then utilized to translate the analog information into digital data. Additionally, a 2-bit coarse quantizer operates simultaneously to identify in

which cycle of the folding characteristic the input signal lies. Finally, a digital encoder is required to obtain the 8 binary digital codes.

The design of each building block will be investigated individually in the following sections. The simulated performance will also be presented.
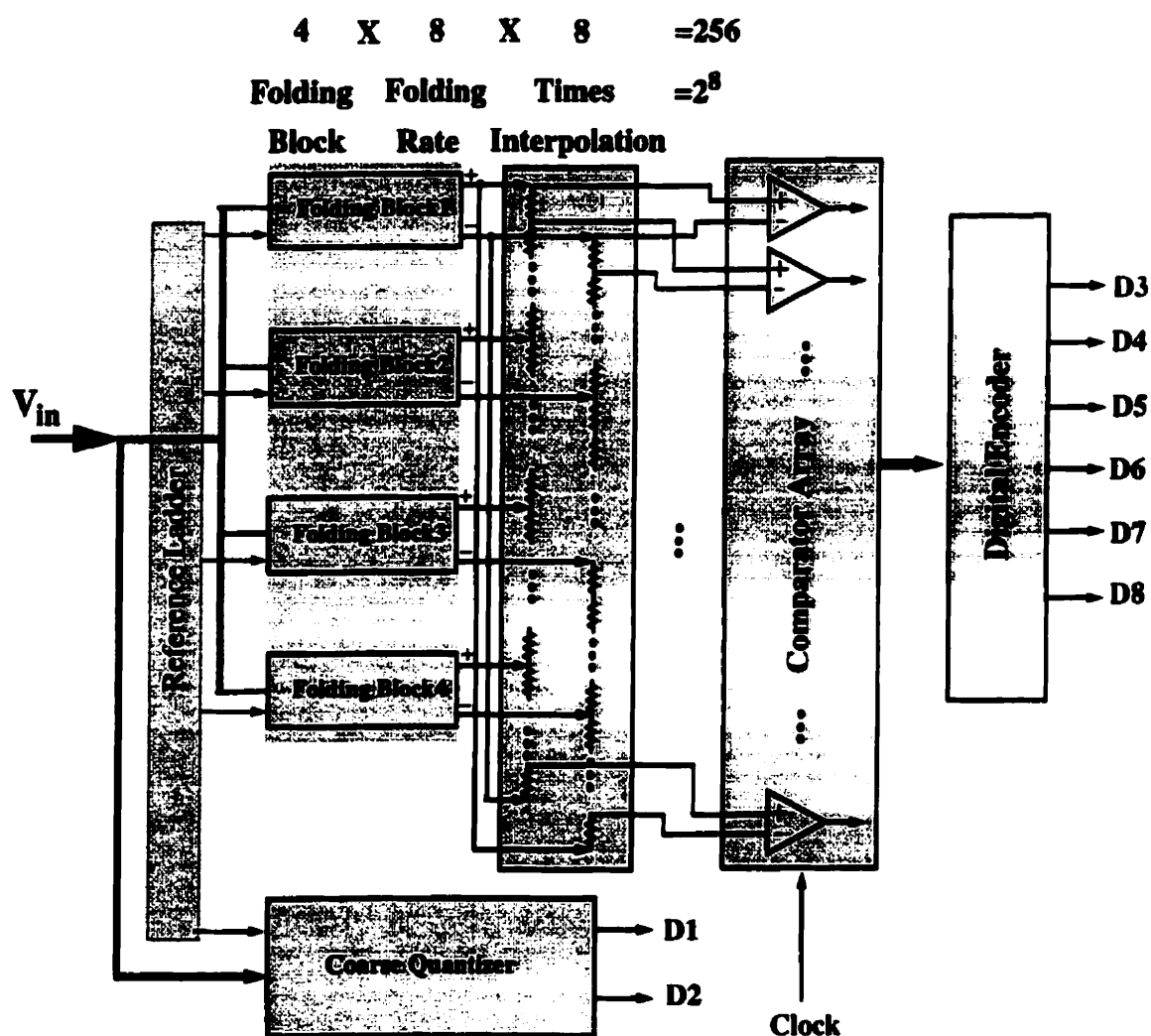
Fig. 2.7. Block diagram of the 8-bit folding-interpolating ADC

2.4 Folding and Interpolating Block

The folding-interpolating block is one of the most crucial parts of the A/D converter since it largely determines the overall performance of the system. For example, the speed and the bandwidth of the A/D converter are affected by the bandwidth of the folding circuits. Moreover, the accuracy of the A/D converter is dominated by the folding circuits in which the correct zero-crossing points must be generated to meet the required resolution. In this section, design of the folding circuit to achieve high speed and high resolution will be considered. In addition, resistive interpolation will be discussed.

2.4.1 Design of the Folding Circuit

Although a variety of circuit topologies could be used to realize the folding operations [1-3], one with good frequency performance must be chosen to meet the required 1-Gsample/s speed and 8-bit resolution. The circuit shown in Fig. 2.8a offers a good frequency response and uses an emitter-follower wired-OR configuration at the differential pair outputs [5]. The emitter followers reduce the capacitive load at output nodes, thus improving the settling behavior of the circuit. Additionally, the emitter-followers in this configuration offer a good driving capability.

By appropriately selecting the reference voltages V_{r1}, V_{r2}, V_{r3} and V_{r4}, a good approximation to a sinusoid can be obtained, as shown in Fig. 2.8b. An appropriate difference between the reference voltage values is a few times the thermal voltage V_T. This difference is chosen to be 125mV so that total input voltage swing is on the order of 1V for an 8-fold circuit [6].

A multiple-frequency effect exists inherently in the folding processing due to the nonlinear periodic folding operation; namely, the frequency of the folded signal is a multiple of that of the input signal. This imposes an extra requirement on the bandwidth of
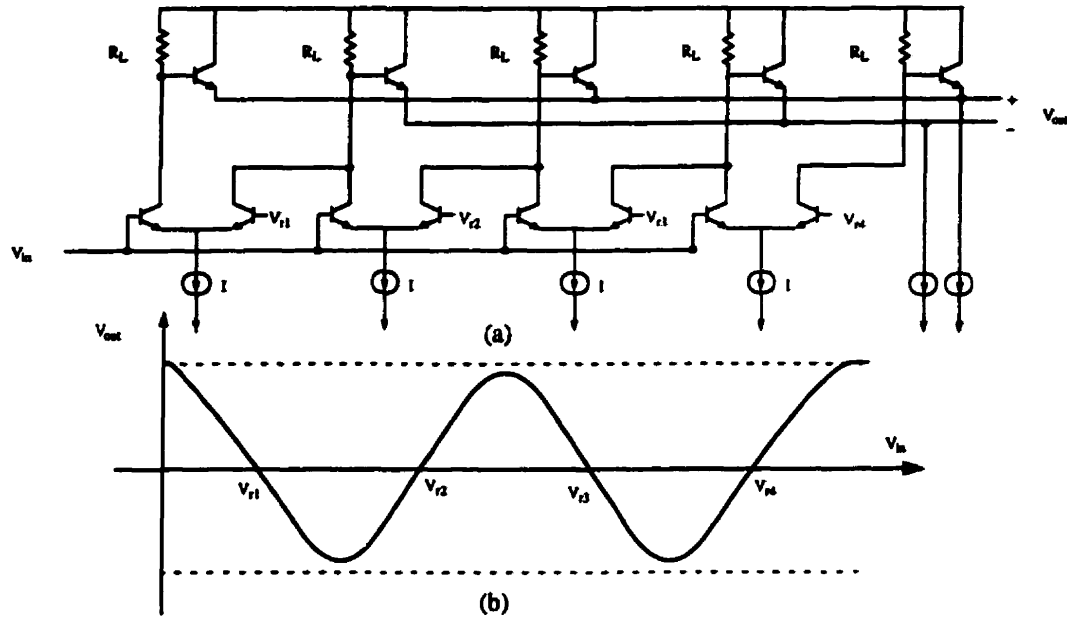
Fig. 2.8. (a) Folding circuit based on wired-OR interconnection (b) output
waveform of the folding circuit

folding circuits, especially for wideband applications. The circuit architecture and bias conditions of the transistors in the circuit play an important role in determining the circuit bandwidth. The option of bias conditions is a trade-off between the bandwidth and power consumption. In addition, the bandwidth of the circuit in Fig. 2.8a is inversely proportional to the value of R_L. A large R_L gives rise to a serious analog bandwidth limitation. However, to reduce the sensitivity to offset in the rest of the converter, the value of the resistor R_L has to be large enough to obtain a large output voltage.

To ensure that the A/D converter achieves the required 8-bit resolution, the accurate zero-crossing points must be generated by the folding circuits. In addition, the shape of the sinusoid-like waveform must have a high linearity around the zero-crossing points because linear interpolations between two adjacent folding signals are desired, as depicted in Fig. 2.9. A modification to the circuit in Fig. 2.8 is therefore made. In this design emitter degeneration resistors R_E are used to improve the linearity. The final circuit used in this design is shown in Fig. 2.10. Moreover, to enlarge the linear range of the input and output

voltage swings, the current source I in Fig. 2.8 can be split into two equal current sources I/2 that directly flow from the two transistors in the differential pairs as shown in Fig. 2.10. Note that 8 reference voltages are required in Fig. 2.10 because a folding rate of 8 is used.
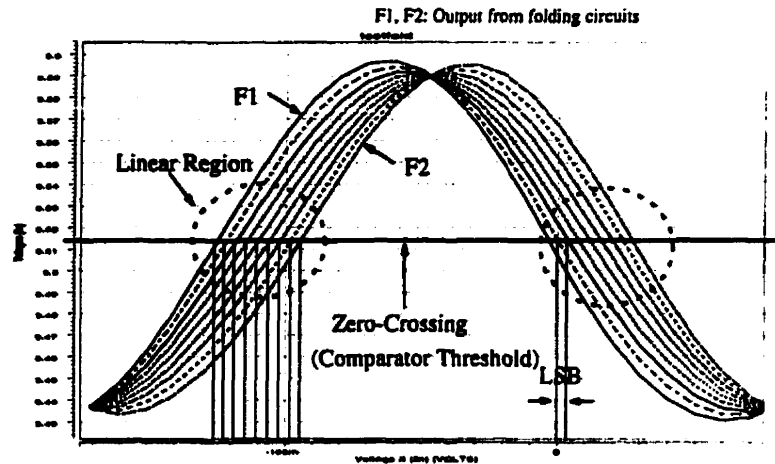
Fig. 2.9. Linear interpolation between the outputs from 2 folding blocks
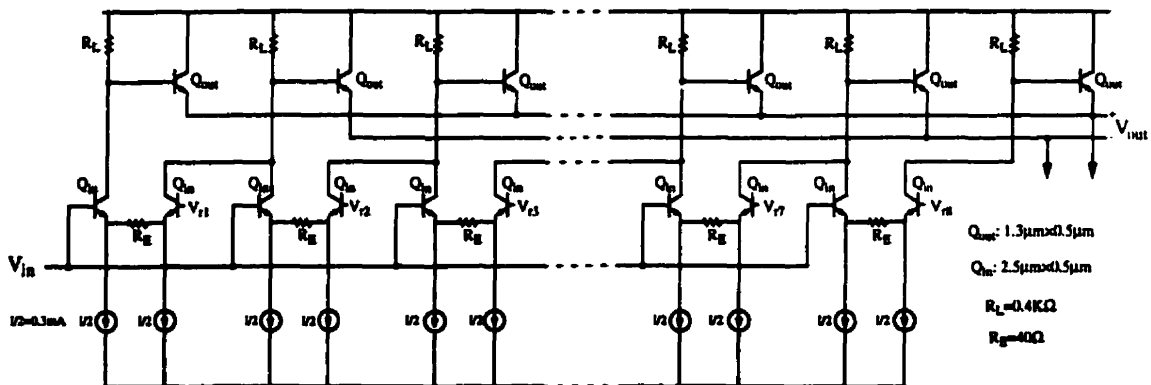
Fig. 2.10 Improved folding circuit using emitter degeneration resistors

Fig. 2.11 presents the simulated improvement in the interpolation errors after using emitter degeneration resistors. The interpolation errors are limited to ±0.6mV which is quite acceptable for the 8-bit resolution required.

Another design issue related to improving the accuracy of the ADC is to minimize the mismatch in the input differential pairs in the folding circuits. In addition to special attention paid to the layout as discussed in Section 3.2.1, another measure taken in this design is to increase the size of the input transistors to minimize the mismatch and to reduce the noise.
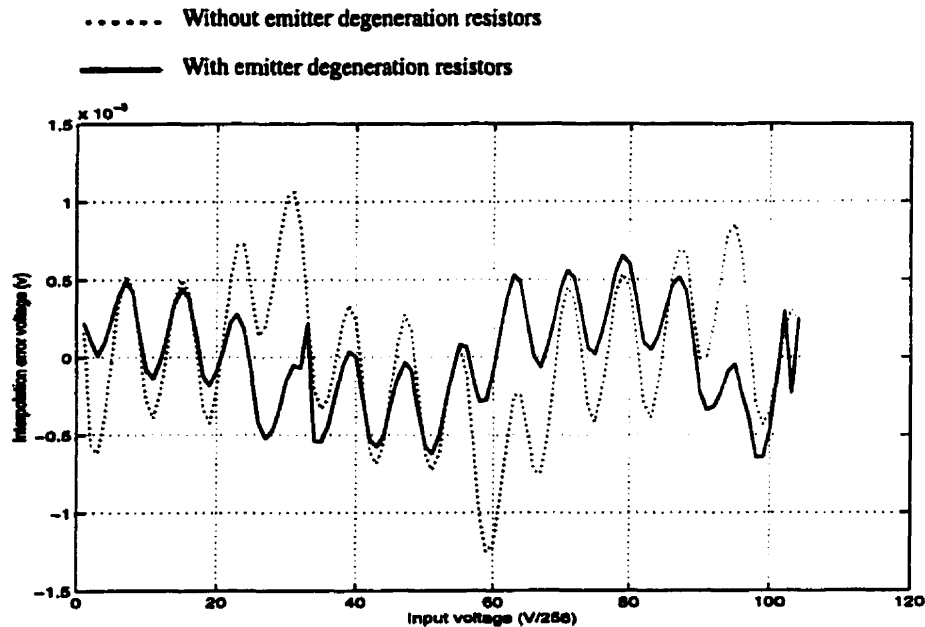
Fig. 2.11. Interpolation error reduced using emitter degeneration resistors

Since the phase of the resulting waveform is governed by the values of the reference voltages, the second folding circuit, whose output is $45°$ shifted from the first one, can be easily constructed by changing the combination of the reference voltages. The same procedure can be used to generate the combination of the reference voltages for the third and the fourth folding blocks. The combinations of the reference voltages for all 4 folding blocks are listed in Table 2.1.

Fig. 2.12 shows the simulated 4 pairs of differential outputs from 4 folding blocks. The phase difference between adjacent folding outputs is $45°$ corresponding to an $1/32V$ offset in the reference voltages as listed in Table 2.1. These 4 signals and their differential

counterparts are utilized to generate the 32 sinusoidal signals and their differential ones by further interpolations.

Table 2.1 The reference voltage values of folding blocks

Reference Voltage (V)	Folding block 1	Folding block 2	Folding block 3	Folding block 4
V_{r1}	-3/8	-11/32	-10/32	-9/32
V_{r2}	-2/8	-7/32	-6/32	-5/32
V_{r3}	-1/8	-3/32	-2/32	-1/32
V_{r4}	0	1/32	2/32	3/32
V_{r5}	1/8	5/32	6/32	7/32
V_{r6}	2/8	9/32	10/32	11/32
V_{r7}	3/8	13/32	14/32	12/32
V_{r8}	4/8	17/32	18/32	19/32

Fi and $\overline{Fi}$: differential outputs form folding block i
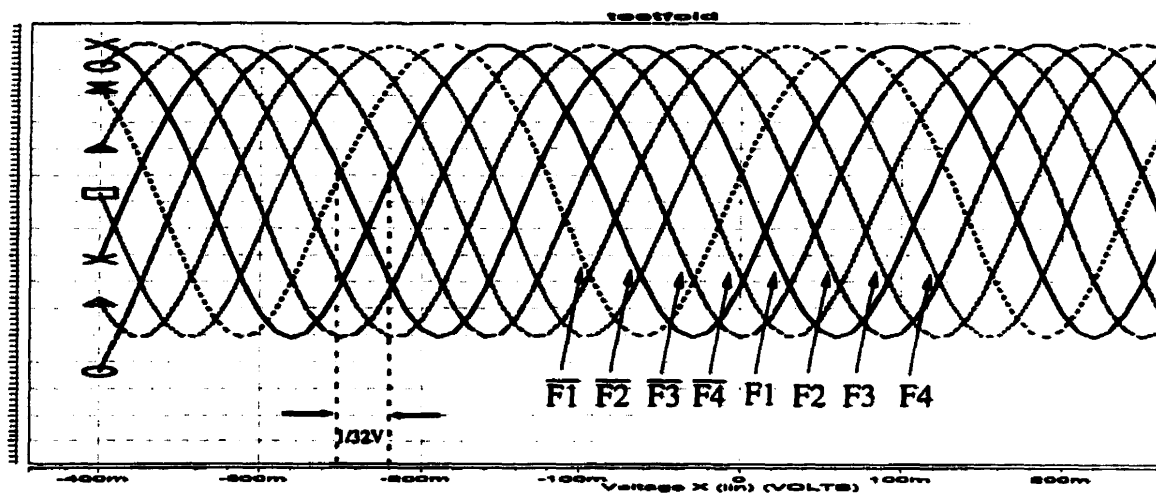
Fig. 2.12. Simulation outputs from 4 folding blocks

2.4.2   Interpolation

The interpolation is implemented using a resistive string because of its simplicity and power-efficiency [7]. In this design, a more detailed diagram of Fig. 2.7 is redrawn in Fig. 2.13. Differential interpolations are implemented by applying the differential outputs of the
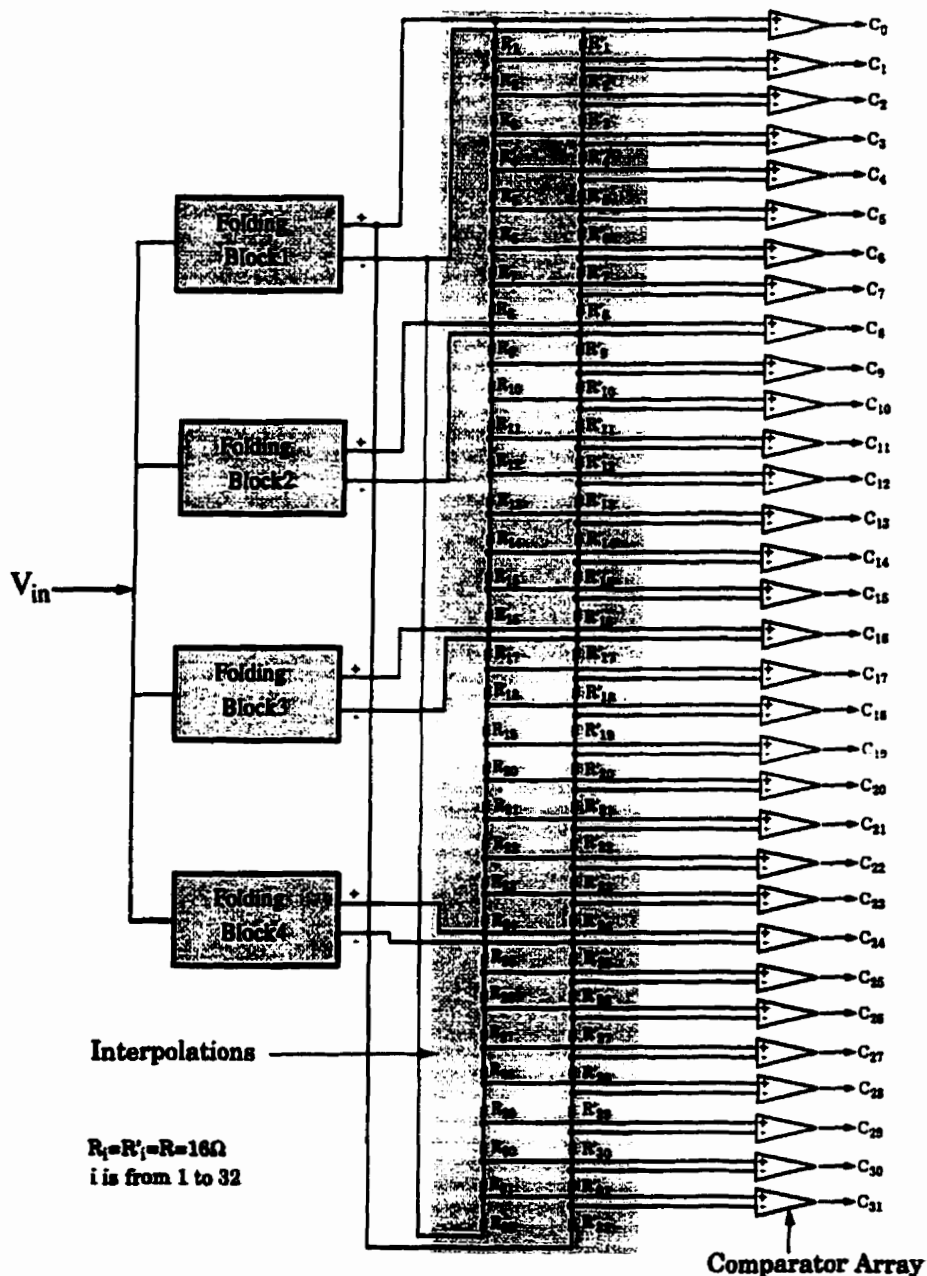
Fig. 2.13. Block diagram of the folding interpolating blocks

folding blocks to the differential resistive strings. The differential implementation improves the accuracy of the converter since the comparator operates on the difference between signals and not on the absolute value of the signal.

Fig. 2.14 shows simulated outputs after differential interpolation between outputs from two folding blocks. The 32 wave patterns can be generated after interpolations among 4 folding blocks as depicted in Fig. 2.13. These 32 signals and their differential counterparts contain all the information to define the fine 5 bits and MSB-2 bit.

Fi and $\overline{Fi}$: differential outputs form folding block i
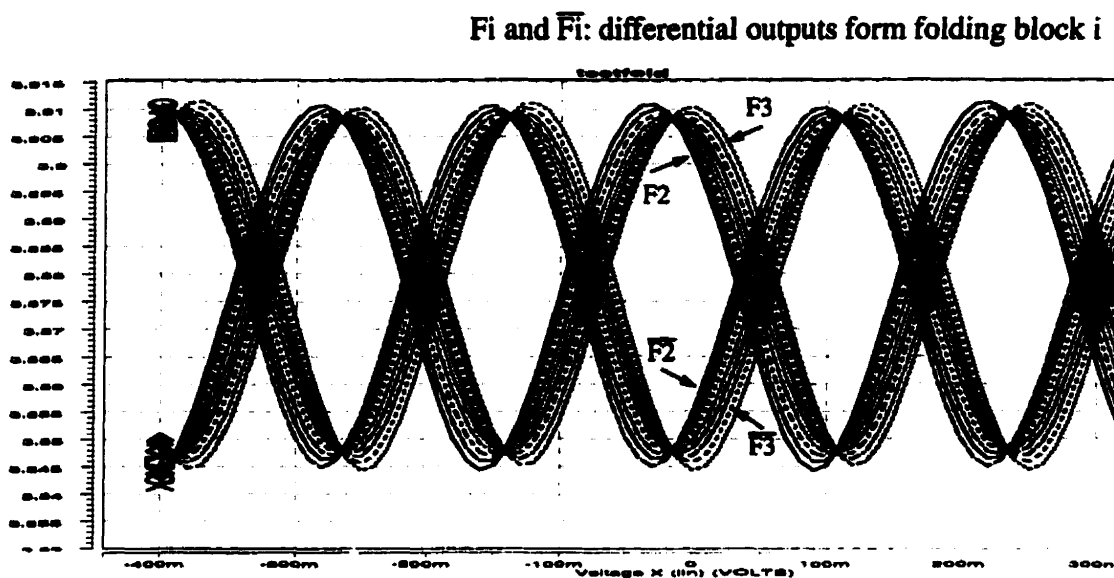
Fig. 2.14.   Simulation outputs from differential interpolations

2.4.3   Reference Ladder

Precise reference voltages are required to ensure accurate zero-crossing points and the accuracy of the converter. The set of reference voltages is usually generated through a resistive ladder, as depicted in Fig. 2.15. Input bias current flows into each differential pair in the folding circuits due to the non-zero base current I_b of a bipolar transistor. This current flows through the resistive ladder, thereby causing voltage fluctuations which perturb the equally-spaced reference voltages from their ideal positions. This well-known effect is

called "reference-bowing" because the reference voltages vary from their ideal positions according to a parabolic or bowed pattern [8]. The deviation of the reference voltages thereby corrupts the desired zero-crossing positions. The way to minimize this deviation is to ensure that the bias current I_{bias} in the resistor ladder is at least two orders of magnitude greater than the input bias current I_b in the differential pair [8]. Therefore, the deviations caused by the input bias current are at an acceptable level.
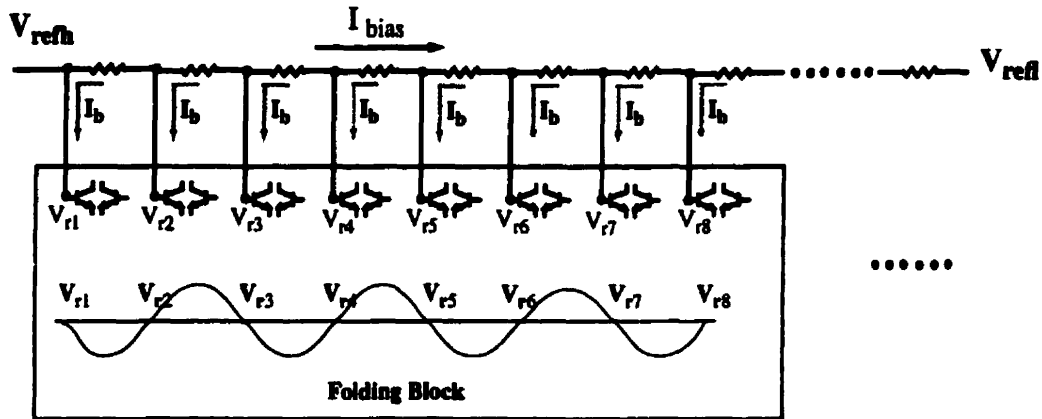
Fig. 2.15. Deviation of reference voltages caused by input bias current I_b

In addition to the "reference-bowing" effect, another important issue is to minimize the mismatch among the resistors. This will be discussed in Section 3.2.1.

2.5 High-Speed Comparator

As shown in the block diagrams of the A/D converter in Fig. 2.7 and the folding interpolating block in Fig. 2.13, the differential voltage signals coming from the interpolation stage need to pass through an array of comparators. Each comparator should be able to produce a correct digital "high" or "low" depending on the polarity of the given differential signals at the required speed.

Fig. 2.16 shows the topology of the comparator used in this design [9]. A 2-stage preamplifier is used before the latch section. Such a comparator architecture offers the

advantages of suppressing the kickback noise to an acceptably low level and providing a relatively high gain, which in turn lowers the offset contributed by the latch, and therefore improves the metastability behavior of the comparator. The emitter followers Q_9 and Q_{10} used in the latch section offer a low output impedance for driving the following stage and improve the capacitance loading effect at output nodes, thus enhancing the speed of the comparators. In addition, the emitter followers offer the isolation of any possible unbalanced interference from the succeeding stages.
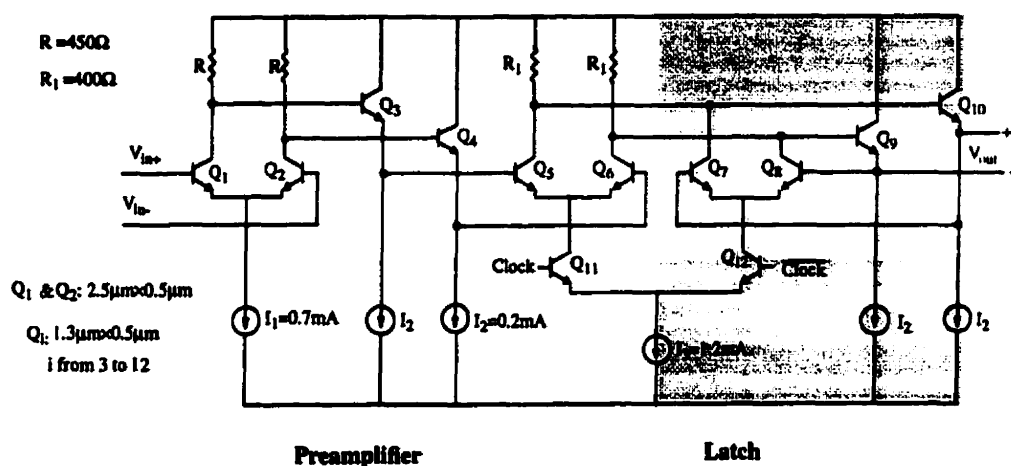
Fig. 2.16.   2-stage preamplifier comparator circuit

Since 32 comparators are required to implement the A/D converter, the optimum power dissipation of each comparator must be investigated. Moreover, in order to minimize the response time mismatch among the comparators, special attention must be paid in the layout as discussed in Section 3.2.2.

A master-slave comparator is used to hold the digital value once the comparator goes to the track mode. Such a master-slave comparator includes two identical comparators clocked 180 degrees out of phase, as shown in Fig. 2.17. The function of this master-slave comparator can also be observed in the simulation results shown in Fig. 2.18. It can be seen that when the master comparator goes into track mode, the slave holds its digital value; and

when the master comparator goes into the latch mode, the slave retains (or holds) its value unchanged until the result of the comparison of the voltages at the master input changes. The simulated results also show that the comparator is able to operate at 1-Gsample/s speed.

Preamplifier   Master   Slave
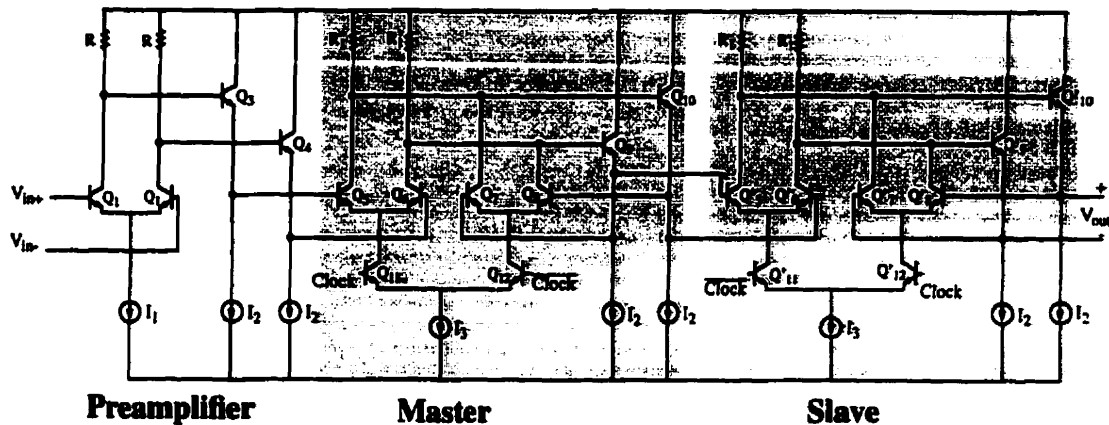
Fig. 2.17. 2-stage preamplifier master-slave comparator circuit
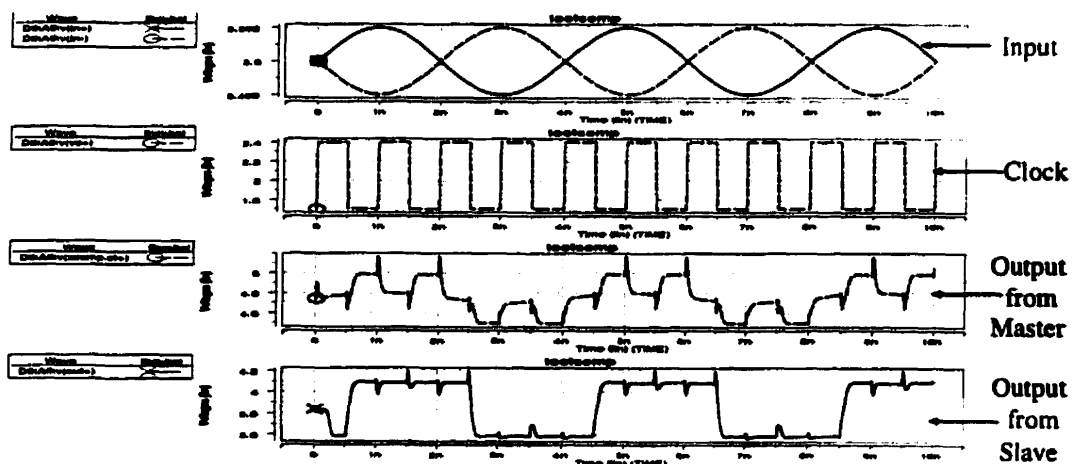
Fig. 2.18. Input signals (top), clock signal (2nd), simulation output from the master comparator(third), simulation output from the slave comparator (bottom)

2.6   Digital Encoder for 5 Fine Bits

Fig. 2.19 shows the block diagram of the encoder used in this design. The encoder
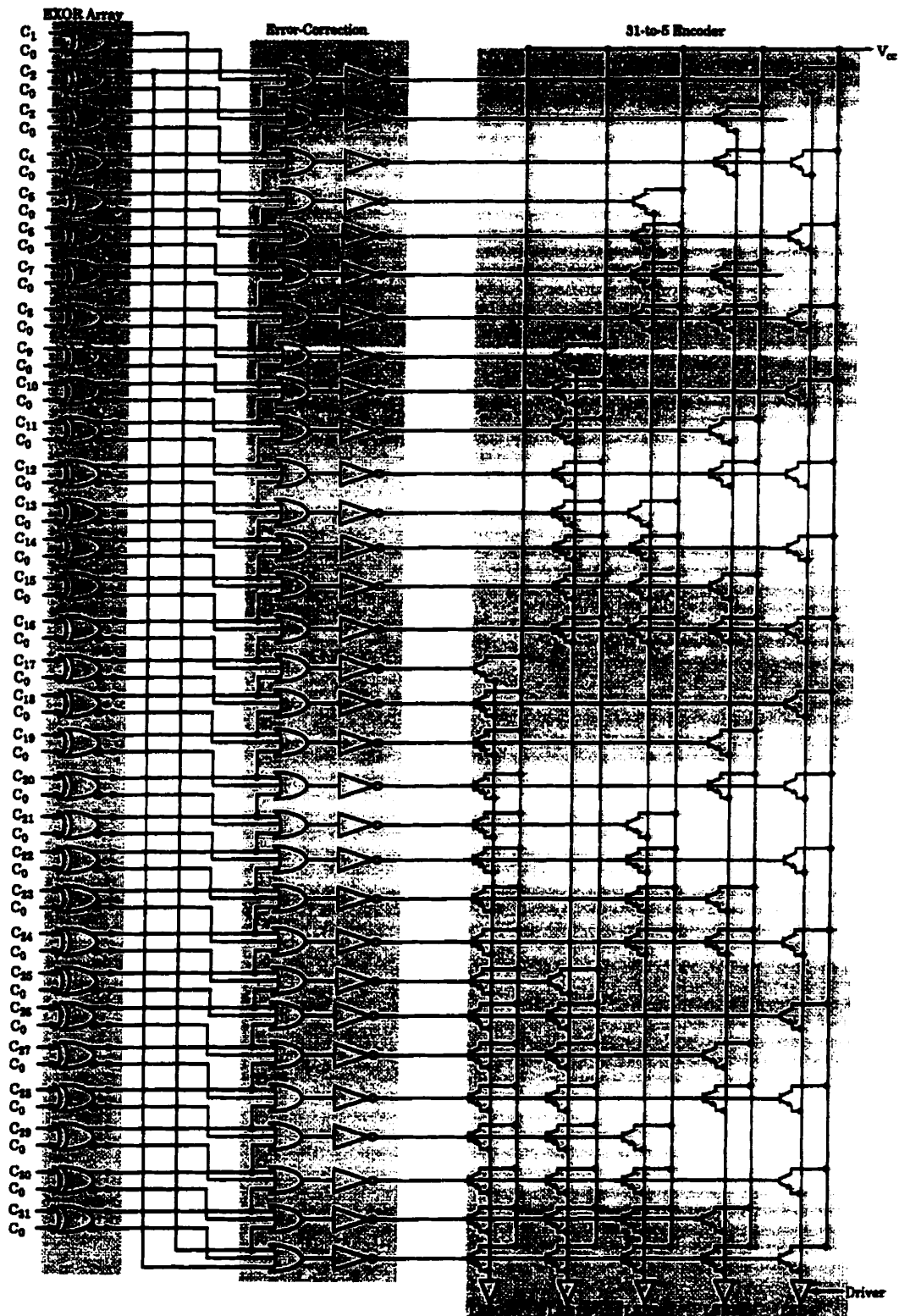
Fig. 2.19.   Block diagram of the 5-bit encoder

comprises 3 function blocks. They are an EXclusive-OR (EXOR) array, an error correction stage, and a 31-to-5 encoder. After the comparator stage, the digital combinations of 32 "ONE" and "ZERO" are obtained. Such combinations must be encoded into a binary code.

Because of the repetitive nature of the folding signals, a circular code, instead of a linear thermometer code, is obtained. Table 2.2 lists the representation of the numbers from 0 to 7 using circular code and thermometer code respectively. When encoding such a circular code, the transition between a group of ONE's and a group of ZERO's must be defined first. An EXOR operation is performed to realize this transition [10]. Fig. 2.20 shows the configuration of such a differential EXOR circuit [5]. Minimum size transistors are used to reduce the chip size. Fig. 2.21 shows the simulated results for the differential EXOR gate.

Table 2.2 Thermometer and circular code representation of the numbers 0-7

	Thermometer	Circular
4	0001111	1111
5	0011111	1110
6	0111111	1100
7	1111111	1000
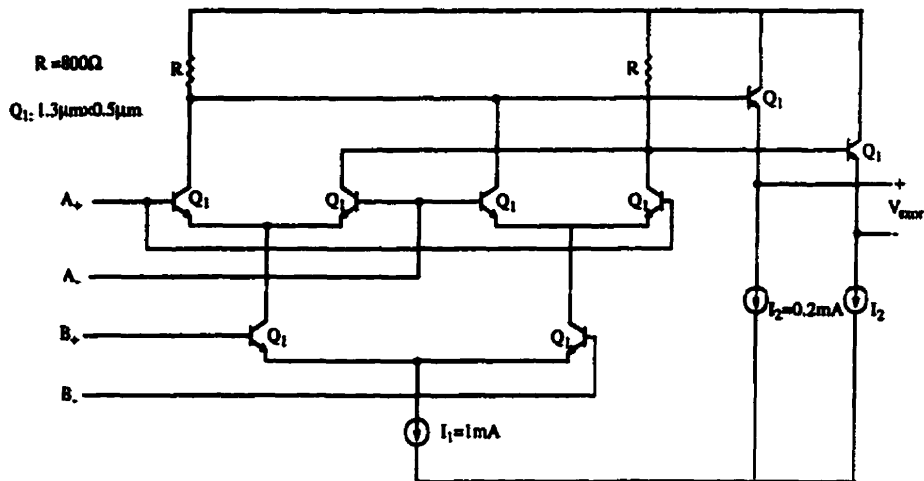
Fig. 2.20. EXOR circuit
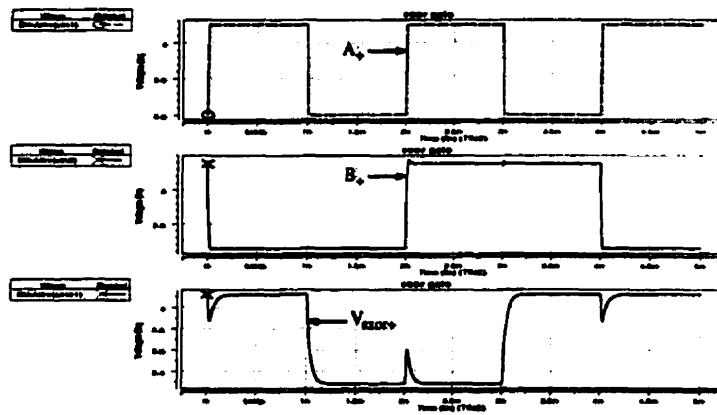
Fig. 2.21. Simulation output waveform from the EXOR gate. Two inputs
(Top), EXOR Output (Bottom)

After the EXOR stage, a thermometer-like codes are obtained. An error-correction stage (OR gates and inverters) [8, 11] is used to correct any inconsistencies due to comparator metastability, noise and cross talk. A 3 input OR gate is used in this design. The thermometer codes must be encoded into the corresponding 5-bit binary code. This is accomplished by a 31-to-5 OR ROM encoder [10] as shown in Fig. 2.19. In the design of the encoder, special attention is needed to achieve the required speed of each gate while

using minimum power in order to keep the power consumption of the overall system as low as possible.

2.7 The Coarse Quantizer

The block diagram of the coarse quantizer is highlighted in Fig. 2.22. A buffer and a comparator are utilized to generate the MSB. MSB-1 is produced by employing a folding block with folding rate equal to 4 and a comparator. Fig. 2.23 shows the outputs from the MSB-1 folding block. MSB-2 can be obtained directly from the fine quantizer without using any additional circuitry.
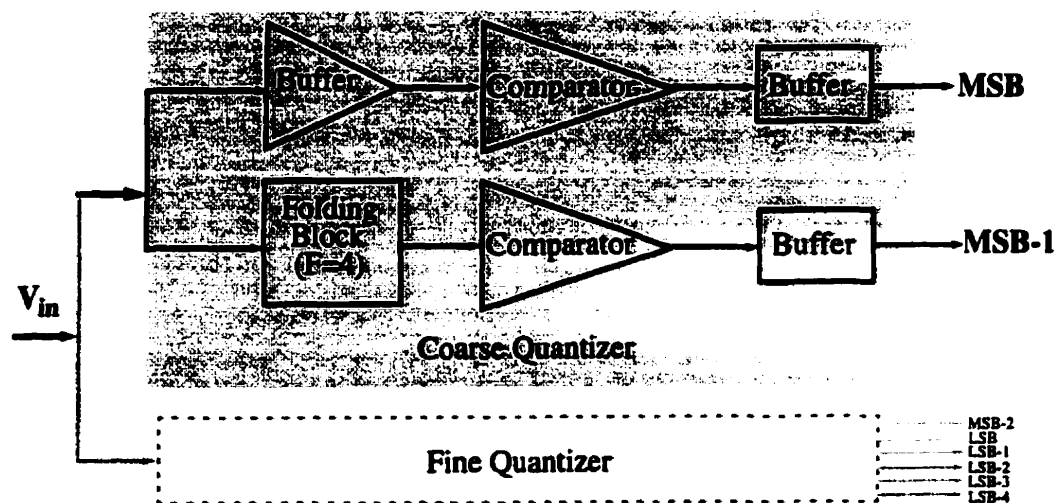
Fig. 2.22. Block diagram of the coarse quantizer
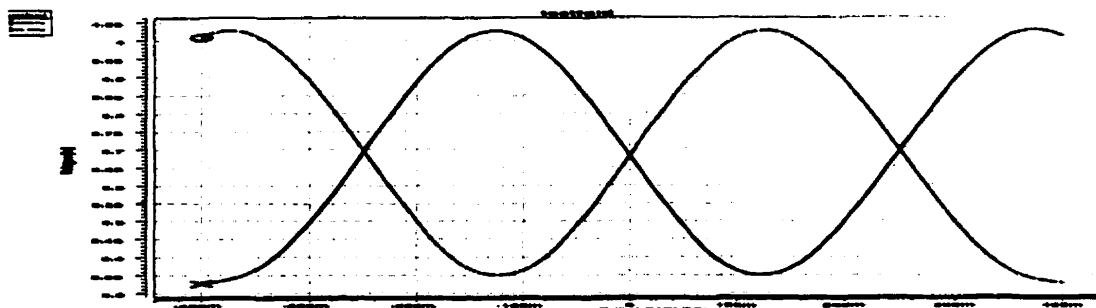
Fig. 2.23. Simulation outputs from MSB-1 folding block

Even a very small voltage offset or timing mismatch between the coarse and fine quantizers can result in large errors. As illustrated in Fig. 2.24, a small misalignment at the MSB transition results in a significant error. Therefore special attention must be paid to ensure equal delays for the MSBs generated by the coarse quantizer and the LSBs produced by the fine quantizer. The extra buffers after the comparators in the coarse quantizer in Fig. 2.22 are used to achieve the equal delay in this design.
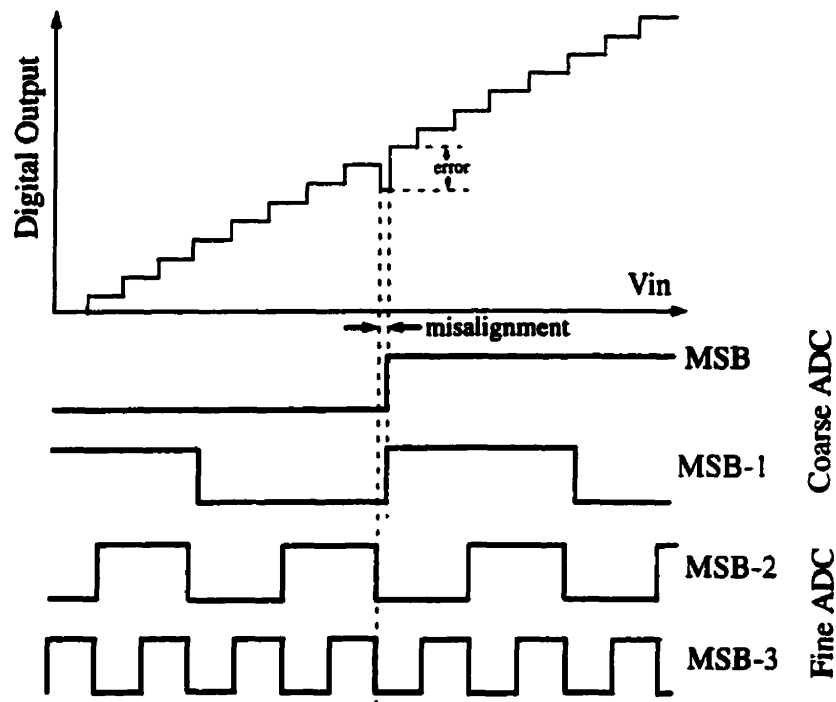
Fig. 2.24. Misalignment between a coarse ADC and a fine ADC

2.8 System Simulation

The whole system simulation was conducted by combining all the circuit blocks together, including the bias circuits. The Fast Fourier Transform (FFT) test approach was used to characterize the performance of the ADC and evaluate how well the converter transforms a known analog input signal into digital data. A pure sinusoid input is commonly used for this test. After converting this signal, the frequency components of the digital

output stream are determined by performing a discrete Fourier Transform. Ideally, except for quantization noise, the transform will indicate that the digital waveform of the converter has only one spectral component, the component which corresponds to the input signal. Any nonlinearities in the converter's transfer function will result in spectral frequencies other than the input frequency being present in the Fourier transformed data. By examining the spectral content of the output digital waveform, the SNDR (or ENOB) of the ADC can be determined.

One advantage of the FFT test is that all error sources are included in the results. In addition, the performance of the A/D converter at its specified sampling rate and input bandwidth can be easily examined.

The typical configuration for FFT testing is illustrated in Fig. 2.25. An ideal sinewave signal is applied to the A/D converter under test. The performance of the ADC is simulated using HSPICE. The digital data stream obtained from HSPICE is converted to an analog signal through an ideal DAC constructed by a program. The SNDR (or ENOB) of the system can be obtained by performing the FFT analysis of the reconstructed analog signal through MATLAB. Fig. 2.26 shows that the simulated ENOB at different input frequencies when the A/D converter is clocked at 1-Gsample/s.
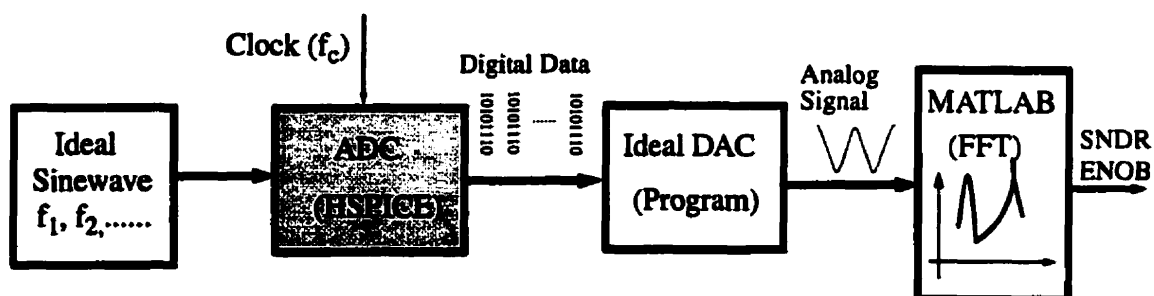
Fig. 2.25. Dynamic performance of the ADC simulation setup
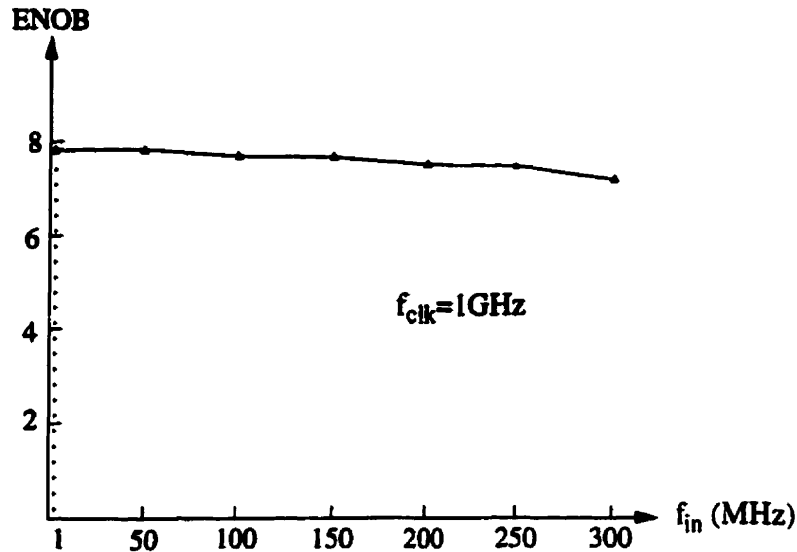
Fig. 2.26. Simulation dynamic performance of the ADC, input at full scale

Due to constraints on simulation time, memory and diskspace, the simulations of the ENOB (or SNDR) of the ADC did not include layout parasitics.

Based on the simulation results of the A/D converter, the ADC is expected to achieve an ENOB greater than 7.5bit when input frequency is less than 300MHz. The total power consumption is 2.75W. The expected characteristics of the ADC are listed in Table 2.3. However, due to the fact that the ADC operates at very high frequency, its experimental characteristics will be affected by parasitics and component mismatches. In particular, a decrease of the ENOB is expected.

Table 2.3 The ADC Characteristics

Parameter	Simulation Results
Technology	NT25, 0.5μm Si BJT f_T=25GHz
Resolution	8-bit
Sampling Rate	1-Gsample/s

Table 2.3 The ADC Characteristics

Parameter	Simulation Results
Signal Bandwidth	≤300MHz
ENOB	7.7-bit
Power Dissipation	2.75W
Chip Area	2.5mm×3.5mm

2.9 Summary

In this chapter, the architecture and design of the 8-bit, 1-Gsample/s folding-interpolaing A/D converter was described. The design of each individual circuit block in the A/D converter was discussed. The simulation results for each of the circuit blocks and the entire ADC were presented.

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CHAPTER 3

The A/D Converter Implementation and Experimental Results

3.1 Introduction

This chapter deals with the implementation and test of the A/D converter designed in Chapter 2. Layout techniques used to achieve the required performance is discussed. Experimental results verifying the functionality and testing of the high frequency performance of the A/D converter are also presented.

3.2 Layout of the ADC

The A/D converter relies on the layout to meet the stringent requirements on speed and resolution of the design. An appropriate layout not only maximizes the yield but also is the only way to achieve the required specifications predicted by simulations. Special attention was given to the component matching, and wiring of signal and clock paths. Since the ADC is a mixed-signal circuit, issues related to the noise-rejection were also considered.

3.2.1 Component matching

Component matching is important in analog circuits. In practical situations there will be mismatches among components which are intended to be identical. Mismatches adversely affect the linearity and accuracy of the converter. Mismatches in the input differential transistor pairs within the folding circuits and the pre-amplifiers in the

comparators, and mismatches between the cross-coupled latches can cause significant offset errors. Special layout techniques must be used to improve the matching among these transistors. This includes the use of the common-centroid approach and the use of united cells connected in parallel for large objects.

Another important issue is the layout of the reference ladder and the resistive strings in the interpolators. The absolute value of the individual resistor is not important but the ratios of the resistors in the ladder and strings are critical. If all the individual resistors change by the same amount, the reference voltages can remain the same and equal interpolation can be retained. Therefore, careful consideration must be given to keeping the ratio of resistors unchanged. Using a common-centroid and parallel connected united cell approaches, maintaining the same contact configuration and layout orientation for each resistor are required. In addition, "dummy resistors stripes" must be added to the extremities of the resistor stripes.

3.2.2   Clock and Signal Path Layout

The low frequency accuracy of the A/D converter is limited by comparator offsets caused by parameter mismatches. However, at high frequencies, the accuracy of the converter decreases mainly due to timing mismatches among comparators, which make the comparators sample values of the input signal at different times. These timing mismatches originate from differences in the arrival of the clock and input signal to their respective circuitry. In this design, the comparator array consists of 32 comparators. The timing mismatches must be minimized to meet the speed and resolution required because the converter has to operate at 1-Gsample/s with a resolution of 8-bit. To minimize the timing mismatches, the wiring for each of the clock and signal paths in the layout must be highly symmetrical. Therefore a tree-structure is used for the layout of the clock and analog signal paths in this design. The conceptual diagram is presented in Fig. 3.1a. In a conventional

implementation, as depicted in Fig. 3.1b, the signal travels different path lengths to arrive at its respective circuit. These different path lengths can cause large delay variations and

(b) a tree-structure   (a) a conventional structure
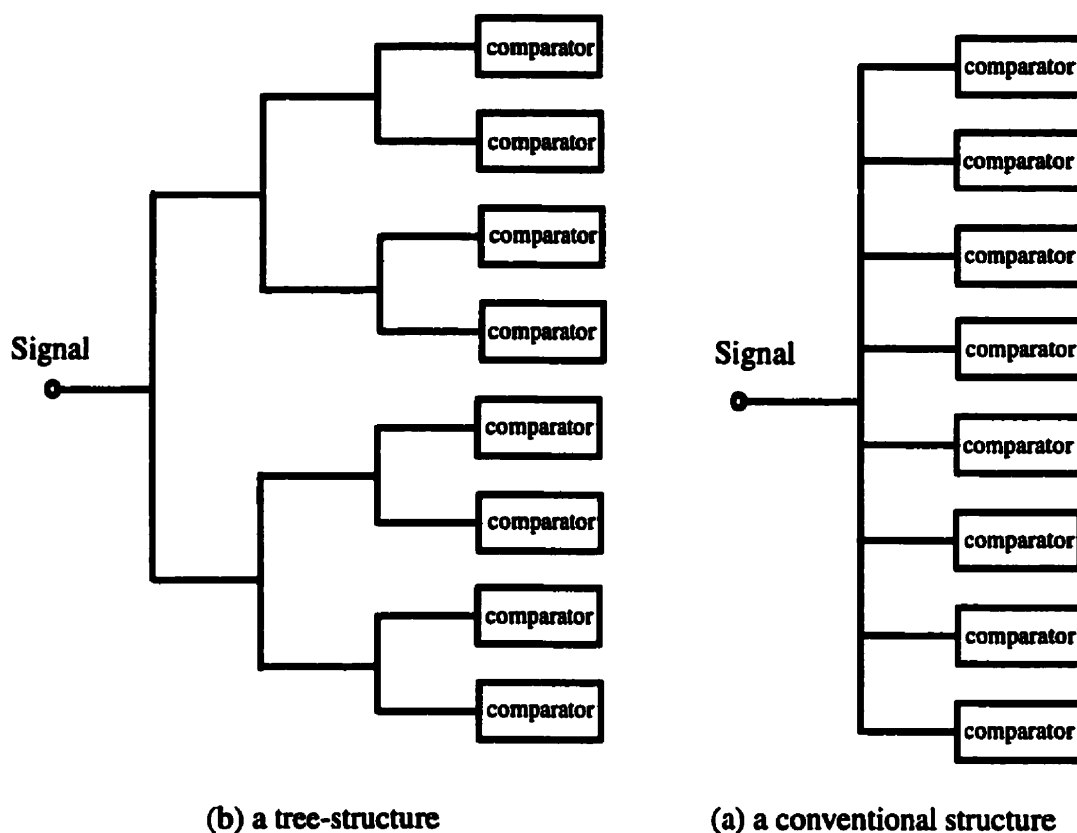
Fig. 3.1. Comparison of a tree-structure wiring with a conventional wiring for a crucial high-speed signal

consequently result in significant errors in the A/D converter. In the tree structure, shown in Fig. 3.1a, each comparator has an identical path length away from the signal source, allowing the signal to arrive at each comparator simultaneously.

3.2.3 Noise Consideration

One of the major problems of mixed analog and digital circuits is noise coupling. Signals in the analog portion of the A/D converter are basically constant or slightly varying

in time while signal in the digital portion of the ADC consists of changing pattern of pulses. Consequently any noise generated in the digital section of the ADC is coupled into the analog circuits through the power supply and the substrate. Routing an analog signal parallel to a digital line also results in a capacitive coupling between two lines.

To avoid the digital noise or cross-talk over the power supply connections, separate power supply lines and pins are used for the digital and analog sections. Moreover, separate power supply is used for digital output drivers since it has to handle large current spikes.

To minimize the noise coupling through the substrate, the analog portion is physically separated from the digital portion by guard rings and wells [1]. Shielding layers are also used to reduce capacitive coupling between the circuit elements. For example, an n-layer is put underneath the resistors, capacitors and clock buses [2].

3.2.4　Overall Layout

The layout of the A/D converter, using the NT25 silicon bipolar technology provided by Nortel Networks is presented in Fig. 3.2. The signal flow is from left to right. The area of the chip is 2.5mm×3.5mm including bonding pads. Approximately 30% of the chip area is used for the analog portion of folding and interpolation stages and 60% is used for the digital portion. The remaining 10% is used for the pads and peripheral circuits.

The physical layout in Fig. 3.2 corresponds to the electrical circuit topology shown in Fig. 2.7. On the left is the reference ladder. The blocks next to the reference ladder are the four folding blocks in the fine quantizer and the one folding block in the coarse quantizer. The resistor strings used for the interpolations are placed immediately next to the folding blocks. The comparator array is located just after the interpolation stage. The EXOR array, the error-correction stage, and the encoder follow in turn, and on the right are the 8 output drivers.

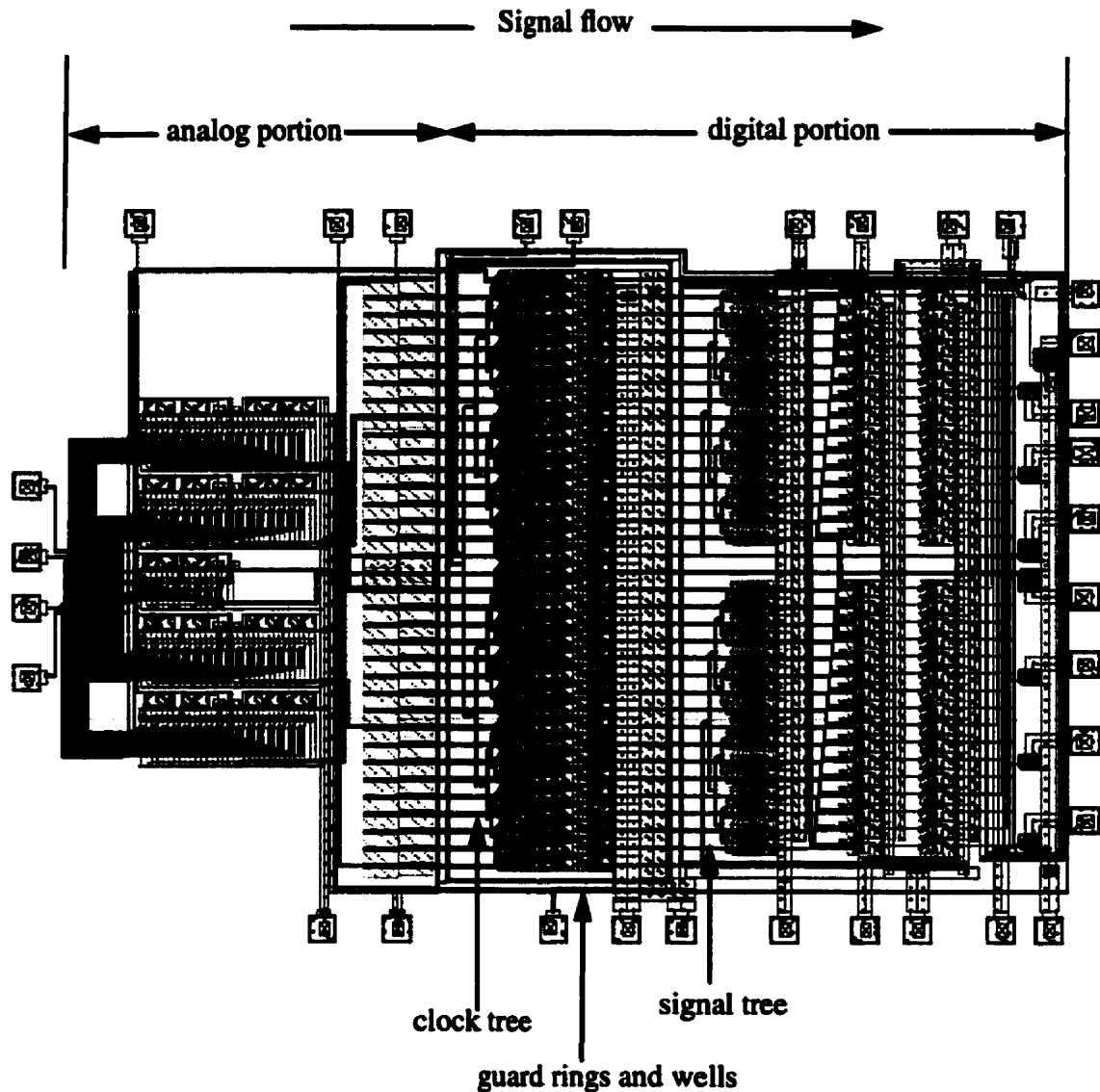Fig. 3.2. Layout of the ADC using the NT25 technology

An important issue in the layout involves ensuring correct metal widths to meet the current density requirements in all the metal layers and having enough contacts and vias to handle the current going through various interconnections. The metal lines running vertically in Fig. 3.2 are power lines which need to be wide enough to meet current density

requirements. Also, metal layers are used for connections as much as possible to keep interconnect resistance and delay low. Crossing between metal lines is kept to a minimum.

3.3   The A/D Converter Implementation

The micrograph of the A/D converter implemented using the NT25, a 0.5μm silicon bipolar technology with f_T of 25GHz, is shown in Fig. 3.3. The chip was packaged in a 64-pin Trinquint multilayer ceramic package (MLC 132/64). This package is suitable for speeds up to about 3.5GHz.

Fig. 3.3.   Micrograph of the implemented A/D converter

3.4 A/D Converter Testing *

The packaged A/D converters were evaluated and tested for full speed using the Triquint's ETF-MLC 132/64 test fixture. In this test fixture, a heat sink incorporated into one of the retainer assemblies provides efficient cooling, and capacitive decoupling is also provided for chip power supplies.

By ensuring appropriate bias conditions and reference voltages, the static and dynamic performance of the A/D converter were tested. In the static test the functionality of the A/D converter was determined by applying a very low frequency ramp signal and monitoring how the A/D converter converts the input signal. Fig. 3.4 presents the measured 8 digital output waveforms obtained applying such a low frequency ramp signal at the input. It can be seen that the ADC operates properly.

In the dynamic test a low distortion sinusoidal input signal was applied to the input of the ADC. The harmonic distortion of the signal source must be at least a few dB lower than the distortion of the ADC under test. The digital outputs from the A/D converter were acquired using Tek digital sampling oscilloscope and stored as a file using a computer. The subsequent signal processing was performed using MATLAB. Fig. 3.5 presents the plot of ENOB of the ADC at different input frequencies when the converter is clocked at 1-Gsample/s. A resolution of greater than 7 effective bits was obtained for input frequencies up to 200MHz, At input frequency of 300MHz, the ENOB drops to around 6-bit. The difference between the simulation and measured results can be attributed to parasitics and component mismatches.

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* See Appendix A for details

Fig. 3.4. Measured 8-bit output waveforms from the ADC for a low frequency ramp signal
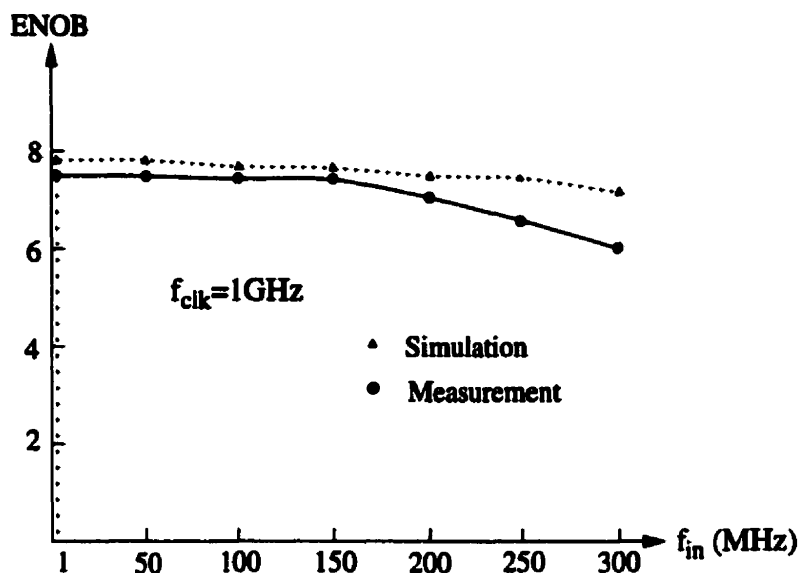
Fig. 3.5. Measured dynamic performance of the ADC, input at full scale

Eight packaged A/D converters were tested. No significant difference in performance was noted. Table 3.1 summarizes the characteristics of the 8-bit, 1-Gsample/s folding-interpolating A/D converter.

Table 3.1: Measured ADC performance

Architecture	Folding Interpolating
Process	0.5μm Si BJT f_T=25GHz
Resolution	8-bit
Sampling Rate	1-Gsample/s
Signal Bandwidth	200MHz
ENOB	7.4-bit
Linearity	≤ ±0.5 LSB
Power Consumption	2.5W
Chip Area	2.5x3.5mm²

Since power consumption is an important specification in ADC design. The figure of merit F can be used to characterize the performance of ADCs [3]. F is defined by the following equation:

$$F = \frac{2^N f_{samp}}{P_{dis}} \tag{3-1}$$

where, N is the resolution, f_{samp} is the sampling frequency, and P_{dis} is the power dissipation, As illustrated in Fig. 3.6, most ADCs have figure of merit $F \leq 4x10^{10}$ LSBs-Hz/W [3]. The present design with a figure of merit $F = 1.02x10^{11}$ LSBs-Hz/W is considerably better. Particularly, a digital error correction technique was used in the present design to achieve a more robust performance than the design suggested by van Valburge [6] but at the expense of additional power consumption.

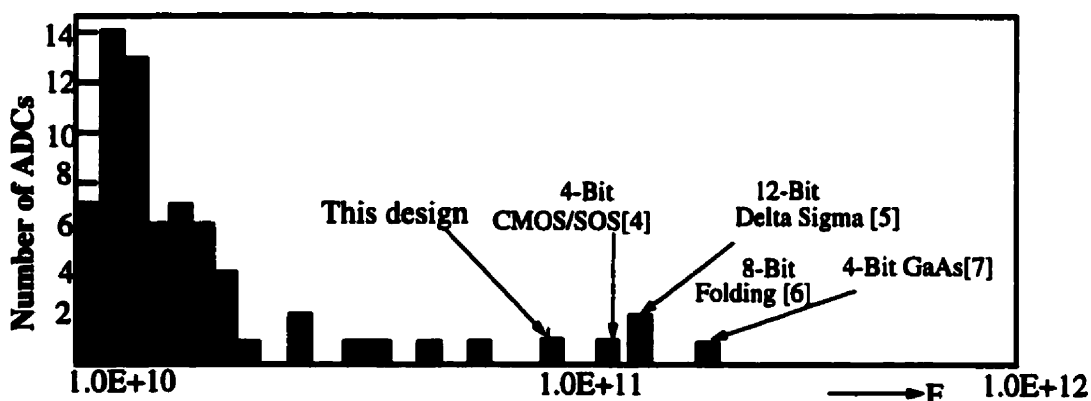Fig. 3.6. A Histogram for the figure of merit F on previously
reported ADCs [3] and the one reported here

3.5   Summary

This chapter discussed the implementation and the experimental results of the A/D converter using the NT25, a 0.5μm silicon bipolar technology with f_T of 25GHz. The test results of the ADC are presented and are generally in good agreement with simulations and expected specifications.

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CHAPTER 4

Conclusions

This work was motivated by the demand for high-speed, high-resolution analog-to-digital converters for applications in direct IF sampling receivers for wideband communications systems. The use of silicon bipolar process for this work is aimed at integrating a Gsample/s ADC with a DSP system usually realized using a BiCMOS process.

The folding-interpolating architecture used in this work overcomes the drawbacks associated with parallel and feedforward architectures. Folding-interpolating converters offer an optimum solution for Gsample/s, high-resolution ADCs in terms of complexity, power dissipation and chip area.

A monolithic 8-bit, 1-Gsample/s folding-interpolating A/D converter was designed and implemented using the NT25, a 0.5 μm self-aligned, double polysilicon bipolar process with maximum unity gain cutoff frequency f_T of 25GHz. The A/D converter consists of a reference ladder; four folding blocks for the fine quantizer and one folding block for the coarse quantizer; interpolation resistive strings; a comparator array; a digital encoder including an EXOR array, an error-correction stage, and a 31-to-5 OR ROM; and a coarse quantizer.

In order to achieve the required specifications predicted by simulations and maximize the yield of the design, special layout techniques were employed in the layout of the ADC.

The experimental results of the A/D converter show that it is capable of working to 1-Gsample/s and achieving better than 7-bit ENOB when input signal frequency is less than 200MHz. The maximum power dissipation of the ADC is 2.5W and the chip area is 2.5mm×3.5mm.

Future work should focus on reducing the power consumption and chip area by minimizing the power dissipation from the comparators and the digital encoder. To improve the performance when the input frequency is above 200MHz, a S/H circuit can be added to the ADC.

APPENDIX A

A/D Converter Testing

In this appendix, the testing methodology used to characterize the performance of the A/D converter is described. The discussion focuses on the dynamic test of the ADC.

A.1   Testing Methodology

Several analysis techniques enable characterization of an A/D converter performance based on collecting digital output data taken from the converter under test in response to a known input signal. In particular, performing a Fast Fourier Transform (FFT) on digitized waveforms generates the ADC's digital output spectrum from which SNR, SNDR, and ENOB can be ascertained [1,2].

When an ideal sinusoidal input signal of a known frequency is fed through an ideal ADC, the FFT performed on the collected digital data results only in the frequency that corresponds to the input frequency, as illustrated in Fig. A.1a.

When a converter is not ideal and has nonlinearities, the input signal is distorted during the conversion process. The resulting FFT has harmonics and a higher than ideal noise floor as shown in Fig. A.1b. The relationship between these harmonics, the noise floor and the

fundamental are used to specify the performance of the ADC. The ENOB of the converter can be obtained using the following equation:

$$\text{ENOB} = \frac{\left(\dfrac{\text{signal}}{\text{noise+distortion}}\right) - 1.76}{6.02} \tag{3.31}$$
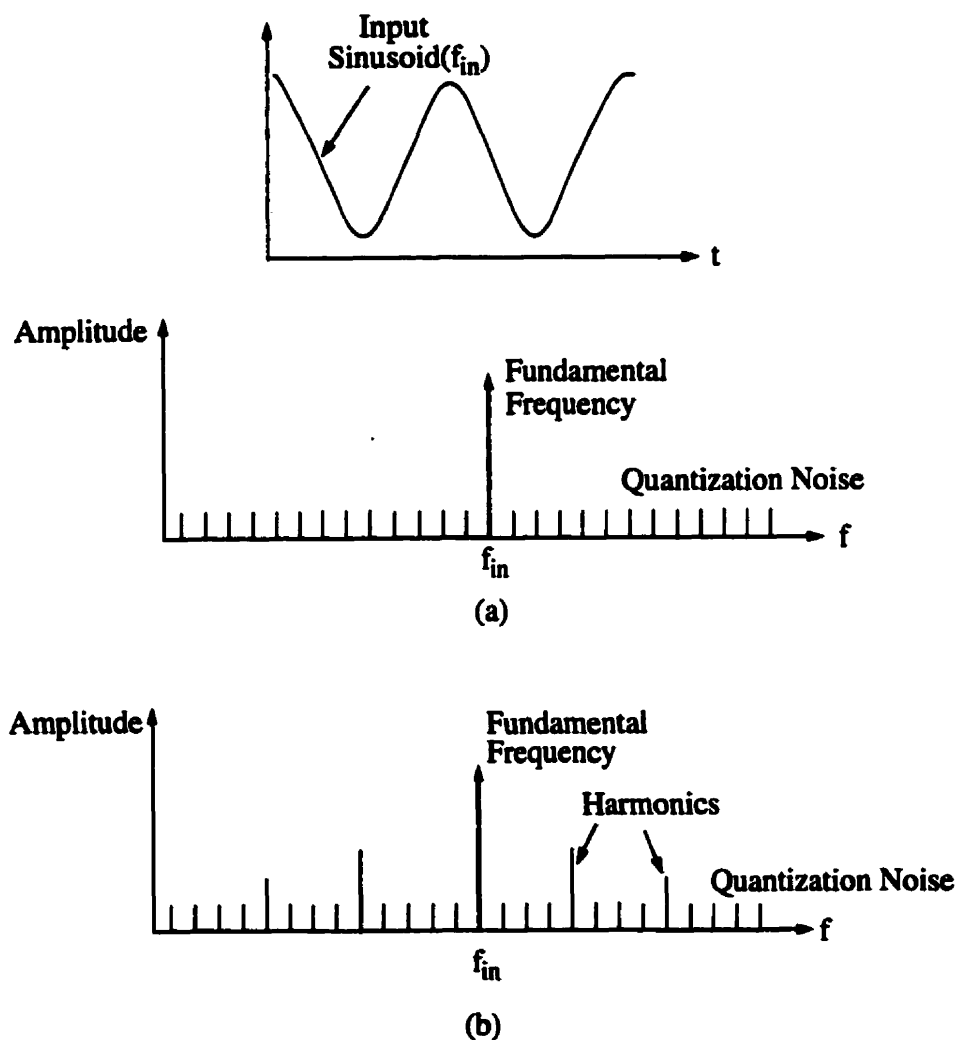

Fig. A.1. (a) FFT of a pure sine wave with an ideal converter, (b) FFT of a pure sine wave with a nonideal converter

The FFT test directly evaluates how well the converter transforms a known analog signal into digital data. One advantage of this test method is that all error sources are included in the results. In addition, the performance of the A/D converter, at its specified sampling rate and input bandwidth, can be easily examined. This is the method used in this work.

A.2 Test Setup and Procedure

The test equipment used for characterizing the performance of the A/D converter includes DC power supplies, a Rohde & Schwarz signal generator, a Colby PG3000A pulse generator, a Tek 11801C digital sampling oscilloscope, and a personal computer. The test setup is shown in Fig. A.2.
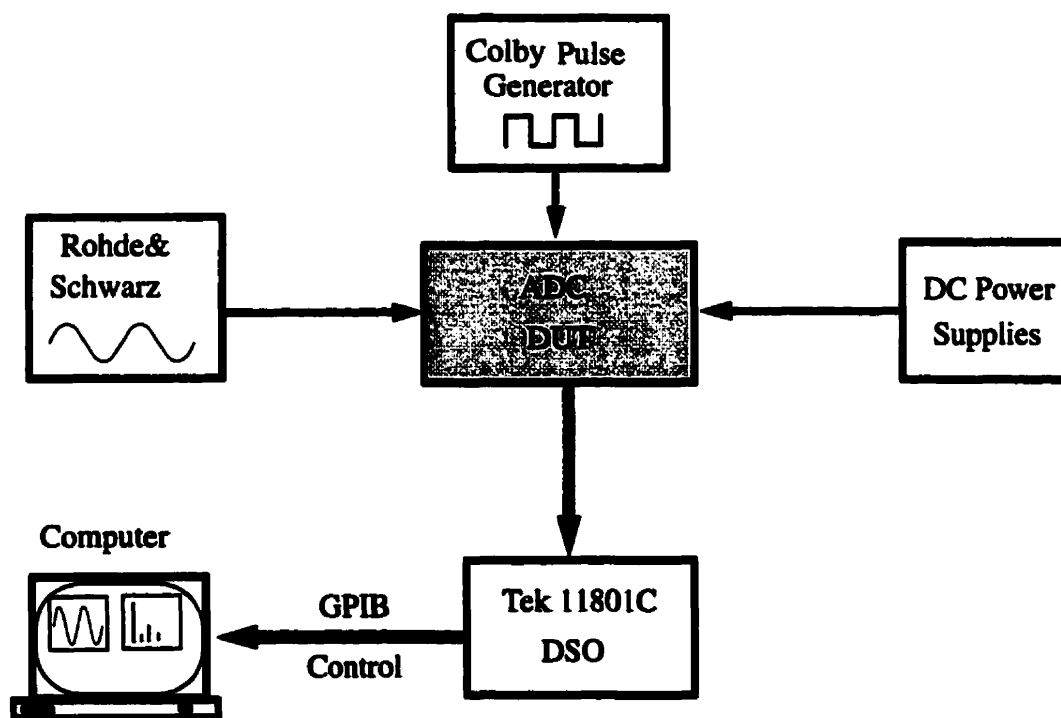

Fig. A.2. A/D converter test setup

The analog and digital power are provided by the DC power supplies. A low distortion sinusoid input with proper DC offset generated by Rohde & Schwarz signal generator is fed to the ADC under test. The clock driving signal is generated by the Colby PG 3000A pulse generator. The digital output from the ADC under test is monitored using Tek11801C DSO. A personal computer is connected through the GBIP data bus of the DSO to collect the digital output data. This data is then stored as a file on the harddisk for subsequent processing. The FFT spectrum analysis is performed on the output digital waveform using MATLAB, the corresponding ENOB (or SNDR) of the A/D converter can be therefore obtained.

References

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