An 84 GHz Bandwidth and 20 dB Gain Broadband Amplifier in SiGe Bipolar Technology

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***Abstract* — This paper reports on the design, fabrication and characterization of a lumped broadband amplifier in SiGe bipolar technology. The measured differential gain is 20 dB with a 3-dB bandwidth of more than 84 GHz, which is the highest bandwidth reported so far for broadband SiGe bipolar amplifiers. The amplifier consumes a power of 990 mW at a supply of -5.5 V.**

***Index Terms* — SiGe, broadband amplifier.**

I. Introduction

Broadband amplifiers are widely used in high speed communication systems. Recently a lumped broadband amplifier with a bandwidth of 62 GHz [1] and a distributed amplifier with a bandwidth of 81 GHz [2] in SiGe bipolar technology have been reported. This paper discusses design considerations for broadband amplifiers and presents a four-stage amplifier which shows a 3-dB bandwidth of 84 GHz and a differential gain of 20 dB.

II. Circuit Design

The amplifier is fully differential. It is based on a cascode topology. The cascode is a multiple-device configuration that is useful in high-frequency circuit design. It shows little high-frequency feedback through the base-collector capacitance (no Miller effect) with a very large 3-dB bandwidth. A broadening of the bandwidth of the cascode can be achieved by driving this stage with cascaded emitter followers (EFs) [1]. The EFs shift down the level of the signal to drive the lower differential pair in the cascode with the proper DC-level. Moreover, the voltage gain of the emitter follower has a frequency dependence that is analogous to the frequency dependence of an RLC series resonant circuit [3] with a resonant frequency:

$$\omega_r = \sqrt{\frac{\omega_t}{r_b C_L}} \qquad (1)$$

where r_b and ω_t are base resistance and cutoff frequency of the transistor and C_L is the capacitive load at the output. The gain-peak shown by the EFs at high frequencies combined with the frequency response of the cascode can result in an overall wider bandwidth. The main problem related to the use of more emitter followers cascaded to achieve a large bandwidth is the potential instability of the common collector configuration. By using a small-signal model, it can be shown that the output impedance of the emitter follower is inductive if $1/g_m > R_S + r_b$, where R_S is the source resistance. Special attention needs to be paid to the input impedance: it can be found that, besides having negative reactance, the real part can also become negative [4]. These properties of the emitter follower can cause sustained oscillations or ringing during switching transients [5]. In cascaded EFs, it can be triggered by the inductive output impedance of the driving EF (possibly supported by an inductive behavior of the connection line) and the capacitive input impedance (combined with a negative real part) of the loading EF, see Fig. 1. The inductive output impedance of an EF in series with the input reactance of the next EF and the inductance of the connection line can form an LC tank. In this configuration oscillations and instability result at a certain frequency when $R_{in}(\omega) + R_{out} < 0$ [6]. To prevent this, small resistors can be added in series with the emitter or the base causing energy loss and thereby damping oscillations. Another way to damp oscillations is to reduce the quiescent current of the last EF which directly drives the current switch in the cascode [7].

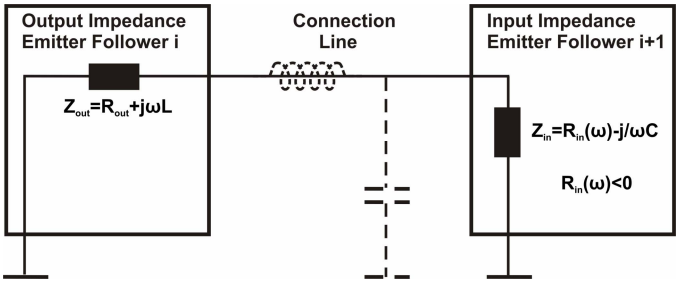

Fig. 1 Model of an emitter follower driving another emitter follower.

In this paper we propose a design methodology to avoid the ringing. The frequency at which the real part of the input impedance of a common emitter starts to become negative can be expressed in first approximation as:

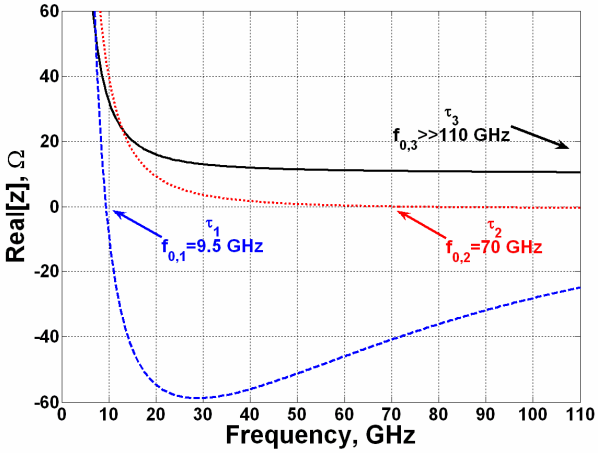

Fig. 2 (a) Simulated dependence of the real part of the input impedance of an EF on the time constant τ of the load.

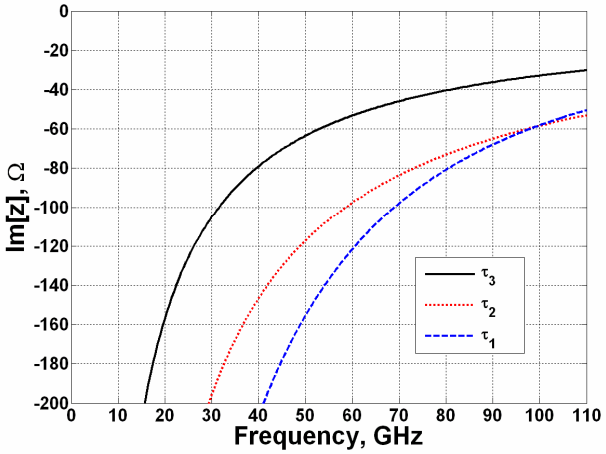

Fig. 2 (b) Simulated dependence of the imaginary part of the input impedance of an EF on the time constant τ of the load.

$$\omega_0 = \sqrt{\frac{\omega_t}{\beta_0 (R_L C_L - 1/\omega_t)}} \qquad (2)$$

where β_0 is the low frequency current gain of the transistor and R_L denotes the resistive load at the output of the EF [4]. The formula above shows that the time constant $\tau_L = R_L C_L$ must be small to shift ω_0 to high frequencies. The dependence of the input impedance on the output load is shown in Fig. 2 (a) and (b). The simulations have been performed with different load time constants: $\tau_1 > \tau_2 > \tau_3$.

The simulation results above show that by reducing the load seen by the common collector at its output it is possible to move ω_0 to very high frequencies (Fig. 2 (a)). Also the reactance will be less negative which means less energy in the LC tank (Fig. 2 (b)). Suggested by the theory and the simulation results presented before, a cascade of four emitter followers has been designed by using this rule:

$$A_i^{EF} > A_{i+1}^{EF} \qquad (3)$$

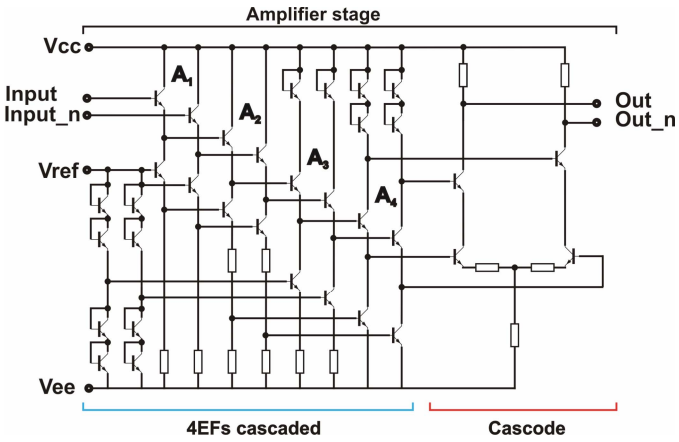

Fig. 3 Amplifier stage.

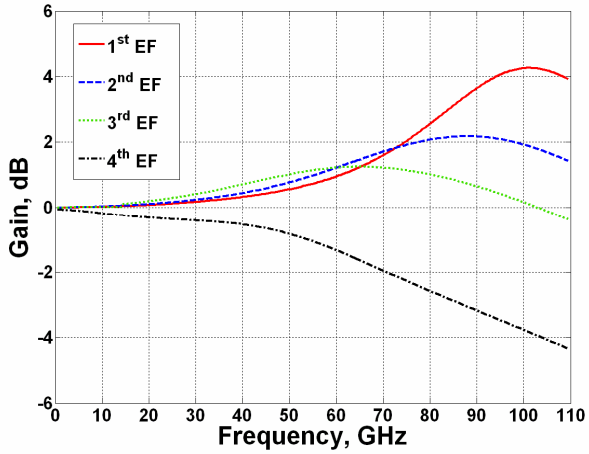

Fig. 4 Simulated voltage gain versus frequency for each emitter follower.

where A_i^{EF} indicates the size of the transistor. Starting from the input in Fig. 3, the emitter length of each subsequent emitter follower transistor in the cascade is reduced. The current density is the same for each transistor. The voltage gain of each EF is shown in Fig. 4. According to (1), the first EF shows a gain-peak at very high frequencies. The gain-peak is damped and shifted to lower frequencies throughout the cascade. This is mainly due to the base-resistance of the transistors. The resonant frequency (1) ω_r depends on C_L and r_b as well. The first transistor is the largest and sees a smaller load at its output. The second sees a smaller load at its output too, but since it is smaller than the first one its base-resistance will have a larger impact on the gain-peak. The same evaluation can be done for the third emitter follower. The last one is very small and will show the largest base-resistance. Moreover, it drives the transistor in the lower differential pair of the cascode. The transistors used in the cascode are quite large compared to the ones used as emitter followers. This explains the voltage gain behavior for the fourth EF shown in Fig. 4. The overall voltage gain of a cascade of these four

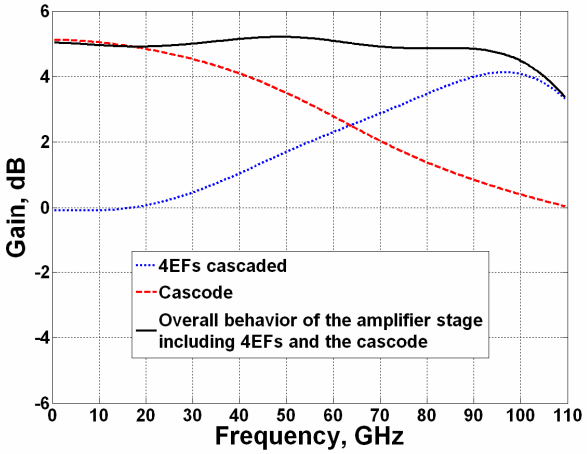

Fig. 5 Simulated voltage gain versus frequency: the cascade of four EFs, the cascode, and the amplifier stage.

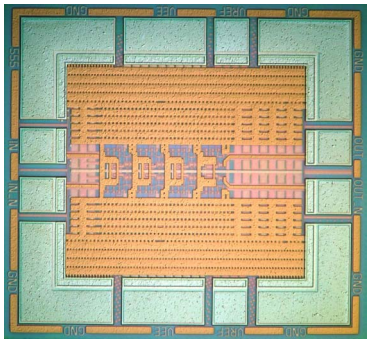

Fig. 6 Chip photograph of the four-stage broadband amplifier.

emitter followers is presented in Fig. 5. The circuit simulated is the amplifier stage proposed in Fig. 3. From the simulation results, it can be seen that the combination of a cascode with the driving stage described above can result in a broadband amplifier with very flat frequency response. In this configuration, as shown in Fig. 5, the voltage gain is less than 6 dB. In order to increase it, four amplifier stages have been cascaded in our project. The load resistor of the last stage is $75\,\Omega$. By using four emitter followers there is not enough headroom to use a current source for the cascode. For this reason resistors have been used instead of current sources.

III. Technology

The broadband amplifier is manufactured in an advanced SiGe:C bipolar process based on the technology presented in [8]. The process uses shallow and deep trench isolation. The transistors have a double-polysilicon self-aligned emitter base configuration with a SiGe:C base which is integrated by selective epitaxial growth. The transistors are fabricated using 0.35 µm lithography. The minimum effective emitter width is 0.18 µm. In comparison to [8] the transistors used for the fabrication of this circuit have a pedestal collector with lower dopant density resulting in a cutoff frequency f_T of 180 GHz, a

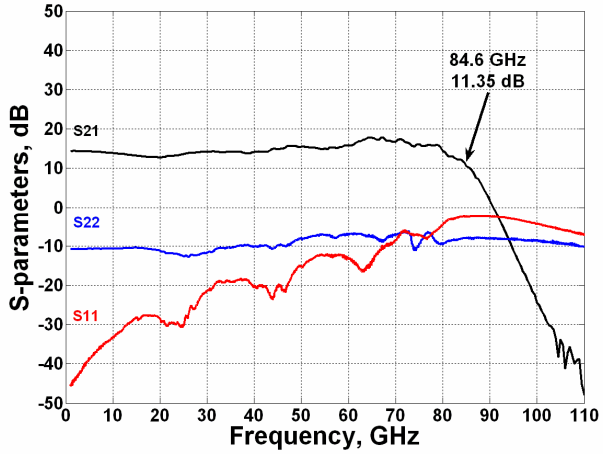

Fig. 7 Single-ended measurement of the S-parameters (differential gain is 6 dB higher).

maximum oscillation frequency f_{MAX} of 250GHz, a reduced base collector capacitance and an increased collector-base breakdown voltage. The maximum f_T is obtained at a current density of 5 mA/µm^2. The chip photograph is presented in Fig. 6.

IV. Measurements Results

The fabricated circuit has been carefully characterized by S-parameter measurements and by applying high data rate signals to the chip. All measurements have been performed at a supply voltage of -5.5 V while the current consumption was 180 mA.

S-parameter measurements have been performed single-ended using an Agilent vector network analyzer. The chip was mounted on a substrate to provide the supply voltage. The substrate was put on a probe station where the input and output pads were contacted by probes. Fig. 7 shows the single-ended measured gain, the input and the output return loss at $50\,\Omega$ source and load impedance. The single-ended low-frequency gain is 14.35 dB and the 3-dB bandwidth is 84.6 GHz. The differential gain is 20.35 dB. The phase of S21 varies linearly with frequency up to 60 GHz, indicating small variations in the group delay, as shown in Fig. 8. Simulations indicate that the degradation of the group delay at 80 GHz is partly due to the heating of the mounted chip. The stability of the amplifier has been evaluated by means of the stability factor K and $|\Delta|$ (see Fig. 9) [6].

In order to test the broadband amplifier with high data rate signals, a PRBS-generator chip [9] has been mounted close to the amplifier on a substrate. Short bond wires connected the outputs of the PRBS-generator and the amplifier inputs. A single-ended clock signal was applied to the PRBS source via a 40 GHz probe. The differential output signal has been measured via 67 GHz GSSG-probe with a 70 GHz sampling oscilloscope 86100A from Agilent. To trigger the oscilloscope, the precision timebase has not been used.

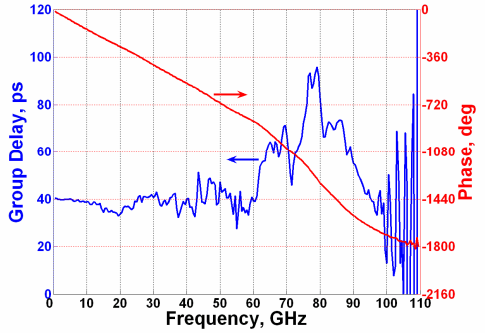

Fig. 8 Phase and group delay variation of S21 versus frequency.

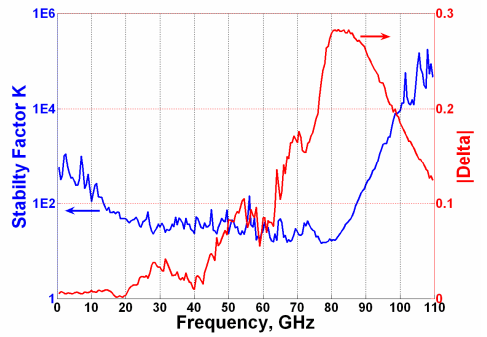

Fig.9 Stability factor K and $|\Delta|$ versus frequency.

The differential output eye diagram and the bit pattern at 80 Gb/s are plotted in Fig. 10 and 11. In order to prove that the design technique used to develop the amplifier can avoid ringing, we show in Fig. 12 also a measured bit pattern at 10 Gb/s. At both data rates the step response is damped. The amplitude of the output signal is 2x750 mV.

V. Conclusion

In this paper design considerations for broadband amplifiers have been proposed. A test-chip has been developed in SiGe bipolar technology. The differential gain is 20 dB. The 3-dB bandwidth of the amplifier is 84 GHz, which is to the author's knowledge the widest bandwidth for a broadband amplifier in SiGe bipolar technology reported to date.

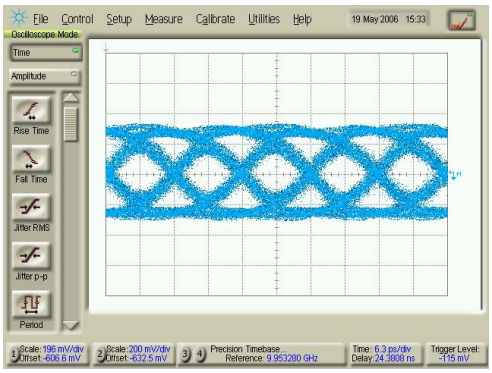

Fig. 10 Measured differential 80 Gb/s eye diagram
x-axis: 6.3 ps/div, y-axis: 500 mV/div.

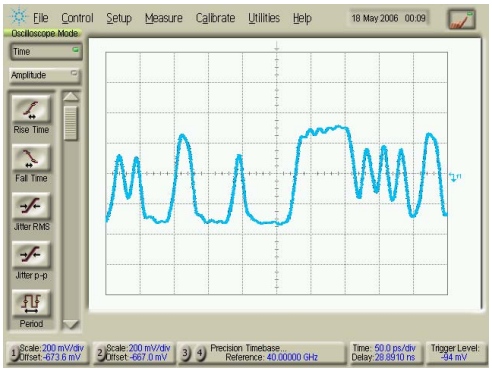

Fig. 11 Measured differential 80 Gb/s bit pattern
x-axis: 50 ps/div, y-axis: 500 mV/div.

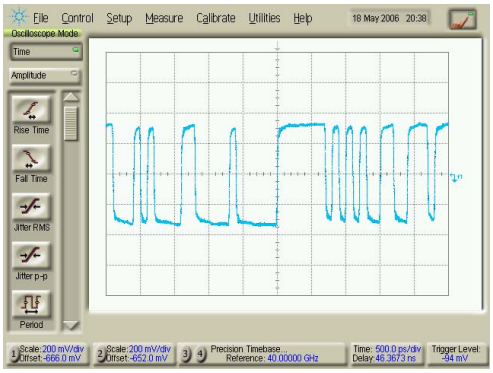

Fig. 12 Measured differential 10 Gb/s bit pattern
x-axis: 500 ps/div, y-axis: 500 mV/div.

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