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An 8kb RRAM-Based Nonvolatile SRAM with Pre-Decoding and Fast Storage/Restoration Time

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Abstract: Combining the advantages of low-power consumption of static random access memory (SRAM) with high stability and nonvolatile of resistive memory (RRAM), an improved 8T2R nonvolatile SRAM (nvSRAM) memory cell was proposed in this paper. In order to solve the problem that data cannot be stored when SRAM is powered off, RRAM technology was introduced into SRAM to realize an SRAM with nonvolatile function. The differential mode was adopted to improve the data restoration speed. Meanwhile, a pre-decoding technology was proposed to realize fast address decoding, and a voltage-mode sensitive amplifier was used to achieve fast amplification of two bit lines, so as to improve the reading speed of the memory. An 8kb nvSRAM was implemented with a CMOS 28 nm 1P9M process. The simulation results show that when the power supply voltage was 0.9 V, the static/read/write noise margin was 0.35 V, 0.16 V and 0.41 V, respectively. The data storage time was 0.21 ns, and restoration time was 0.18 ns. The time for the whole system to read 1 bit of data was 5.2 ns.

Keywords: static random access memory; resistive memory; nonvolatile; noise margin; restoration time

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1. Introduction

Recently, with the popularity and continuous development of portable electronic products such as smart phones, digital cameras, tablet computers and mobile memory devices, the memory market has been expanding. At the same time, the rapid increase in data has presented new challenges for the development of memory. Under the influence of advanced technology, the development of flash memory has also reached a bottleneck on the 32 nm node [1]. People are gradually turning to nonvolatile memory (NVM) technology. New memory based on new materials and technologies, especially nonvolatile memory, is gradually being developed. At present, the main nonvolatile devices include EEPROM, FeRAM, RRAM, etc. [2–4].

SRAM has the same operation speed as a logic circuit and has low power consumption in static mode. It also utilizes a manufacturing process similar to that for logic circuits without additional cost, so it is widely used in logic ICs. The disadvantage of SRAM is that data cannot be stored in the event of power failure, which places certain restrictions on its development [5–7]. RRAM has the advantages of high integration density, fast operation speed, low power consumption, and non-volatile, multi-value storage [8,9], which provides practical solutions for analog storage [10], computing in memory [11], artificial intelligence [12], etc.

The research on nvSRAM started in 1984. Fujitsu of Japan adopted ferroelectric components to carry out a series of research and development on nvSRAM [13]. In the 1990s, Cypress of the United States developed nvSRAM based on SONOS technology [14]. In 2006, Toshiba of Japan studied nvSRAM based on MRAM, focusing on the application of MRAM and RRAM in nvSRAM [15]. With the fast progress in technology, nonvolatile

devices have been directly integrated with SRAM, and high-density nvSRAM has become the mainstream development focus [16]. nvSRAM is composed of SRAM and NVM. NVM can store and restore data, so as to realize the function of nonvolatile memory. nvSRAM can store data in non-volatile components in case of system power failure. When the power is restored, the data can be restored to SRAM. Compared with traditional SRAM, nvSRAM has the same performance as well as nonvolatile functionality, which ensures that high-end instruments and equipment can store data in real time. Nowadays, nvSRAM products are gradually finding use in ATMs, automotive electronics, printing equipment, industrial control and other fields [17,18].

RRAM uses the different resistance states of some thin-film materials under the action of electrical excitation to store data [19–22]. Compared with three other mainstream NVMs such as FeRAM, MRAM and PCM, RRAM has high integration, fast reading and writing speed [22,23], low writing power consumption and high compatibility with the current traditional CMOS process. In 2015, Lee proposed an nvSRAM of 7T1R, which effectively reduced the energy consumption in the data restoration phase by using DSI technology [24]. The next year, Tosson proposed a high-speed and low-power 8T1R nvSRAM architecture, which improved speed and power consumption by sharing RRAM cells [25]. Therefore, nvSRAM, which integrates RRAM and SRAM, has the functions of both traditional SRAM and nonvolatile memory. It is one of the nonvolatile memories that are the focus of current research.

2. RRAM-Based nvSRAM Structure and Memory Cell

2.1. nvSRAM Structure

The system structure of nvSRAM is shown in Figure 1. It is mainly composed of a memory cell array, decoding circuit, input and output driving circuit, power control circuit, data storage and restoration circuit, and system control circuit. The system selects a memory cell in the array through the control circuit and decoding circuit. The write driving circuit makes the memory cell enter write mode. When the data are input through I/O, the data are quickly written into the memory cell. At the same time, the written data can be read out through the read driving circuit. In actual operation, a power threshold is set by software. When the power supply voltage is lower than this threshold, the circuit outputs an enable signal. After about 10 ns, the data-storage circuit starts. So, when the system has a voltage fault, the data in the memory cell are stored through the data storage circuit. When the power supply of the system recovers, the data are restored to the memory cell through the data restoration circuit.

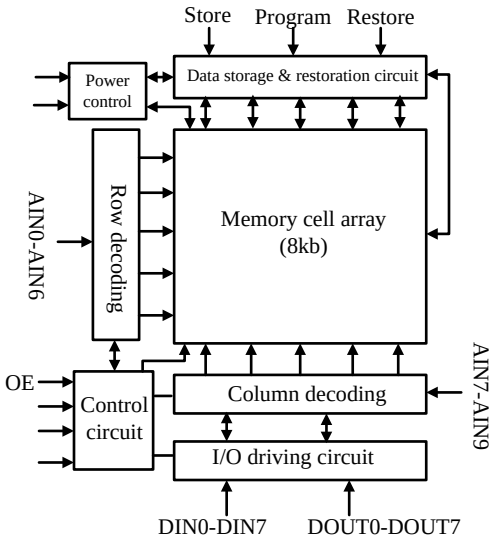


Figure 1. nvSRAM system structure.

2.2. Memory Cell Design

The memory cell of nvSRAM is mainly composed of SRAM and nonvolatile cells. The improved 8T2R nvSRAM memory cell proposed in this paper is shown in Figure 2. A pair of 1T1R RRAM are added to the traditional 6T SRAM storage nodes. While maintaining the traditional functions of SRAM, the data storage and data restoration functions are realized by controlling the memory cells of the RRAM. Different from the previous research, in the 1T1R structure, one end of the NMOS transistor is connected to the storage node, and the other end is connected to the lower electrode of the RRAM [22–26]. The gate of the transistor is controlled by the new signal RWL, and the upper electrode of two RRAMs is controlled by RBL and RBLB, respectively. Since bipolar RRAM is used, when the RRAM performs set and reset operations, different voltages are applied to the upper and lower electrodes of the RRAM to control the change in resistance. The upper electrode of the RRAM is introduced into independent control signals, and the resistance value of the RRAM is controlled through a driving circuit and power control circuit. Only when the RWL signal is turned on can the data of the SRAM and RRAM be transmitted, so that the static power consumption is zero when the NVM is not working. Under normal circumstances, nvSRAM performs read and write operations. Only when the voltage of the SRAM drops to a certain value, will the system switch to the data storage mode, and the data are stored in RRAM. The voltage required during this period is provided by the outside system. When the voltage of the SRAM is restored, the data restoration operation starts to restore the data in RRAM to the storage node of the SRAM. The Memory cell truth table is shown in Table 1.

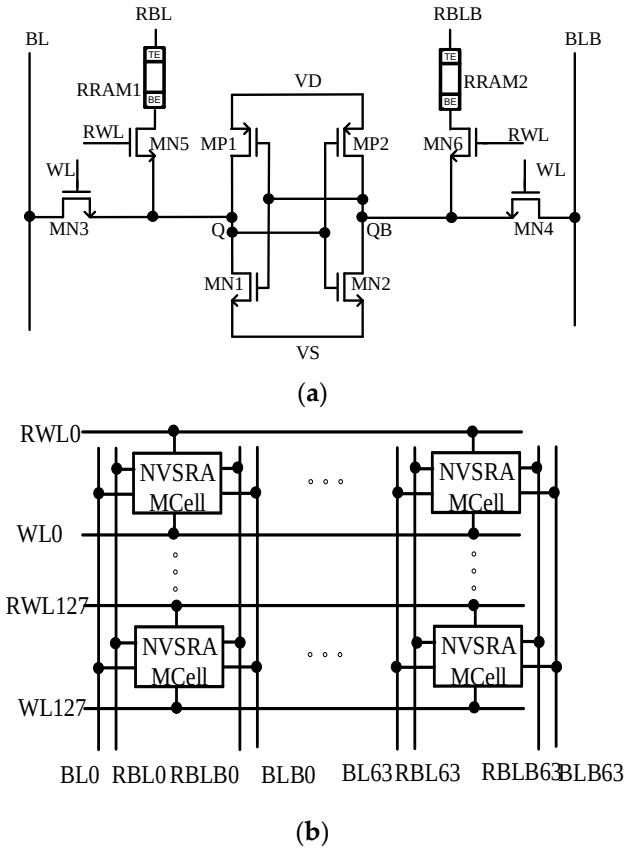


Figure 2. (**a**) 8T2R nvSRAM memory cell, (**b**) 128 × 64 array.

Table 1. Memory cell truth table.

Mode	BL	BLB	WL	RBL	RBLB	RWL	VD
Hold	0.9	0.9	0	0	0	0	0.9
Read(1)	0.9	0	0.9	0	0	0	0.9
Read(0)	0	0.9	0.9	0	0	0	0.9
Write(1)	0.9	0	0.9	0	0	0	0.9
Write(0)	0	0.9	0.9	0	0	0	0.9
Store	0.9	0.9	0	1.6/0	1.6/0	0.9	1.6
Restore	0.9	0.9	0	0	0	0.9	0.9

The principle of data storage operation is shown in Figure 3. When Q = 0, QB = 1, the supply voltage of nvSRAM is VD, WL and RWL are low, and nvSRAM maintains the data retention mode of SRAM at this time. Through turning off MN3 and MN4, the two bit lines free the data of the storage node from the interference of the BL and BLB signals. Meanwhile, RRAM1 and RRAM2 on both sides are in the state of high resistance and low resistance, respectively. When the system power supply fails, the nvSRAM enters the data storage mode. At this time, the voltage VD is switched to RVD, which is controlled by an independent power control circuit and is greater than VD. When the power supply rises, the voltage of storage node QB will rise to RVD with the change in power supply, while the voltage of Q is still 0. Both RBL and RBLB are connected to the read–write drive circuit of the RRAM. When the signal Store is valid and the signal Program is high, the voltage of RBL and RBLB becomes RVD through the control of the write drive circuit. When decoded by the address decoding control circuit, the RWL is high, making MN5 and MN6 turn on. Then, the upper electrode of RRAM1 is RVD, and its lower electrode is connected to storage node Q through the drain of MN5. While the voltage of storage node Q is 0, RRAM1 performs a set operation. This changes the resistance value of RRAM1 from high to low and completes the operation of writing 0. The upper electrode of RRAM 2 is also RVD, and its lower electrode is connected to storage node QB through the drain of MN6. Therefore, the voltage of storage node QB is RVD, which makes the voltage difference between the upper and lower electrodes of RRAM2 small, so RRAM2 maintains the current resistance value. Similarly, when signal Store is valid and signal Program is low, the voltage of RBL and RBLB becomes low through the control of the write drive circuit. After decoding by the address decoding control circuit, the RWL is high, which makes MN5 and MN6 on. At this time, the upper electrode of RRAM2 is low, and the lower electrode is connected to storage node QB through the drain of MN6. The voltage of storage node QB rises to RVD with the rise in the power supply voltage. The voltage difference between the lower and upper electrodes of RRAM2 is much greater than the reset voltage, so RRAM2 performs the reset operation. The resistance value of RRAM2 changes from low to high to complete the operation of writing 1. The upper electrode of RRAM1 is also 0, while the lower electrode is connected to storage node Q through the drain of MN5. The voltage of storage node Q is low, so that the voltage difference between the upper and lower electrodes of RRAM1 is small, and RRAM1 maintains the current resistance value.

The principle of data restoration operation is shown in Figure 4. RRAM1 and RRAM2 are in the state of low resistance (L) and high resistance (H), respectively. Due to the failure of the nvSRAM system power supply, there are no data maintained in the storage node. When the power supply gradually rises from 0 to VD and the signal Restore is high, the voltage of RBL and RBLB becomes low through the control of the read drive circuit. After decoding, the RWL is high, which makes MN5 and MN6 turn on. RRAM1 and RRAM2 are in the state of low and high resistance, respectively. MN6 turns on and makes the voltage of RRAM2 gradually rise, while turning on MN5 makes the voltage of RRAM1 gradually lower. When the power supply of the nvSRAM system is restored, the voltage of the two storage nodes is restored to low and high, respectively.

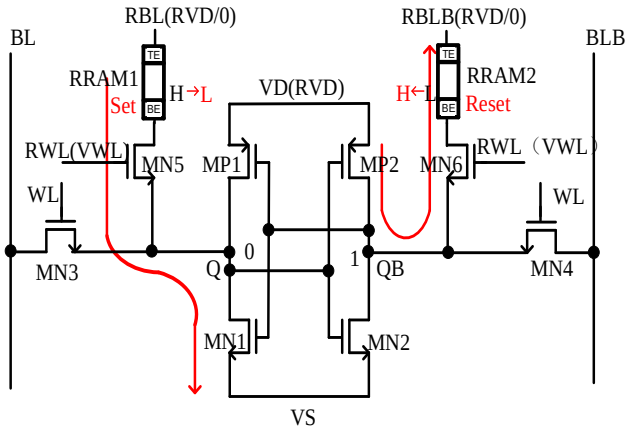


Figure 3. Data storage operation.

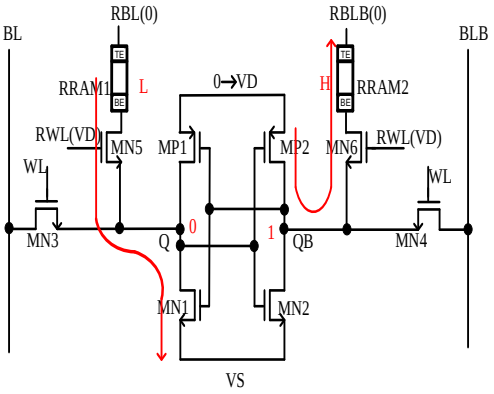


Figure 4. Data restoration operation.

When RRAM is forming, it is difficult to form all the memory cells in the same BL. This is due to the excessive load on the BL and the leakage of the device. Memory cells in a BL are divided into multiple modules to reduce the impact of the load. At the same time, memory cells are reset after forming back to HR status to reduce the leakage of the device and improve the success rate of cell forming.

3. nvSRAM Peripheral Circuit Design

3.1. Decoding Circuit

In this paper, a pre-decoding design is proposed to process the address signal by stages [27]. The first stage performs preprocessing, and then the second stage drives the output signal. Since the capacity of the memory is 8kb, there are 10 address decoding signals DIN0–DIN7, and eight input and output signals, I/O DIN0–DIN7 and DOUT0–DOUT7, respectively. Considering the need to share the SRAM address signal for decoding control of RRAM and the read–write driving ability of RRAM, the memory array is divided into 128 rows and 64 columns. The control of 128 row address signals requires 7-bit address signals (AIN0–AIN6). The column decoding circuit is jointly controlled by the address signal and I/O signal. AIN7–AIN9 can output eight groups of control signals through decoding of 3–8 decoder. Each group of signals controls an 8-bit row at the same time, and then controls different column signals through eight input or output signals, so as to complete the decoding operation of address rows and columns.

The row decoding circuit is shown in Figure 5, which consists of a three-input NAND and inverter. The NAND and inverter form the second-stage decoding circuit, which drives WL through a large inverter to improve the driving ability of WL. Because each row of the memory array shares the WL signal, it needs a row decoding circuit with large driving capacity to drive a whole row of WL signals. When the input signals A, B and C are high,

and the NAND outputs low, the subsequent inverter outputs high to drive WL. When the input signal changes from A to XA <0:7>, and the input signal is high in turn while B and C are also high, WL <0:7> will be output in turn. Therefore, when XA <0:7>, XB <0:3> and XC <0:3> decode together, 128 WL decoding signals <0:127> can be generated.

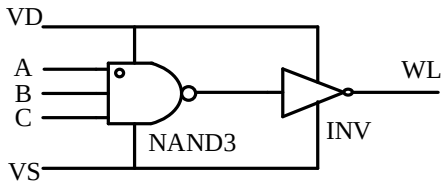


Figure 5. Row decoding circuit.

As shown in Figure 6, the column decoding circuit is mainly composed of two transmission gates and two PMOS for pre-charge [28]. The two transmission gates are controlled by the same set of YT and YN. The input of the transmission gate is BL and BLB, and the output is DL and DLB. DL and DLB are connected to the read–write control circuit. EQB is the gate control signal of MP6 and MP5, which controls the pre-charge switch of BL and BLB. When YT is low and YN is high, both transmission gates are on. While EQB is low, BL and BLB are charged to high. When EQB is high, the pre-charge process ends. Because there are 128 memory cells on the same BL, the pre-charge PMOS needs a larger size to ensure that the BL and BLB can be pulled up to high under large load. When the system reads and writes, it can control different column units by selecting different groups of YN and YT. YN and YT are generated by address and clock control signals.

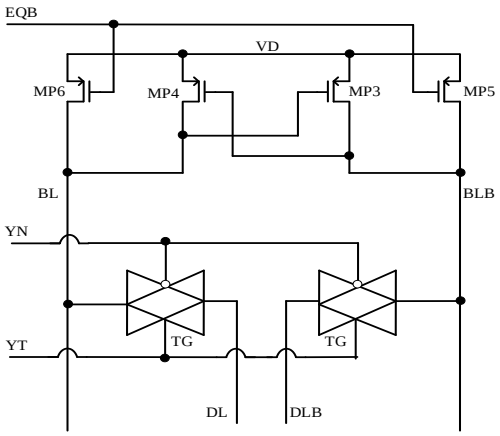


Figure 6. Column decoding circuit.

3.2. Read Drive Circuit

As shown in Figure 7, the read drive circuit includes a sensitive amplifier, latch and three-state gate [29]. The sensitive amplifier adopts a latch structure, which has faster speed compared with the traditional one. The voltage difference of the two bit lines is amplified by the sensitive amplifier, and the data are output through the latch and the three-state gate. SAE is the control signal. When SAE is high, the tail current source transistor turns on, and the sensitive amplifier starts to work. In read operation stage, when Q = 0 and QB = 1, EQB is low, and DL and DLB are pre-charged to high, DL and DLB output to BL and BLB by the three-state gate. When WL is on, because BL is high and storage node Q is low, BL forms a discharge path with the access and pull-down transistor, which will cause BL to produce a voltage drop. The voltage of BLB and QB remains the same. After rapid amplification by the sensitive amplifier, BL is low and BLB is high. When the BL and BLB voltages are transmitted to the input of the latch, the three-state gate outputs low, which completes the operation of reading 0. Similarly, when Q = 1 and QB = 0, after discharge of the memory

cell, DL is high and DLB is low. After the two signals pass through the input of the latch, the latch outputs low, and the three-state gate outputs high, which completes the operation of reading 1. At the same time, when the latch input is high, the output maintains the data of the previous clock cycle until the next reading cycle. The latch of the next stage ensures the reliability of data read out by the memory cell in each clock cycle.

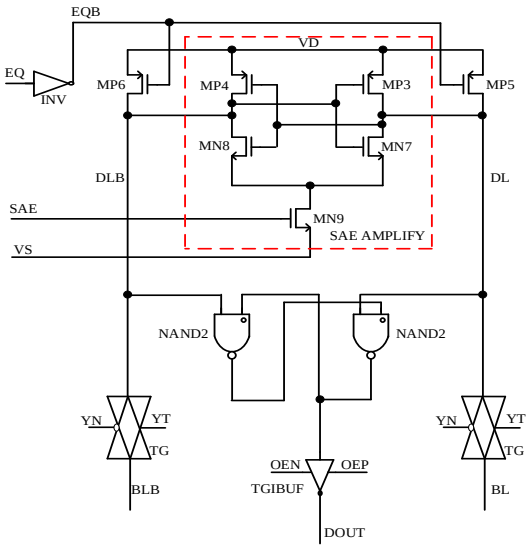


Figure 7. Read drive circuit.

3.3. Write Drive Circuit

The write drive circuit is shown in Figure 8. The input buffer generates two reverse signals QN and QT through two input NANDs, a three-state gate and inverter. The outputs of QN and QT are controlled by the three-state gate. When the input DIN and AE are high, output is low. Meanwhile, the control signal CKP is low and CKN is high, so the three-state gate is on. Then, QT is high, and QN is low.

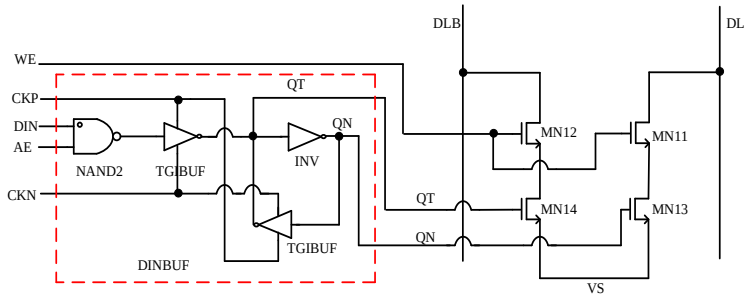


Figure 8. Write driver circuit.

Before the write operation starts, DL and DLB are pulled to high through the pre-charge transistor. When the signal WE is high, the system enters the write operation mode. Then, MN12 and MN11 are on, and QT and QN are high and low, respectively. Therefore, a path is formed between DLB, MN12, MN14 and VS. DLB will be pulled down and output to BLB through the transmission gate. MN13's off keeps BL high. When WL is on, BLB forms a discharge path, which flips the voltage of the memory cell QB. At the same time, the storage node Q will also reverse with the flip of QB, so that the node data of the memory cell change from Q = 0, QB = 1 to Q = 1, QB = 0, and the operation of writing 1 is completed. When QT is low and QN is high, DL forms a path to ground so that DL is low. DL and DLB are sent to BL and BLB through the transmission gate. At this time, BL is low, and BLB is high. The memory cell changes from Q = 1 and QB = 0 to Q = 0 and QB = 1 after internal discharge, and the operation of writing 0 is completed.

3.4. Data Storage and Restoration Circuit

The data storage and restoration circuit mainly includes a RRAM read/write drive circuit and decoding drive circuit, as shown in Figure 9. RVD is the system input, and MP6 and MP7 are MOS transistors of 2.5 V. The output of RBL0 is driven by controlling input signals such as Store, Program, and Restore. When Store, Program and Restore are low, MN5 turns on, and RBL0 is low, so the system maintains the normal operation mode of SRAM. When Store/Program is high and Restore is low, MP7 is on, and MN3 and MN5 are off. Then, RBL0 is pulled up to RVD due to MP7. While RWL is valid, RRAM is in set operation mode. Since Program becomes low, MN5 is turned on, and RBL0 is pulled down to low, which make RRAM enter reset operation mode. In case Store/Program is low and Restore is high, MN3 and MN5 are on, RBL0 is pulled down, and the system is in data restoration mode when RWL is valid.

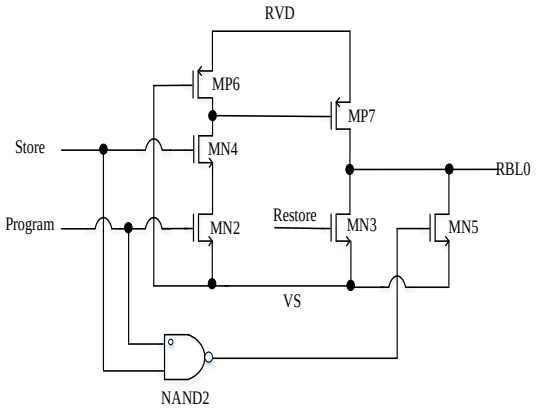


Figure 9. RRAM read/write drive circuit.

RRAM will share the address signal with SRAM during decoding. When RRAM performs set and reset operations, the voltage of RWL will be greater than the system power supply VD of nvSRAM, so RWL needs an independent voltage driving circuit. The driving circuit of RWL is shown in Figure 10 [30]. MN0 and MP0 are 0.9 V MOS transistors. MN1, MN2, MN3, MP1, MP2 and MP3 are 2.5 V MOS transistors. Additionally MN1 is a MOS transistor with low threshold voltage, which isolates the voltage of Y and Z nodes to prevent device damage. While the input signals A, B and C are all VD, the voltage at X is VD. Then, the voltage at Y and Z is 0 through the inverter. Since MP3 is turned on, RWL is pulled up to VWL, and RRAM is driven to set or reset operation.

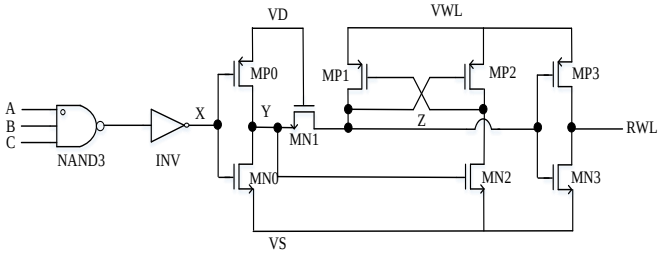


Figure 10. RWL driving circuit.

4. Experimental Results

The memory cell and array are the core of the whole nvSRAM. Additionally, the control voltage of the memory cell must first be determined, so as to design the peripheral circuit. The proposed nvSRAM was fabricated using a 28 nm 1P9M CMOS process. The material of the RRAM was $Ti/Al_2O_3/HfO_2$, and its size was 110 nm × 110 nm with a three-layer structure. The test was performed separately for 1T1R RRAM and nvSRAM [31]. Figure 11 shows a micrograph of all test chips. The nvSRAM die and test environment are

shown in Figure 12. Figures 13–15 shows the test results for RRAM, and Figures 16–18 are simulation results.

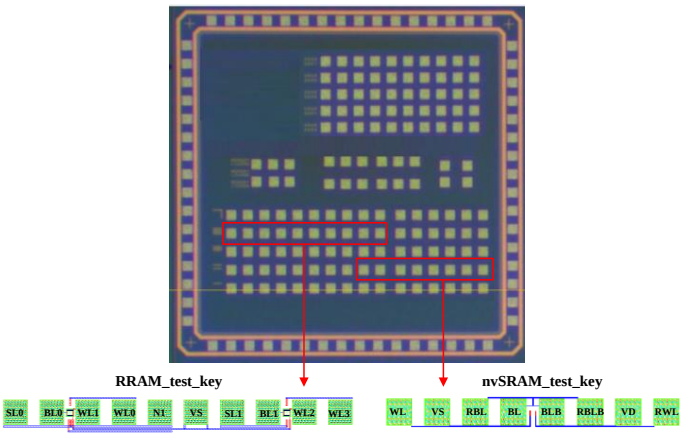


Figure 11. Micrograph of all test chip.

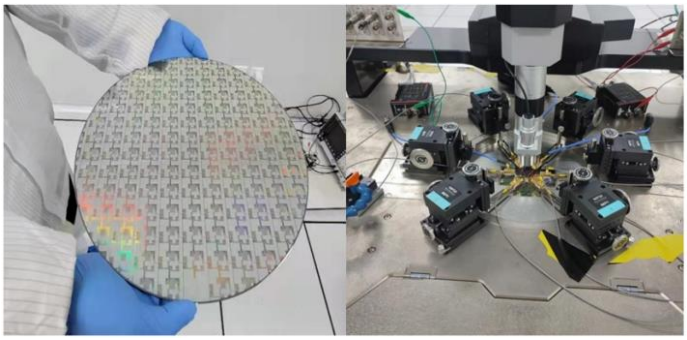


Figure 12. Die of nvSRAM and test environment.

In order to determine the peripheral operating conditions of the memory cell, firstly the RRAM was tested and analyzed. Before the RRAM performed set and reset operations, the device had to be formed to make the resistive material conductive. During the set operation, the current had to be limited to RRAM to prevent the over-forming phenomenon, which may have resulted in reset failure. The following test was the test after each RRAM was successfully formed. The DC test was carried out for RRAMs in different areas, and multiple cycle test analysis was performed at the same time to reduce the randomness of data caused by process errors.

Figure 13a is a 20-cycle test of RRAM. The test data show that when the voltage was less than 0.7 V, RRAM completed the change from high resistance to low resistance. When the voltage was less than 0.9 V, RRAM completed the change from low resistance to high resistance. Compared with the test data for the first 10 cycles, it was found that the resistance window for the last 10 cycles of RRAM was obviously better. Figure 13b,c are the tests of 10 cycles of RRAM, respectively, and the current limit of set was adjusted to 150 μA and 200 μA, respectively.

The test results from the first and last five cycles show that the resistance window of the last five cycles was indeed larger than that of the first few cycles, which means that more cycle tests could make the memory cell have a larger resistance window and stronger data stability.

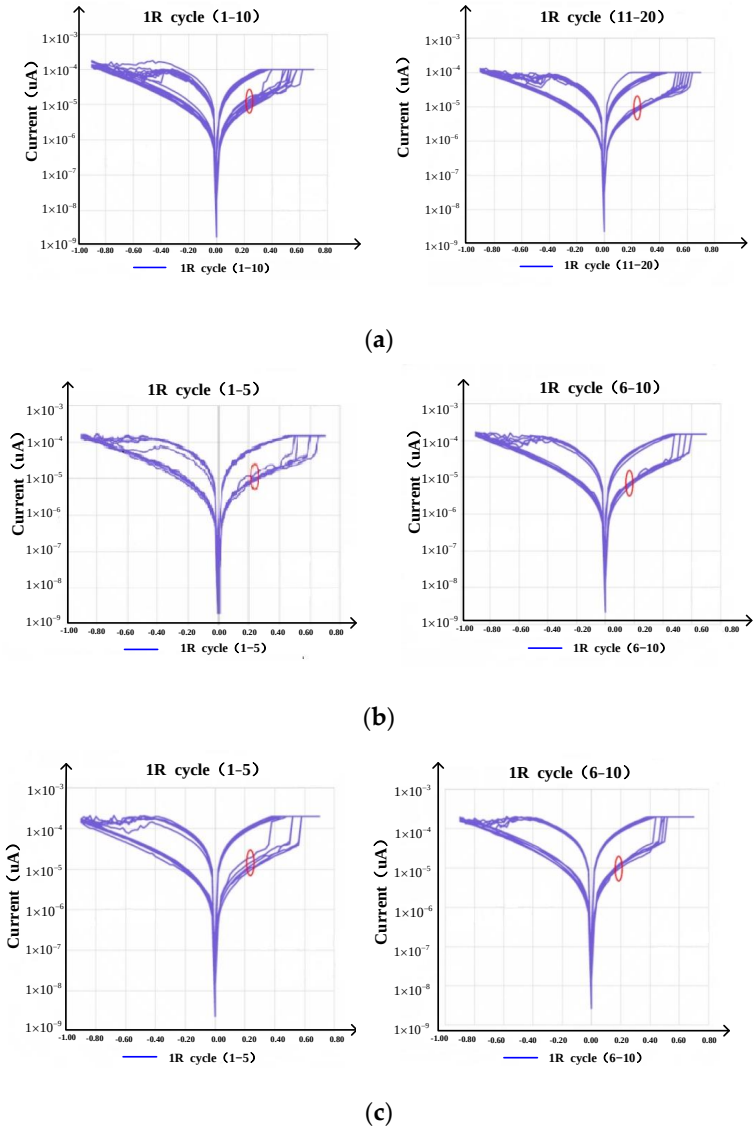
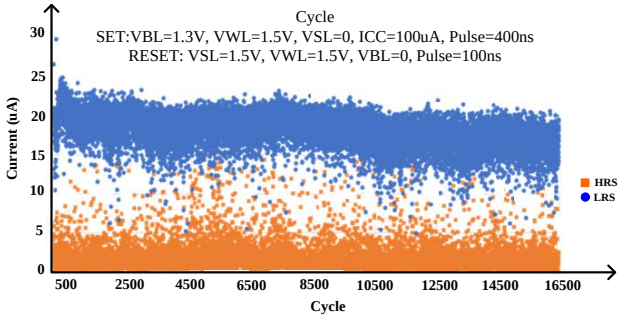


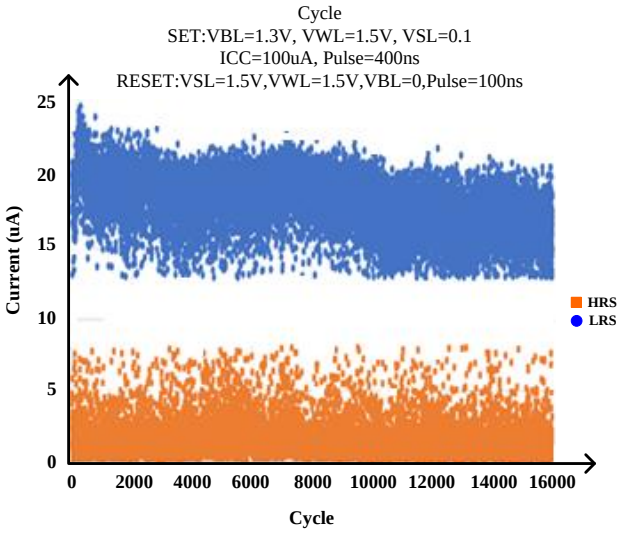
Figure 13. DC test results for 1T1R RRAM: (**a**) 20 cycles (current:100 μA); (**b**) 10 cycles (current: 150 μA); (**c**) 10 cycles (current: 200 μA).

To more accurately test the conditions of the set and reset operations of RRAM with 1T1R structure, a pulse mode is used. Then, RRAM in different dies was tested with the cycle test, and the current distribution of high/low resistance was counted. Figure 14a is the original data of cycle test. The current of the RRAM was about 15 μA when the resistance was low and about 5 μA when the resistance was high. At the same time, there were few resistance differences. Figure 14b shows the current distribution after removing the data with high-resistance current greater than 8 μA and low-resistance current lower than 15 μA, respectively. Figure 14c shows the current distribution after removing the data with high-resistance current greater than 5 μA and low-resistance current lower than 13 μA, respectively.

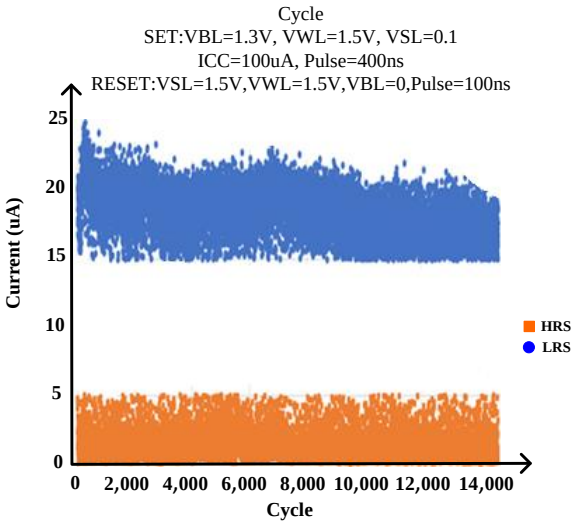
The current distribution diagram was transformed into the corresponding resistance value distribution, as shown in Figure 15. It can be seen from the distribution of resistance values that 90% of the resistance values of high resistance and low resistance were about 10 times the resistance of the window, and the data had good stability.



(**a**)



(**b**)



(**c**)

Figure 14. Pulse test results for 1T1R RRAM: (**a**) original data; (**b**) the data after removing the data of high-resistance current greater than 8 μA and low-resistance current lower than 15 μA; (**c**) data with high-resistance current greater than 5 μA and low-resistance current lower than 13 μA after data removal.

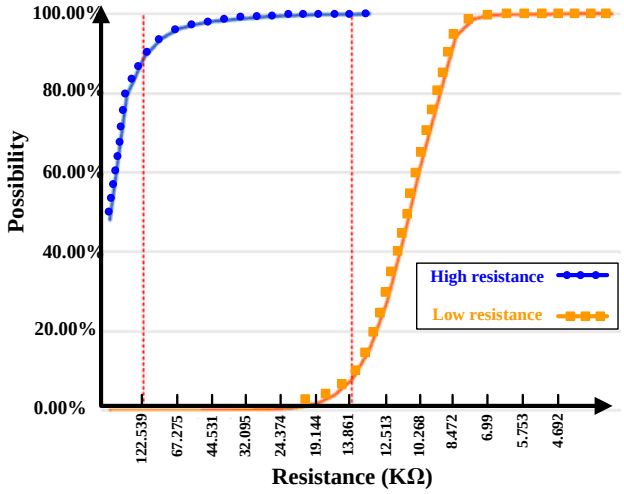


Figure 15. Resistance distribution diagram of RRAM.

At room temperature, the resistance values of 1024 bit HR and LR were counted, respectively, as shown in Figure 16. The average value of HR was 94.7 K, and the average value of LR was 12.7 K. The resistance windows of HR and LR indicated that the RRAM had good storage characteristics.

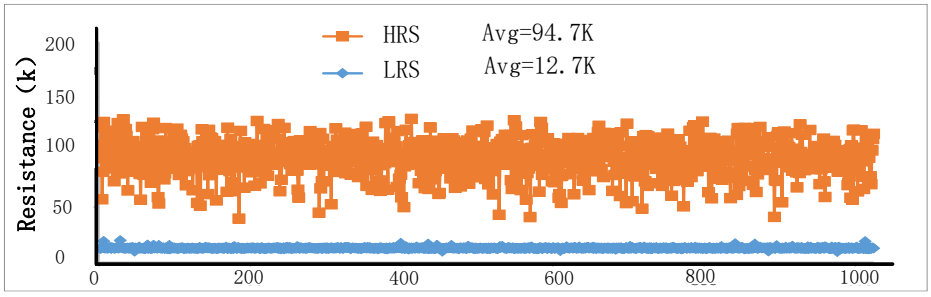
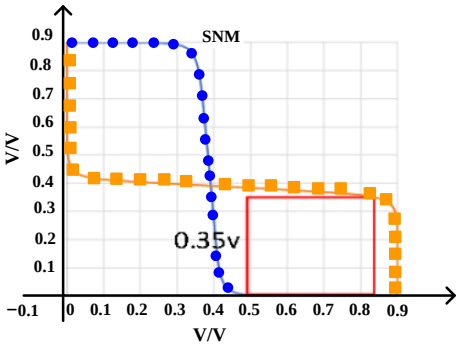


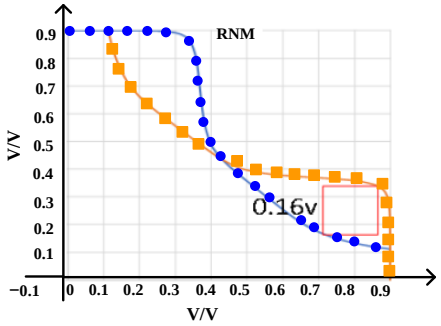
Figure 16. Distribution of HR and LR values.

From the DC test results for the RRAM, it was determined that when a separate RRAM performed a set operation, a voltage of about 0.7 V was required to complete the set operation, and the voltage for the reset was 0.9 V. According to the test results for the 1T1R RRAM, when VWL = 1.5 V, the set voltage was 1.3 V, the current limit was 100 µA, and the reset voltage was 1.5 V. Based on above data analysis, and considering the influence of signal loss, the basic principle of circuit design in this paper was that the Vset and Vreset voltages of the RRAM were 1.6 V, and the voltage of VWL was controlled by a separate RWL driving circuit.

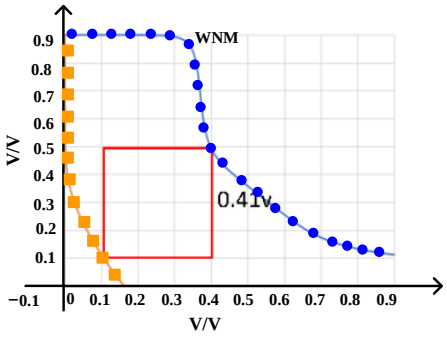
Based on the VTC test method, the noise margin of the memory cell was as shown in Figure 17. When the power supply voltage was 0.9 V, the static noise margin (SNM) was 0.35 V, read noise margin (RNM) 0.16 V, and write noise margin (WNM) 0.41 V. After adding the 1T1R RRAM, the memory cell still had good data anti-interference ability.



(**a**)



(**b**)



(**c**)

Figure 17. Noise margin: (**a**) static noise margin; (**b**) read noise margin; (**c**) write noise margin.

The simulation results for the data storage and restoration circuit are shown in Figure 18. First, a data 0 is written into the selected memory cell through the write mode of the SRAM. When the system fails, nvSRAM enters the data storage mode. By controlling the power module and the RBL driver module, the RRAM performs set and reset operations, respectively, to write the data of the storage node to RRAM. When the system enters pre-charge mode, the data of the SRAM storage node are lost. When the restore mode is entered, the data are restored to the storage node of SRAM through the control circuit module and RBL drive module.

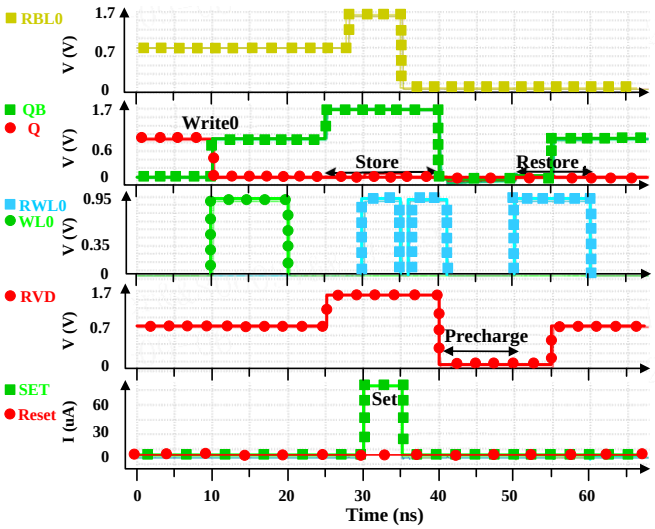


Figure 18. Simulation results for data storage and restoration circuit.

The simulation results for the nvSRAM read–write circuit are shown in Figure 19. Firstly, the memory cell is selected through the decoding circuit, then the data are written into it through I/O and the write driving circuit. After that, the data are read out by controlling the read driving circuit. While writing the data to the memory cell in one cycle, in the next cycle, the system reads the data. The time from writing to reading is 5.2 ns. In the figure, WE is the write control signal, SAE is the switch signal of the sensitive amplifier, and DOUT is the output.

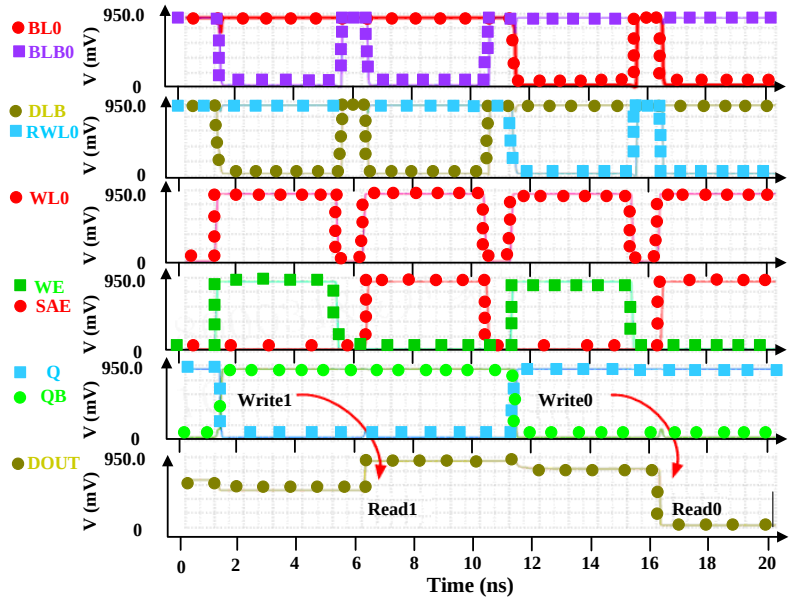


Figure 19. Simulation results for reading and writing speed.

A performance comparison between the improved 8T2R nvSRAM proposed in this paper and the previous nvSRAM is shown in Table 2. The memory cell has low power supply voltage, low power consumption and high density. As with other traditional processes, its characteristic size is basically the same. Compared with the nvSRAM of other structures, our memory cell has faster data storage and restoration times that make the data storage and restoration operations more efficient and reduce the risk of data loss.

Table 2. Performance comparison of different nvSRAMs.

	This work	[16]	[32]	[33]	[22]	[34]
Memory cell structure	8T2R	6T2R	7T2R	8T2R	7T1R	4T2R
Technology	28 nm UMC	130 nm STM	0.18 μm TSMC	0.18 μm TSMC	32 nm	90 nm
Power supply	0.9 V	1.8 V	0.7 V	1.8 V	0.9 V	4 V
Restoration mode	Differential	Differential	Differential	Differential	Single	Differential
Nonvolatile mode	Before power failure	Real time	Before power failure	Before power failure	Before power failure	Real time
Storage time	0.21 ns		1 ns	0.87 ns	0.24 ns	1.45 ns
Restoration time	0.18 ns		0.37 ns	0.36 ns	0.22 ns	0.02 ns
Current (when storing data)	0–200 μA	0–50 μA	0–230 μA	0–260 μA	0–40 μA	0–230 μA
Voltage (when storing data)	1.6 V	1.8 V	2.5 V	4.0 V	2.0 V	1.5 V
Memory cell size	0.97 μm^2	32.6 μm^2	1 μm^2	1.55 μm^2	1.18 μm^2	0.6 μm^2

5. Conclusions

This paper presented an improved 8T2R nvSRAM memory cell structure based on RRAM technology for the application of new memory. Aiming at the problem where the data in the SRAM cannot be restored after a power failure, RRAM technology is introduced into the SRAM. The data in the SRAM are stored in RRAM before power failure. When the power supply is restored, the data are restored to SRAM, which solves the disadvantage of SRAM volatility. Meanwhile, a proposed pre-decoding technique improves the reading and writing speed. The memory cell was realized with a UMC CMOS 28 nm 1P9M process, occupying only 0.97 μm^2. The simulation results show that when the power supply voltage is 0.9 V, the static noise margin is 0.35 V, the read noise margin is 0.16 V, and the write noise margin is 0.41 V. Additionally, the data storage time is 0.21 ns and restoration time is 0.18 ns. Further, a peripheral circuit was designed, and an 8kb nvSRAM realized. The time for the system to read 1 bit data is 5.2 ns. Compared with the previous research results, it has lower power consumption and faster data storage and restoration times, thus increasing the stability of data storage. This work only verified the design of the memory cell and peripheral circuit from the aspect of function, which had certain limitations. The nvSRAM array was only simulated. Since a differential structure requires a forming process before reading and writing, and the voltage of forming is high, we should also consider the impact of the forming process, so that the design will be more conducive to the read speed of the SRAM. In the design of nvSRAMs based on RRAM technology, most designs use the high and low resistance states of RRAM to store data. This single mode makes the SRAM and RRAM combination a one-to-many mode. However, research found that RRAM has a multi-value storage feature, that is, a single RRAM can store multi-bit data. This discovery provides a new idea for the design of nvSRAM, that is, multiple SRAM cells can share one or two RRAMs to realize the non-volatile storage function.

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