An Accurate Interface for Capacitive Sensors

Xiujun Li, *Member, IEEE,* and Gerard C. M. Meijer

***Abstract*—A new smart interface based on a first-order charge-balanced SC-oscillator is presented for capacitive sensors, which are shunted by a parasitic conductance. In the novel interface, the effect of shunting conductance is reduced by using the charge/discharge method. The effect of the stray capacitances is eliminated by using the two-port measurement. Moreover, all multiplicative and additive errors of the interface are also eliminated by using the auto-calibration technique and the chopping technique.**

***Index Terms*—Capacitance measurement, capacitive sensors, oscillators.**

I. Introduction

CAPACITIVE sensors can be used in various applications, such as those that measure the position, speed and acceleration of moving objects, force, pressure, liquid levels, dielectric properties, and flow materials. A main drawback of capacitive sensors is their sensitivity to pollution and condensation, which can cause a serious reliability problem. For instance, the measurement system for capacitive sensors based on a modified Martin oscillator [1]–[3] offers a relatively high resolution. Moreover, a very low baseline drift has been obtained by means of the auto-calibration technique called the three-signal method [4]. However, these capacitive measurement systems cannot accurately measure the capacitance in the presence of shunting conductance.

In [6], a capacitive-sensor interface was presented to eliminate the shunting conductance effect by performing a series of eight measurements and using an auto-calibration technique. However, a long measurement time (400 ms) is required to measure the capacitance.

In [5], a capacitive interface based on the charge/discharge method has been presented. That paper shows that the shunting conductance effect can be reduced when semiconductor switches with low ON resistance and fast commutation time are used to control the charge and discharge of the capacitive sensor.

In this paper, a new smart interface is proposed for capacitive sensors that are shunted by parasitic conductance. The novel interface is designed based on a first-order charge-balanced SC-oscillator.

II. Measurement Concept and New Interface

Fig. 1 shows a simple electrical model of a capacitive sensor, including the effects of a shunting conductance G_s and two parasitic capacitances C_{p1} and C_{p2}. The capacitor C_s is the sensing capacitor. In most applications, the values of these parasitics are application dependent and not very stable. Therefore, the influence of these parasitics should be eliminated or significantly reduced. One can reduce the effect of the two parasitic capacitances C_{p1} and C_{p2} by applying a two-port measurement technique [6]–[8]. The effect of the shunting conductance can be reduced by applying the following measurement method.

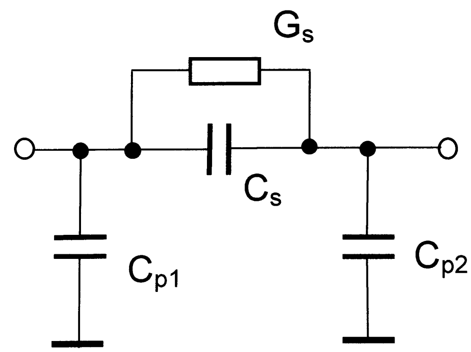

Fig. 1. Simple electrical model of the capacitive sensor.

Fig. 2 shows a simplified schematic diagram of the interface for capacitive sensors. An amplifier, a comparator, the capacitances C_{off}, C_{int} and a controlled current source I_{ch} form a basic relaxation oscillator. V_{ex} is a signal source to charge the measured capacitor.

The relaxation oscillator converts the charge from capacitors, C_s and C_{off}, into the period-modulated output signal.

To perform the measurement of the capacitance C_s, two cycles are required: the charging cycle and the discharge cycle. Fig. 3 shows these two cycles for the capacitance measurement.

During the charging cycle, the measured capacitor C_s is charged to voltage V_{ex} via switches S_1 and S_4 [see Fig. 3(a)]. Because of the low impedance of the voltage source V_{ex} and low ON resistance of the switches, the effect of the shunting conductance on the charge ($V_{ex}C_s$) of the capacitor is negligible. In this cycle, the oscillator converts the charge from the capacitor C_{off} into a time interval T_1 [see Fig. 3(c)]. The value of T_1 is given by

$$T_1 = \frac{V_{comp,p-p}C_{off}}{|I_{ch}|} \tag{1}$$

where $V_{comp,p-p}$ is the peak-to-peak value of the comparator output voltage V_{comp} and $|I_{ch}|$ is the modulus of the value of the charge/discharge current I_{ch}.

During the discharging cycle [see Fig. 3(b)], one terminal of the measured capacitor is connected to ground by the switch S_2. The switch S_3 connects the other terminal to the input of the integrator that is at virtual ground potential.

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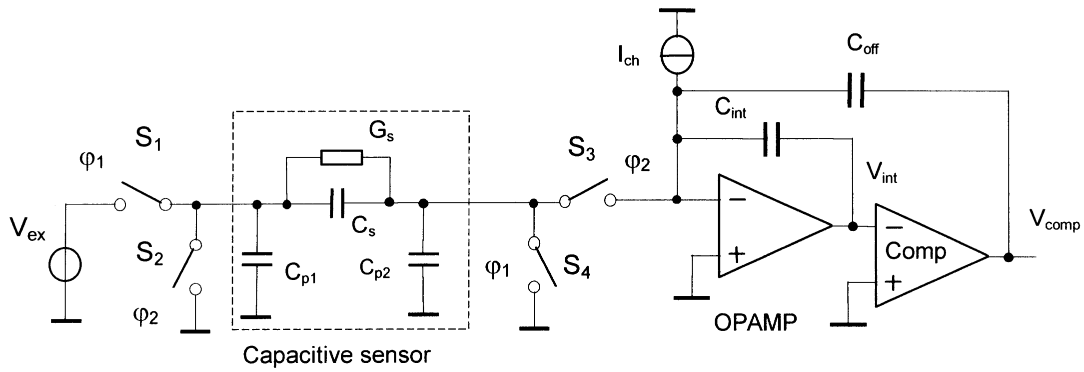


Fig. 2. Schematic diagram of the interface.

At the moment of t_1 [see Fig. 3(c)], together with the charge over C_{off}, the charge $(V_{ex}C_s)$ in the capacitor C_s is completely transferred into the integrator via the switch S_3.

In the ideal case, because there is no voltage drop across C_s and G_s during the discharge cycle, the shunting conductance will not affect the charge-to-time interval conversion in the oscillator. In this cycle, the oscillator converts the charge from the capacitor C_{off} and capacitor C_s into a time interval T_2 (see Fig. 3(c)). The value of T_2 is given by

$$T_2 = \frac{V_{comp,p-p}C_{off}}{|I_{ch}|} + \frac{|V_{ex}|\,C_s}{|I_{ch}|} \tag{2}$$

where $|V_{ex}|$ is the modulus of the value of the excitation signal V_{ex}.

The period of the output signal of the oscillator T is presented by

$$T = T_1 + T_2 = 2\frac{V_{comp,p-p}C_{off}}{|I_{ch}|} + \frac{|V_{ex}|\,C_s}{|I_{ch}|}. \tag{3}$$

As compared to circuits earlier presented in [6], the improvement is achieved by removing the dc biasing voltage across C_s, which eliminates the effect of undesired discharging of C_s. In practice, a small residual effect will remain due to the finite, nonzero discharge time of C_s.

The circuit shown in Fig. 2 has some drawbacks: 1) It is sensitive to the offset voltage of the opamp and the comparator and the delay time of the oscillation loop. 2) It is sensitive to the values of the current I_{ch} and the capacitor C_{off}. 3) It is sensitive to the drift of the excitation signal V_{ex}.

As presented in [4], the three-signal auto-calibration technique will eliminate the effect of those multiplicative and additive errors and parameters, which are constant during the three measurements. To implement the three-signal auto-calibration technique, in addition to the measurement of capacitor C_s, two other measurements for C_{ref} and the offset C_{off} are performed. In the circuit, this is realized by controlling the switches S_1, S_2, S_5 and S_6 [see Fig. 4(a)]. All three voltage-sources V_{ex}, V_{01} and V_{02} are derived from the comparator output using the counter and frequency divider in the switch control unit.

As an example, suppose that the value of capacitor C_s has to be converted into the time domain. Fig. 4(b) shows some relevant signal levels and control signals in the interface circuit.

In one complete cycle for the measurement of capacitor C_s, four measurements are included, which have a chopping sequence of $+--+, +-- \cdots$. The application of such chopping technique eliminates the offset effect of the interface and the effect of any other low-frequency signals.

The use of C_{01} measurement ensures a proper sample-and-hold action of the oscillator. The use of C_{02} measurement ensures a linear range of the oscillator [7], [8].

As that presented in [8], the periods of the output signal of the oscillator T_s, T_{ref} and T_{off}, corresponding to the measurement of C_s, C_{ref} and C_{off} (C_{01} and C_{02}), are given by the equations

$$\begin{aligned} T_s &= 4\frac{|V_{ex}|\,C_s}{|I_{ch}|} + 4\frac{V_{01,p-p}C_{01} + V_{02,p-p}C_{02}}{|I_{ch}|} \\ T_{ref} &= 4\frac{|V_{ex}|\,C_{ref}}{|I_{ch}|} + 4\frac{V_{01,p-p}C_{01} + V_{02,p-p}C_{02}}{|I_{ch}|} \\ T_{off} &= 4\frac{V_{01,p-p}C_{01} + V_{02,p-p}C_{02}}{|I_{ch}|} \end{aligned} \tag{4}$$

where $|V_{ex}|$ is the modulus of the value of the excitation signal V_{ex}. $V_{01,p-p}$ and $V_{02,p-p}$ are the peak-to-peak values of the voltage excitations V_{01} and V_{02} for the capacitors C_{01} and C_{02}, respectively.

Then, the measured results for the capacitor's value are found by the equation

$$C_s = \frac{T_s - T_{off}}{T_{ref} - T_{off}} \cdot C_{ref}. \tag{5}$$

This result does not depend on the unknown offset and the unknown transfer factor of the interface. In this way, the interface is auto-calibrated for additive or multiplicative errors. Even in the case of slow variations of the offset and transfer factor, these effects are eliminated. The algorithm can be implemented using, for instance, a microcontroller.

III. Experimental Results

A prototype based on the circuit shown in Fig. 4 has been built. The switches $S_1 \cdots S_6$ are implemented with a simple quad bilateral switch (CD4066). The relaxation oscillator is implemented using an opamp (OPA2350), a comparator (MAX987) and some extra components. The logic control circuit is implemented with some simple gates. The frequency of the oscillator is between 7 kHz and 16 kHz, depending on the sensor signals. A microcontroller of the type INTEL D87C51AF, which has

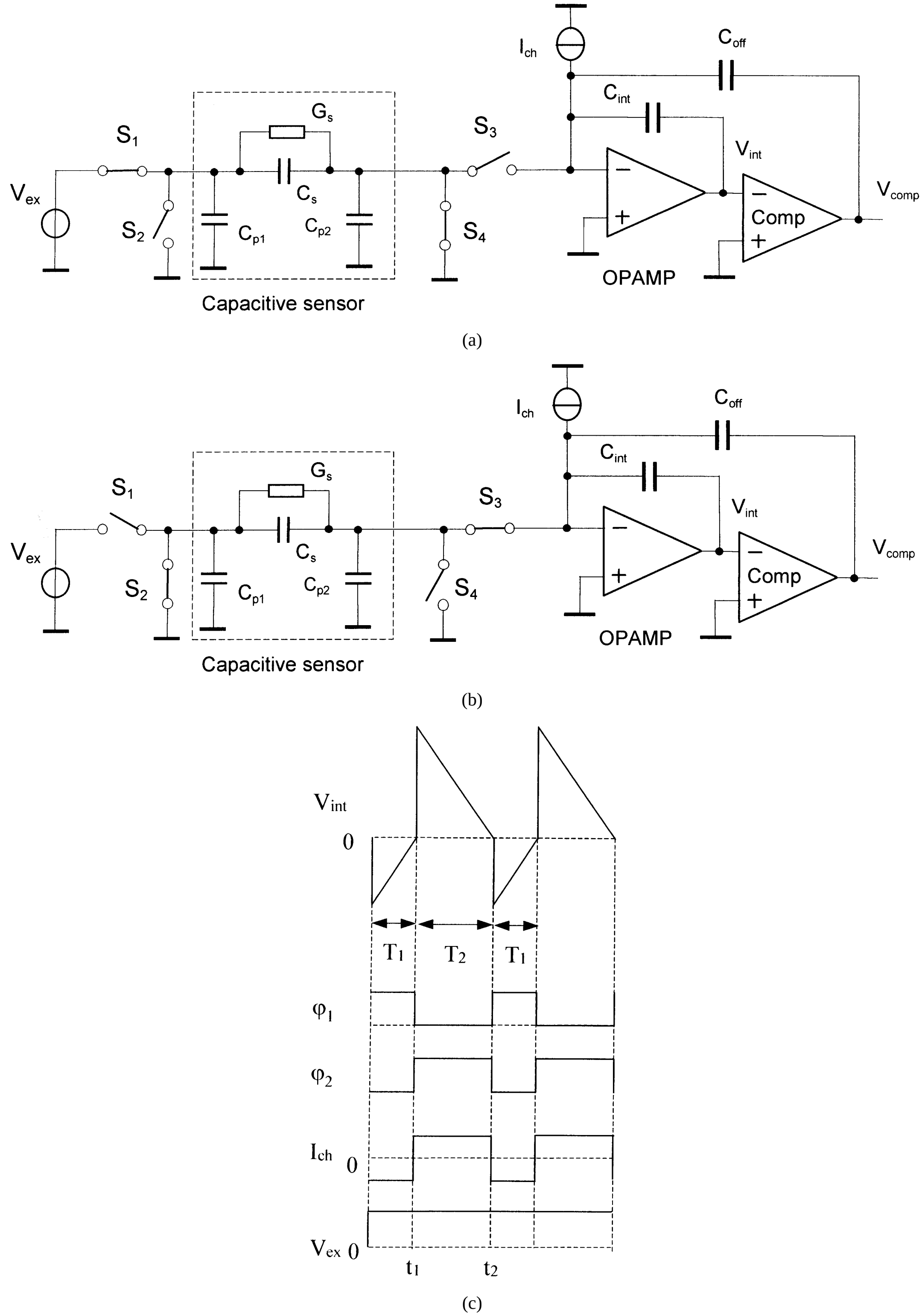


Fig. 3. (a), (b) Two cycles for the capacitance measurement and (c) some of its signals.

a counting frequency of 3 MHz, is employed to measure the output period of the interface, to process the measured data and to communicate with the outside digital world. The system is powered with a single 5-V supply voltage.

The standard deviation and the relative accuracy of the interface have been measured for the case that $C_s = C_{ref} = 2.2$ pF and $G_s = 0.0005\ \mu$S $\sim 15\ \mu$S with a measurement time of about 100 ms. The measurement time amounts to $(NT_{off} + NT_s + NT_{ref})$, which can be changed by changing the period number N. Fig. 5 shows the measured standard deviation and relative error of the interface as a function of the shunting conductance.

It is shown that the measured standard deviation amounts to 0.01% and the error is less than $\pm 0.44\%$ for a shunting con-

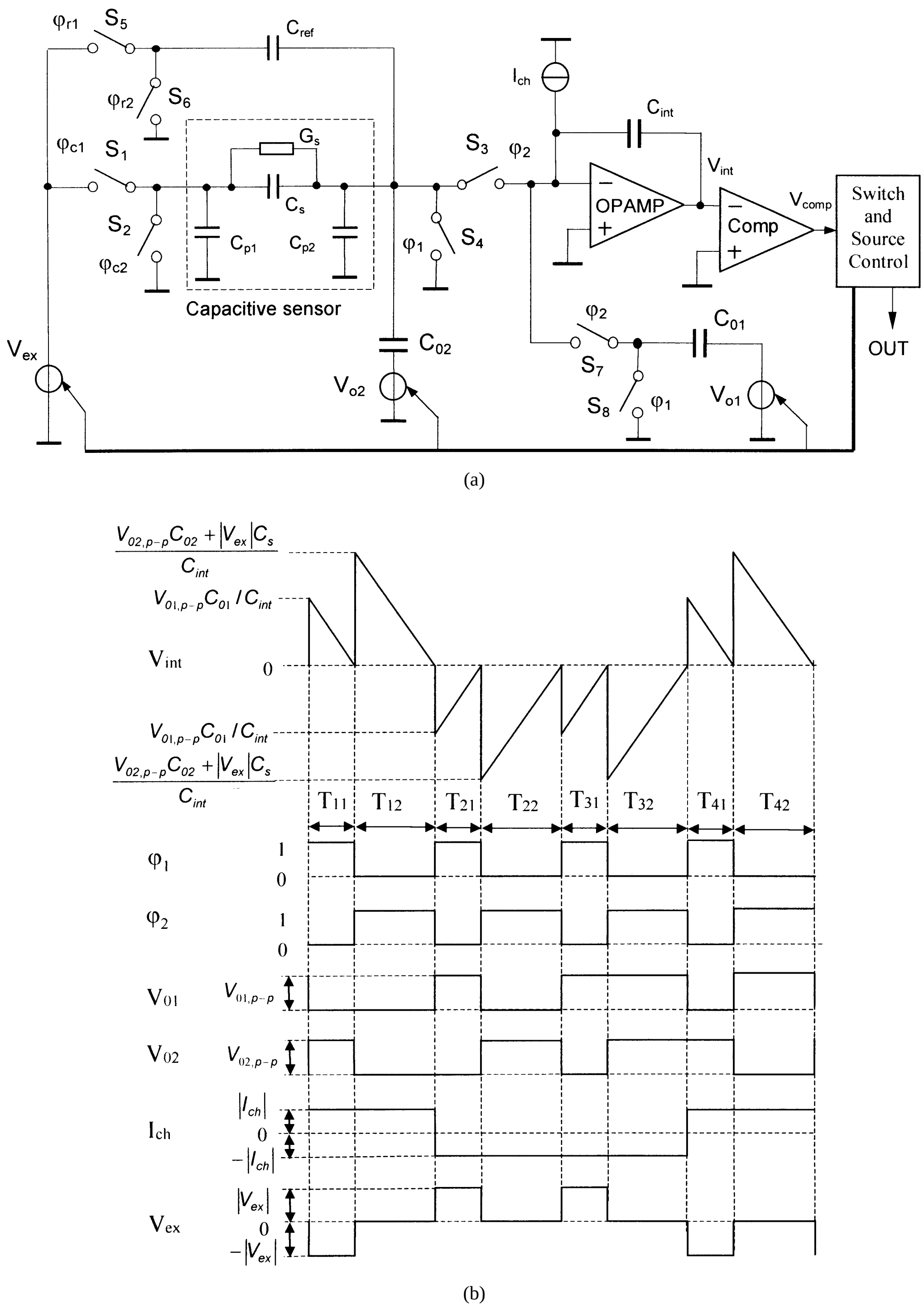
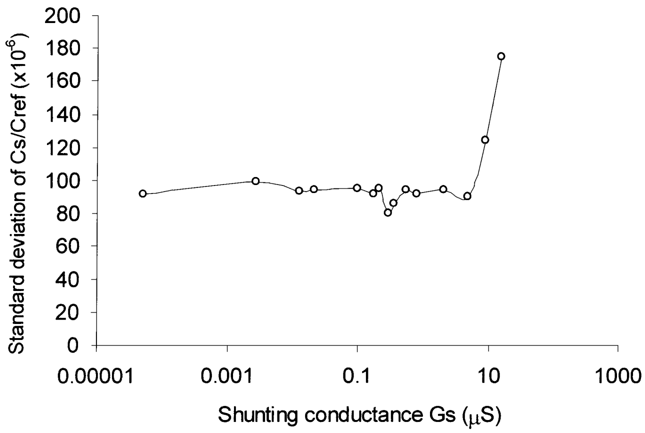


Fig. 4. Improved interface circuit and some of its signals.

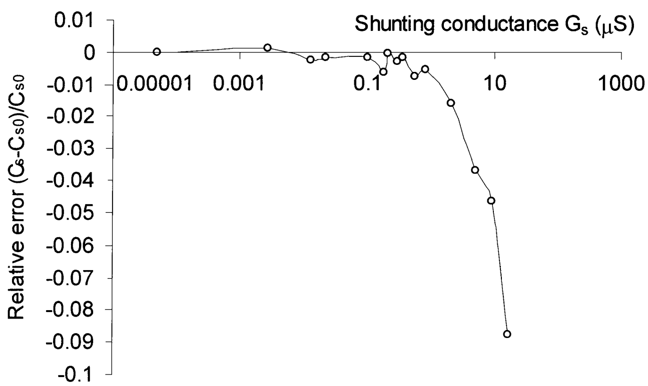
ductance up to 1 μS. This figure shows a rapid increase of the relative error for high values of the shunting conductance. This is due to the fact that the transition time from the charge cycle to discharge cycle is not infinitesimal, which results in a small amount of charge loss.

The standard deviation of the interface originates mainly from two parts [7]: the oscillator noise which is inversely proportional to the square root of the measurement time and the quantization noise caused by sampling in the microcontroller, which is inversely proportional to the measurement time. For short measurement times, the quantization noise is dominant.

For large values of the sensor capacitance, the linearity is limited by the nonidealities of the integrator opamp. Especially, the finite dc gain and limited bandwidth of the opamp will cause nonlinearity, which is proportional to e^{-1/C_s}. For example, when the dc gain and bandwidth of the opamp are 120 dB and 38 MHz, the oscillator frequency is 100 kHz and $C_S = 1000$ pF, the nonlinearity amounts to 0.26%.



(a)



(b)

Fig. 5. (a) Measured standard deviation and (b) relative error of the interface.

IV. Conclusion

In this paper, a novel interface circuit for the capacitive sensors has been designed based on a first-order charge-balanced SC-oscillator. The effect of the shunting conductance is strongly reduced by reducing the voltage across the capacitor during its discharge. The three-signal auto-calibration and the advanced chopping techniques ensure the accuracy and reliability of the interface. The proposed capacitive-sensor interface is very suitable for implementation in low-cost CMOS technology.

References

[1] F. N. Toth, H. M. M. Kerkvliet, and G. C. M. Meijer, "Ultra-linear, low-cost measurement system for multi-electrode pF-range capacitor," in *Proc. IEEE IMTC*, Boston, MA, Apr. 1995, pp. 512–15.

[2] J. van Drecht, "Relaxation Oscillator," Pat. Appl. 91.010 76, 1991.

[3] X. Li, G. W. de Jong, G. C. M. Meijer, F. N. Toth, and F. M. L. van der Goes, "A low-cost CMOS interface for capacitive sensors and its application in a capacitive angular encoder," *Analog Integr. Circuits Signal Processing*, vol. 14, no. 3, pp. 221–231, 1997.

[4] G. C. M. Meijer, J. van Drecht, P. C. de Jong, and H. Neuteboom, "New concepts for smart signal processors and their application to PSD displacement transducers," *Sens. Actuators A*, vol. 35, pp. 23–30, 1992.

[5] S. M. Huang, R. G. Green, A. B. Plaskowski, and M. S. Beck, "Conductivity effects on capacitance measurements of two-component fluids using the charge transfer method," *J. Phys. E: Sci. Instrum.*, vol. 21, pp. 539–548, 1988.

[6] X. Li and G. C. M. Meijer, "Elimination of shunting conductance effects in a low-cost capacitive-sensor interface," *IEEE Trans. Instrum. Meas.*, vol. 49, pp. 531–534, June 2000.

[7] F. van der Goes, "Low-Cost Smart Sensor Interfacing," Ph.D. thesis, Delft Univ. Technology, Delft, The Netherlands, 1996.

[8] F. van der Goes and G. C. M. Meijer, "A novel low-cost capacitive-sensor interface," *IEEE Trans. Instrum. Meas.*, vol. 45, pp. 536–540, Apr. 1996.

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