An Active Clamp Circuit for Voltage Regulation Module (VRM) Applications

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***Abstract*—This paper discusses the design, fabrication, and test of a CMOS active clamp circuit. The active clamp is a linear voltage regulator, with a voltage deadband to allow for voltage ripple, that is designed to operate in parallel with a switchmode voltage regulator. Its specific function is to sink or source large transient currents to microprocessor loads, thus allowing operation with very small output capacitance. Laboratory tests on a prototype IC exhibit stable behavior with negligible overshoot with only 47 microfarads of output capacitance with loads of about nine amperes. Output impedances of 2–3 mΩ are achieved.**

***Index Terms*—Active clamp, linear regulator, VRM.**

I. Introduction

PRESENT day microprocessors such as the Intel Pentium series devices require over 14 amps of supply current at voltages in the range of 1–2 V. The load demand can exhibit abrupt changes from light load (<0.5 amps) to full load in a fraction of a microsecond [1]. Future processor generations are projected to require greater current, up to 100 amps, at supply voltages as low as 1 V. Furthermore, these future processors are projected to impose load steps with di/dt on the order of 450 amp/μS when the processor switches between inactive and active modes, or vice-versa. These trends impose difficult requirements upon the switching regulators supplying power to the microprocessors. One particularly difficult requirement is to maintain the output voltage within a certain tolerance band under large and abrupt load changes.

The goal of this work is to design an integrated circuit capable of supplying the transient currents to these processors. The implementation of this circuit, referred to as an "Active Clamp" can be thought of as two large single-ended transconductance amplifiers, each connected in a unity-gain feedback scheme. The active clamp is designed to be capable of sinking or sourcing the full peak currents, demanded by the processor, but only for a short period of time. Additionally, first order dynamic response is desired, in order to avoid overshoot, which would result in large output voltage excursions above or below a certain tolerance band.

This paper is organized as follows. Section II describes in detail the intended application of the circuit. Section III describes the circuit topology and control issues. Section IV discusses important implementation issues such as integrated circuit layout techniques. Section V contains test results, and Section VI contains conclusions and comments.

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II. Application

A. Active Clamp Function

Fig. 2 shows the interconnection of the active clamp circuit with a typical dc–dc converter. The active clamp circuit works in parallel with the output of a switching regulator. Under steady state load conditions, the active clamp circuit does nothing, i.e., it appears as a high impedance terminal. If an abrupt load change occurs which is sufficient to cause the output voltage of the switching regulator to exceed a certain tolerance band, the active clamp circuit will turn on. Typical waveforms of the application are shown in Fig. 1. The top waveform shows the load current changing from low (<1 A) to high (10 A). The middle waveform is the output voltage of the switching regulator. Before the load changes, the output voltage contains steady-state ripple, since the active clamp is off and in a high impedance state while the converter is operating normally. Once the load steps up, the output voltage begins to sag since the switching regulator cannot increase its inductor current instantaneously. When $V_{\rm out}$ drops below δV from its average, the active clamp turns on and behaves as a linear regulator. As such, $V_{\rm out}$ will droop below the tolerance band due to the finite regulation of the circuit. The output voltage begins to recover as the inductor current (lower waveform) of the switching regulator increases. Thus the active clamp circuit must be able to handle the full load current, but only for a short period of time. This is typically tens of microseconds, determined by the time required for the switching regulator to take over the load current. Note that a similar function is needed when the load changes from high to low. Since the inductor current cannot decrease instantaneously, the output voltage will increase, at which point the active clamp should turn on and sink current. From this point on, the function as shown in Fig. 1 will be referred to as the "pull-up" function, and the complementary function as the "pull-down" function.

In addition to the load capability, it is also desired that each transconductance amplifier have a high enough bandwidth such that the system consisting of the active clamp circuit and the output capacitors of the switching regulator behave nearly as a first order system. This is an important specification due to the nature of the application, which is voltage regulation. Any overshoot in the output voltage may result in long term reliability problems in the microprocessor being powered. The more likely scenario is that voltage undershoot at the output voltage may cause soft logic errors in the microprocessor.

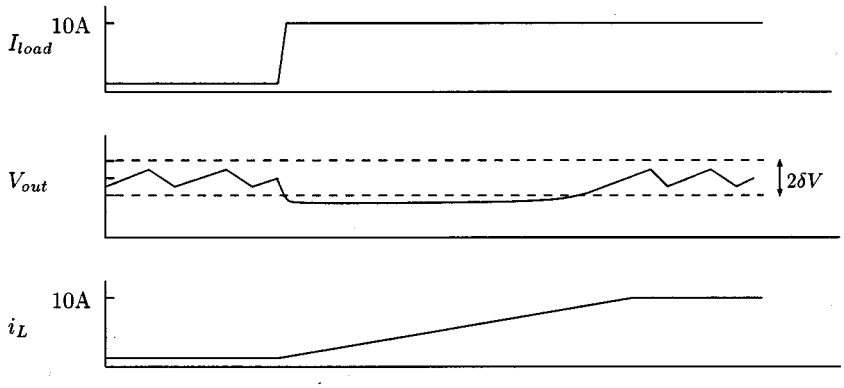


Fig. 1. Typical application waveforms.

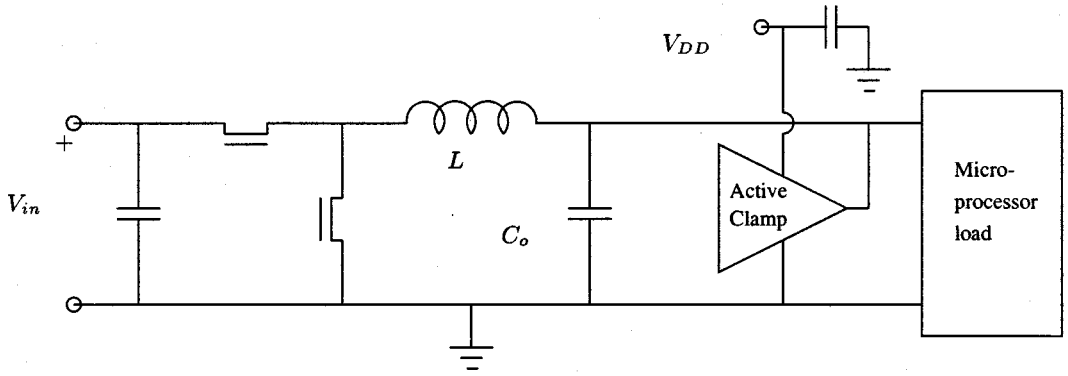


Fig. 2. Interconnection of active clamp circuit with switchmode regulator.

B. Output Capacitor Requirements

In determining the required output capacitor in a VRM application, two requirements are relevant. One is the output capacitance needed to satisfy a maximum ripple specification, and the other is the output capacitance needed to ensure that the output voltage does not exceed a certain tolerance band under maximum load change conditions. For the output ripple requirement, an examination of current state of the art switching regulators is useful. The Pentium II and III applications require about 14 amps from a switching regulator operating at about 300 kHz. For the 5 V to 2 V buck application, a filter inductor of $L = 2.0\ \mu$H will yield a peak–peak current ripple of about 2 amps, a typical design. In order to achieve a peak–peak output ripple of 50 mV, a capacitor of only about 17 μF is needed if equivalent series resistance (ESR) is neglected. With a 20 μF ceramic chip capacitor with ESR typically less than 10 mΩ, the ESR contribution to the output ripple voltage will only be on the order of 20 mV peak–peak. It is likely that some designers would select a larger capacitor when considering ripple, in order to further reduce the voltage ripple and to avoid the possibility of a capacitor reliability problem because of the large ripple current. Nevertheless, designs in the range from 20 μF to 50 μF are feasible with ceramic chip capacitors, or with solid tantalum chip capacitors requiring total capacitance approaching 200 μF, due to higher ESR.

C. Benefit of Active Clamp

To better understand the potential benefit of the active clamp circuit in the VRM application, analysis must be done on the various scenarios that may occur under an abrupt load change without the use of the active clamp circuit. The first, and less likely, scenario is that the duty cycle of the switching regulator does not saturate. In this case, a very simple analysis based on an averaged model as shown in Fig. 3 can be made. Solving for the output voltage as a function of time, with a step in load current, results in

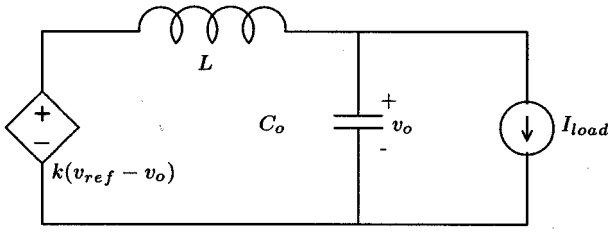


Fig. 3. Simple average circuit model for voltage-mode controlled buck converter.

$$v_o(t) = -\frac{I_o}{\omega_c C_o}\sin(\omega_c t) \tag{1}$$

where

I_o current magnitude in amps;
C_o output capacitance;
ω_c crossover frequency of the feedback loop.

Assumptions here are that all forms of damping including output capacitor ESR are negligible, current feedback is not used, and the input impedance is stiff. Using equation (1), an estimate of the first peak of the voltage transient response can be made.

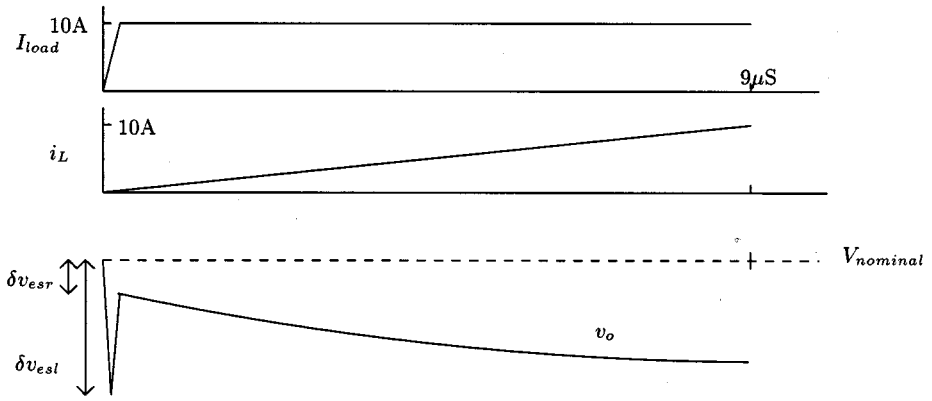


Fig. 4. Circuit waveforms under duty cycle saturation.

Using an aggressive cross-over frequency of 100 kHz, a load step of 14 amps, and an output capacitor of 20 μF results in a peak voltage of 1.1 V. A 1.1 V excursion in the output voltage is obviously not acceptable, especially given that the nominal voltage is approximately 2 V. With $C_o = 200$ μF, an excursion of 111 mV would be expected. With $C_o = 2000$ μF, one would expect only a 11 mV excursion. Again, emphasis must be made that the assumption that the duty cycle does not saturate is unrealistic. It should be noted that a Maxim test board rated at 15 A is designed with 2000 μF of electrolytic capacitance at the output [5]. From the above analysis, it would seem that 2000 μF is an over-design.

A more realistic scenario is that the duty cycle nearly always saturates (i.e., reaches its maximum or minimum) under a large load transient. Waveforms depicting a simple analysis incorporating saturation are shown in Fig. 4, and described here. Assume the converter output is initially at 2 V, supplying zero load current. The load then steps to 14 amps. The converter reacts by applying full duty cycle. If the input is stiff at 5 V, the voltage across the inductor is about 3 V if the output does not sag very much. With 3 V on the inductor, it requires about 9 μS for the current in the 2 μH inductor to ramp up to 14 amps. At the end of this 9 μS transient, the output voltage can begin its recovery, hence this is the approximate time point where the voltage bottoms out. The total charge removed from the output capacitor, assuming a ramp current waveform, is 65 μC. This analysis is independent of the output capacitor value and assumes a stiff (i.e., large input capacitance) input voltage and also assumes that 100% duty cycle can be applied. Now with a 20 μF output capacitance, the voltage transient will be about 3.25 V peak. With 200 μF or 2000 μF, the transient voltage would peak at 325 mV or 32.5 mV, respectively. To achieve a $\pm$5% tolerance band on the output voltage, approximately 600 μF of output capacitance is needed. Note that the analysis assuming duty cycle saturation results in a larger voltage transient than that assuming no duty cycle saturation, for the same output capacitance. From this analysis, the Maxim test board with 2000 μF does indeed make sense.

The advantage of the active clamp circuit is that the output capacitor will only need to be designed to handle the ripple current, and not to contain the output voltage during load transients. For the application discussed here, ceramic chip capacitors as small as 20 μF may be sufficient when incorporating an active clamp circuit, whereas output capacitance of at least 600 μF would otherwise be needed. Another trend in microprocessor voltages is the decrease in the percent change tolerated on the supply. If a $\pm$2% tolerance band is required in the application described above, then approximately 1625 μF of output capacitance would be needed. Again, this is substantially larger than that required to handle the ripple current. In reference [6], a slightly different application is analyzed. In this application, the load is specified at 20 A maximum at 3.3 V, with a tolerance of $\pm$2%. The output capacitor bank required to support a full step load transient in this application includes 20 000 μF of bulk hold-up capacitance in conjunction with a network of paralleled high frequency (lower inductance, lower ESR) tantalum and ceramic capacitors. In this scenario and that involving the specification of future microprocessors, the active clamp will yield far greater benefits.

Although the use of an active clamp can reduce the amount of output capacitance needed, the energy needed to hold up the output voltage must come from a source. This source is the bypass capacitor on V_{DD} as shown in Fig. 2. Note that this supply may nominally be at a higher voltage than the input or output of the switching regulator, perhaps as high as 12 V. In addition, the amount of voltage sag that can be tolerated during a transient is much higher on this supply. As such, the amount of capacitance needed on V_{DD} to store the required energy is substantially less than that needed at the output.

III. Circuit Description

A. Circuit Overview

Fig. 5 shows a functional schematic of the active clamp circuit. Note that both pull-up and pull-down functions are included. The parts of the schematic enclosed by a dashed box are implemented in an IC;[1] these include the transconductance amplifier (G_M stage), as well as the circuitry to set the tolerance band ($\pm\delta V$). The arrows in the figure denote the only direction in which the output current can flow from the G_M stages.

[1]In previous work, a discrete implementation of the active clamp was designed, built and tested. This design utilized bipolar transistor IC kit parts, high speed commercial operational amplifiers, and discrete passive components to realize the active clamp function. For a detailed description of the work, refer to [2].

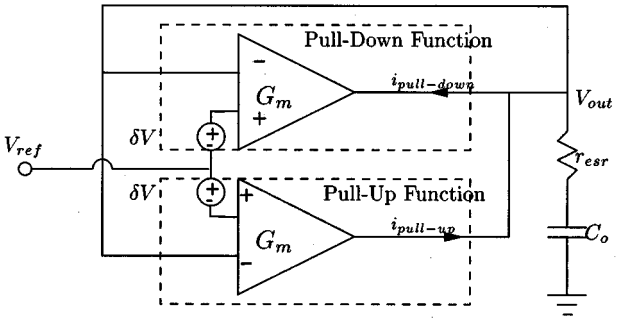


Fig. 5. Functional schematic of active clamp circuit.

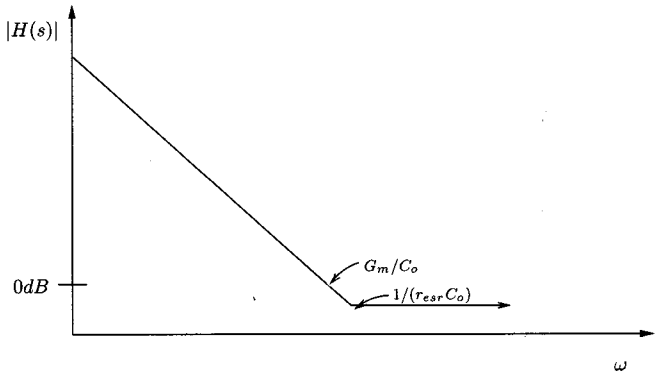


Fig. 6. Bode plot magnitude of control loop.

Thus, the pull-up G_M stage can only source current while the pull-down can only sink current. The pull-down function is only active when V_{out} is greater than $V_{ref} + \delta V$, while the pull-up function is only active when V_{out} is less than $V_{ref} - \delta V$. As a result, both functions can never be active at the same time. This allows analysis of the loop dynamics to be made separately for each function.

B. Frequency Response and Gain

The transconductance amplifier is designed to have a high enough bandwidth as to not affect the loop dynamics of the overall system, i.e., it has only high frequency poles. From Fig. 5, the control loop of either function consists of a transconductance amplifier driving a capacitor with finite ESR. The open loop transfer function $H(s)$ is

$$H(s) = \frac{V(\text{out})}{V(\text{in})} = G_m\left(\frac{1}{sC_o} + r_{esr}\right) = G_m r_{esr}\left(\frac{\frac{1}{r_{esr}C_o} + s}{s}\right) \tag{2}$$

where G_m is the transconductance and r_{esr} is the ESR of the output capacitor C_o. Equation (2) shows that there is a pole at the origin and a zero at $-1/(r_{esr}C_o)$. The crossover frequency is G_m/C_o. To ensure that the gain of $H(s)$ falls below unity, the zero frequency must be higher than G_m/C_o. This results in the following inequality, which is necessary for stability:

$$1/G_m \geq r_{esr}. \tag{3}$$

In the neighborhood of the frequencies of interest, ceramic chip capacitors have been measured to have ESR equal to or less than approximately 5 mΩ. Equation (3) leads to the need of using multiple chip capacitors in parallel, to lower the effective ESR. Note that the zero frequency remains constant, regardless of how many capacitors are in parallel, since the total ESR is inversely proportional to the total capacitance. Higher capacitance does, however, lower the gain of the integrator, which tends to stabilize the system. Fig. 6 shows a simplified Bode plot of the open loop system (simplified because high frequency poles are neglected). The solid line is the magnitude of $H(jw)$ taking into account the zero due to the output capacitor's ESR.

The output resistance of the closed-loop system is easily calculated as the open-loop output resistance (R_{out}) divided by one plus the loop gain ($G_m R_{\text{out}}$). This evaluates to approximately $1/G_m$.

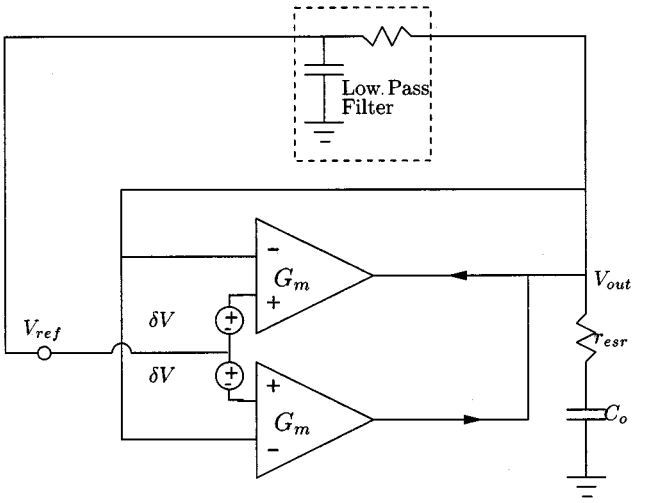


Fig. 7. Low pass filtering scheme for supplying voltage reference to active clamp circuit.

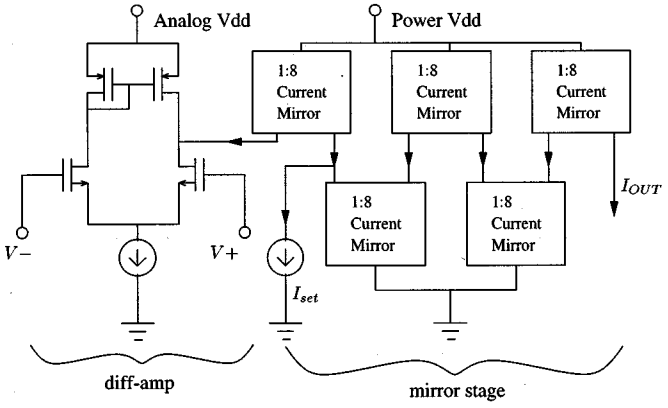


Fig. 8. Schematic: Pull-up function of active clamp IC.

C. Voltage Reference Scheme

Another issue is the method in which the reference voltage is set. The reference voltage level (i.e., the commanded output voltage) can be generated in one of two ways. The first, and straightforward approach, is to simply use a voltage reference

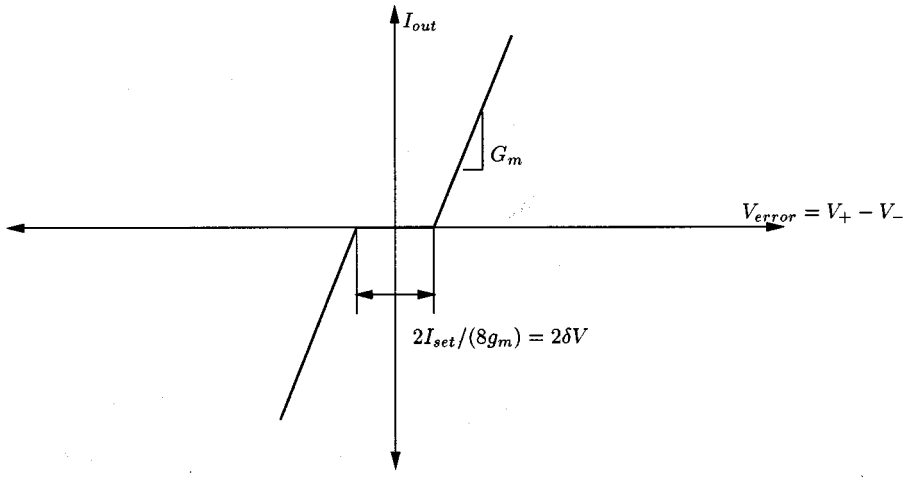


Fig. 9. Approximate transfer curve of output current versus input error voltage for upper and lower clamp combined.

of some kind. The second method, and the one adopted here, is to use an R–C network to low pass filter the output voltage of the switching regulator. This scheme is depicted in Fig. 7. This method allows the tolerance bands to be tightened substantially, since the reference voltage is derived directly from the output of the dc–dc converter. In fact, with the scheme of Fig. 7, the tolerance bands will be mainly limited by the output voltage ripple. We note that this method has also been developed and used in the commercial part in [8].

IV. Integrated Circuit Implementation

A. General Topology

Fig. 8 shows a functional schematic of the transconductance amplifier used in the pull-up function of the active clamp IC. Note that current mirrors are used for each current gain stage. The total transconductance is the g_m of the differential input stage times the current gain product of all the following current mirror stages. In this application, the resulting transconductance is

$$G_m = g_m 8^5 = 1/(2\ \mathrm{m}\Omega) = 500\ (\mathrm{Amps/Volt}) \qquad (4)$$

where g_m is the transconductance of the differential input stage. The factor 8^5 is a result of five stages of $1:8$ current mirrors.

A double-to-single ended differential stage is used for the input of the clamp circuit. This topology was chosen due to the need for high CMRR [7]. Since the clamp circuit will be operating in a high current and consequently high magnetic field environment, the inputs to the IC are especially vulnerable to systematic noise. Differential noise can be controlled by careful layout of the printed circuit board. Common mode noise, however, is difficult to eliminate from the inputs. As such, the higher the CMRR of the circuit, the more likely that any problems related to common mode noise can be avoided.

The current source I_{set} is used to set the tolerance band of the clamp circuit. The differential stage always has a quiescent current flowing through it. The first current mirror stage will turn on only if a positive error signal exists across the differential stage, that is if $V_{error} = V^+ - V^- \geq 0$. The following four current mirror stages will only turn on when the error signal is large enough to cause a current in the first mirror stage to exceed I_{set}. The calculation of the tolerance band results in $\delta V = I_{set}/(8g_m)$ where δV is one half of the total band in the application. These set points are shown in Fig. 9 for the system consisting of the pull-up and pull-down functions combined. Note that the voltage ripple of the switching converter must nominally exist within the tolerance band of $2\delta V$ during steady state operation to avoid excessive power dissipation in the clamp circuit.

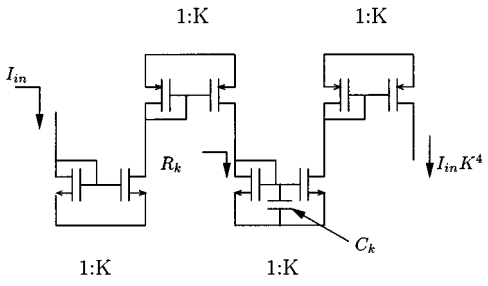


Fig. 10. Series of $1:K$ current mirrors.

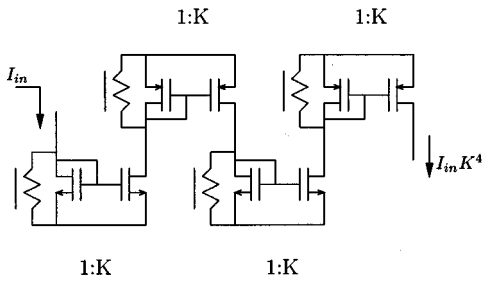
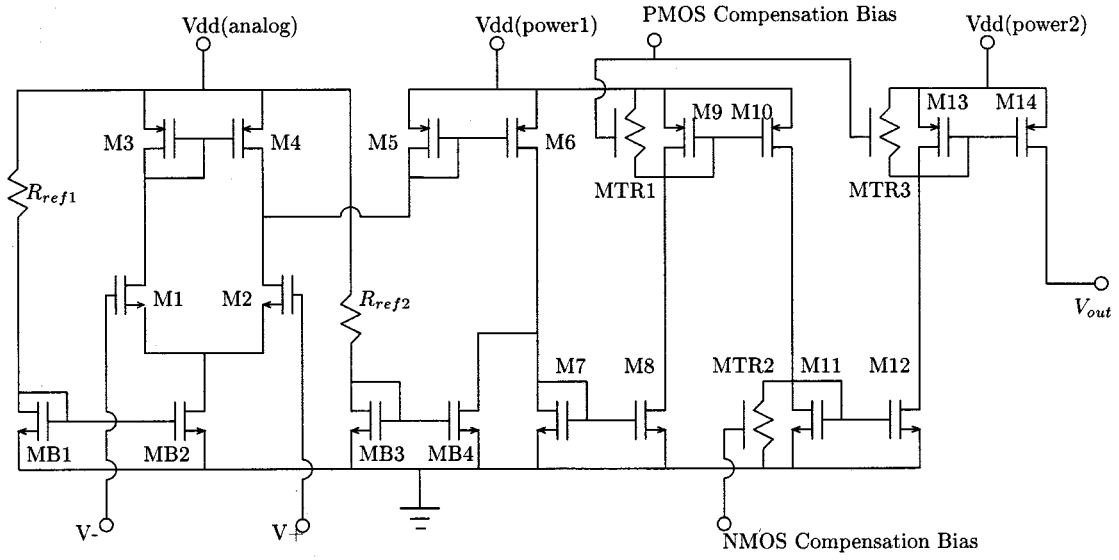


Fig. 11. Series of $1:K$ current mirrors with "leak" resistors.

B. Frequency Response and Compensation

The use of multiple current gain stages is required to avoid introducing one or more low frequency nondominant poles into the system. Since the final transistor of either clamp functions must be sized to handle large currents, it will present a large capacitance to the previous stage. As discussed in [3], several gain stages should be used in cascade, each with the same gain. Fig. 10 shows a series of $1:K$ current mirrors. The approximate resistance (R_k) of each node is $1/g_m$, where g_m is the



Device	Size(um)	Device	Size(um)	Device	Size(um)
M1	2550/1.2	M8	2160/.6	MB1	108/1.2
M2	2550/1.2	M9	2214/.6	MB2	1080/1.2
M3	1740/1.2	M10	17712/.6	MB3	144/.6
M4	1740/1.2	M11	2970/.6	MB4	576/.6
M5	108/.6	M12	23760/.6	MTR1	268/.9
M6	864/.6	M13	23400/.6	MTR2	432/.9
M7	270/.6	M14	187200/.6	MTR3	6758/.9

Fig. 12. Complete schematic of CMOS active clamp circuit with table of sizes (pull-up function).

transconductance of the diode connected transistor(gate connected to drain). The approximate equivalent capacitance (C_k) of each node is $(K+1)C_{gs}$, where K is the current mirror ratio and C_{gs} is the gate to source capacitance of the diode connected transistor. Thus, the pole associated with each node is

$$p_k = \frac{g_m}{(K+1)C_{gs}} \text{ (rad/s)}.$$

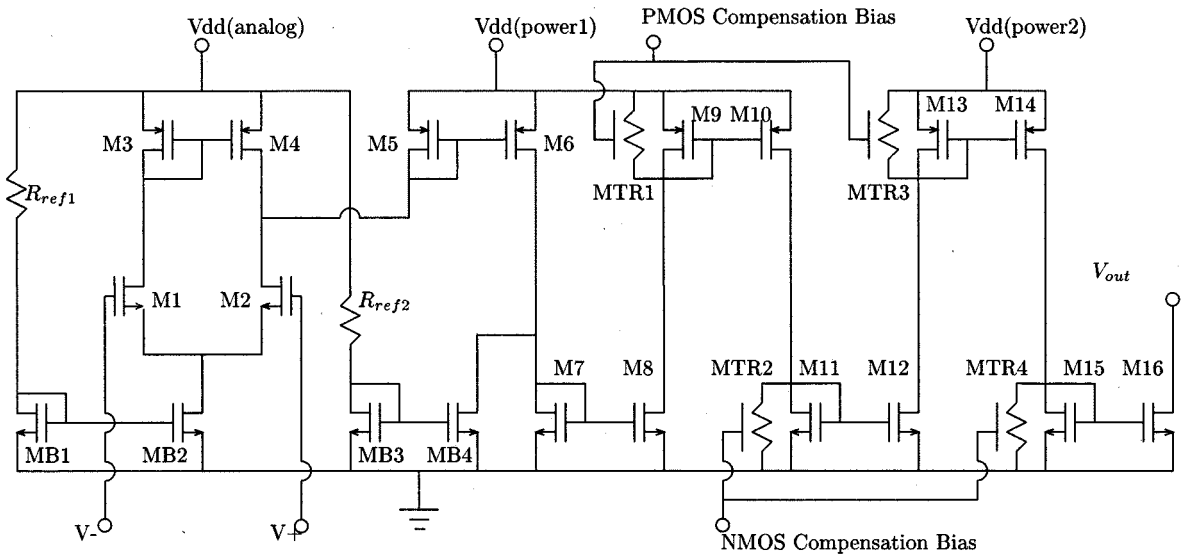
Note that the pole p_k is simply at a frequency $K+1$ times lower than the transition frequency f_t of the device.

Since each node contributes a pole at the same frequency, and that frequency is only $K+1$ times lower than f_t, the series of current mirrors will not contribute any relevant poles to the system so long as g_m is high enough. However, since g_m is proportional to the square root of the drain current I_D, g_m approaches zero as the input transistor approaches the cut-off region of operation. This presents a problem to the speed of the clamp circuit, since the turn-off process may contain a larger delay and lead to instability. This problem is solved by using a "leak" resistor in parallel with the diode connected transistor of the simple current mirror stages, as shown in Fig. 11. This effectively pins the input impedance to a maximum value, determined by the resistance of the leak resistor. The leak resistors are actually implemented by MOSFET devices in the triode region. The bias for the triode devices is provided off chip for adjustment in the testing process and are not shown in Fig. 11. Fig. 12 shows the complete schematic of the upper clamp along with all the transistor sizes. The lower clamp schematic and sizes are shown in Fig. 13.

The pole contributed by the output of the differential input stage is at a high enough frequency as to be negligible. This is a result of the way in which the tolerance bands are set. Since the clamp is not actually active until the drain current of M6 exceeds I_{set}, it is guaranteed that M5 will be on when the clamp activates. The leads to the equivalent resistance at the differential pair output node to be $1/g_{m,\,\mathrm{M5}}$, which results in only a high frequency pole. Also note that a "leak" resistor is not required on the input to the second current mirror stage, since MB4 achieves this role. The combination of R_{ref2}, MB3 and MB4 are the devices that implement the current source I_{set} in Fig. 8.

C. Layout Issues

Due to the high current nature of the application, the layout of the active clamp IC is critical. Guard rings were used extensively throughout the design to increase isolation. The chip was fabricated in an 0.5 μm CMOS triple metal layer process. This process utilizes a p^+ type substrate and a p-type epitaxial layer. As such, isolation between NMOS devices may not be as high as that of



Device	Size(um)	Device	Size(um)	Device	Size(um)
M1	2550/1.2	M9	2214/.6	MB1	108/1.2
M2	2550/1.2	M10	17712/.6	MB2	1080/1.2
M3	1740/1.2	M11	2970/.6	MB3	144/.6
M4	1740/1.2	M12	23760/.6	MB4	576/.6
M5	108/.6	M13	117000/.6	MTR1	268/.9
M6	864/.6	M14	93600/.6	MTR2	432/.9
M7	270/.6	M15	7470/.6	MTR3	6758/.9
M8	2160/.6	M16	59760/.6	MTR4	1872/.9

Fig. 13. Complete schematic of CMOS active clamp circuit with table of sizes (pull-down function).

PMOS devices since the NMOS devices all have the same bulk. Since additional junction isolation was not possible for the NMOS devices, care was taken to leave additional space between all transistors in the IC. Fig. 14 shows a die photograph of the clamp circuit. Only one IC was fabricated, but it contains all the necessary blocks to realize either the upper or lower clamp function. As the photo shows, both the large output PMOS (M13,14 in Fig. 12) and NMOS (M15,16 in Fig. 13) final mirror stages are present on the same chip. For the pull-up clamp function, the large NMOS mirror is not used. For the pull-down clamp function, all stages are used, but the large PMOS mirror is connected to have close to unity current gain. This is necessary to achieve similar current gains between the two clamp functions, since the pull-down clamp function has an additional mirror stage.

The output stage mirrors of the clamp circuit need to drive currents approaching 10 amps. It is thus imperative to minimize the parasitic resistance at the terminals of the stages [4]. A resistance of only 0.25 Ω on the output and supply inputs of the stage would create a total drop of 5 V for an output current of 10 amps. This is obviously not acceptable as it will limit the maximum current drive of the circuit. The sheet resistance of the metal layers ranges from approximately 40 m$\Omega/\square$ (metal 3) to 80 m$\Omega/\square$ (metal1,2). Fig. 15 shows a representative layout of one unit cell of a 1 : 8 NMOS mirror stage and the unit cell's equivalent schematic. The drain of the input transistor (M_{in}) is approximately 8 times smaller than that of the output transistor (M_{out}) as expected. This middle area is filled with N-type diffusion, except for one area as indicated by the white box between the two drain areas. This is needed to isolate the two drains. The solid black area indicates the polysilicon gate of the devices. The small crossed-hatched box connecting the polysilicon gate and the drain of M_{in} indicate an ohmic contact to form the input connection of the current mirror. The common source of the two transistors resides both above and below the active region of the device. The lowest strip in the layout indicates a long well contact. This is necessary to help prevent latch-up due to the high current nature of the application.

The layout of the unit cell was made in such a way as to facilitate the construction of large arrays of cells. Fig. 16 displays such an array. The drains of the input ($D_{M\,\text{in}}$) and output ($D_{M\,\text{out}}$) transistors form small islands spaced evenly throughout the array. The source and well contacts basically form long fingers through the array. Some areas within the drains of the output transistors were designed with only diffusion creating the electrical path. This allowed metal 1 to be used to connect adjacent fingers of the source area.

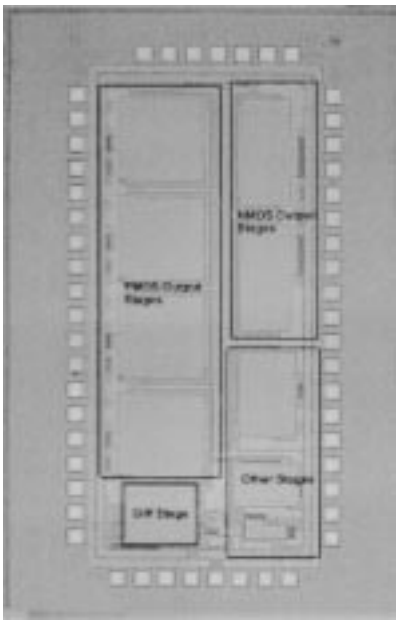


Fig. 14. Die photo of active clamp circuit.

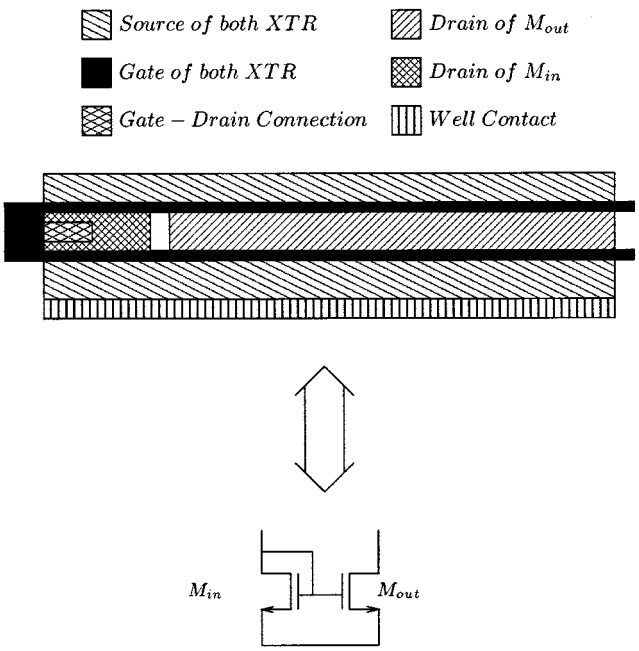


Fig. 15. Layout (top view) of NMOS 1 : 8 current mirror unit cell.

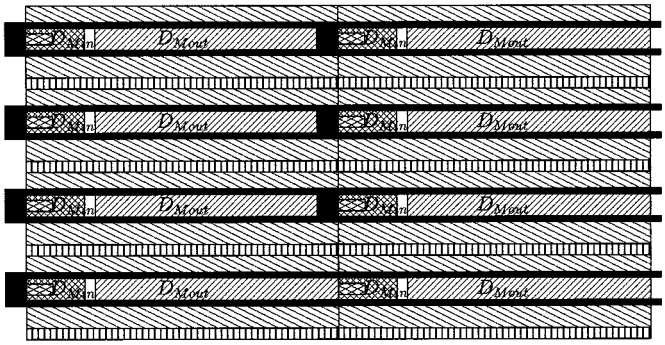


Fig. 16. Layout (top view) of multiple NMOS 1 : 8 current mirror unit cell.

A cross section of the cell is shown in Fig. 17. The line where the cross-section is taken is indicated in the upper part of the figure. The two drain areas are indicated, along with the various contacts. Any area not explicitly labeled, contains field oxide. The gate oxide is not shown. The two metal 1 sections that are a distance above the diffusion are the ones used for the connection between adjacent source fingers. Metal 2 is used for the input of the mirror. Since metal 2 is also part of the contact structure for the output drain connection, holes are needed in the sheet of metal 2 to maintain isolation. As such, metal 2 appears as a nearly continuous sheet of metal, with evenly spaced holes throughout. A top view of the metal layers is shown in Fig. 18. Metal 3 is used to connect all the drains of the output transistors together and to bring the current off chip. Since metal 3 is the top most metal layer, it is one continuous sheet over the array with no holes whatsoever. The PMOS "cell" and construction is nearly identical to that of the NMOS with the obvious difference in the type of material used.

From Fig. 12, the largest device on the circuit is the last PMOS output transistor (M14), which is nearly 1/5 of a meter in width. To avoid potential latch-up type behavior, this mirror stage was broken up into 4 smaller identical pieces, each of which is surrounded by guard rings. The same was done for the final NMOS stage. The final chip size was approximately 1.6 mm $\times$ 3.3 mm. The IC was mounted into a plastic QFP 44 pin package. Conductive epoxy was used to mount the IC inside the electrically grounded gold cavity, to help prevent latch-up. Finally, for the high current input/output paths of the design, multiple bond wires and pins were used to reduce the series impedance.

V. Test Results

A. Overview

As discussed in Section IV-C, an IC was fabricated in an 0.5 μm 3 metal layer CMOS process. A printed circuit board was made to test the chip. Initial attempts were made to use only one IC to implement either of the clamp functions. This approach failed, possibly due to deficiencies in the QFP package. The lead frame of the package, along with the bond wires, may form parasitic magnetic coupling paths between the high current output stages and the sensitive voltage input pins. Another possible explanation is substrate coupling between stages. In fact, with only one IC, it was demonstrated that open loop operation resulted in oscillations which implies the existence of parasitic feedback paths. In order to achieve proper operation, two ICs were used to implement one of the clamp functions. This is not necessarily a failing point, since for the projected currents of 60 amps or more, it would be highly unlikely that only one IC could be used. It would be likely that many of the larger current mirror stages would be build on a separate IC, using a higher voltage power process. This would be effective for cost reasons in order to use a higher supply voltage, which also reduces the capacitance needed on the supply as discussed in Section II-C. In the experimental work discussed here, the first IC has the differential stage and the first three mirror stages. The second IC has the last two or three stages, depending on which function is being implemented.

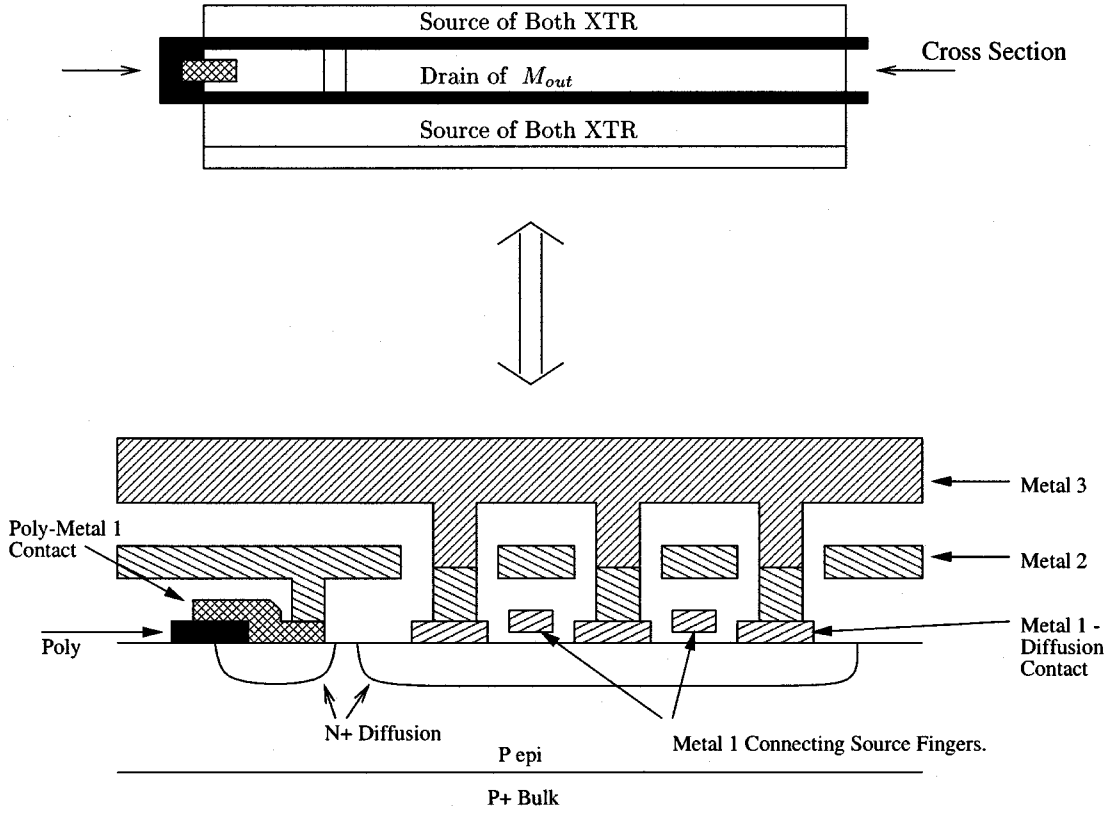


Fig. 17. Cross section (side view) of NMOS 1 : 8 current mirror unit cell.

As determined in laboratory experiments, additional compensation was needed in the active clamp test board. This is shown as the R_s and C_s components in Fig. 19. The R_s–C_s network in the output voltage sense path adds an additional pole to the feedback loop. The analysis made in Section III-B neglected all higher frequency poles and zeros. Without additional compensation, the loop gain of the system in the frequency range of these high frequency poles and zeros may be close to unity. To create a single pole role-off in the loop-gain magnitude above the frequency of the ESR zero(due to r_{esr}, C_o), R_s and C_s are added. The same compensation network is used in the reference loop, as is used in the output voltage feedback loop. This is done to match the common-mode signals between the two loops.

B. Test Board Setup

A functional schematic of the test board is shown in Fig. 20 for testing the pull-up function. A function generator is used to apply a very low duty cycle pulse to the input of the gate driver chip. This chip then turns on the power MOSFET, thus simulating the processor going from light load to high load. The test board for the pull-down clamp function is very similar, except that the load circuit goes to a separate supply rather than ground. Thus, when the switch turns on, current is sourced into the output node simulating the processor going from high load to light load. Since the low-pass filtering scheme, as described in Section III-C, is used for setting the reference voltage, a dc–dc converter would usually be used to set the nominal output voltage. For simplicity in test, a high impedance voltage supply is used instead. Table I lists various relevant parameters in the test board setup. Note that R_{LPF} and C_{LPF} are the values for the low-pass filter resistor and capacitor, respectively. For C_o, ten 4.7 μF ceramic chip capacitors were used in parallel to achieve a low effective ESR of approximately 0.5 mΩ. This results in a zero frequency of approximately 42 Mrad/s. With the target G_M of 500 A/V, the cross-over frequency of G_M/C_o would be about 10.6 Mrad/s. In practice, G_M is closer to 370 A/V which gives a cross-over frequency of 7.9 Mrad/s. The values of R_s and C_s result in a compensation pole frequency of approximately 10 Mrad/s. $V_{DD}(power2)$ is set at a higher voltage, 4.25 V, than $V_{DD}(analog)$, 3.3 V, or $V_{DD}(power1)$, 3.3 V, in order to achieve higher current drive. The process used for the fabrication is actually a 3.3 V process, so using 4.25 V for the supply may cause long term reliability problems. This is a minor point since a higher voltage process can be used. The 3.3 V process was used because it was readily available at the time of fabrication.

C. Results

Both pull-up and pull-down clamp functions were tested at various load currents. To measure the transconductance accurately, two different load currents were used and the resulting waveforms were superimposed on each other. The G_M could then be calculated. Fig. 21 shows the output voltage for the pull-up clamp function under two different load steps, 0.3 A and 6.3 A. The difference in voltage, ΔV, after the transient, is approximately 16 mV. This gives a G_M^{-1} (pull-up function) of 16 mV/6 amps $= 2.66$ mΩ. Fig. 22 shows the analogous waveforms but for the pull-down clamp function. Here the ΔV is approximately 18 mV. This give a G_M^{-1} (pull-down function)

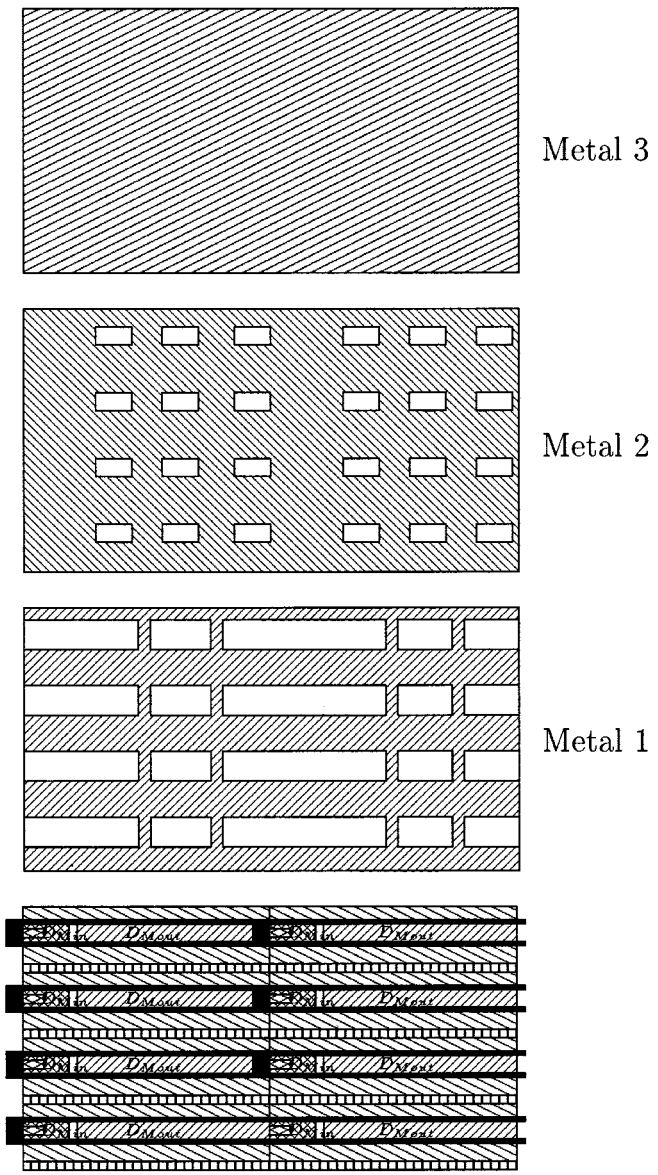


Fig. 18. Top view of metal layers in array of unit cells.

of 18 mV/6 amps $= 3$ mΩ. These two figures also show that for light loads, the transient response contains zero overshoot. For higher load currents, some overshoot exists, but is limited to approximately 10 mV. The highest current achieved in the experiments is approximately 9 A. This is mainly limited by the output transistors entering the triode region.

The power dissipation of the circuit consists of two parts. It is assumed here that the transient power dissipation is negligible since the frequency at which the microprocessor switches between wake and sleep modes is typically very low. This leaves the static dissipation in the differential input stage and the current through the first mirror. For this particular experiment, the current I_{ref1} is measured to be approximately 77 μA. Due to the current mirror formed by MB1–MB2, the static current is 10 I_{ref} which results in 0.77 mA for each of the two clamp function half circuits. This results in 5 mW of static power dissipation in the differential to single-ended input stages since the analog supply rail is at 3.3 V.

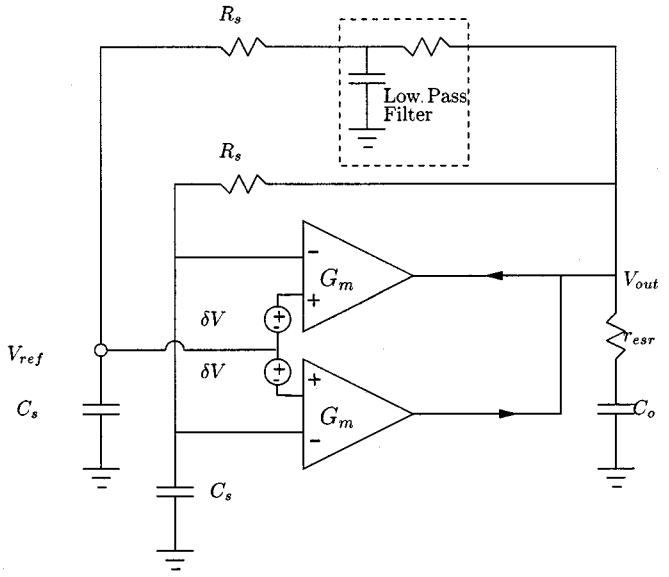


Fig. 19. Additional compensation elements on test board.

Another component of loss is due to the current through the output transistor of the first mirror, MB6 in Figs. 12 and 13. This current is due to ripple voltage appearing on the inputs of each of the transconductance amplifiers. Let the output current of the first mirror stage be I_1. Assuming the output voltage ripple has a peak to peak value of 40 mV in an application, and the transconductance of the differential stage is approximately (1/2.5 mΩ)/8^5 $=$ 12.2 mA/V, I_1 then varies between 0 and 2.0 mA for each of the clamp functions. Since only one mirror stage of either clamp function is active at a given time, the total average current is approximately 1.0 mA. This leads to 3.3 mW of dissipation in the first mirror of both functions. The total average power dissipation is thus 8.3 mW.

VI. Conclusion

An active clamp circuit designed to provide transient currents for microprocessor loads has been designed, fabricated and tested. Laboratory experiments demonstrate stable and nearly first order response to step load changes with as little as 47 μF of output capacitance. The maximum current attained is approximately 9 A. This is mainly limited by the final output transistors entering the triode region. A low-pass filtering reference scheme is used to set the command voltage for the clamp circuit. This method allows the tightening of the tolerance bands, which are limited by the output voltage ripple of the dc–dc converter.

Fundamentally, the active clamp device allows the use of a small ceramic type output capacitor in a modern microprocessor power supply, without simultaneously requiring that the associated switching regulator be designed for extremely fast transient response. Designs of pure switchmode voltage regulation modules (VRM's) rely on small filter inductances and high switching frequencies to achieve sufficiently fast load transient response.

We note that other researchers in academia [9], [10] and industry [8] have developed active clamp circuits similar to that described in the present work. However, only the part in [8] is

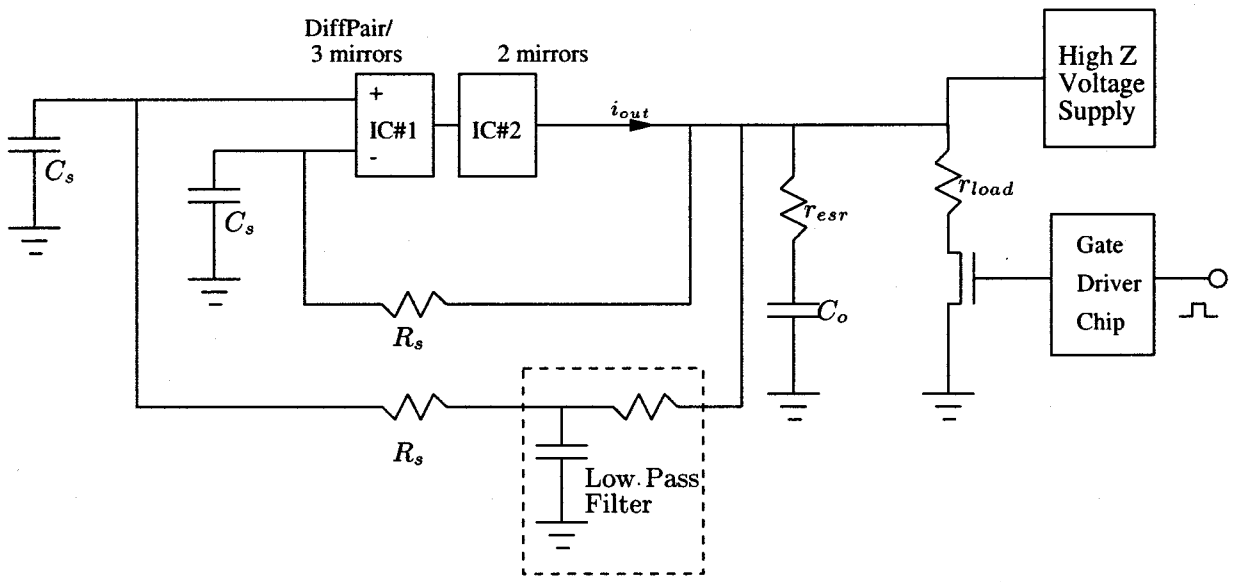


Fig. 20. Functional schematic of test board.

TABLE I
TEST BOARD PARAMETERS

C_o	10x4.7uF =47uF
R_{esr}	$5m\Omega/10 = .5m\Omega$
C_s	$\simeq 1nF$
R_s	100Ω
C_{LPF}	$4.7uF$
R_{LPF}	$6.8k\Omega$
$V_{out}(nominal)$	1.5V
$V_{DD}(analog)$	3.3V
$V_{DD}(power1)$	3.3V
$V_{DD}(power2)$	4.25V

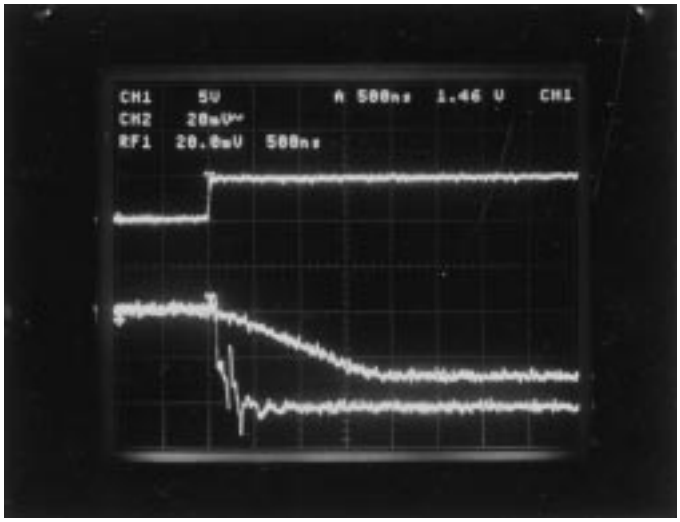


Fig. 21. Photo of output voltage under load transient (pull-up function). Top: Function generator signal, middle: Output voltage with $I_{load} = 0.3$ A, bottom: output voltage with $I_{load} = 6.3$ A.

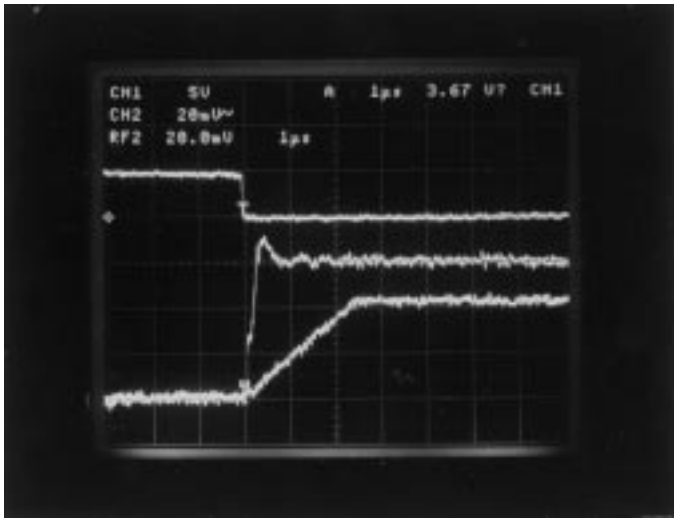


Fig. 22. Photo of output voltage under load transient (pull-down function). Top: Function generator signal, Middle: Output voltage with $I_{load} = 0.3$ A, Bottom: Output voltage with $I_{load} = 6.3$ A.

an integrated circuit implemenation, as in the present work. The part as described in [8] evidently has poorer speed of response since it is recommended that the part be used with 500 μF of output capacitance for similar load transient magnitudes.

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