An Activity-Triggered 95.3 dB DR −75.6 dB THD CMOS Imaging Sensor With Digital Calibration

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***Abstract*—Imaging sensors are being used as data acquisition systems in new biomedical applications. These applications require wide dynamic range (WDR), high linearity and high signal-to-noise ratio (SNR), which cannot be met simultaneously by existing CMOS imaging sensors. This paper introduces a new activity-triggered WDR CMOS imaging sensor with very low distortion. The new WDR pixel includes self-resetting circuits to partially quantize the photocurrent in the pixel. The pixel residual analog voltage is further quantized by a low-resolution column-wise ADC. The ADC code and the partially quantized pixel codes are processed by column-wise digital circuits to form WDR images. Calibration circuits are included in the pixel to improve the pixel linearity by a digital calibration method, which requires low calibration overhead. Current-mode difference circuits are included in the pixel to detect activities within the scene so that the imaging sensor captures high quality images only for scenes with intense activity. A proof-of-concept 32×32 imaging sensor is fabricated in a 0.35 μm CMOS process. The fill factor of the new pixel is 27%. Silicon measurements show that the new imaging sensor can achieve 95.3 dB dynamic range with low distortion of -75.6 dB after calibration. The maximum SNR of the sensor is 74.5 dB. The imaging sensor runs at frame rate up to 15 Hz.**

***Index Terms*—Activity-triggered detection, CMOS imaging sensor, difference image, digital calibration, high linearity, wide dynamic range.**

I. Introduction

THE continuous improvement of CMOS imaging sensors in recent years has opened up new application areas in scientific research ([1], [2]) and biomedical diagnostics ([3]–[7]), such as space telescope, DNA microarray, bioluminescence detection, and computed tomography. An imaging sensor serves as a data acquisition system in these applications, which require wide dynamic range (WDR) and high linearity over the full range. Charge-coupled devices (CCD) have been mainly used for these applications. However, powerful on-chip processing capabilities make CMOS imaging sensors more attractive than CCD sensors besides its cost advantage [8]. CMOS imaging sensors have already been developed for several biomedical applications ([6]–[10]). However, a lot of these new applications ([1]–[5], [9], [10]) require WDR CMOS imaging sensors with dynamic range (DR) around five decades (> 96 dB) and linearity better than 12 bits (< -72 dB). WDR imaging sensors usually generate high output data rate which demands high processing power. Hence, activity-triggered image acquisition is desirable.

WDR CMOS imaging sensors have been designed with nonlinear techniques and linear techniques [11]. Logarithmic pixels have wider DR than linear pixels [12]. However, the noise level of a logarithmic pixel is high. The DR of a linear pixel is normally limited by its potential well size. The well size can be adjusted nonlinearly to accommodate the wide DR [13]. The DR can be also extended by scaling the integration time according to the photo current level [14]. Equivalently, a WDR image can be synthesized from images captured from multiple exposures ([15], [16]). More recently, a lateral overflow integration capacitor scheme was developed to greatly expand the DR [17]. These WDR imaging sensors expand the DR nonlinearly by spilling extra photo charges, or changing the pixel conversion gain, so that the pixel linearity is not preserved over the wide DR. In-pixel Σ-Δ A/D conversion can linearly expand the imaging sensor DR [18]. However, the oversampled output data rate can be high.

This paper introduces the design of a new WDR CMOS imaging sensor with high linearity and lower output data rate. The new pixel design enables both the activity detection and the WDR image acquisition. A partial quantization scheme is implemented in the new pixel, which linearly expands the imaging sensor DR to be 95.3 dB. The linearity of the partial quantization scheme over the wide DR is improved using a digital calibration method with a back-end digital signal processor (DSP). The pixel distortion after calibration reaches -75.6 dB. The partial quantization pixel also achieves high signal-to-noise ratio (SNR). The fill factor of the new pixel is 27%. Part of the concepts in this paper has been presented in [19].

The paper is organized in six sections. The existing WDR CMOS imaging sensor techniques are summarized in Section II. Circuits of the new imaging sensor are detailed in Section III. The digital calibration method is introduced in Section IV. Measurement results are given in Section V. Section VI draws conclusions.

II. WDR Pixel Design

The accumulated photo voltage ($V_{\rm ph}$) of a conventional 3 T active pixel is

$$V_{\rm ph} = \frac{T_{\rm int}}{C_{\rm int}} I_{\rm ph} \tag{1}$$

where $T_{\rm int}$ is the integration duration. $C_{\rm int}$ is the integration capacitor, which is the diode capacitance for the 3 T active pixel.

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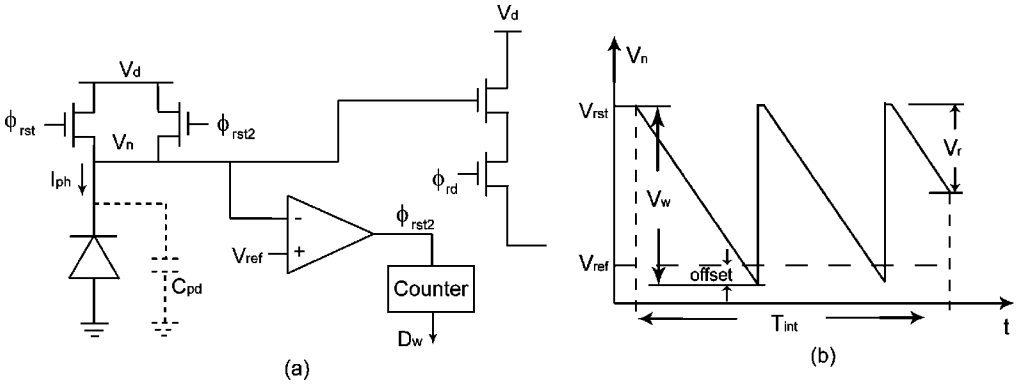

Fig. 1. The linearly expanded WDR pixel. (a) The pixel block diagram. (b) The pixel dynamics.

$I_{\rm ph}$ is the photo current. $V_{\rm ph}$ is limited by the maximum allowed voltage at the integration node, which is generally known as the well capacity ($V_{\rm w}$). Conventional CMOS imaging sensors keep $T_{\rm int}$ and $C_{\rm int}$ constant for the pixel array. The DR of one pixel is limited by the well capacity as

$$DR = \frac{(V_{\rm w}C_{\rm int})/T_{\rm int}}{I_{\rm min}} \tag{2}$$

where $I_{\rm min}$ is the minimum photo current that the sensor can detect. This is determined by the least significant bit (LSB) size of the quantizer or the pixel read-out noise level, whichever is larger [20]. The maximum SNR of this pixel is [11]

$$\mathrm{SNR} = \frac{V_{\rm w}^2}{\dfrac{qV_{\rm w}}{C_{\rm int}} + \sigma_{\rm rd}^2} \tag{3}$$

where $\sigma_{\rm rd}^2$ is the input-referred read-out voltage noise power.

In order to expand the imaging sensor's DR beyond the limitation of (2), two types of WDR methods have been developed based on (1). The accumulation time $T_{\rm int}$ can be scaled nonlinearly for different photo currents [14]. Small photo current can be detected with long integration, while large photo current can be accommodated within $V_{\rm w}$ with short integration. As the integration duration is nonlinear, the linearity of this type of WDR imaging sensor is low. The maximum SNR is still limited by $V_{\rm w}$ as stated in (3). Another method is to scale the accumulation capacitor $C_{\rm int}$ for different photo currents [10], [17]. A small photo current can be sensed by a small $C_{\rm int}$, while a large photo current can be accommodated within $V_{\rm w}$ by a large $C_{\rm int}$. As the capacitance cannot be scaled as easily as the integration time, existing designs use only one extra capacitor for scaling. With a proper capacitor, the DR can improve by 32 times. The maximum SNR improves as the accumulated charge can increase beyond the potential well limitation. However, the pixel linearity over the wide DR is still low because the conversion gain changes for different photo currents.

In order to design a highly linear WDR imaging sensor with high SNR, the DR should be expanded linearly. Ideally, the DR can be linearly expanded by adding a comparator and a counter in the pixel as shown in Fig. 1(a). The photo diode gets reset whenever $V_{\rm n}$ falls below the threshold voltage, as shown in Fig. 1(b). The number of pixel overflow events ($D_{\rm w}$) is recorded by a counter. The equivalent well size in this pixel is $V_{\rm rst}$-$V_{\rm ref}$.

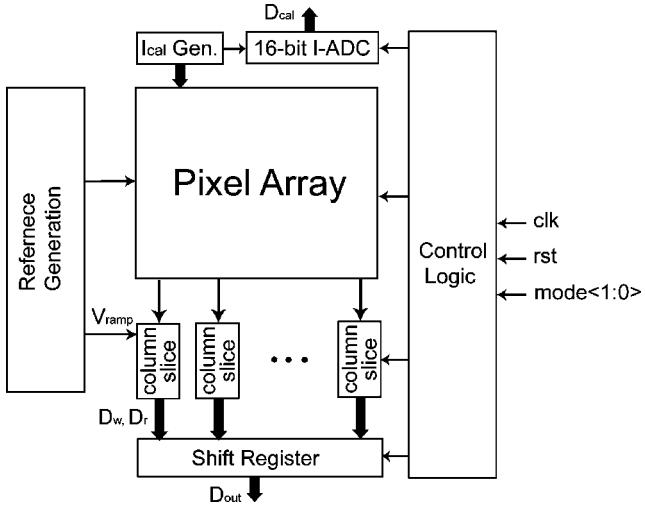

Fig. 2. The block diagram of the designed imaging sensor.

At the end of the accumulation, the accumulated photo voltage can be simply calculated as

$$V_{\rm ph} = D_{\rm w} \cdot V_{\rm w} + D_{\rm r} \cdot \mathrm{LSB}_0 \tag{4}$$

where LSB_0 is the LSB of the quantizer, while $D_{\rm r}$ is the quantized residual voltage ($V_{\rm r}$).

Several problems need to be addressed at the circuit level to make this partial quantization scheme a practical WDR technique. The counter is usually large which reduces the pixel fill factor greatly. An in-pixel counter also injects switching noise to the analog front-end. The in-pixel comparator has nonlinear offsets. Circuits are designed to deal with these issues in this work.

III. Circuit Description

The imaging sensor is designed in a 0.35 μm two-poly four-metal (2P4M) CMOS process. The functional block diagram of the designed imaging sensor is shown in Fig. 2. The imaging sensor uses column-wise processing.

A. Pixel Circuit

The new pixel circuit with the column-wise pathway is shown in Fig. 3. It includes a basic 4 T APS pixel, an in-pixel comparator, a one-bit memory, a current sampler, and calibration

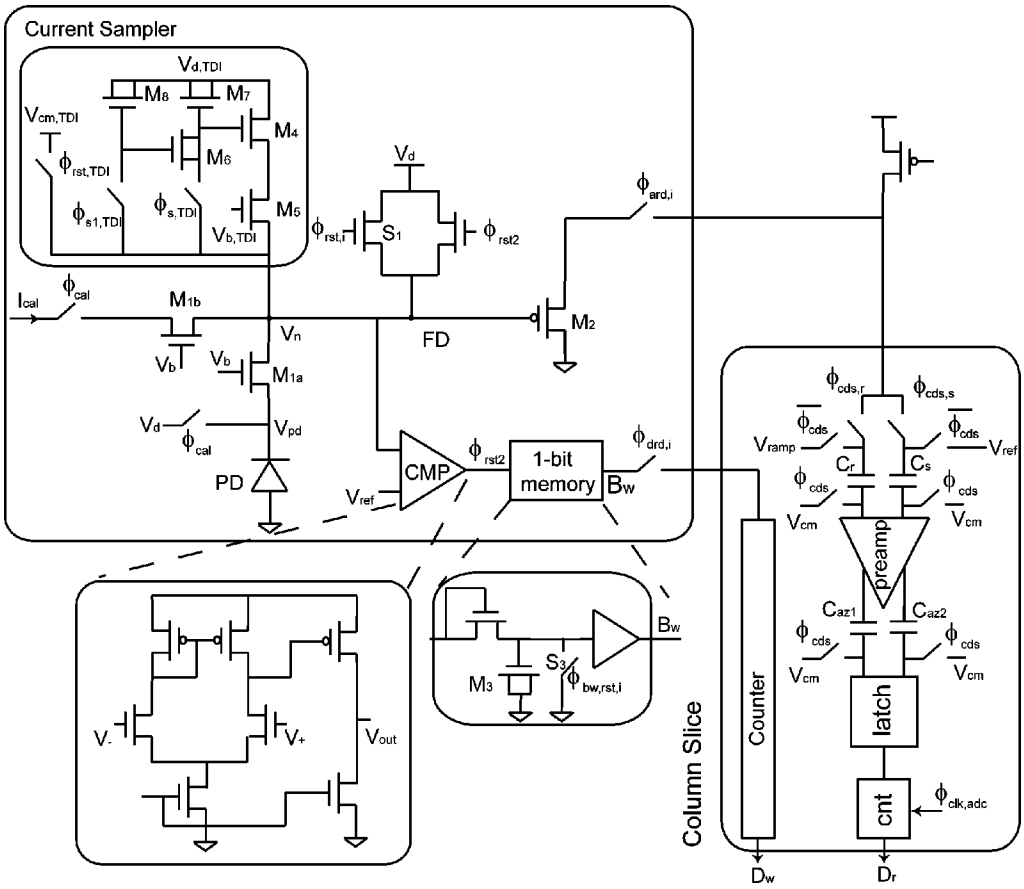

Fig. 3. The pixel circuit and the column-wise pathway of the new imaging sensor.

circuits. The pixel operates in three modes: the difference mode, the WDR mode, and the calibration mode.

1) Difference Mode: The sensor normally runs in the difference mode to reduce the output data rate, which saves data transmission power and the digital power of following processing circuits. In the difference mode, the current sampler is active. $V_{\rm ref}$ of the comparator is set to a low value, which keeps the comparator output low. The difference mode runs through two frames.

At the beginning of the sampling frame, both sampling switches stay on. $\Phi_{\rm s,TDI}$ turns off early, which injects charge only onto the MOS capacitor M6. At the end of the frame, $\Phi_{\rm s1,TDI}$ turns off, and injects most charge onto M8 which is about 5 times larger than M6 [21]. The designed sampler can sample the photo current with offset less than 0.1%, which is enough for activity detection in most applications.

In an accumulation frame, the difference current between the new photo current and the sampled current accumulates on the floating drain (FD) after the difference shutter ($\Phi_{\rm rst,TDI}$) turns off. The reset level $V_{\rm cm,TDI}$ is in the middle of the voltage range so that both positive and negative difference currents can be accumulated. At the end of the frame, the accumulated voltage is quantized by the column-wise ADC.

An off-chip DSP checks the difference image, which indicates the activity in the scene. If the activity is beyond a certain level, the imaging sensor switches to the WDR mode to capture a high-quality image. The current sampler is switched off during the WDR mode. The supply voltage of the sampler ($V_{\rm d,TDI}$) is 0.4 V lower than $V_{\rm d}$ to suppress the leakage current from the sampler [22].

2) WDR Mode: To avoid image lag in the 4 T APS pixel, the transfer gate M1a never resets during the accumulation. Instead, $V_{\rm b}$ stays fixed so that the potential well of the diode is always full in the steady state, as shown in Fig. 4. The photo charge spills over to the FD during the accumulation.

The WDR mode starts as a rolling shutter ($\Phi_{{\rm rst},i}$) resets the pixel. When the accumulated voltage on the FD ($V_{\rm n}$) reaches the threshold voltage $V_{\rm ref}$ of the comparator, the output of the comparator ($\Phi_{\rm rst2}$) resets the FD, as shown in Fig. 4(b). Then, the photo current accumulates on the FD again. The FD voltage $V_{\rm n}$ changes as shown in Fig. 1(b). An overflow event is recorded by a MOS capacitor M3. M3 is regularly read and reset by the column slice to count the overflow number. At the end of the accumulation, the residual voltage of the pixel is read out and quantized by the column-wise ADC.

Correlated double sampling (CDS) is performed on the residual voltage. The ADC first samples ($\Phi_{\rm cds,s}$) the residual voltage on $C_{\rm s}$. The pixel is reset before the analog read-out control ($\Phi_{{\rm ard},i}$) switches to the next row. The pixel reset voltage is sampled on $C_{\rm r}$. This CDS is performed over two frames. It can effectively remove $1/{\rm f}$ reset noise [23]. The quantization takes place after the CDS phase ($\Phi_{\rm cds}$) turns off .

With a constant well size $V_{\rm w}$, the accumulated photo voltage of this partial quantization scheme can be calculated by (4).

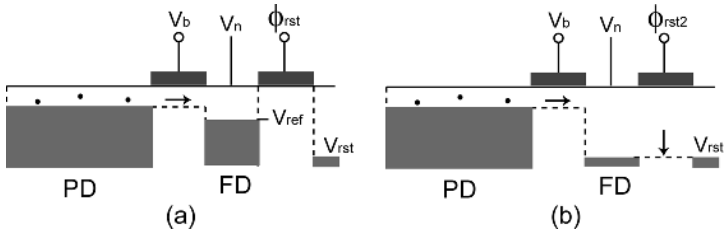

Fig. 4. The potential diagram of the pixel during the WDR mode.

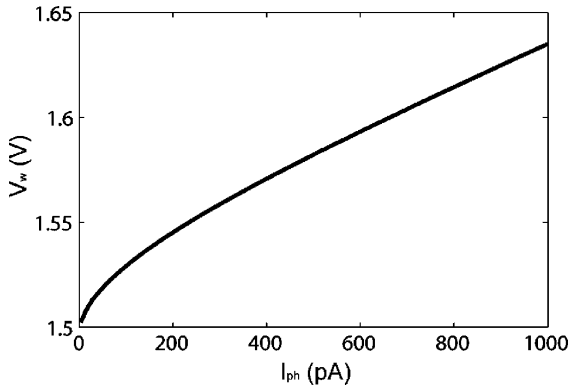

Fig. 5. Simulated $V_{\rm w}$ at different photo currents of the partial quantization pixel.

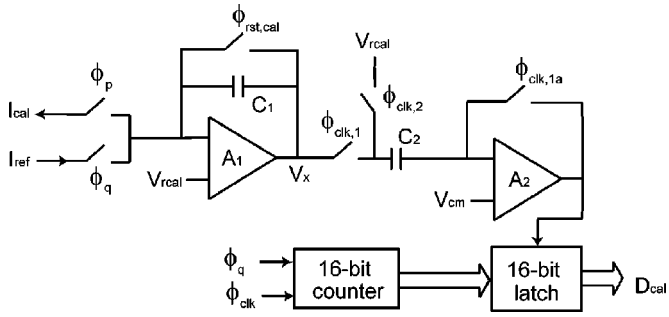

Fig. 6. The 16-bit dual-slope current ADC.

Nonetheless, $V_{\rm w}$ is nonlinear because the asynchronous reset by the weak-current comparator (1 nA) depends heavily on the photo current. Fig. 5 shows the simulated $V_{\rm w}$ with different photo currents using HSPICE. A digital calibration scheme is developed to compensate for this nonlinearity. At first, this nonlinear $V_{\rm w}$ function is sampled in the calibration mode. In the WDR mode, the accurate well size $V_{\rm w}$ is interpolated from the sampled nonlinear function, and is applied in (4) to calculate the accurate photo voltage.

3) Calibration Mode: In the calibration mode, the PD is switched off. Instead, the pixel accumulates an on-chip calibration current ($I_{\rm cal}$). Identical cascade transistors M1a and M1b keep the same FD capacitance in the calibration mode and the WDR mode. The exact $I_{\rm cal}$ value can be measured from an on-chip 16-bit current ADC, as shown in Fig. 6. With (4), the well capacity $V_{\rm w}$ for current $I_{\rm cal}$ can be calculated, which forms one sample on the nonlinear function in Fig. 5. Twelve on-chip current sources are designed for each column.

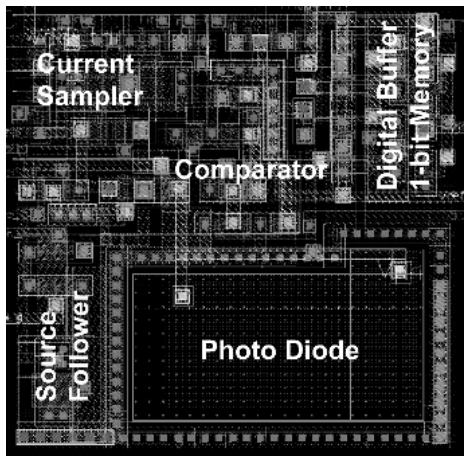

Fig. 7. The pixel layout 25 μm× 25 μm.

The current ADC is a dual-slope ADC. In the pre-charge phase $\Phi_{\rm p}$, $I_{\rm cal}$ charges C_1. In the quantization phase $\Phi_{\rm q}$, the reference current $I_{\rm ref}$ discharges C_1. V_x is compared with $V_{\rm rcal}$ continuously in $\Phi_{\rm clk,2}$ phases. CDS is performed in $\Phi_{\rm clk,1}$ phases. The zero crossing moment will be latched by the output of A_2, which is proportional to $I_{\rm cal}$. The system clock is 20 MHz. Each $I_{\rm cal}$ quantization takes about 3.2 ms. Measurements of the calibration currents in one column last about 38.4 ms.

The layout of the pixel is shown in Fig. 7. The pixel area is 25 μm× 25 μm. The photodiode size is 17 μm× 10 μm, which gives a fill factor of 27%. The current sampler accounts for about 19% of the pixel. Without the current sampler, the fill factor is 33%.)

4) Temporal Noise Analysis: With a small photo current which does not trigger an overflow, the pixel temporal noise mainly comes from the photo current shot noise and the read-out circuit noise. The noise power is

$$\overline{v_{\rm n}^2} = \frac{qV_{\rm ph}}{C_{\rm int}} + \overline{\sigma_{\rm rd}^2}. \tag{5}$$

At the low current end, the circuit noise dominates. Therefore, the SNR increases 6 dB per photo current doubling. At the large current end, the photo current shot noise dominates. The SNR increases 3 dB per photo current doubling.

When the photo current is large enough to trigger overflows, the pixel temporal noise mainly comes from the reset noise and the photo current shot noise. The overall noise power is

$$\overline{v_{\rm n}^2} = \frac{qV_{\rm ph}}{C_{\rm int}} + D_{\rm w}\frac{kT}{C_{\rm int}} \tag{6}$$

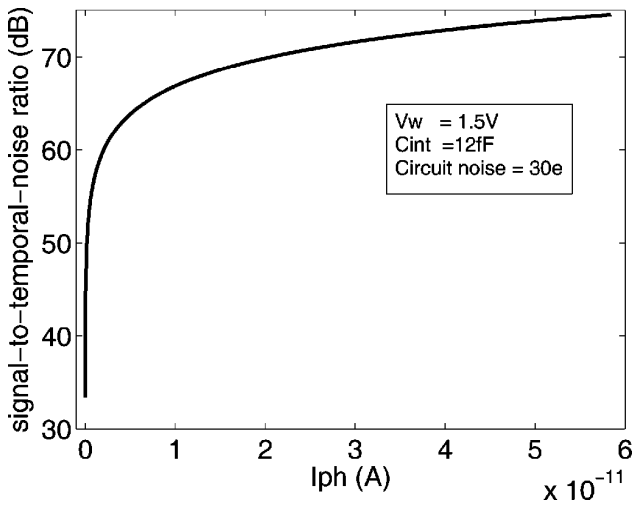

Fig. 8. The pixel SNR for photo currents which trigger overflows: $V_{\rm w} = 1.5$ V, $C_{\rm int} = 12$ fF, $\sigma_{\rm rd} = 30$ e$^-$.

where $D_{\rm w}$ is the overflow number. The reset noise is much smaller than the shot noise. Therefore, the SNR improves by 3 dB per photo current doubling. The pixel SNR can be simulated and plotted in Fig. 8. In the simulation, the well capacity $V_{\rm w}$ is 1.5 V. The DR is extended by 256 times. The integration capacitance is 12 fF. The read out circuit noise is 30 e$^-$. As the partial quantization scheme extends the DR greatly, the pixel SNR can be better than the previous designs [20], [23].

B. Column-Wise Counter

To expand the pixel DR by 256 times, an 8-bit counter is needed by the pixel. A normal 8-bit counter needs 8 D-flip-flops (DFFs), which requires about 300 transistors. If this counter is included in the pixel, the fill factor will be low. The digital spikes will contaminate the analog sensor as well. A new counter is designed at the column level, as shown in Fig. 9.

The column-wise counter includes an SRAM bank for different pixels in the column. The logics add the overflow bit $B_{\rm w}$ from the pixel to the content of the SRAM periodically. The counter runs on the counter clock $\Phi_{\rm clk,cnt}$. The clock rate is $256 \times N_{\rm r} \times f_{\rm frame}$, where $N_{\rm r}$ is the row number. At the beginning of each frame of every row, SRAM of this row is reset by $\Phi_{\rm eqw}$. The digital read-out control signal $\Phi_{{\rm drd},i}$ selects both the SRAM and the 1-bit memory of the ith row to perform the addition. After the addition, the falling edge of $\Phi_{\rm clk,cnt}$ latches the new overflow number. Then, the column digital write signal $\Phi_{\rm dwr}$ controls the new overflow number to be written into the same SRAM. After that, the next row is turned on for refreshing. Within a frame, the SRAM of one pixel will be refreshed by 256 times. The adder and the register should operate at this frequency.

After the addition, the clock $\Phi_{{\rm bw,rst},i}$ resets the 1-bit memory in the pixel of i-th row. To prevent a write and reset conflict, a weak reset is designed by applying a low gate voltage on the NMOS switch S3. If the comparator generates a high pulse during the reset phase $\Phi_{{\rm bw,rst},i}$, the NMOS diode is still able to pull up the voltage on M3.

Because the adder is shared by different pixels in the column, the transistor count per pixel can be greatly reduced. On average, 48 transistors are needed for each pixel, which could be further reduced by using dynamic RAM (DRAM). DRAM can be easily implemented in this architecture because the refreshing circuits are already in place.

C. Column-Wise ADC

As shown in Fig. 3, a single-slope ADC is designed to quantize the pixel residual voltages in one column. The ADC design is similar to the one introduced in [24]. A high quality ramp signal is generated by a similar ramp signal generator in [25] with on-chip calibration. The column-wise ADC is designed for 9 bit resolution. The frequency of the column-wise ADC clock ($\Phi_{\rm clk,adc}$) is $512 \times N_{\rm r} \times f_{\rm frame}$.

IV. Digital Calibration

In the calibration mode, the pixel is configured to sample the nonlinear well capacity $V_{\rm w}$ with M samples $\{(I_{\rm cal}, V_{\rm w})_i\}_{i=1,\ldots,M}$. In the WDR mode, the imaging sensor generates raw image data ($D_{\rm w}$, $D_{\rm r}$). A DSP estimates the accurate well capacity $V_{\rm w}$ through linear interpolation from the M samples in real time, and recovers the accurate image from the raw image data.

A. Recovery Procedure

For a photo current $I_{\rm ph}$, the pixel quantizes it into $D_{\rm w}$ and $D_{\rm r}$ so that

$$I_{\rm ph} = K(D_{\rm w}V_{\rm w} + D_{\rm r}\,{\rm LSB}_0) \tag{7}$$

where $K = C_{\rm int}/T_{\rm int}$.

With an approximate $V_{\rm w0}$ applied, a crude $I_{\rm ph0}$ can be calculated. Based on $I_{\rm ph0}$, the interpolation segment region x can be identified as shown in Fig. 10. With interpolation, the accurate $V_{\rm w}$ can be calculated.

$$V_{\rm w} = (I_{\rm ph} - I_{{\rm cal},x})S_x + V_{{\rm w},x} \tag{8}$$

where S_x is the slope in this region. With (7) and (8), the accurate photo current can be found.

$$I_{\rm ph} = \frac{K(D_{\rm w}V_{{\rm w},x} + D_{\rm r}LSB_0 - D_{\rm w}I_{{\rm cal},x}S_x)}{1 - KD_{\rm w}S_x}. \tag{9}$$

The interpolation region x should be verified with this photo current value. If it is in the wrong region, the new region would be used for another iteration. Theoretically, it might take several iterations before the final $I_{\rm ph}$ is found. However, experiments show that no iteration is needed because the pixel nonlinearity generally is small, and the nonlinear function is well formed.

During the experiment, a digital version of this algorithm is coded in a DSP. The mathematical derivation of this digital algorithm can be found in ([19], [26]).

B. Decoder

The calibration and recovery procedures are implemented by two decoders in the off-chip DSP. Fig. 11 shows structures of the

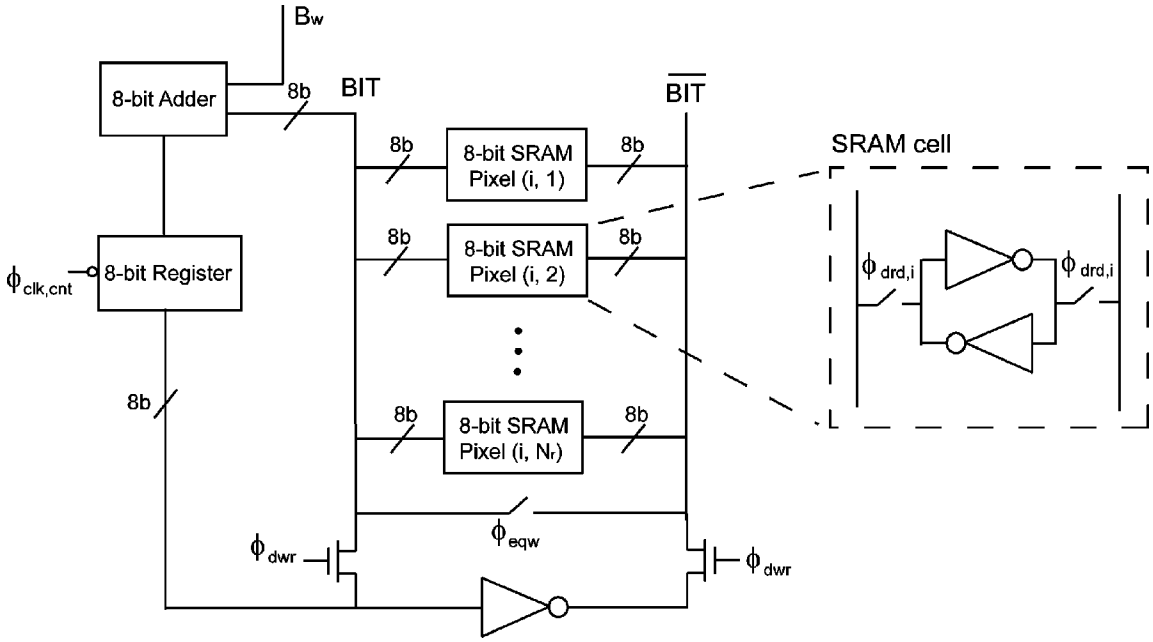

Fig. 9. The column-wise counter.

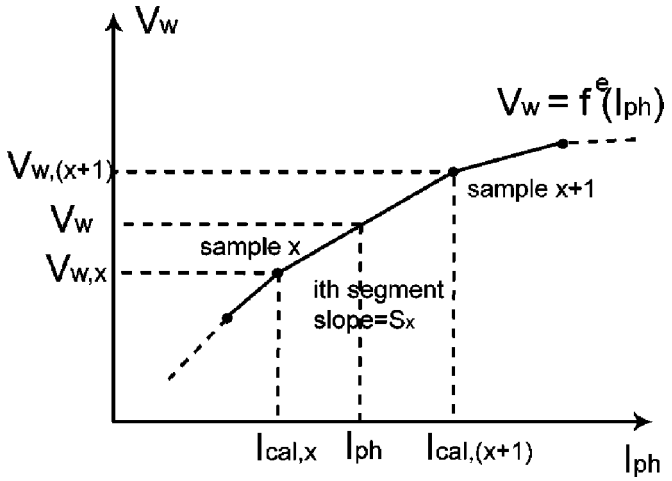

Fig. 10. Estimate the accurate well capacity $V_{\rm w}$ through linear interpolation.

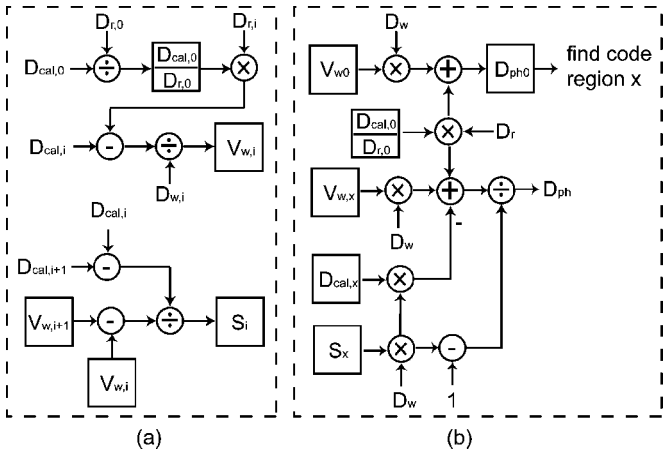

Fig. 11. Decoder structures in the DSP back-end. (a) Parameter decoder in the calibration mode. (b) $I_{\rm ph}$ decoder for real-time recovery during the WDR mode.

decoders. The rectangular boxes are memory elements. Signals outside boxes are inputs or outputs to the DSP.

The decoder in Fig. 11(a) calculates the interpolation parameters in the calibration mode. $D_{\rm cal}$ is the digitized value of $I_{\rm cal}$. The speed of this decoder is not critical. The decoder in Fig. 11(b) recovers the photo current during the WDR mode. It supports the real-time calculation. As the current ADC quantizes currents into 16 bits, $4M-2$ bytes memory is required for each pixel on average. For a 1 K-pixel image sensor, $4M-2$ KB memory is needed in the DSP. If all pixels are processed in serial, the decoder needs to run at the rate $f_{\rm frame}\times N_{\rm r}\times N_{\rm c}$ Hz, where $N_{\rm c}$ is the column number. Although 16-bit multipliers are needed in the decoder, only one such decoder is needed in the DSP. If the image size is not large, multiplications can be done in serial as well. Hence, the hardware overhead for digital calibration is low.

V. Experimental Results

A proof-of-concept 32×32 imaging sensor is fabricated in a 0.35 μm 2P4M CMOS process. The micrograph of the die is in Fig. 12. The die area is 2.7 mm^2 $\times$ 3.5 mm^2. The main measurement setup is shown in Fig. 13. The imaging chip is illuminated by an integrating sphere US-120-SF (Labsphere, Inc.), with the light source Fiber-Lite PL900 (Dolan Jenner Industries). The optical power meter is S-120 (Thorlabs). The output data from the imaging chip is captured by a logic analyzer 16902B and is further processed by a computer.

A. Optical and Electrical Parameters

The column-wise ADC is measured. A sinusoidal signal is applied to one column-wise ADC. A spectrum analyzer (SR760, Stanford Research Systems) shows that the input spurious-free

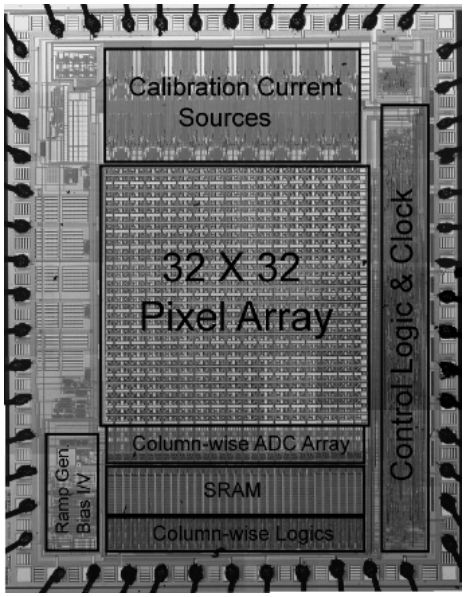

Fig. 12. The micrograph of the imaging sensor 2.7 $\text{mm}^2 \times 3.5\ \text{mm}^2$.

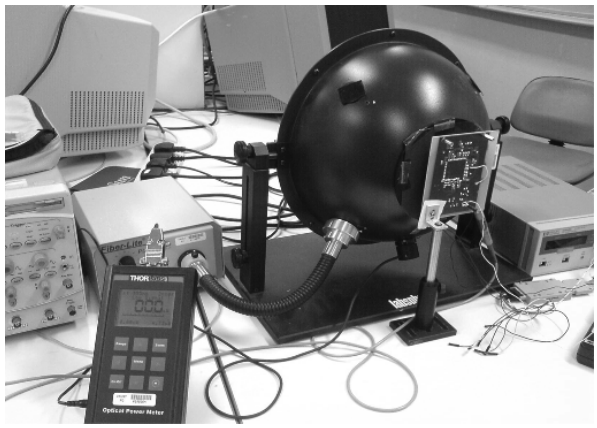

Fig. 13. The measurement setup.

dynamic range (SFDR) is about 83 dB. 512-pt FFT testing routine is performed on the ADC at 15 Hz frame rate. The spectrum is shown in Fig. 14. The overall signal-to-noise-distortion ratio (SINAD) is 50.9 dB. The SFDR is 53.7 dB. The effective number of bit (ENOB) is 8.2 bits. The ADC LSB size is 5.9 mV.

The pixel capacitance is measured to be 12 fF by the on-chip current ADC. The sensitivity of the imaging sensor is 13.3 $\mu\text{V}/\text{e}^-$. With the optical meter, the responsivity of the imaging sensor is measured to be 0.38 A/W at the wavelength of 555 nm. The dark current of a pixel is 0.96 fA at room temperature, which corresponds to a dark current density of 0.56 nA/cm^2.

B. Difference Mode

The imaging sensor starts in the difference mode, and switches to the WDR mode when the difference image pixel value reaches a threshold. Various digital thresholds are set within the potential well. The imaging chip is able to switch to the WDR mode correctly if the scene changes significantly.

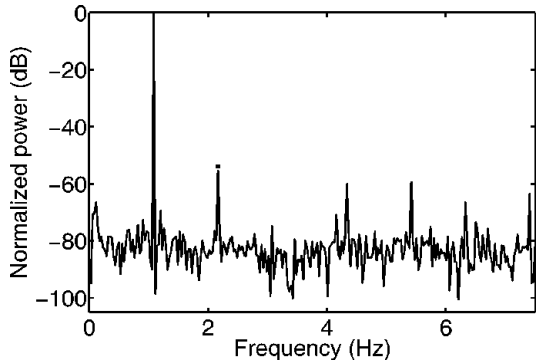

Fig. 14. The spectrum of the fabricated column-wise ADC: $f_{\text{frame}} = 15\ \text{Hz}$.

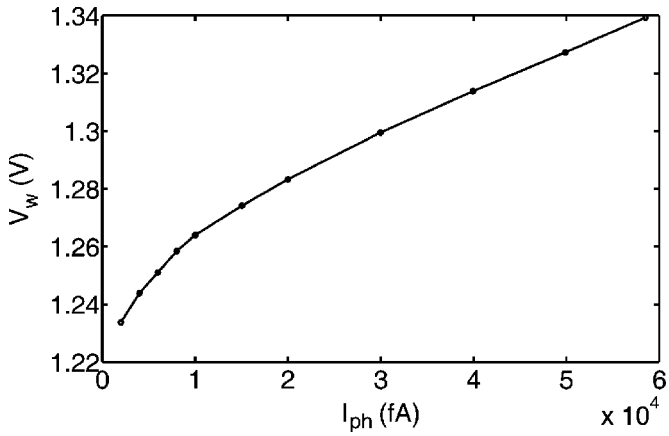

Fig. 15. The sampled well size of one pixel.

C. Linearity

With the current ADC, the calibration procedure is performed on pixels of the imaging sensor. V_{w} of one pixel is sampled by 11 I_{cal} currents, and is shown in Fig. 15. The digitized photo current I_{ph} and V_{w} have been converted to their analog values with the ADC LSB sizes. The nonlinearity is strong, particularly at the low current end.

The pixel linearity is measured by 17 currents. Without calibration, a uniform V_{w} is used to estimate the accumulated photo voltage V_{ph}. The estimated photo voltages are shown in Fig. 16, with a spectrum simulated from this line. The harmonic distortion is -36.4 dB. The sampled nonlinear function is used to recover the accurate photo voltages. The recovered photo voltages after calibration are shown in Fig. 17, with a spectrum simulated from this line. The harmonic distortion is improved to -75.6 dB.

The linearity in Fig. 17 is tested in the electrical domain, which includes only the circuits. Linearity test in the optical domain cannot be performed with the existing equipment because it requires an optical source with better than 14-bit linearity. Nonetheless, the difference between the two measurements is only the photodiode. For highly linear imaging applications, the photodiode requires high linearity [10].

For this work, we tried to visualize the effect of the digital calibration on captured images. A gradient pattern as shown in Fig. 18(a) is printed by an HP laser printer and is captured by the imaging sensor. Without calibration, the recorded image is shown in Fig. 18(b). The image after calibration is shown

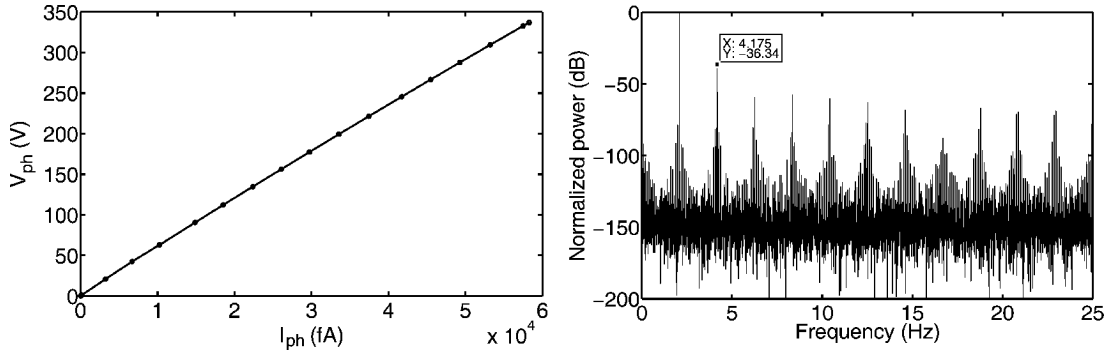

Fig. 16. The pixel linearity before calibration.

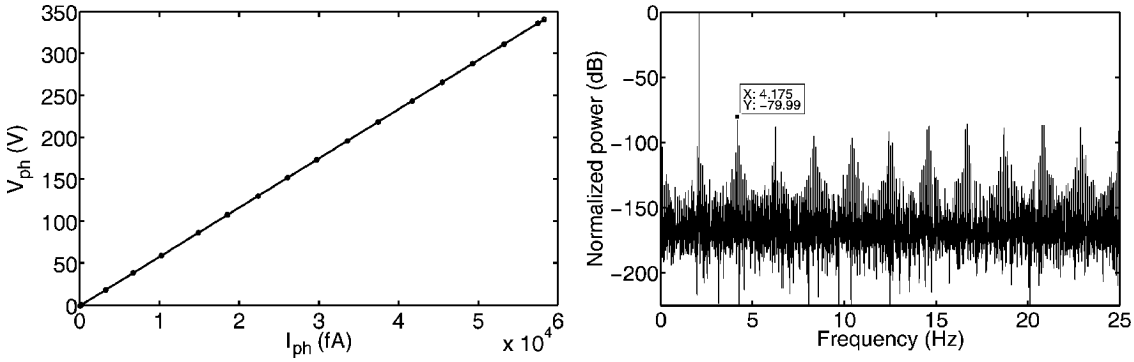

Fig. 17. The pixel linearity after calibration.

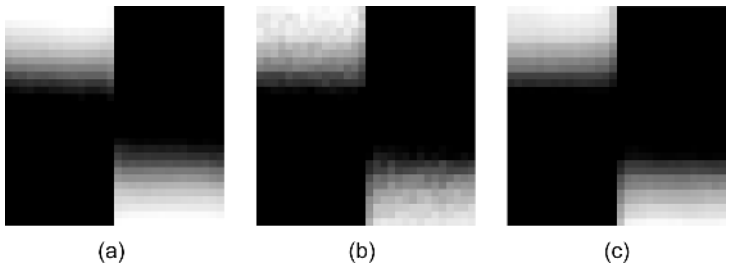

Fig. 18. Pixel linearity measurement. (a) The display pattern. (b) The recorded image before calibration. (c) The recorded image after calibration.

in Fig. 18(c). The captured raw image has strong fixed pattern noise (FPN). The FPN is much lower after calibration. The gray-scale uniformity is also improved after calibration.

D. FPN, Temporal Noise and DR

The imaging sensor is uniformly illuminated by the integrating sphere. Before calibration, the measured FPN of images is 5.1%. The FPN is mainly due to the mismatch of pixel-level circuits. After calibration, the overall measured FPN is 1.0%. FPN of the processing and read-out circuits is measured by applying a current into all the pixels, and comparing the recovered $V_{\rm ph}$ after calibration. The uniformity among pixel circuits after calibration is better than 12-bit. Therefore, the measured FPN is dominated by the photo diode variation and the optical equipment.

The temporal noise of the imaging sensor is dominated by the ADC quantization noise at low illumination level. Therefore, the pixel analog output is measured for noise instead. At a low illumination level which does not trigger overflow, the measured temporal noise of one pixel is 3.1 $\rm mV_{rms}$. The accumulated photo voltage is 1.287 V. The SNR is 47.4 dB. At a high illumination level, the measured pixel temporal noise is 37.4 mV. The accumulated photo voltage is 330.6 V. The SNR is 73.9 dB. The photo current ratio of the two illumination levels is about 256, while the SNR improvement is 26.5 dB. The SNR improves 3.3 dB per signal doubling, which agrees with the temporal noise analysis well.

At 15 Hz frame rate, the maximum photo current that the partial quantization scheme can process is 58.4 pA. The minimum detectable photo current is limited by the ADC LSB. The dynamic range of the imaging sensor is about 95.3 dB. Fig. 19 shows photos taken at different dynamic ranges. The scene includes the S-120 light meter and the PL900 light source, which is quite bright. Fig. 19(a) and (b) are images taken with partial quantization disabled. The integration time controls the image exposure. The high DR scene cannot be completely captured by the sensor. With partial quantization enabled, the whole scene can be captured as shown in Fig. 19(c). Limited by the small

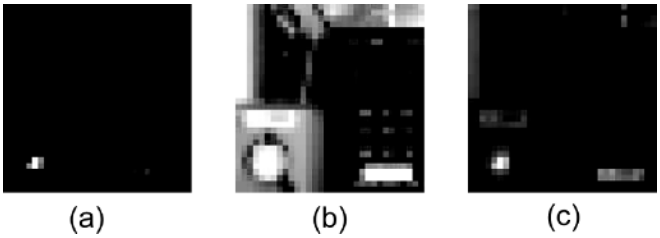

Fig. 19. Images taken with different dynamic ranges. (a) Small DR: under-exposed. (b) Small DR: over-exposed. (c) Wide DR.

TABLE I
PERFORMANCE SUMMARY OF THE DESIGNED IMAGING SENSOR

	Performance	
Process	0.35um 2P4M N-Well CMOS	
Supply Voltage	3.3V	
Pixel Size	25μm×25μm	
Fill Factor	27%, 33%(without sampler)	
Frame Rate	up to 15Hz	
Dark Current	0.56 nA/cm^2	
Sensitivity	13.3V/e$^-$	
Responsivity	0.38A/W	
Dynamic Range	95.3dB	
Maximal SNR	74.5dB	
	Before cal.	After cal.
Linearity	-36.4dB	-75.6dB
FPN	5.1%	1.0%
Power Consumption	316μW @ 15Hz	

size of the imaging sensor, the scene cannot be smoothly seen. However, the light source and the light meter can still be readily recognized.

E. Discussion

The measured performance of the designed imaging sensor is listed in Table I. The measured power only includes the analog and digital power of the imaging sensor. The imaging sensor requires a digital back-end for calibration, which will burn more digital power. This extra digital power is not important for imaging systems with static power supply. The new WDR linear imaging sensor can also be used in power-limited implantable biomedical sensors, such as capsule endoscopy [27], [28]. In these applications, only the imaging sensor is implanted. The raw image data is transmitted to an external receiver through a wireless link. The digital calibration back-end is included in the receiver. The external receiver is usually not sensitive to the extra digital power, while the implanted capsule's data transmission power is considerably reduced due to lower data rate from the imaging sensor with the activity detection feature.

The designed WDR CMOS imaging sensor is compared with previous designs. As most CMOS imaging sensor designs do not list the characteristics completely, only two previous designs are listed in Table II. The bioluminescence detection CMOS imaging sensor [7] achieved about 60 dB dynamic range and linearity. A large pixel is used in [7] to improve the sensitivity of the imaging sensor by collecting more photons. To achieve the same sensitivity, a similar large photodiode can be used in our pixel. The WDR CMOS imaging sensor in [14] achieved 96 dB dynamic range. However, its linearity was not measured. As no design efforts have been made to improve the linearity, the nonlinear integration durations alone will lead to low linearity. On the other hand, the new imaging sensor design can achieve both WDR and high linearity using the digital calibration technique.

TABLE II
CMOS IMAGING SENSOR PERFORMANCE COMPARISON

	[7]	[14]	This work
Process	0.18um	0.35um	0.35um
Pixel Size (μm^2)	240×210	10.5×10.5	25×25
Frame Rate (Hz)	0.03	28	15
Dynamic Range (dB)	61	96.3	95.3
Maximal SNR (dB)	58	50	74.5
Linearity (dB)	>0.1%	Not measured	-75.6

The pixel of the designed imaging sensor is larger than that of some WDR CMOS imaging sensors, which is due to the new features. However, the pixel size can be reduced with a smaller feature size CMOS process. The current sampler, which accounts for 19% pixel size, can also be removed if the activity detection feature is not needed. With a 0.18 μm CMOS process, the pixel size can be reduced to about 10 μm× 10 μm, which is close to the CCD pixel size. It should be sufficient for most scientific and biomedical imaging sensors.

VI. CONCLUSION

The design of a new activity-triggered wide dynamic range highly linear CMOS imaging sensor is introduced. The imaging sensor normally runs in the difference mode. It switches to capture WDR images if the activity in the scene is intense.

The co-existence of the two modes is enabled by the new pixel design. A low charge injection current sampler is included in the pixel for the difference mode. A partial quantization scheme is developed to linearly expand the DR of the imaging sensor with an in-pixel comparator. The nonlinear potential well size is compensated by a digital calibration scheme. The decoder cost of the pixel-level calibration scheme is low. A new out-of-pixel counter scheme is designed to separate the digital circuits from the analog pixel.

A proof-of-concept 32×32 imaging sensor is designed in a 0.35 μm CMOS process. The designed pixel has a high fill factor of 27%. Without the current sampler, the fill factor is 33%. The fabricated imaging sensor capture images up to 15 Hz with 95.3 dB dynamic range. After the digital calibration, the pixel distortion is as low as -75.6 dB over the whole dynamic range. The fixed-pattern noise of the designed imaging sensor is dominated by the photodiode variation. The maximum SNR of the fabricated imaging sensor is 74.5 dB. The new CMOS imaging sensor design with its wide dynamic range and high linearity can be used in high-performance scientific and biomedical imaging applications.

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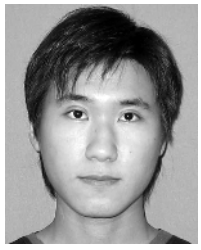

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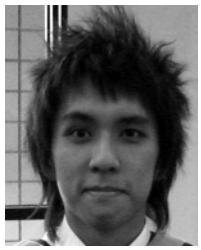

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