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An Adaptive Reconfigurable Active Voltage Doubler/Rectifier for Extended-Range Inductive Power Transmission

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Abstract

We present an adaptive reconfigurable active voltage doubler (VD)/rectifier (REC) (VD/REC) in standard CMOS, which can adaptively change its topology to either a VD or a REC by sensing the output voltage, leading to more robust inductive power transmission over an extended range. Both active VD and REC modes provide much lower dropout voltage and far better power conversion efficiency (PCE) compared to their passive counterparts by adopting offset-controlled high-speed comparators that drive the rectifying switches at proper times in the high-frequency band. We have fabricated the active VD/REC in a 0.5-μm 3-metal 2-poly CMOS process, occupying 0.585 mm^2 of chip area. In an exemplar setup, VD/REC extended the power transmission range by 33% (from 6 to 8 cm) in relative coil distance and 41.5% (from 53° to 75°) in relative coil orientation compared to using the REC alone. While providing 3.1-V dc output across a 500-Ω load from 2.15- (VD) and 3.7-V (REC) peak ac inputs at 13.56 MHz, VD/REC achieved measured PCEs of 70% and 77%, respectively.

Index Terms

Active rectifier (REC); active voltage doubler (VD); adaptive control; high-speed comparators; implantable microelectronic devices (IMDs); inductive power transmission; near field

I. Introduction

Modern implantable microelectronic devices (IMDs) require high power efficiency and performance to enable more efficacious therapies, particularly in neuroprostheses such as retinal and cochlear implants [1]. Inductive wireless power transmission across the skin is currently the only viable solution for providing sufficient power to such IMDs without imposing size and power constraints of implanted batteries [2]. On the downside, unlike batteries that provide a stable power source, unexpected variations in the coils' mutual coupling *M*, which mainly result from coil misalignments, can lead to wide variations in the received voltage across the secondary to the extent that the input voltage may not be sufficient to supply the IMD [3]. Hence, there is a need to improve the robustness of the inductive power links without sacrificing efficiency to allow the IMDs to operate over a wider range of received input voltages. There are also other applications such as wireless sensors, radio frequency identification, and near-field communication, in which extending the range of loosely coupled inductive links is highly desired [4].

Active rectifiers (RECs) and voltage doublers (VDs) using synchronous switches have been widely used to convert ac input signals to dc outputs for inductively powered applications [5]–[8]. RECs require peak inputs higher than the desired outputs, which may be temporarily limited by the weak coupling of the inductive links. On the contrary, active VDs are capable

of generating higher output voltages, but their power conversion efficiencies (PCEs) are generally lower than those of active RECs with similar size. In order to address such limitations, we have proposed a power-efficient reconfigurable active VD/REC for robust wireless power transmission through inductive links over an extended range. Both VD and REC modes are integrated into a single structure, employing low dropout active synchronous switches, leading to high PCE. Moreover, by adding an output-voltage-sensing circuit, VD/REC can automatically change its operating mode to either VD or REC depending on which one is a better choice for generating the desired output voltage to accommodate with a wider range of mutual coil arrangements.

Fig. 1 shows the block diagram of a wireless power transmission link that includes the proposed VD/REC. A power amplifier (PA) drives the primary coil L_1 at the designated carrier frequency (f_c = 13.56 MHz), which improves the coils' quality factors (Q) and increases the overall power transmission efficiency, while maintaining the sizes of LC components small for implantable applications [3]. A coupled signal across the secondary L_2 creates an ac voltage V_{IN} (= V_{INP} − V_{INN}) across L_2C_2 which is tuned at f_c. VD/REC, which follows the L_2C_2 tank, converts V_{IN} to an automatically adjusted dc voltage V_{OUT} for supplying the load after regulation. If V_{IN} falls below a certain level, which is determined by comparing a portion of V_{OUT} with a reference voltage V_{REF} using a hysteresis comparator, then Mode = 1 and VD/REC operates in VD mode. Since the VD can generate the desired V_{OUT} with much lower V_{IN} than the REC, VD/REC can still provide sufficient V_{OUT} to the load even with decreased V_{IN}. On the other hand, if V_{IN} increases above V_{REF} + hysteresis window, then Mode = 0 and VD/REC will operate in the REC mode, which can achieve higher PCE than the VD mode while generating the desired V_{OUT}.

The rest of this brief, which is an extended version of [9], is organized as follows. Section II describes the concept and implementation of active VD/REC. Section III presents the circuit details and design considerations including the offset-controlled high-speed comparators, start-up circuit, and mode selection circuit. The measurement results are in Section IV, followed by the conclusion in Section V.

II. Active VD/REC Architecture

A. Concept of the Active VD/REC

The concept of active VD/REC starts from combining two separate ac-to-dc converters, a REC and a VD, into a single structure in which the operating mode, REC or VD, is selected by an external mode selection signal. Fig. 2 shows the conceptual diagram of the active VD/REC converter which consists of a full-wave REC and a VD with active diodes. The full-wave REC requires two diodes D_1 and D_2 and a cross-coupled NMOS pair N_1 and N_2. Either the D_1–N_2 path or the D_2–N_1 path is activated depending on the amplitudes of V_{INP} and V_{INN} to transfer the input power to the output filtering capacitors C_F/2. The VD requires only two diodes D_1 and D_{N1}, charging one C_F per half cycle depending on the polarity and amplitude of V_{IN} (= V_{INP} − V_{INN}). Therefore, V_{OUT} becomes almost doubled compared to the peak voltage of V_{IN}. In order for VD/REC to include both structures, D_1 is shared, and D_2 and N_2 have enable functions to turn them on/off in the REC and VD modes, respectively. N_1 operates as part of a cross-coupled pair in the REC mode, while it is reconfigured as an NMOS diode D_{N1} in the VD mode. V_{INN} and V_M are also shorted through a switch N_3 in the VD mode. VD/REC utilizes active diodes D_1, D_2, and D_{N1}, in which rectifying pass transistors are driven by fast comparators to operate as switches in the deep triode region with low dropout voltages. Therefore, these active diodes dissipate less power compared to passive diodes, leading to higher PCE in both operating modes.

B. Implementation of the Active VD/REC

Fig. 3 shows a simplified schematic diagram of the VD/REC, consisting of PMOS and NMOS active diodes D_1, D_2, and D_{N1}, in which pass transistors P_1, P_2, and N_1 are driven by high-speed comparators CMP_{P1}, CMP_{P2}, and CMP_{N1}, respectively, to minimize ac–dc dropout voltage and power loss. Mode signals EN and EN_B, which are derived from the mode control circuit, can reconfigure the VD/REC topology for rectification or doubling functions, as shown in Fig. 2. In the REC mode ($EN = 0$ and $EN_B = 1$), the gates of N_1 and N_2 are connected to V_{INN} and V_{INP}, respectively, resulting in a cross-coupled NMOS pair with positive feedback, while CMP_{N1} is deactivated. Both PMOS active diodes are utilized in this mode, alternating every half cycle to transfer input power to the load. For example, when $V_{INP} > V_{INN}$, N_2 turns on, while N_1 turns off. Then, when $V_{INP} > V_{OUT}$, the CMP_{P1} output goes low, turning P_1 on with a low dropout voltage. The input current in this case flows from V_{INP} through P_1 to charge $C_F/2$ and returns back to V_{INN} through N_2. In the VD mode ($EN = 1$ and $EN_B = 0$), P_2 and N_2 are always off, and CMP_{P2} is deactivated. Only P_1 and N_1 operate as active diodes, while N_3 strongly connects V_{INN} to V_M for charging the filtering capacitors C_F, one per half cycle, to almost double V_{OUT} in reference to V_{SS}.

Since the comparators in active diodes are supplied from V_{OUT}, which is initially at 0 V, self-start-up capability is a feature necessary in active VD/REC. The start-up circuit in Fig. 3 monitors V_{OUT} and sets $SU = EN = EN_B = 0$ when V_{OUT} is too low. At start-up, N_1 and N_2 are cross-coupled through multiplexers (MUXs), and P_1 and P_2 are diode connected through P_3 and P_4, respectively, forming a passive REC, which charges V_{OUT} regardless of the comparators' status up to the point where V_{OUT} reaches a desired level. Then, SU toggles to enable VD/REC to operate normally. PMOS body terminals V_{B1} and V_{B2} are always connected to the highest potential among $V_{INP,N}$ and V_{OUT} via their body bias circuits.

III. Circuit Details and Design Considerations

In order to drive large pass transistors at 13.56 MHz, comparators need to have short turn-on/turn-off delays, which may otherwise reduce the PCE by either decreasing the input power delivered to the load or allowing instantaneous reverse current back from C_F. We have used high-speed comparators with built-in offset-control functions to expedite V_{OUT} transitions by compensating for both turn-on and turn-off delays [10]. Fig. 4 shows the schematic diagram of the high-speed comparator CMP_P, which is equipped with three offset-control functions: turn-on, turn-off, and output-locking offsets. In Fig. 4, P_6, P_7, N_7, N_8, P_{11}, and N_{14} form a common-gate comparator, in which input voltages (V_{OUT} and $V_{INP,N}$) are applied to the sources of P_6 and P_7. The turn-on offset block, consisting of P_8 and P_9 current sources and P_{10} control switch, injects additional offset current to force V_1 to increase earlier, leading to fast turn-on of $P_{1,2}$ in Fig. 3. The offset-control signal V_{OS1P} deactivates P_{10} just after turning $P_{1,2}$ on and activates it again after the current-starved inverter (INV_1 and N_{15}) delay, which does not need to be accurate as long as it is shorter than one carrier cycle. The turn-off offset function utilizes the size mismatch between N_7 and N_8, where the larger N_8 pulls additional current from the V_1 node, forcing V_1 to start dropping earlier to turn $P_{1,2}$ off at the right time. After the comparator output V_{CP} goes high and turns $P_{1,2}$ off, N_{11} is activated by V_{OS2P} for the current-starved inverter delay time to keep V_1 low and prevent V_{CP} from bouncing due to $V_{INP,N}$ variations. CMP_N has a similar but symmetrical structure. In addition, 4-bit off-chip digital control signals, CTL0:1 for CMP_P and CTL2:3 for CMP_N, are utilized to adjust the switching times of VD/REC against process variations.

In the start-up circuit in Fig. 5(a), when V_{OUT} is very low, P_{12} turns off and SU goes low, resulting in P_1 and P_2 in Fig. 3 to stay diode connected through P_3 and P_4, respectively. During the same period, both EN and EN_B of the mode control circuit in Fig. 5(b) become

low, so all comparators are in the sleep mode while N_1 and N_2 are cross-coupled through MUXs, leading the VD/REC to operate as a passive REC. With $SU = EN_B = 0$, N_{13} in Fig. 4 forces $V_{CP1,2}$ to be high, further supporting P_1 and P_2 to be diode connected. When $V_{OUT} > V_{Th(N16)} + V_{Th(P12)}$, SU toggles high, turning P_3 and P_4 off, releasing the comparator outputs, and allowing P_1 and P_2 to operate as switches [10]. The mode control circuit consists of two pairs of level shifters and logic gates, one of which is shown in Fig. 5(b), to level shift the mode signal to either V_{B1} or V_{B2} (in Fig. 3) for creating the EN and EN_B signals, which control various switches at proper voltage levels. In Fig. 5(c), the body bias circuit automatically connects V_{B1} and V_{B2} to max(V_{INP}, V_{OUT}) and max(V_{INN}, V_{OUT}), respectively, through P_{17} and P_{18} [6].

IV. Measurement Results

A. Chip Micrograph and Measured Waveforms

VD/REC was fabricated in the ON Semiconductor 0.5-μm 3M2P n-well standard CMOS process, occupying 0.585 mm^2. Fig. 6 shows the chip micrograph and floor plan of the VD/REC, low dropout regulator (LDO), and bandgap reference (BGR). The sizes of the main rectifying transistors are as follows: $W_{P1,2}$ = 3300 μm, $W_{N1,2}$ = 1800 μm, and W_{N3} = 12 000 μm with a minimum length of L = 0.6 μm.

Fig. 7 shows the measured input/output waveforms in the REC and VD modes with $R_L \| C_F/2$ = 1 kΩ‖0.5 μF (no regulator) at f_c = 13.56 MHz. The same supply voltage was applied to the PA on the primary side to verify the V_{OUT} difference between the REC and VD modes. In the REC mode (Mode = 0), V_{INP} and V_{INN} charge V_{OUT} alternatively, resulting in $V_{IN,peak(REC)}$ = 3.35 V and V_{OUT} = 2.7 V. In the VD mode (Mode = 1), V_{INN} is shorted via N_3 to V_M, the middle voltage of V_{OUT}, and V_{INP} goes well above $V_{IN,peak(REC)}$ to achieve V_{OUT} = 3.55 V with $V_{IN,peak(VD)}$ = 2.6 V. Large instantaneous input currents flow into the VD/REC during the conduction period, inducing the voltage drop across N_3, which is $V_{INN} - V_M$. $V_{IN,peak(VD)}$ is less than $V_{IN,peak(REC)}$ because of a reduction in the inductive link Q factor due to higher input and output currents in the VD mode.

B. Power Transmission Range and PCE Measurements

In order to verify the benefits of using the VD/REC over a REC, we have measured $V_{IN,peak}$ and V_{OUT} while sweeping the relative distance (d) and orientation (θ) between a pair of coupled coils L_1 and L_2, as shown in Fig. 8. In this test setup, whose specifications are shown in Table II, a class-C PA on the transmitter side (Tx) drives the inductive link to induce a 13.56-MHz sinusoidal signal across the VD/REC. Fig. 9 shows the measured $V_{IN,peak}$ and V_{OUT} versus d and θ and demonstrates how using the VD/REC extends the inductive link power transmission range in terms of the coils' relative distance and angular misalignment compared to REC only. The hysteresis window of the off-chip comparator was set to 2.6–3.7 V and indicated on the graphs as horizontal dashed lines. In the d-sweep test, the VD/REC operates in the REC mode when d is small. V_{OUT} drops as d increases, and when d > 5.5 cm, VD/REC switches to the VD mode, increasing V_{OUT} by 0.8 V (30.8%). As a result, VD/REC maintains sufficient V_{OUT} > 2.5 V for coil separations up to d = 8cm, compared to the REC only, which fails at d > 6 cm (a 33% improvement). Similarly, VD/REC improved the inductive link tolerance to coil rotations by extending the range from θ = 53° (REC only) to θ = 75° (VD/REC) at d = 3 cm (a 41.5% improvement).

To consider the practical conditions in which the output voltage of the VD/REC varies due to coil misalignments as well as loading changes, we measured the PCE while sweeping V_{OUT} by adjusting the Tx output power delivered to the primary coil L_1. The PCE of VD/REC can be defined as the delivered power to the load over the input power from the L_2C_2

tank. Fig. 10 shows the measured PCE versus V_{OUT} in both REC and VD modes with R_L = 0.5 and 1 kΩ at f_c = 13.56 MHz. The highest PCEs of the REC and VD modes were 77% and 70%, respectively, at V_{OUT} = 3.1 V with R_L = 0.5 kΩ. The PCE drops for V_{OUT} > 3.7 V and V_{OUT} < 2.8 V are mainly due to the pass transistor sizing and comparator offsets which were designed for V_{OUT} = 2.8–3.7 V. The VD/REC still operates properly against V_{OUT} variations with *PCE* > 74% within V_{OUT} = 2.6–4.3 V in the REC mode and *PCE* > 68.5% within V_{OUT} = 2.5–3.7 V in the VD mode for R_L = 0.5 kΩ. The V_{OUT} range is determined based on the hysteresis comparator window of 2.6–3.7 V. Table I benchmarks the proposed active VD/REC against several recently reported RECs and VDs. Table II provides a few additional specifications of the VD/REC and the inductive link used in our measurements.

C. In Vitro Experiments

Inductively powered IMDs that employ the active VD/REC converter need to be hermetically sealed in biocompatible materials and placed in a conductive tissue environment with high permittivity, which can affect not only the secondary coil characteristics but also the VD/REC performance [11]. In order to emulate the implant environment, we conducted *in vitro* experiments with the test setup in Fig. 11, in which the secondary coil (L_2) was wrapped in a piece of steak (bovine sirloin). Fig. 12 shows the measured $V_{IN,peak}$ and V_{OUT} while sweeping the coils' relative distance (d) in the air (Fig. 8) and muscle (Fig. 11) environments. The muscle environment leads to a small reduction in both $V_{IN,peak}$ and V_{OUT} compared to the air environment when d is increased. This is because wrapping L_2 with a piece of steak increases its parasitic capacitance and resistance, leading the quality factor (Q) of the secondary coil to decrease and the power loss in its parasitic resistance to increase. However, these curves show that using the VD/REC still extends the inductive link power transmission range in both environments to d > 8 cm.

V. Conclusion

Inductive power transmission across the skin is considered the most promising solution for providing sufficient power to IMDs without suffering from size and power constraints of implanted batteries. However, large variations in the received voltage across the secondary coil, which mainly result from coil misalignments or loading variations, can lead to insufficient supply voltage for the IMD. In order to overcome this limitation, we have developed a power-efficient reconfigurable active VD/REC, which can automatically change its operating mode to operate as either a VD or a REC, depending on which one is more suitable for generating the desired output voltage at the highest possible PCE, enabling robust power transmission across the inductive link over an extended range. The presented VD/REC has been equipped with active diodes, in which high-speed comparators synchronously control MOS switches at proper times owing to their turn-on and turn-off offset functions, achieving high PCE and low dropout voltage. The measured results while sweeping the coils' relative distance and orientation clearly verify that using the VD/REC extends the inductive power transmission range in both air and muscle environments.

Acknowledgments

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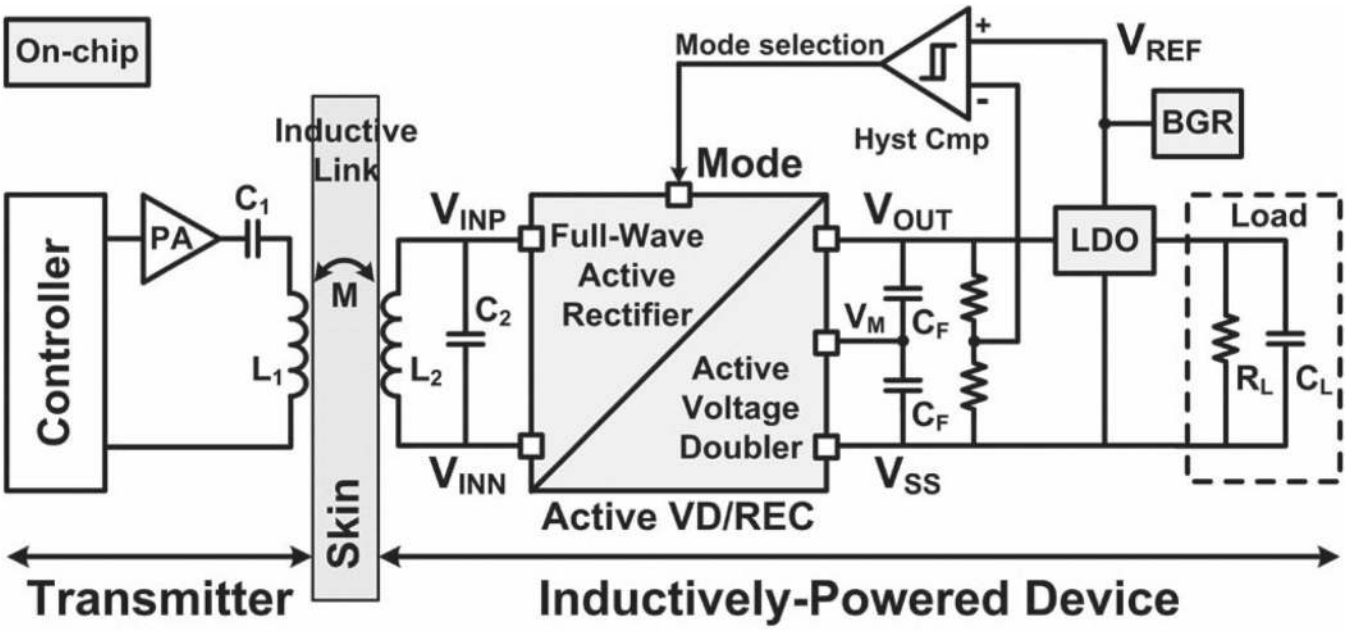

Condition	Mode	Operation	Key Feature
$V_{OUT} > V_{REF(Hyst)}$	0	Full-wave rectifier	High power efficiency (PCE)
$V_{OUT} < V_{REF(Hyst)}$	1	Voltage doubler	High output voltage (V_{OUT})

Fig. 1.
Block diagram of an inductively powered device with emphasis on the wireless power transmission through the proposed active VD/REC converter.

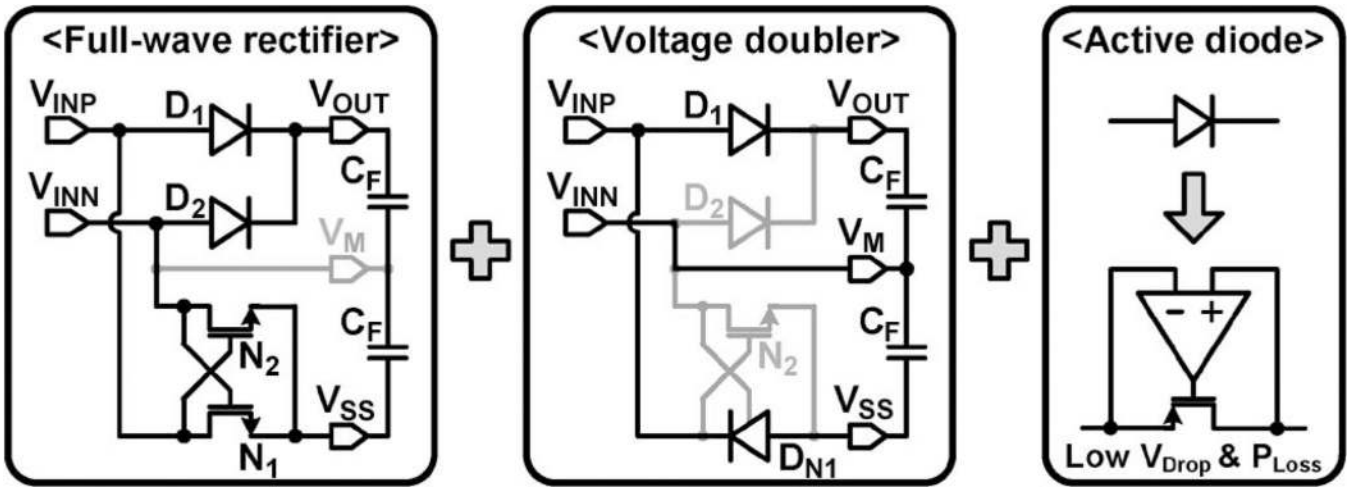

Fig. 2.
Conceptual diagram of the active VD/REC converter in which a full-wave REC and a VD are combined using active diodes.

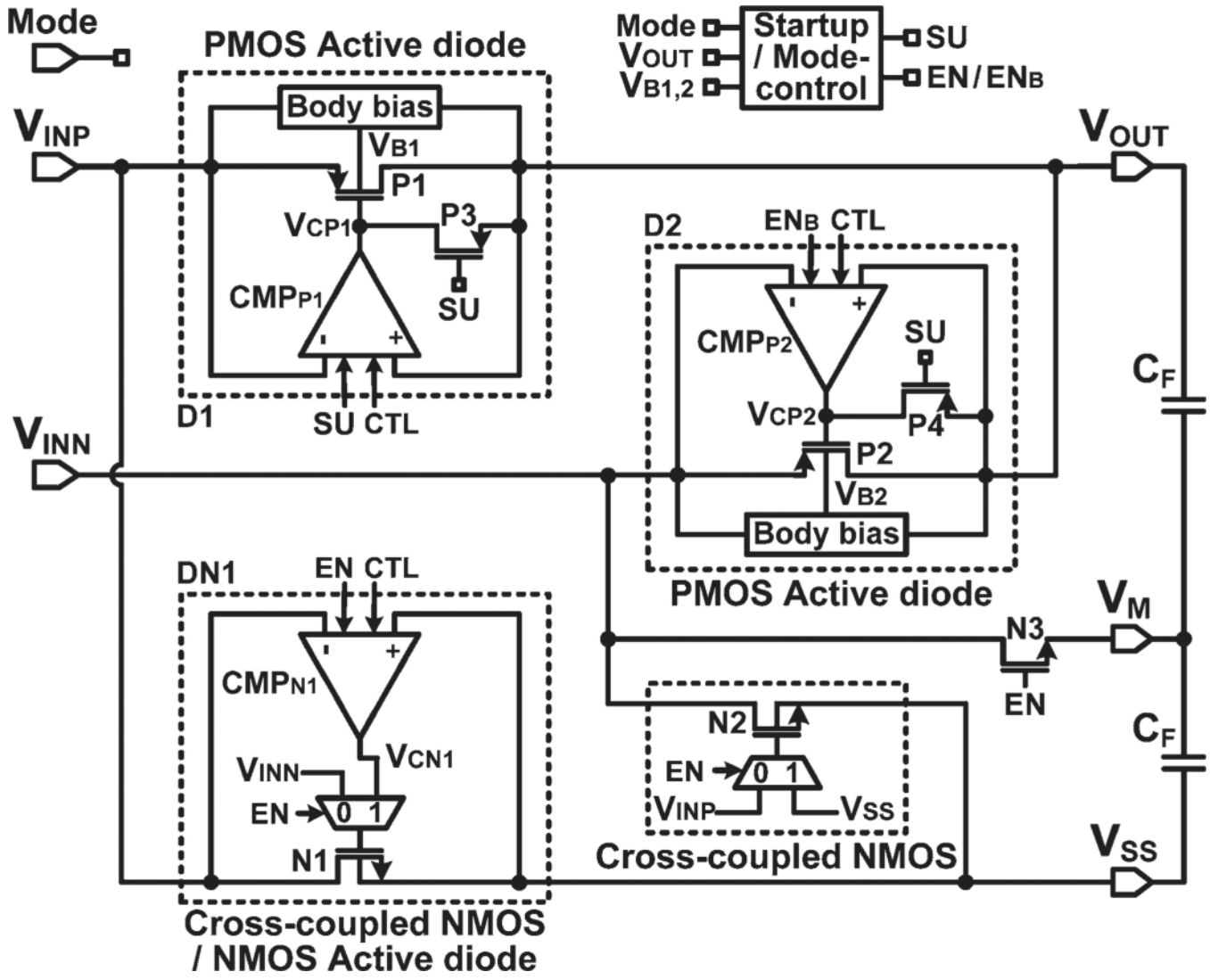

Fig. 3.
Schematic diagram of the proposed VD/REC employing active diodes to achieve lower dropout voltage and higher PCE for both REC and VD modes.

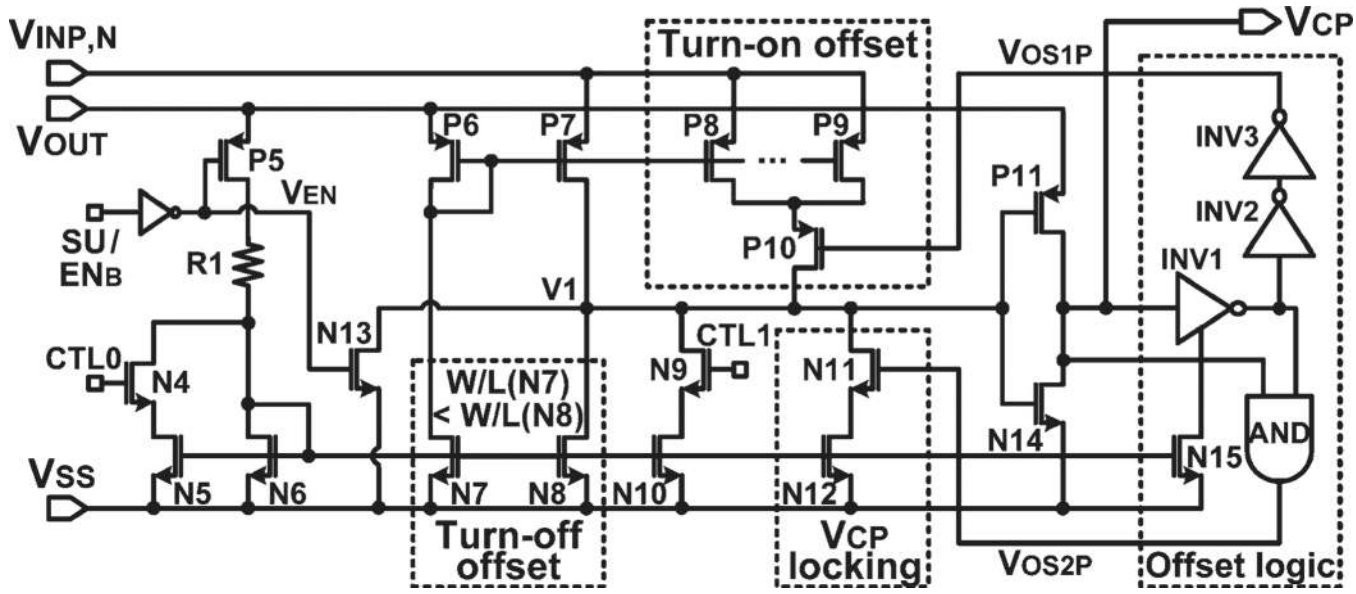

Fig. 4.

Schematic diagram showing three built-in offset-control functions, which are turn-on, turn-off, and output-locking offsets, in our high-speed comparator CMP_P [10].

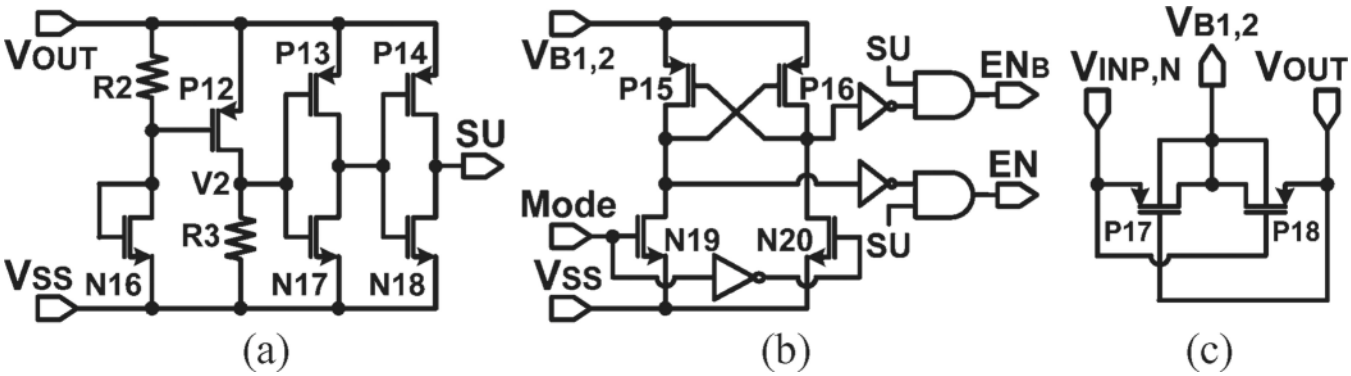

Fig. 5.
Schematic diagrams of the (a) start-up circuit, (b) mode control circuit, and (c) body bias circuit.

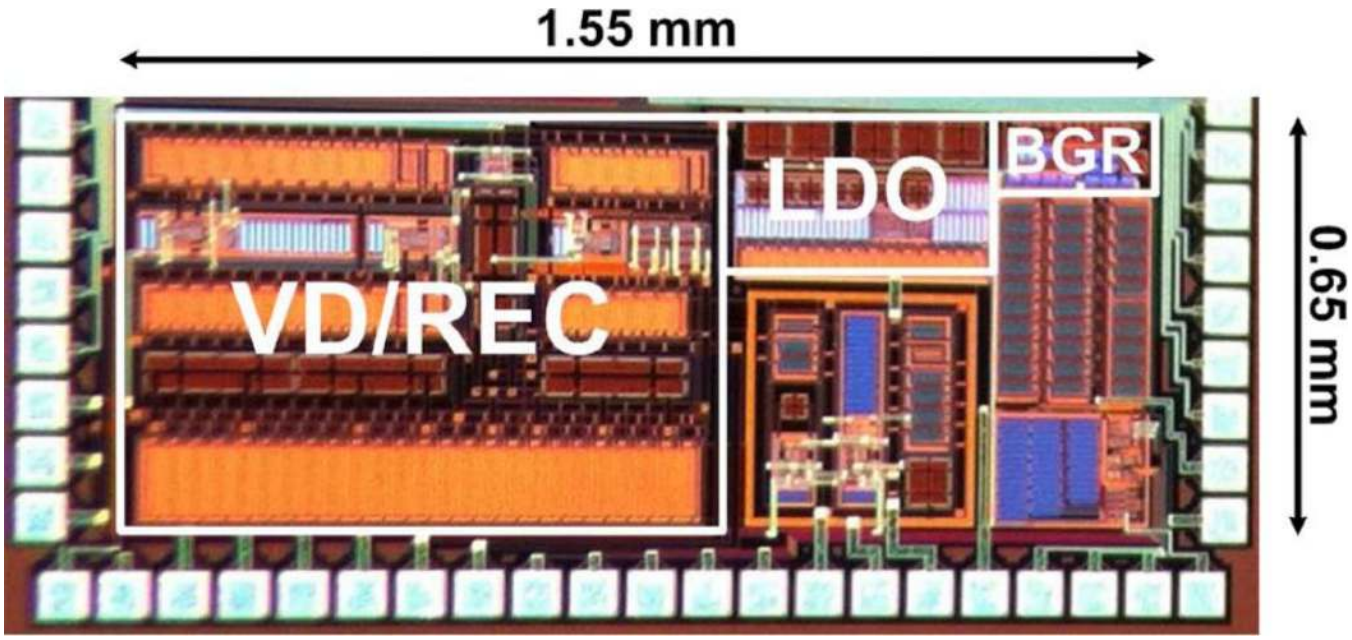

Fig. 6.
Fabricated chip micrograph of the VD/REC in the ON Semiconductor 0.5-μm standard CMOS process, occupying an area of 0.585 mm^2.

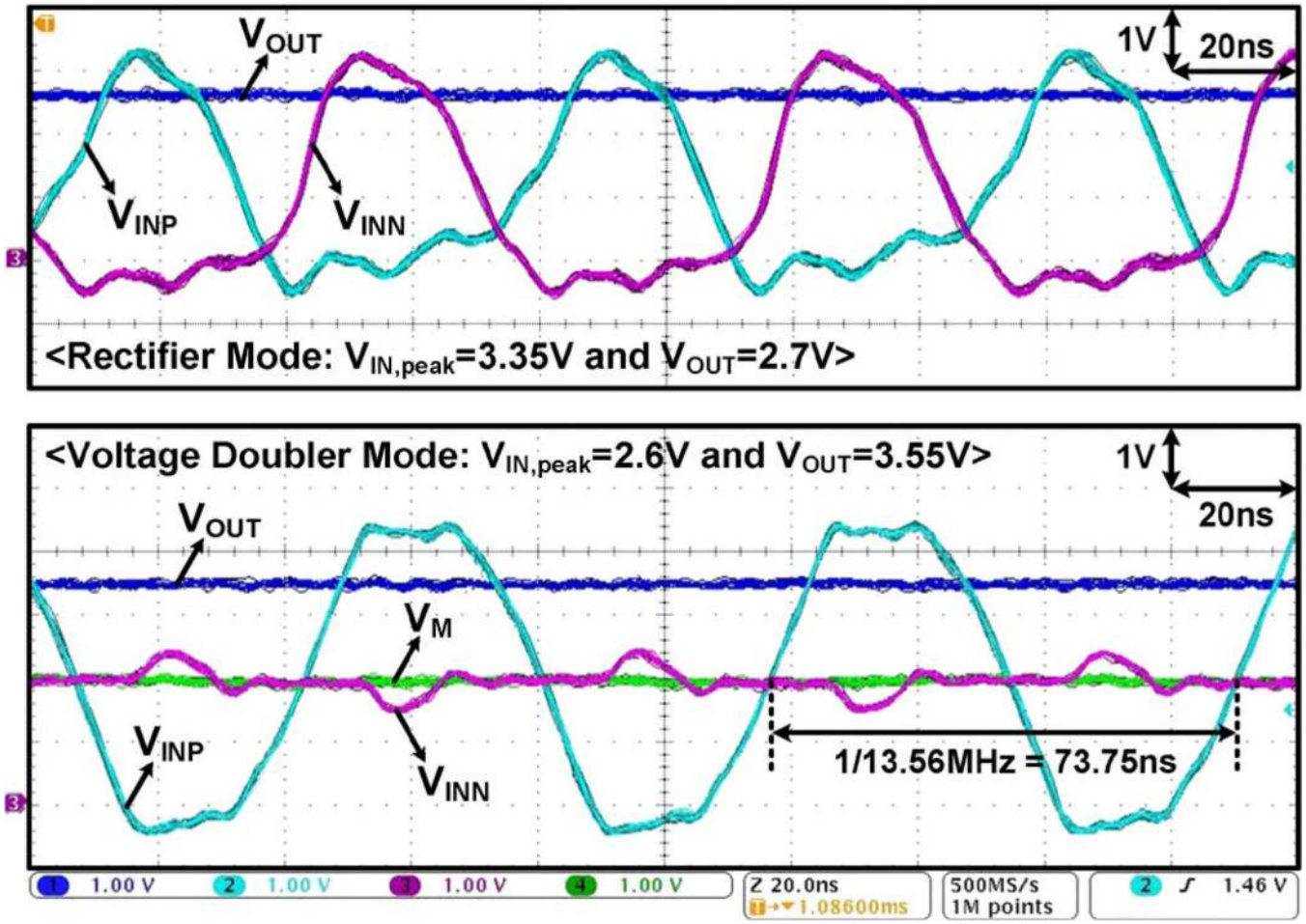

Fig. 7.
Measured input/output voltage waveforms in the (top) REC and (bottom) VD modes when $R_L \| C_F/2$ = 1 kΩ||0.5 μF (no regulator) and f_c = 13.56 MHz.

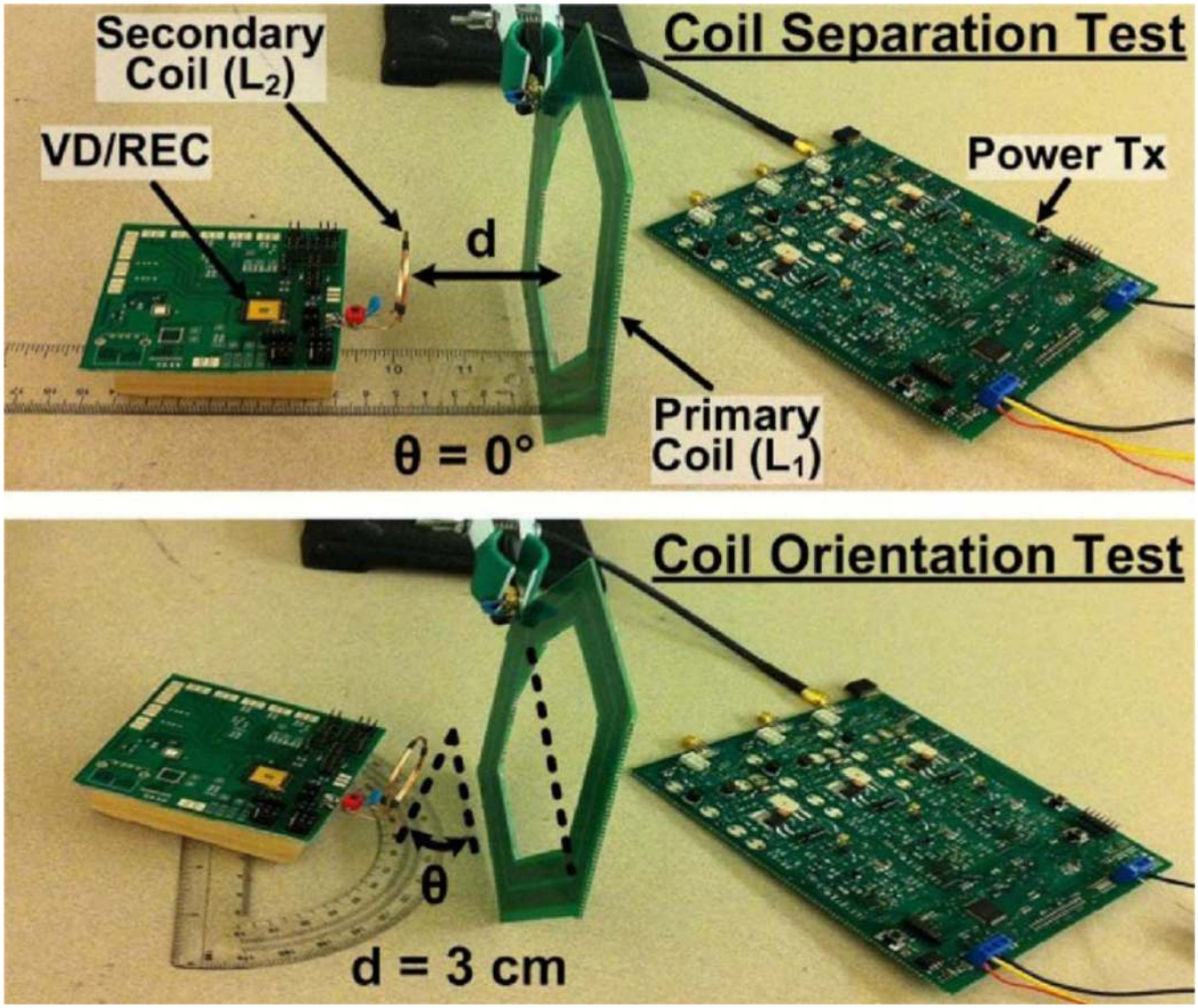

Fig. 8.
Test setup for measuring the PCE and input/output voltages of the active VD/REC ac-to-dc converter when sweeping the relative coil (top) distance and (bottom) orientation.

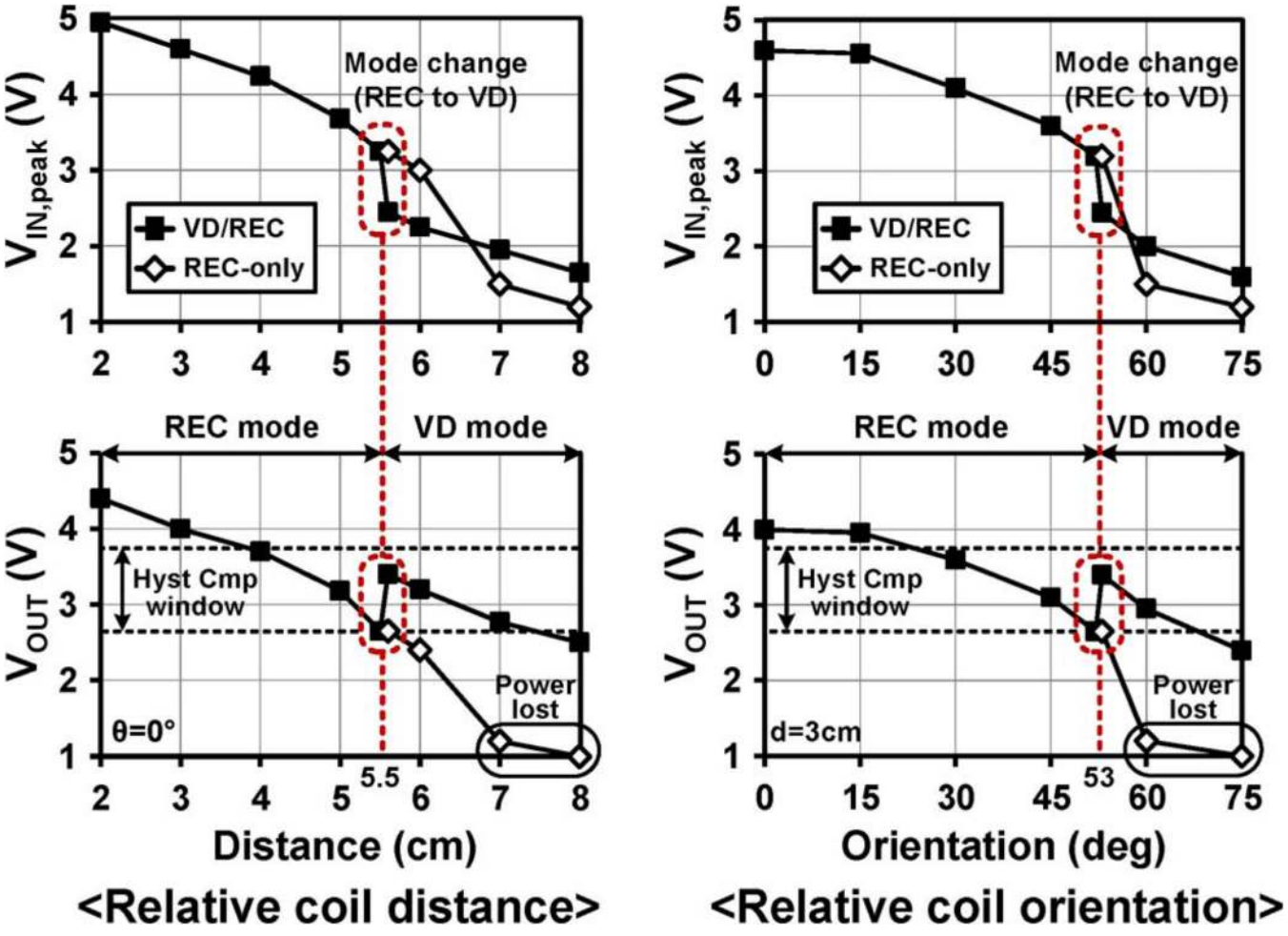

Fig. 9.

Measured input and output voltages while sweeping the coil relative distance (*d*) and orientation (θ) in Fig. 8, which clarify that using VD/REC extends the inductive link power transmission range.

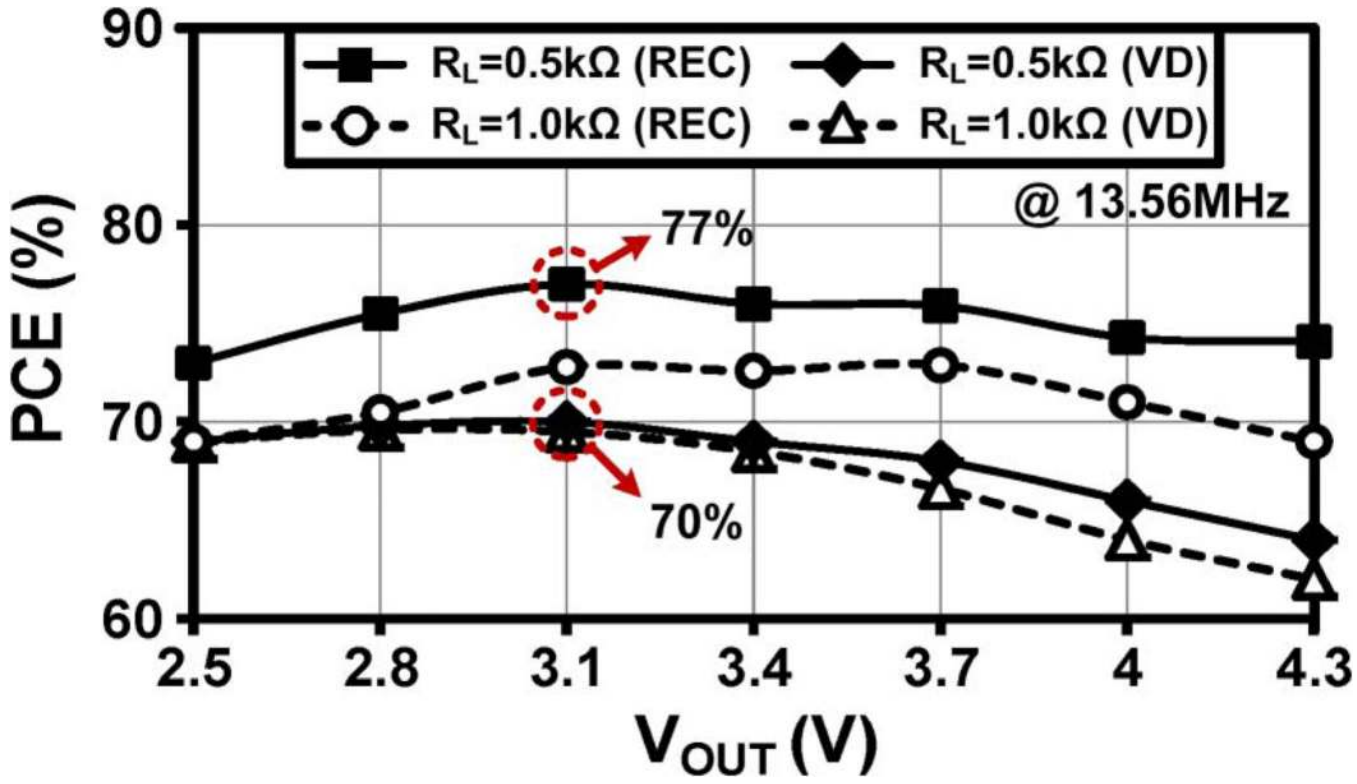

Fig. 10.
Measured PCE versus V_{OUT} with R_L = 0.5 and 1 kΩ at f_c = 13.56 MHz, leading to the highest PCEs of 77% and 70% in the REC and VD modes, respectively.

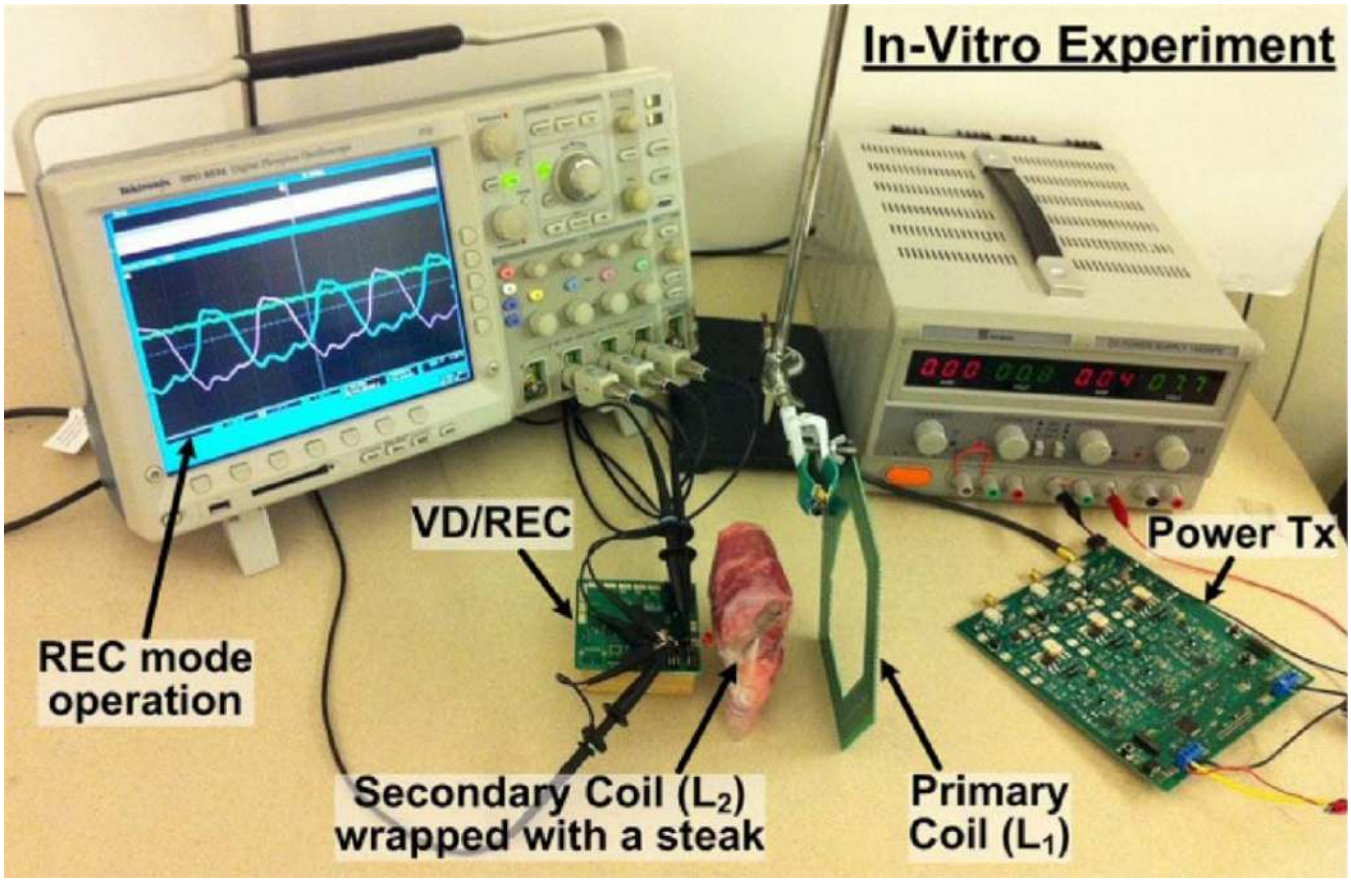

Fig. 11.
Test setup for *in vitro* experiments that resemble an IMD environment with the secondary coil L_2 wrapped in a piece of steak.

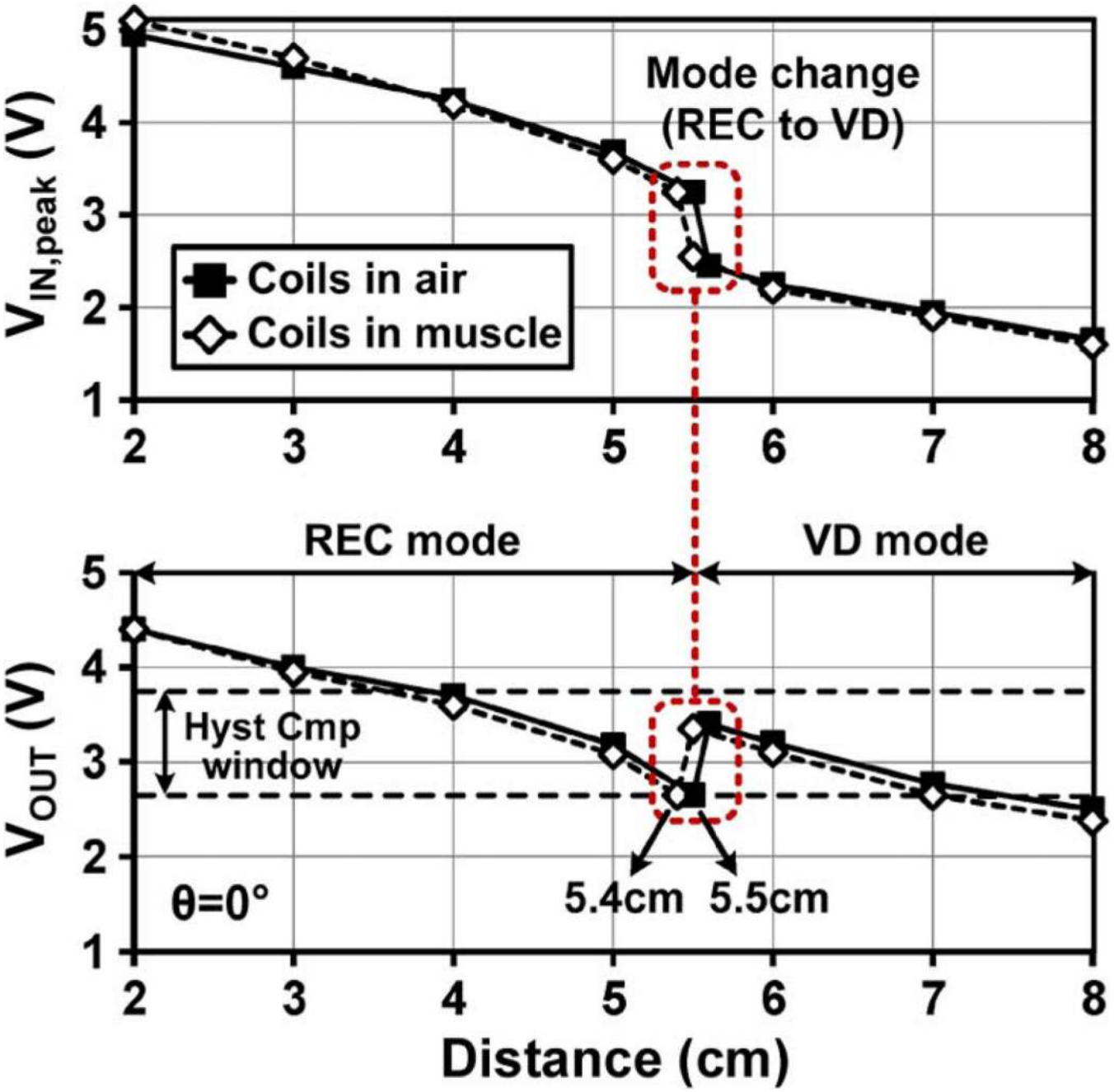

Fig. 12.
Measured input and output voltages while sweeping the coils' relative distance in the air (Fig. 8) and muscle (Fig. 11) environments.

TABLE I

REC and VD Benchmarking

Publication		**[5]**	**[6]**	**[7]**	**[8]**	**This work**	
Technology		**0.18µm**	**0.5µm**	**0.18µm**	**0.8µm**	**0.5µm CMOS**	
Structure		**REC**	**REC**	**Multiplier**	**VD**	**Active VD/REC**	
						VD	**REC**
$V_{IN,\,peak}$ (V)		1.25	3.8	0.8	11.1	**2.15**	**3.7**
V_{OUT} (V)		0.96	3.12	1.8	20	**3.1**	**3.1**
VCE (%)*		76.8	82.1	56.3	90.1	**72.1**	**83.8**
R_L (kΩ)		2	0.5	270	20	**0.5**	
f_c (MHz)		10	13.56	13.56	13.56	**13.56**	
Area (mm^2)		0.86	0.18	0.83	N/A	**0.585**	
PCE (%)	Sim.	N/A	87	N/A	90.5	**75**	**81**
	Meas.	76	80.2	54.9	N/A	**70**	**77**

*Voltage conversion efficiency (VCE) = $V_{OUT}/(V_{IN,\,peak} \times$ multiplication factor)

TABLE II

Additional Active VD/REC Measurement Setup Specifications

Nominal output power	6 ~ 37 mW
Output filtering capacitor (C_F)	1 μF
Output ripple (R_L = 0.5 kΩ)	50 mV_{pp}
Bandgap reference voltage (V_{REF})	1.187 V
Primary coil diameter / inductance (L_1)	16.8 cm / 0.88 μH
Secondary coil diameter / inductance (L_2)	3.0 cm / 0.41 μH
Total area of the VD/REC	0.585 mm^2