An Advanced Surface-Potential-Plus MOSFET Model

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ABSTRACT

Like other surface-potential based model, our surface-potential-plus model starts with charge-sheet approximation, uses the quasi-Fermi-potential to integrate drift and diffusion current and formulates an inversion charge equation that can be analytically solved for given terminal voltage. This eliminates the need for precise computation of the surface potential. Based on the inversion charge solution, a continuous, symmetric and accurate MOS model is developed. Various small dimensional effects including polysilicon depletion, quantum mechanical effects, velocity overshoot, source-side injection limit effect, and quasi ballistic transport of nano-scale MOSFETs are integrated naturally into this model. Comparison with measured data validates the new model. The modeling framework is easily extendable to SOI and double-gate MOSFETs.

Keywords: MOSFETs, compact modeling, surface-potential-plus model, small dimensional effects.

1 INTRODUCTION

Most current compact MOSFET mo dels such as MOS-11, HSIM and SP-2000 are in some way formulated in terms of the solutions for the surface potential at the source and drain boundaries of the channel based on the charge-sheet model developed by J.R.Brew[1]. Thus, all these models are also called surface-potential based charge-sheet models. The main difficulty in these models is that the boundary surface potential cannot be expressed explicitly in terms of terminal voltages, but must be found empirically, approximately or numerically. And then, the channel current and various charges are computed in terms of the boundary surface potentials. As a result, all surface potential based MOSFET models have to expect poor computation efficiency and simulation speed, which is not available for comple x circuit simulation. More importantly, how to correctly and accurately treat small dimensional effects and advanced process such as retrograde and halo doping are also major challenges in all surface potential based models.

The industrial standard BSIM3/4 model [2] began a pioneering attempt to directly calculate the inversion charge in terms of bias. USIM, UUCM, EKV and ACM also made useful efforts in modeling inversion charge [3-6]. These works indicate that a charge-based MOSFET model is direct, and computationally efficient in modeling I-V and C-V characteristics. The **BSIM** team is striving to develop a new generation MOSFET model that has complete physics basis and is flexible for new physics effects. This paper presents an advanced surface-potential-plus model that starts with the charge-sheet assumption, formulates an inversion charge equation that can be analytically solved for given terminal voltage. Based on the inversion charge solution, a continuous, symmetric and accurate MOS model is developed. Various small dimensional effects including polysilicon depletion, quantum mechanical effects, velocity overshoot, source–side injection limit effect, and quasi ballistic transport are integrated into the model. Comparison with measured data validates the new model. The modeling framework is easily extendable to SOI and double-gate MOSFETs.

2 EXACT CHARGE RELATION

For simplicity, the channel charges are normalized by $C_{ox}V_t$, the surface potential and all voltages are also normalized by the thermal voltage V_t. According to the charge-sheet approximation, the drain current is written as

$$I_{ds} = \mu_s W V_t^2 C_{ox} q_I \left[d\phi_s / dx - dq_I / q_I / dx \right] \quad (1)$$

where all symbols have the common meanings.

In present all surface-potential-based models, the inevasible step is to obtain the surface potential in various approximate methods and then formulate the various charges and current in the surface potential solution. In contrast, the surface-potential-plus model uses the quasi-Fermi-potential to integrate drift and diffusion current and formulates an inversion charge equation. The drain current formulated in the quasi-Fermi-potential is expressed as [7]

$$I_{ds} = \mu_s W V_t^2 C_{ox} q_I dV_{ch} / dx \quad (2)$$

where V_{ch} is the difference between the electron and the hole quasi-Fermi-potential or channel voltage.

When (2) is substituted into (1)

$$dq_I / q_I = \left[d\phi_s - dV_{ch} \right] \quad (3)$$

Eq.(3), the core of the surface-potential plus model, is also one master equation of the charge sheet model.

The traditional approach to modeling MOSFETs must solve the Poisson equation under the uniform doping substrate assumption. However, a retrograde doping profile is more common in today's fabrication process. We start from Gauss's law of an ideal retrograde doping substrate. In this case, Gauss's law directly gives the common voltage and charge equilibrium equation

$$q_I = V_{GB} - V_{FB} - \phi_s - q_b \quad (4)$$

Differentiating the inversion charge with respect to the surface potential and gate voltage

$$dq_I = dV_{GB} - n d\phi_s \tag{5}$$

where n is expressed

$$n = 1 + \frac{\gamma}{2\sqrt{\phi_s}\left[1 + q(N_{sub} - N_{epi})t_{epi}^2 / 2\varepsilon\phi_s\right]^{1/2}} \tag{6}$$

It is evident that n degenerates into the uniform doped case if the epitaxial layer concentration equals to the substrate or thickness tends to zero. Combining (3) and (5) results in

$$dq_I / q_I + dq_I / n = dV_{GB} / n - dV_{ch} \tag{7}$$

Integrating (7), one obtains

$$\ln(q_I / n) + q_I / n = [(V_{GB} - k)/n - V_{ch}] \tag{8}$$

where k is an integral constant. Extrapolating (8) into the strong inversion case indicates k is just the intrinsic threshold voltage V_{T0} of MOS-C for $V_{ch} = 0$. As a result, a physics-based unified inversion charge relation is obtained

$$\ln(q_I / n) + q_I / n = [(V_{GB} - V_{T0})/n - V_{ch}] \tag{9}$$

(9) is the W-Lambert equation $xe^x = W$, and the exact analytical solution is its principal branch value

$$q_I = nW_0\{\exp[(V_{GB} - V_{T0})/n - V_{ch}]\} \tag{10}$$

This well-known function is implemented in software packages such as Mathematica and Maple.

Eqs.(7)~(10), respectively, consist of derivative, integral and exact solution of the inversion charge relation, which have the different uses in different modeling cases.

(9) thus (10) embodies the exponential-linear dependence of the inversion charge on the gate and channel voltages from sub-threshold to strong inversion region. For example, (9) can be degenerated to the strong inversion case for a given large gate voltage

$$q_I = (V_{GB} - V_{T0}) - nV_{ch} - \Delta V = V_{GB} - V_{TB} - \Delta V \tag{11}$$

with the gate-substrate extrapolation threshold voltage V_{TB} and ΔV due to the non-pinning characteristics of the surface potential.

$$V_{TB} = V_{T0} + nV_{ch} \text{ and } \Delta V = nV_t \ln[(V_{GB} - V_{TB})/nV_t] \tag{12}$$

Our (9) and (7) are similar to the inversion charge relation of USIM and UUCM. The similar relation has also been obtained in EKV and ACM models. However, UCCM results from an experimental data fitting. USIM depends on some special definitions, e.g., the channel saturation voltage and h_x. In EKV and ACM models, on one hand, the linear-relationship between the inversion charges and surface potential is a fundamental. However, this assumption does not always exist in all operation regions. On the other hand, both the pinch-off voltage and pinch-off inversion charge concepts are contradictory to each other. Moreover, the above-mentioned models do not have an exact solution of the channel inversion charges. The new surface-potential-plus model develops a set of channel charge relation available for the uniform and retrograde doping. It is very interesting that effective gate voltage expression in BSIM3/4 is a good approximation to (10).

Fig.1 shows the G-B threshold voltage as a function of the channel voltage with a uniform doping. For simple comparison, the classical definition is also plotted. One can find an excellent agreement between both cases. Once the threshold voltage is obtained, the inversion charges can calculated from (4). Fig.2 shows the comparison of the inversion charges between the analytical and the numerical results. All these demonstrate that this model can direct calculate the exact channel charges without involving the surface potential calculation.

3 CHARGE-CONTROLLED CURRENT EQUATION

For a constant gate voltage, Combing (1) and (7) gives a charge-controlled current in a differential mode

$$I_{ds} = -\mu_s WC_{ox}V_t^2 \frac{(1 + q_I / n)dq_I}{dx} \tag{13}$$

Integrating (13) along the channel results in a complete channel current expression in an integral mode

$$I_{ds} = \frac{\mu_s WC_{ox}V_t^2}{L}\left[\frac{q_s^2 - q_d^2}{2n} + (q_s - q_d)\right] \tag{14}$$

It is very convenient to transform (14) into a charge-controlled current in a square law mode for comparison with the traditional current expression

$$I_{ds} = \frac{\mu_s WC_{ox}V_t^2}{2nL}\left[(q_s + n)^2 - (q_d + n)^2\right] \tag{15}$$

In order to conveniently get various small-signal expressions, a reverse-forward mode of the charge-controlled current is also useful

$$I_{ds} = I_F - I_R = \frac{\mu_s WC_{ox}V_t^2}{2nL}(q_s + n)^2 - \frac{\mu_s WC_{ox}V_t^2}{2nL}(q_d + n)^2 \tag{16}$$

where I_F and I_R are the forward and reverse current, respectively.

Note that the present charge-controlled expression is C_∞ continuous, symmetric, and asymptotically results in saturation behavior.

4 SMALL DIMENSIONAL EFFECTS

The practical CMOS process is scaling down into deep-submicron region. The above-discussed ideal MOS transistor model is hierarchically extended to include various small dimensional effects within the framework of the channel charge core model.

4.1 Horizontal mobility degradation and saturation inversion charges

The high longitudinal field in MOSFETs results in a horizontal mobility degradation and finally a carrier velocity saturation. A universal relationship is developed and a two-region model describes this effect. After this relationship is substituted into (1) and simplified, one obtains the linear region current expression

$$I_{ds0}=\frac{\mu_s WC_{ox}V_t^2}{L[1+V_t(q_s-q_d)/E_cL]}\left[\frac{q_s^2-q_d^2}{2n}+(q_s-q_d)\right] \quad (17)$$

If one equates (17) to the saturation region current $I_{dsat}=WC_{ox}V_tq_{dsat}v_{sat}$, an analytical drain saturation inversion charge expression is obtained

$$q_{sat}=\frac{q_s^2+2q_s/n}{q_s+(E_cL+2V_t)/nV_t} \quad (18)$$

It is convenient to obtain the saturation drain voltage from (8) for the known inversion charge. This is a great challenge in the traditional surface-potential-based models An effective inversion charge function that smoothes the inversion charges from q_d to q_{sat} is used to get the complete drain current including the horizontal mobility degradation and velocity saturation effect.

$$q_{eff}=\sqrt[2n]{q_d^{2n}+q_{sat}^{2n}} \quad (19)$$

4.2 Vertical mobility degradation

On the basis of the "universal" mobility relation, the vertical mobility can expect

$$\mu_s=\frac{\mu_0}{1+\theta_1E_{eff}^1+\theta_2E_{eff}^2} \quad (20)$$

The effective field is integral average value along the channel direction.

4.3 Overshoot

In the deep-submicron region, the velocity overshoot is observed to be a significant effect even though the supply voltage is scaled down according to channel length. An approximate non-local velocity field expression has proven to provide a good description of this effect

$$v=v_d\left(1+\frac{\lambda}{E}\frac{\partial E}{\partial x}\right)=\frac{\mu E}{1+E/E_c}\left(1+\frac{\lambda}{E}\frac{\partial E}{\partial x}\right) \quad (21)$$

This relationship is substituted into Eq.(1) and simplified under the context of the channel charge core model, one can obtain the current expression including the velocity overshoot effect

$$I_{ds}=\frac{\mu_s WC_{ox}V_t^2}{L_{eff}[1+V_t(q_s-q_{eff})/E_cL_{eff}]}\left[\frac{q_s^2-q_{eff}^2}{2n}+(q_s-q_{eff})\right]\left[1+\frac{\lambda\ln(q_s/q_d)}{L_{eff}}\right] \quad (22)$$

4.4 PDE and QME correction

The depletion in the polysilicon gate and quantum energy level in the inversion layer result in a reduction of the capacitance and a shift of the threshold voltage, modeling these effects are very important in small dimensional MOSFETs. Gauss's law with the inclusion of the polysilicon depletion effect is written as

$$q_I=V_{GB}-V_{FB}-\left(1+\frac{N_{eff}}{N_g}\right)\phi_s-q_b \quad (23)$$

Following a similar procedure, we obtain the same formulation for inversion charge with different parameters

$$dq_I/q_I+dq_I/n_p=dV_{GB}/n_p-dV_{ch} \quad (24)$$

$$\ln(q_I/n_p)+q_I/n_p=[(V_{GB}-V_{Tp})/n_p-V_{ch}] \quad (25)$$

with $n_P=n+\frac{N_{eff}}{N_g}$ and $V_{T0p}=V_{T0}+2\phi_f\frac{N_{eff}}{N_g}$.

An effective potential method is used to model the quantum effect of MOSFETs. Thus, the channel potential can be expressed as

$$\phi_s=\phi_{s0}-\phi_q \quad (26)$$

The parabolic potential approximation in the substrate gives

$$\phi_q=\lambda_q\phi_{s0}^{2/3} \quad (27)$$

Following the same procedure in treating PDE, the same formulated channel inversion charge is obtained

$$dq_I/q_I+dq_I/n_q=dV_{GB}/n_q-dV_{ch} \quad (28)$$

$$\ln(q_I/n_q)+q_I/n_q=[(V_{GB}-V_{Tq})/n_q-V_{ch}] \quad (29)$$

with

$$n_q=n/\left[1-\frac{2}{3}\lambda_q(2\phi_f)^{-1/3}\right] \text{ and } V_{Tq}=V_{T0}+\lambda_q(2\phi_F)^{2/3} \quad (30)$$

4.5 Source-side injection limit effect and quasi ballistic transport

Recently, the nano-size MOSFETs are fabricated and their performance limit and ballistic transport are reported. In the surface-potential-plus model, the unified current including the source-side inject thermal velocity limit effect and quasi ballistic transport mechanism is developed for nano-scale MOSFETs. The continuity of the channel current gives source-side carrier transport velocity

$$v_{sHD}=I_{ds1}/WC_{ox}V_tq_s \quad (31)$$

In the quasi ballistic transport nano-scale MOSFETs, the source-side carrier velocity is also written

$$v_{sBT}=\frac{1-r}{1+r}v_{th} \quad (32)$$

where v_{th} is the thermal velocity, and r the backscattering coefficient:

$$r=\frac{L_{eff}}{NL_{eff}+\lambda} \qquad (N\geq 3.0) \quad (33)$$

N is a scaling coefficient depending on MOSFET structure and λ is the mean free path parameter.

Effective source-side velocity should be limited by v_{sBT}, thus, its unified equation can be described by:

$$v_{s(eff)}=\frac{v_{sHD}}{\left[1+(v_{sHD}/v_{sBT})^{2M}\right]^{1/2M}} \quad (34)$$

As a result, the unified current with source inject velocity limit and quasi ballistic transport is obtained

$$I_{ds}=\frac{I_{ds1}}{\left[1+(v_{sHD}/v_{sBT})^{2M}\right]^{1/2M}} \quad (35)$$

The surface-potential-plus model embodied with the traditional drift-diffusion, hydrodynamic, and nano-size quasi-ballistic transport is expected to provide extensive flexibility to various advanced technologies and other MOSFET structures, such as SOI and double-gate.

5 RESULTS AND DISCUSISON

The surface-potential-plus MOSFET model ensures a complete symmetry of the source and drain even small

dimensional effects are included through a hierarchical structure consideration. The I-V model was first implemented using BSIMPro's Environment (MDE). The measured data on devices with gate lengths from 0.125um to 10 um are fit with one set of parameters without binning. The results are shown in Figs.3~5. The C-V simulation is related in a simple manner as long as various charges are obtained, thus no demonstration is necessary. One can see from these figures that the presented charge-based MOSFET model shows high fit accuracy and the convincing scalability characteristics.

6 CONCLUSIONS

In this paper, an advanced surface–potential-plus MOSFET model is presented. Various small dimensional effects are discussed and integrated simply into the model framework. The high fit accuracy to measured data and scalability of this model are also originally demonstrated. This surface-potential-plus model has complete symmetry, C_∞ continuity, and more fast simulation speed. This new model is also including DD, HD and QBT mechanisms and is extendable to SOI and double-gate MOSFETs.

REFERENCES

[1]J.R.Brew. Solid State Electron.vol.21, 345-355 1978.

[2]BSIM,http://www.device.eecs.berkeley.edu/~bsim3.

[3]C.Enz,F.Krummenacher, and E.Vittoz. Analog integrated circuits and signal processing. vol.8, 83-114, 1995.

[4]H. Gummel and K.Singhal. IEEE Trans on Electron Devices, vol. 48, 1585-1593, 2001.

[5]C.K.Park,C.Y.Lee,B.J.Moon and Y.H.Byun et al., IEEE Trans Electron Devices, vol.38, 399-406, 1991.

[6]O.C.Gouveia-F,A.I.A.Cunha,.http://www.dolphin.fr.

[7]Y.P.Tsividis, Operation and modeling of the MOS transistor. New York: McGraw-Hill, 1999.

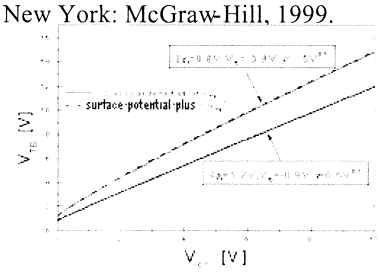

Fig.1 Comparison of the gate-substrate threshold voltage.

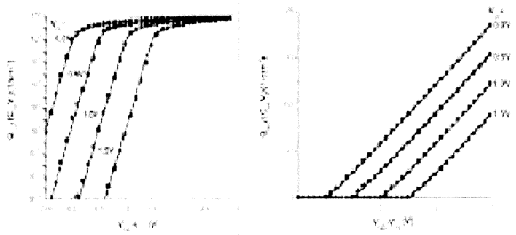

Fig.2 Comparison of obtained inversion charges (Point: numerical; curve: analytical).

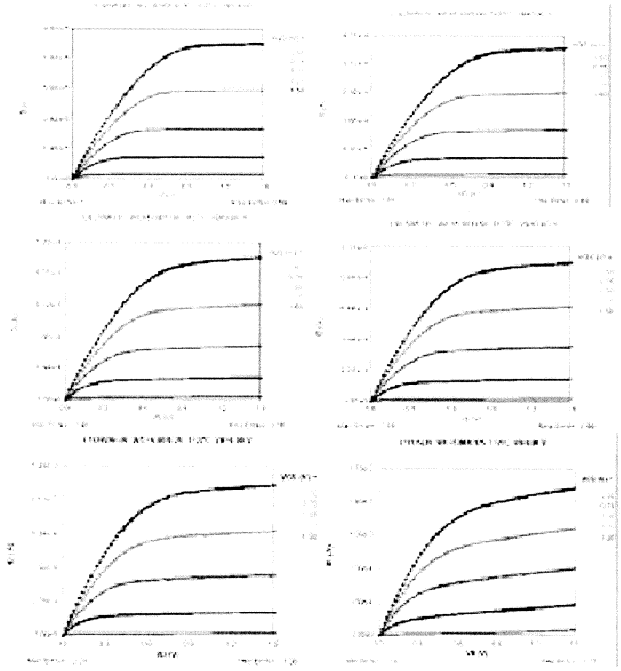

Fig.3 Comparison of Id-Vd curves of simulation and data.

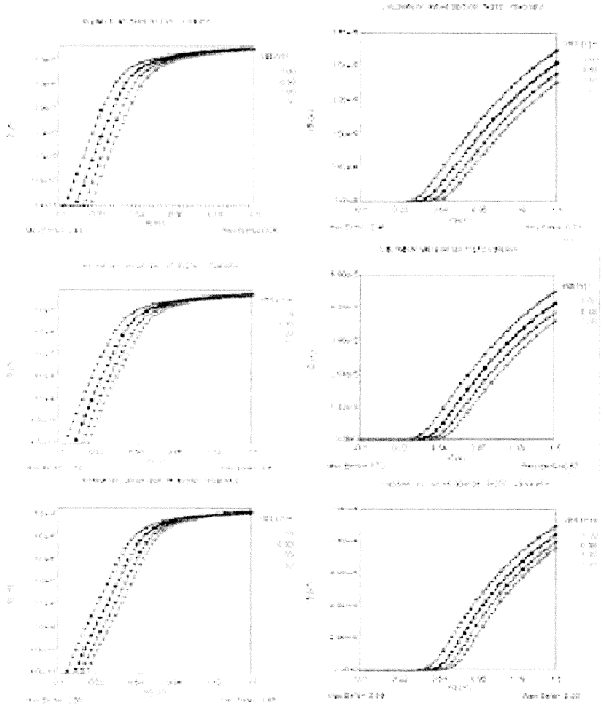

Fig.4 Comparison of Id-Vg curves of simulation and data.

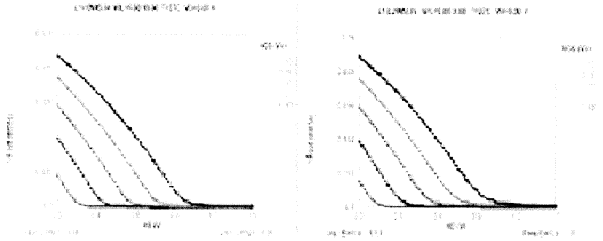

Fig.5 Comparison of Gds curves of simulation and data.