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An Agile Supply Modulator with Improved Transient Performance for Power Efficient Linear Amplifier Employing Envelope Tracking Techniques

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***Abstract*—This paper presents an agile supply modulator with optimal transient performance that includes improvement in rise time, overshoot and settling time for the envelope tracking supply in linear power amplifiers. For this purpose, we propose an on-demand current source module: the bang-bang transient performance enhancer (BBTPE). Its objective is to follow fast variations in input signals with reduced overshoot and settling time without deteriorating the steady-state performance of the buck regulator. The proposed approach enables fast system response through the BBTPE and an accurate steady-state output response through a low switching ripple and power efficient dynamic buck regulator. Fast output response with the help of the added module induces a slower rise of inductor current in the buck converter that further helps the proposed system to reduce both overshoot and settling time. This paper also introduces an efficient selective tracking of envelope signal for linear PAs. To demonstrate the feasibility of the proposed solution, extensive simulations and experimental results from a discrete system are reported. The proposed supply modulator shows 80% improvement in rise time along with 60% reduction in both overshoot and settling time compared to the conventional dynamic buck regulator-based solution. Experimental results using the LTE 16-QAM 5 MHz standard shows improvement of 7.68 dB and 65.1% in ACPR and EVM, respectively.**

***Index Terms*—Bang-bang source, buck converter, buck regulator, dynamic regulator, envelope tracking (ET), fast transient response, overshoot reduction, power amplifier (PA), rise time enhancer, settling time improvement, supply modulator, switching converter, switching regulator.**

I. Introduction

With exponential growth in high-level integration and functional density in portable devices, battery run-time has become an instrumental deciding factor for the consumer electronics market. Due to its significant portion in power consumption, the power amplifier (PA) has become a critical component that determines battery run-time in portable devices. Usually, the PA operates at power back-off (PBO) levels, but its efficiency is low at these frequent power levels [1]. To improve power efficiency at PBO levels, the envelope tracking (ET) technique is favored in literature; the main concept is shown in Fig. 1 [2]–[8]. An ideal envelope tracking method generates a drain voltage which follows the RF output envelope signal with an operational margin to guarantee PA functionality and to optimize PA efficiency. The power efficiency of the entire PA system is the product of PA efficiency and envelope tracking supply modulator efficiency (1) [1], [3], [8]. Here, η_{PA_ET} is the overall system efficiency (including PA and envelope tracking supply modulator) and η_{PA} is the drain efficiency of the power amplifier, and η_{ET_SM} is the efficiency of the envelope tracking supply modulator.

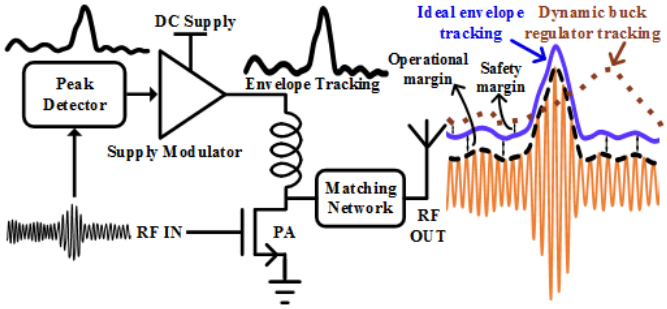

Fig. 1. Envelope tracking technique for RF PAs

$$\eta_{PA\_ET} = \eta_{PA} \cdot \eta_{ET\_SM} \tag{1}$$

According to (1), there is an imperative need for a highly efficient envelope tracking supply modulator for overall system efficiency [3], [9], [10]. Due to high power efficiency, the switching regulator as a supply modulator is preferred in applications where power efficiency is instrumental, e.g., PA systems [1].

For using the regulator with time variant input signals for applications such as envelope tracking systems, the transient response of the regulator determines the envelope's tracking speed. Tracking becomes challenging for high peak-to-average power ratio (PAPR) standards as shown in Fig. 1. Here, a safety margin (V_{SM}) on top of the operational margin is needed to provide room for the voltage ripple and settling error of the

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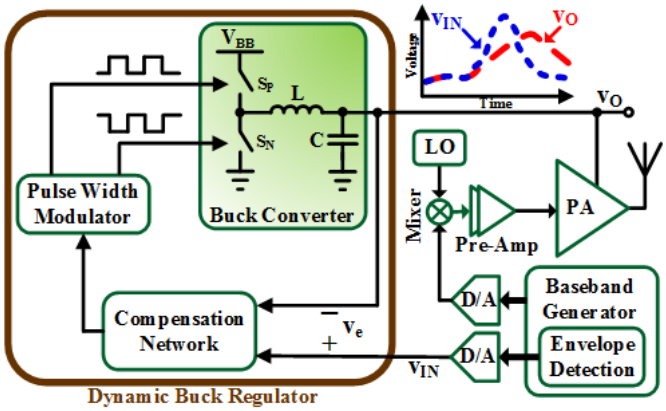

Fig. 2. Dynamic buck regulator as a supply modulator for envelope tracking in the simplified architecture of a wireless transmitter

switching regulator. The dynamic buck regulator may not be able to follow the RF output envelope signal with needed margins (operational and safety) for a high PAPR system with acceptable power efficiency and switching ripple for wideband applications [1], [11], [12]. Due to the limited bandwidth of the dynamic buck regulator, it introduces memory effects in the power amplifier [13]. This significantly reduces the linearity of the power amplifier [14]. To mitigate the memory effect, the digital predistortion (DPD) comes with huge implementation complexities [15]–[17]. An agile supply modulator is required to accommodate wide band standards. As shown in Table I, the bandwidth of envelope tracking increases with modulation bandwidth, which becomes challenging for a power efficient implementation [1].

Several techniques have been proposed for high-speed supply modulators including buck, buck-boost, and several combinations of linear with switching amplifiers [2]–[12], [18]–[22]. However, considering the high bandwidth of modern wireless standards, the needed high switching frequency penalizes the efficiency of the converter. Compared to a two-phase buck converter, the three-level buck converter solution provides higher bandwidth and smaller current ripple but with higher conduction loss [23]. To provide highly efficient envelope tracking along with high bandwidth, a switching amplifier with a linear regulator is proposed in [2]–[10], [24]–[29]. The combination has shown good results but comes with increased complexities of control and synchronization [30]. The power efficiency of the combined system might be limited due to poor power efficiency of the linear regulator. Improvement in supply modulator transient response has also been achieved with the help of different compensation networks and switching control solutions [31]–[34]. Some off-chip solutions for improving transient responses of the switching regulator include the use of an auxiliary transformer, inductor, capacitor, diode and higher order filters [23], [35]–[42]. However, it is not practical to have excessive off-chip components in a system where area and cost effectiveness are essential. Hence, in existing work regarding envelope tracking techniques, the tradeoffs are present to provide higher efficiency, wider bandwidth and less complexity. In addition, overshoot has also become an issue due to the downside trend of breakdown voltage in the CMOS technology nodes. The modulator settling time is also an important parameter for proper management of data in highly demanding wireless standards [32].

TABLE I
ET BANDWIDTH FOR DIFFERENT MODULATION SCHEMES

Ref.	Modulation	ET Bandwidth
[1]	CDMA IS-95 1.25 MHz	5 MHz
[3]	LTE 16-QAM 5 MHz 7.5 dB PAPR	50 MHz
[4]	LTE 16-QAM 10 MHz 6.44 dB PAPR	72.9 MHz/53.8 MHz

In this paper, an agile supply modulator, the bang-bang transient performance enhancer (BBTPE) with a dynamic buck regulator are proposed for envelope tracking purpose in linear PA systems [43]. Here, the approach is to manage slow varying components of an input envelope signal with a power-efficient dynamic buck regulator, and thereby enable BBTPE for fast varying envelope components. The approach alleviates the problem of the transient response of a dynamic buck regulator in terms of rise time, overshoot and settling time. Moreover, to facilitate efficient envelope tracking, the solution presents selective tracking of the envelope signal, wherein the BBTPE helps only in tracking the rising edge of the envelope signal with enough safety margin. With respect to linear amplifier-based approaches, the proposed solution differs in terms of accuracy of tracking and selective tracking, and provides a power efficient solution. This work contributes towards

- Study on the tradeoffs among switching ripple, switching frequency and rise time.
- Study the correlation between overshoot and settling time with rise time improvement.
- Detailed analysis of regions of operation for dynamic buck regulator.
- Demonstration of feasibility of proposed solution via simulation and measurement from low-frequency and RF-frequency prototypes.

The organization of this paper is as follows. In Section II, envelope tracking with dynamic buck regulator is described along with its regions of operation and design tradeoffs. Section III deals with theoretical aspects of the proposed agile supply modulator architecture. In Section IV, system architecture, implementation, simulation and experimental results are discussed. Finally, conclusions are drawn in Section V.

II. Envelope Tracking With Dynamic Buck Regulator

A. Description of Dynamic Buck Regulator as an Envelope Tracker

A simplified architecture of the dynamic buck regulator as an envelope tracker in a wireless transmitter is shown in Fig. 2. The regulator is comprised of switches (S_P and S_N), an LC network along with compensation network to ensure loop stability and steady-state precision, and a pulse width modulator (PWM) [44]. The PA can be modeled as a load impedance Z_L [18]. In this work, the input/reference signal v_{IN} stands for the predicted RF output envelope signal added with

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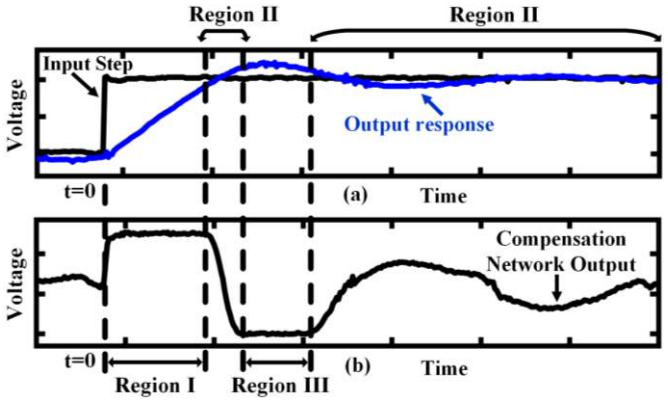

Fig. 3. Typical measured step response (three regions of operation) of dynamic buck regulator with underdamped loop (a) input voltage and output voltage vs. time, and (b) compensation network output voltage vs. time

operational and safety margins. Here, the dynamic buck regulator is also referred as a conventional solution for envelope tracking.

B. Transient Response: Regions of Operation and Design Tradeoffs

Realization of the regulator intended to serve as an envelope tracking supply modulator comes with the design goals of minimizing switching ripple, overshoot, rise time and settling time, as well as maximizing system power efficiency. The optimization procedure of transient and quasi-steady state performance is not evident since, on one hand, the loop must be agile to track fast and large input signals, but on the other hand, switching ripple and regulator losses must be maintained within specifications. To highlight the design tradeoffs, let us consider the step response of the dynamic buck regulator. For this, the following constraint about compensation network (shown in Fig. 2) will be considered.

The compensation network is used to stabilize the loop, and it presents large low-frequency gain with at least one pole at low-frequency, compensating zeros properly located to stabilize the regulator loop, and high frequency poles to attenuate high frequency noise. The compensation network usually has a large bandwidth with three main poles and two zeros. Due to the loop's high low-frequency gain and the low bandwidth of the LC filter, the compensation network output saturates if the error signal is large. If that happens, the feedback loop of the regulator is broken, and the LC network operates in an open loop.

To facilitate the analysis, let us assume that initially the buck regulator is in a quasi-steady state. Fig. 3 shows an example of the input step response of the dynamic buck regulator with an underdamped loop, which corresponds to light load conditions and high loop gain. The different regions of operation during the step response are described as follows.

1) Region I

A large positive input step generates an instantaneous large error signal v_e, i.e., $v_{IN} - v_O \gg 0$ or $v_O \ll v_{IN}$. This further moves the active compensation network out of the linear region to the saturation region due to its large gain and wide bandwidth and keeps raising the output voltage v_O towards the

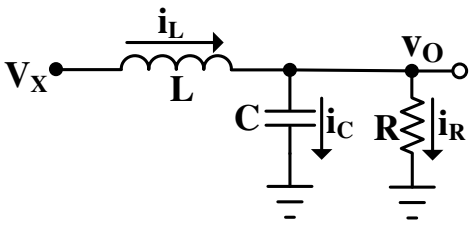

Fig. 4. Configuration of dynamic buck regulator for Region I ($V_X = V_{BB}$) and Region III (V_X = GND)

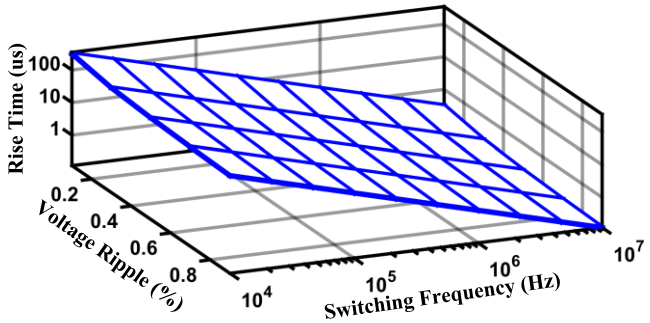

Fig. 5. Rise time versus voltage ripple and switching frequency

input signal as shown in Fig. 3. The output of the compensation network through PWM causes the top switch (S_P) to close and the bottom switch (S_N) to open (Fig. 2). The equivalent circuit driving the output is depicted in Fig. 4 with $V_x = V_{BB}$, where V_{BB} is the battery voltage. In other words, to move the output voltage v_O upwards, i.e., towards input voltage (v_{IN}), the V_x node needs to be connected to the V_{BB}. For this, the top switch (S_P) needs to be turned on, and the bottom switch (S_N) needs to be turned off. To simplify the analysis, the PA is modeled as a resistive load (R). On average, the current in the inductor is set by the current demanded by load R. Since loop gain is large in a quasi-steady state operation and assuming the voltage ripple is small, the output voltage v_O is set to input voltage v_{IN} before occurrence of the input step (from $v_{IN}(0)$ to $v_{IN,F}$). Therefore, the initial conditions in the inductor and capacitor are: $i_L(0) = v_O(0)/R$, and $v_O(0) = v_{IN}(0)$. After the input step is applied and if the compensation network is saturated, then the output voltage $v_O(t)$ is expressed by (2) for $v_O(0) \le v_O(t) \le v_{O,F}$ and $R \neq (L/4C)^{0.5}$ [45].

$$v_O(t) = V_{BB}\left(\frac{s_2 e^{s_1 t} - s_1 e^{s_2 t}}{s_1 - s_2} + 1\right) - v_O(0)\left(\frac{s_2 e^{s_1 t} - s_1 e^{s_2 t}}{s_1 - s_2} + \frac{e^{s_1 t} - e^{s_2 t}}{RC(s_1 - s_2)}\right) + \frac{i_L(0)}{C(s_1 - s_2)}\left(e^{s_1 t} - e^{s_2 t}\right). \quad (2)$$

In (2), $s_{1,2}$ are the roots of the characteristic equation given by $-(1/2RC) \pm \sqrt{(1/2RC)^2 - (1/LC)}$, whereupon $v_{O,F}$ is the final steady-state output voltage. With the help of (2), the response of the regulator to fast transitions in the input envelope signal from the back-off level to the peak power level is characterized by the rise time (t_{rise}). Due to the

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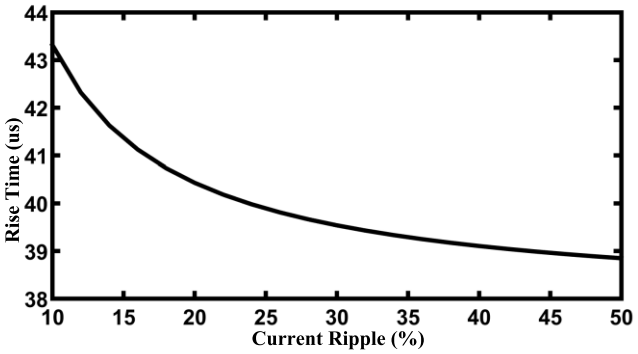

Fig. 6. Output voltage rise time versus current ripple for 0.25% voltage ripple, 50 kHz switching frequency

complexity of the solution for output voltage $v_O(t)$ in (2), the explicit solution for the rise time is even more complex, which makes it difficult to get any insight. Therefore, a numeric solver is used to find the value of t_{rise} from (2) for given parameters. Before discussing the results, let us replace L and C in (2) by the peak voltage ripple (Δv_O), peak inductor current ripple (Δi_L) and switching frequency (f_{sw}) with the help of (3) and (4) so that tradeoffs among different

$$\Delta v_O = \frac{(1-D)V_O}{16LCf_{sw}^2} \tag{3}$$

$$\Delta i_L = \frac{R(1-D)I_L}{2Lf_{sw}} \tag{4}$$

performances and design parameters can be discussed [44].

In (3) and (4), $D(= V_O/V_{BB})$ represents the duty cycle, V_O is the average output voltage in quasi steady state, and I_L is the average inductor current. Here, rise time (t_{rise}) is assessed by measuring the 10% to 90% rise of the regulator output voltage. For an input step of 0.5 V–1.5 V and battery voltage V_{BB} of 4.4 V, the rise time versus voltage ripple, and switching frequency is plotted in Fig. 5 for 15% inductor current ripple, and the load impedance of 1 Ω. The analysis does not include switch S_P resistance or its turn-on time, which further worsens output voltage rise time.

As shown in Fig. 5, increment of voltage ripple, keeping fixed switching frequency and current ripple, slightly decreases the regulator's rise time. This can also be analyzed as the increment in voltage ripple allows a decrease in capacitance of the *LC* tank, thereby moving the roots of characteristic equation away from imaginary axis on left hand-side (LHS) side of s-plane i.e. increasing the speed of response. However, voltage ripple is constrained by the safety margin hence efficiency of the system. The rise time also decreases with increment in switching frequency at fixed voltage and current ripple. These conditions from using (3) and (4) require a decrease in both *L* and *C,* which are inversely proportional to the switching frequency increment thereby increasing the bandwidth. However, increment in switching frequency causes higher switching losses; therefore, this approach is limited by the power efficiency of the buck converter.

As shown in Fig. 6, rise time decreases with increment in current ripple for given voltage ripple and switching frequency. Equations (3) and (4) suggest that this can be achieved by decreasing the inductance, which increases the modulator's bandwidth. However, current ripple is constrained by the current limit of the inductor and semiconductor devices. Therefore, maximum allowed values of voltage ripple, current ripple and switching frequency—all serve to constrain output voltage rise time.

2) Region II

When the regulator's output voltage approaches the input voltage, the error voltage decreases, $|v_e| \approx 0$ and forces the compensation network to enter into its linear region (Region II) as shown in Fig. 3, which again enables the linear operation of the regulator loop. The system configuration for this region is shown as a dynamic buck regulator in Fig. 2. In this stage, if the inductor current is close to the current demanded by the load, and the loop damping factor is not quite small enough, the regulator's output voltage smoothly settles down depending upon linearized response of the loop, i.e., transfer function as shown in (5)

$$H(s) = \frac{V_O(s)}{V_{IN}(s)} = \frac{H_{comp}(s)H_{PWM}(s)H_P(s)}{1 + H_{comp}(s)H_{PWM}(s)H_P(s)} \tag{5}$$

where $H_{comp}(s)$ is the transfer function of the compensation network. $H_{PWM}(s)$ is the equivalent transfer function of the pulse width modulator $(= 1/V_M)$, where V_M is the peak-to-peak amplitude of the sawtooth waveform [44]. $H_P(s)$ is the transfer function of the power stage that contains the LC filter along with load (R), which is equal to $V_{BB}/(s^2LC + sL/R + 1)$ [45].

If the inductor current in this region is excessive (i.e., underdamped *RLC* network), the output voltage moves further away from the input voltage; then, the regulator enters into Region III as shown in Fig. 3.

3) Region III

In this region, at the starting point, the output voltage increases due to excessive inductor current, and generates an instantaneous large error signal $|v_e|$, i.e., $v_{IN} - v_O \ll 0$ or $v_O \gg v_{IN}$. This again saturates the compensation network as shown in Fig. 3. Through PWM, it closes switch S_N and opens switch S_P as depicted in Fig. 4 with V_x = GND. In other words, to move the output voltage v_O downwards, i.e., towards input voltage (v_{IN}), the V_x node needs to be connected to the ground. In order to have $V_x = GND$, the top switch (S_P) needs to be opened and the bottom switch (S_N) needs to be closed. The governing equation of the output voltage, the inductor current and load current for this region can be derived from (2) by substituting $V_{BB} = 0$ and corresponding initial conditions. In this region, the inductor current starts decreasing until it reaches the value of the load current, which creates a maxima condition for output voltage $v_O(t)$. Hence, the overshoot of the output voltage occurs in this region. The value of the overshoot depends upon the dynamics of the region and its

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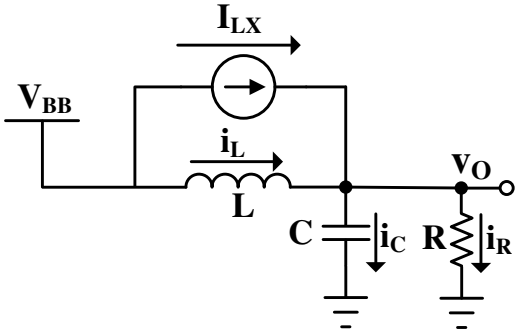

Fig. 7. Conceptual schematic for manipulation of initial inductor current during Region I in proposed solution

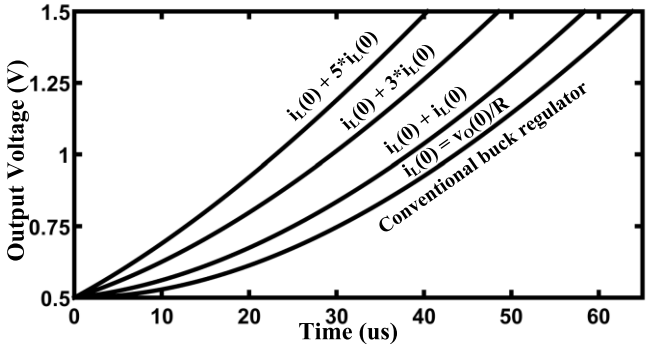

Fig. 8. Output voltage during rise time (Region I) vs. time for different initial inductor current with input step of 0.5 V to 1.5 V

initial conditions. The damping factor (ξ) of the LCR network shown in Fig. 4 increases with increments in inductance value, which decreases the overshoot [44]. However, (4) indicates that it also decreases current ripple, which worsens rise time during Region I as shown in Fig. 6. The damping factor can also be increased by decreasing capacitance; however, (3) suggests that it also increases voltage ripple.

Therefore, Region I is mainly responsible for rise time. The existing tradeoffs makes it infeasible for a dynamic buck regulator to manage specifications of instrumental performance parameters like switching ripple and power efficiency, along with needed rise time. Furthermore, Region III is responsible for overshoot, while final settling depends on loop dynamics in Region II. In the current work, without loss of generality, it is assumed that the input step puts the regulator system into region transitions I → II → III → II before it settles down. For large overshoot cases, Region II operation between Region I and III can be ignored; hence, overall movement of the regions is simplified to I → III → II.

III. Agile Supply Modulator

Most modern wireless standards require PAPR over 12 dB; this sometimes can be clipped within linearity specifications up to a PAPR of 7~8 dB depending upon the standard. Furthermore, the peak of probability density function of transmitter power is around the PBO region, which means that most of the time, the signal is around 25% of the peak value [1], [45]. Due to PDF distribution, a sharp transition in the envelope signal from PBO to the peak power region is not frequent. However, these conditions have to be properly managed by both the PA and supply modulator to avoid distortion. Furthermore, increasing the switching frequency of the dynamic buck regulator (as suggested in Fig. 5) for managing fast signal transition, which has a low probability of occurrence, is not a power-efficient approach. The proposed solution takes advantage of this property.

A. Core Concept of the Proposed Solution

According to (2), with the exception of the passive elements, output voltage, and hence, the subsequent rise time, is a function of battery voltage V_{BB}, initial output voltage $v_O(0)$, and initial inductor current $i_L(0)$.

$$v_O(t) = \frac{e^{-\frac{t-t_3}{2RC}}}{\omega_d}\Big(v_O(t_3)\Big\{-\frac{1}{2RC}\sin\big(\omega_d(t-t_3)\big) + \omega_d\cos\big(\omega_d(t-t_3)\big)\Big\} + \frac{i_L(t_3)}{C}\sin\big(\omega_d(t-t_3)\big)\Big). \quad (6)$$

An intuition about the impact of these parameters on the average speed of an output signal can be realized using a circuit configuration as shown in Fig. 4; in which an increment of V_{BB} increases the voltage difference across inductor L; hence the inductor provides more current during rise time, which increases output voltage speed. On the other hand, the increment of $v_O(0)$ decreases the voltage drop across inductor $(V_X - v_O)$, thereby decreasing the inductor current. The increment of $i_L(0)$ also enhances rise time by providing more current to capacitor C and load R. In these parameters, $v_O(0)$ is determined by the initial condition of the input signal. Additionally, V_{BB} is a technology-constrained parameter, so it cannot be manipulated. Similarly, the initial inductance current $i_L(0)$ is determined by the average current demanded by the load before the transient. One of the main reasons for the limited rise time of output voltage is the slow change in inductor current, which is dictated by the integral of the voltage difference across its terminals and its inductance value. *The proposed technique is based on the manipulation of the current injection to the load that emulates the effect of the higher initial inductor current when needed* as shown in the conceptual diagram of Fig. 7. The auxiliary current source (I_{LX}) is placed parallel to the inductor, and represents the manipulation in the initial inductor current while the system operates in Region I. The output voltage for this region is expressed as (2) by adding the I_{LX} term with $i_L(0)$ in the last term. Fig. 8 shows the modulator output voltage versus time for I_{LX} variation by 0, 100%, 300% and 500% of the initial inductor current $i_L(0)$ for Region I. The figure shows that output voltage is raising faster due to the contribution of I_{LX}. As shown in Fig. 8, $I_{LX} = 5 \cdot i_L(0)$ reduces rise time by a factor of 1.5 for the considered test configuration. The figure of improvement in rise time becomes more pronounced for an overdamped system, and mostly driven by I_{LX}/C when the current of the auxiliary current source exceeds the inductor current.

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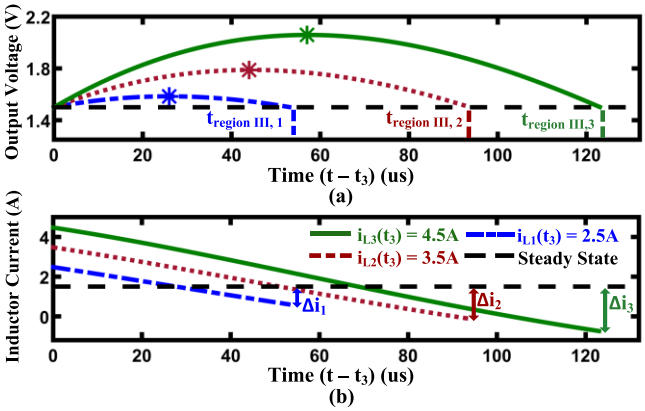

Fig. 9. Region III waveform for different initial inductor currents (4.5 A, 3.5 A, and 2.5 A) (a) output voltage vs. time and (b) inductor current vs. time

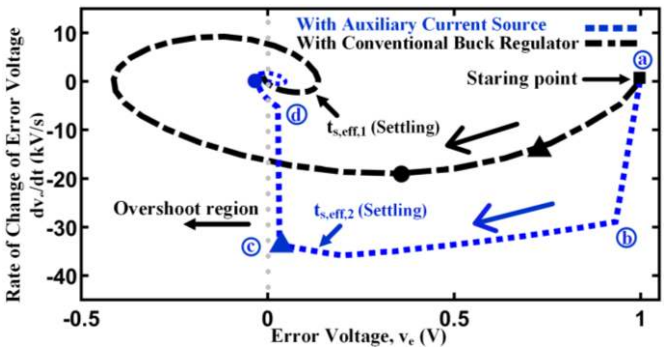

Fig. 10. Rate of error voltage vs error voltage of a simulated system with and without auxiliary current source I_{LX} (4A) in Region I with input signal step from 0.5 V to 1.5 V for buck converter designed with L = 45.2 µH, C = 142.5 µF, R = 1 Ω and V_{BB} = 4.4 V at 50 kHz switching frequency. Here, time mapping symbols ■,▲,●, ts,eff,1, and ts,eff,2 represent 0, 30, 50, 250 and 27 µs respectively.

B. Overshoot, Settling Time and Power Efficiency

During Region I, the auxiliary current source I_{LX} helps to increase output voltage v_O faster than that with the conventional dynamic buck regulator-solution. This decreases the voltage difference across inductor Δv_L more quickly and reduces the time spent in Region I ($t_{region\ I}$) in comparison to the conventional solution. It leads to a decrease in the excessive rising current in the inductor during Region I.

After Region I, the system enters into Region III, ignoring interim Region II since it is a reasonable assumption for high overshoot cases. Thus, the initial inductor current for Region III is smaller for the regulator having an auxiliary current source (I_{LX} during Region I) than that for the conventional dynamic buck regulator. Since I_{LX} is only used in Region I, system configuration for Region III is the same as that of the dynamic buck regulator shown in Fig. 4 with V_X = GND. Considering the worst case for overshoot and settling time, which occurs in underdamped configurations of the *LCR* network, i.e., $R > (L/4C)^{0.5}$, the governing equation of the output voltage for Region III, i.e., $v_O(t) > v_{O,F}$, which starts at $t = t_3$ is shown in (6), which is derived from (2) by removing the V_{BB} terms as for this region $V_x = GND$. Here, the ringing frequency ω_d is $\sqrt{(1/LC) - (1/2RC)^2}$. The equation is plotted for different values of the initial inductor current $i_L(t_3)$ in Fig. 9a. The figure shows that overshoot increases with increment in the initial inductor current $i_L(t_3)$. Intuition for this comes from its last term, which is $(i_L(t_3)/C) * \sin(\omega_d(t - t_3))$, as its amplitude is increasing with $i_L(t_3)$, i.e., increasing overshoot. Therefore, in accordance with these results, it is evident that the dynamic buck regulator with an auxiliary current source during Region I has a smaller overshoot than that in case of the conventional dynamic buck regulator due to the smaller inductor current at the end of the Region I. It means lesser voltage stress on the devices connected at output node for the system having auxiliary current source in Region I.

Comparison of settling time can be done region wise; i.e., input step transition to output steady state that includes region transition from I → III → II, assuming only these transitions are needed to settle down the system. Due to the use of I_{LX} in Region I, time spent and inductor current in Region I by the proposed system is less than that in the dynamic buck regulator system. As shown in Fig. 9a, time spent in Region III ($t_{region\ III}$) is higher for the higher value of the initial inductor current; i.e., $t_{region\ III,3} > t_{region\ III,2} > t_{region\ III,1}$ for $i_{L3}(t_3) > i_{L2}(t_3) > i_{L1}(t_3)$. This shows that time spent in Region III is smaller for the proposed system than that spent in the dynamic buck regulator system.

TABLE II
$t_{s,eff}$ AND V_{ov} VARIATION WITH AUXILIARY CURRENT

$\frac{I_{LX}}{i_L(0)}$	$\frac{t_{s,eff}}{t_{s,eff,conventional}}$	$\frac{V_{ov}}{V_{ov,conventional}}$
0 (conventional system)	1	1
1	0.94	0.83
3	0.17	0.54
5	0.14	0.16

The inductor current during Region III for $R > (L/4C)^{0.5}$ can be obtained from adding a capacitor current and load current of the circuit shown in Fig. 4 [45]. It is plotted for different values of initial inductor current $i_L(t_3)$ in Fig. 9b. At the end of Region III, the figure shows that initial deviation of inductor current from steady state for Region II increases with increment in the initial inductor current in Region III, i.e., $\Delta i_3 > \Delta i_2 > \Delta i_1$ for $i_{L3}(t_3) > i_{L2}(t_3) > i_{L1}(t_3)$. Therefore, settling time in Region II is smaller for the proposed solution than that for the dynamic buck regulator because the conventional regulator starts with a higher deviation in the inductor current. Consequently, settling time in the case of a proposed agile supply modulator is smaller than that in the conventional solution.

Even though settling time is improved in the proposed solution, the key issue is that the linear PA drain voltage must be greater than the minimum required voltage to stay in its linear operation. The time needed to make a linear PA operational is estimated by the time after which the modulator output voltage is greater than the minimum needed PA drain voltage, i.e., $v_{IN} - v_O \leq V_{SM}$, which is the effective settling time for linear PAs ($t_{s,eff}$). Table II shows that both effective settling time $t_{s,eff}$ and overshoot voltage (V_{ov}) decrease with increment in I_{LX} for V_{SM} 50 mV. As soon as the voltage

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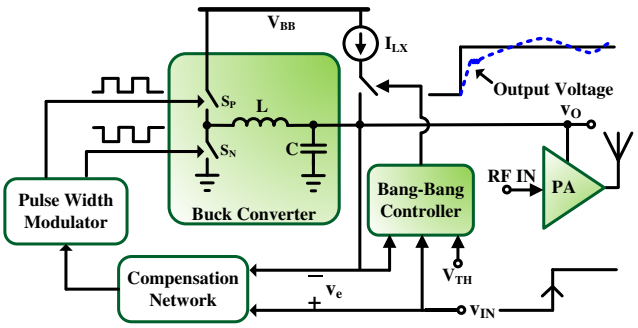

Fig. 11. Proposed agile supply modulator architecture for envelope tracking

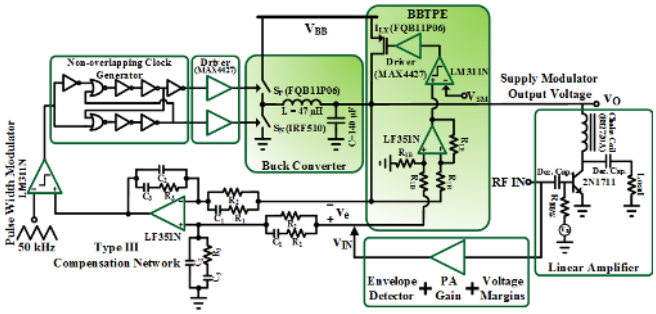

Fig. 12. Low-Frequency Discrete Implementation Setup

undershoot becomes smaller than V_{SM}, the $t_{s,eff}$ moves to Region I and decreases drastically as shown in the table.

The discussed reduction in overshoot and the effective settling time is illustrated with the help of the phase portraits displayed in Fig. 10, which show the rate of change of the error voltage, dv_e/dt vs. error voltage v_e, for an input step from 0.5 V to 1.5 V. It is developed with the derivative function and interchanges of axes of time-domain waveforms. As shown, the auxiliary source is turning on from point (a) to (b); the error voltage does not change immediately, but it drastically increases the rate of change of error. From (b) to (c), it quickly decreases error voltage v_e. After assisting the output voltage by quickly reducing the error signal, i.e., $|v_e| \approx 0$, the auxiliary current source I_{LX} turns off, which results in the jump from (c) to (d). After that, the velocity of the error signal decreases since it is managed by the inductor current only, which leads to a softer convergence towards its final steady state. For corresponding time instances (■▲●), the conventional system shows more error voltage than that in proposed system as shown in Fig. 10. In this case, simulation results show reduction in both voltage overshoot and effective settling time for about 90%.

Impact of the auxiliary current source on the modulator's power efficiency depends upon the input signal slew rate. If the input signal slew rate is within the buck regulator's tracking speed, the auxiliary source is not activated, and the power efficiency will be governed by the regulator itself. Furthermore, in modern modulation schemes, the transition from PBO to the peak power level is not frequent, so the power delivered by the auxiliary current source will be minimal compared with the average modulator's output power.

IV. System Architecture, Implementation, and Experimental Results

A. System Architecture

The auxiliary switchable current source I_{LX} can be treated as an addendum in the system beside the dynamic buck regulator during Region I. For this purpose, a fast threshold voltage detector (bang-bang controller) that monitors the error signal v_e is used in the proposed agile supply modulator architecture as shown in Fig. 11. It activates the switchable current source I_{LX} if the aforementioned error signal v_e is larger than the predefined safety margin voltage V_{SM} in Region I. As a consequence, the auxiliary switchable current source I_{LX} works as a bang-bang (ON-OFF) current source (BBCS) because it is activated only when the error voltage is greater than V_{SM}. Because the added BBCS along with its controller enhances the transient performance of the proposed agile supply modulator, it is referred to as a bang-bang transient performance enhancer (BBTPE). The value of I_{LX} is decided based upon the worst needed rise time for the envelope signal. This allows to use a constant auxiliary source for the complete envelope signal for the selected wireless standard. In addition, the value of V_{SM} is the allowed safety margin between the input voltage and modulator output voltage; it limits BBCS operation. The margin must be greater than the voltage ripple Δv_0 along with a settling error of the dynamic buck regulator so that a minimum steady state output voltage is greater than the minimum drain supply needed for PA to be operational. In addition, a delay by the bang-bang controller in disabling the BBCS will impact efficiency, but not PA linearity. Although a simple threshold detector is used in this prototype, more complex algorithms can be used, which may even consider the use of a predictor to anticipate fast input signal variations that can activate the BBCS in advance.

The added module BBTPE helps the dynamic buck regulator to only follow the rising edge of the envelope signal for linear PAs. During the sharp falling edge, the response of the proposed agile modulator is identical to that of a conventional modulator. *For a linear PA, the drain voltage only needs to be large enough to maintain its functionality; it does not need to follow the envelope signal during the input falling edge.* In this case, the system uses the stored energy of the inductor and capacitor accumulated during the preceding operation. Moreover, in order to track the falling edge of the input signal (envelope signal), the stored energy in the capacitor and inductor of the buck converter needs to be depleted, which results in the loss of efficiency for the system (supply modulator and power amplifier) because the energy was already taken from the supply during the rising edge of the input signal and stored in the inductor and capacitor. *The best solution in the case of linear PAs, that are low sensitive to drain voltage variations, is to keep the additional energy stored in the inductor and capacitor and let the PA to use it*. The result is that during fast falling variations, the drain voltage remains higher than minimum needed voltage headroom for its operation. Therefore, selective tracking is an efficient and simplified approach without affecting the linear PA's functionality.

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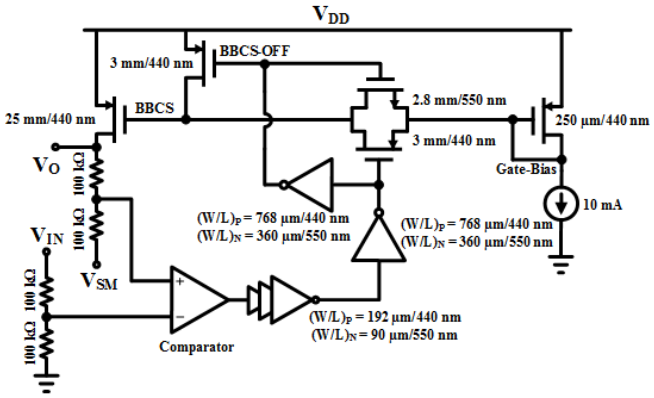

Fig. 13. BBTPE Circuit

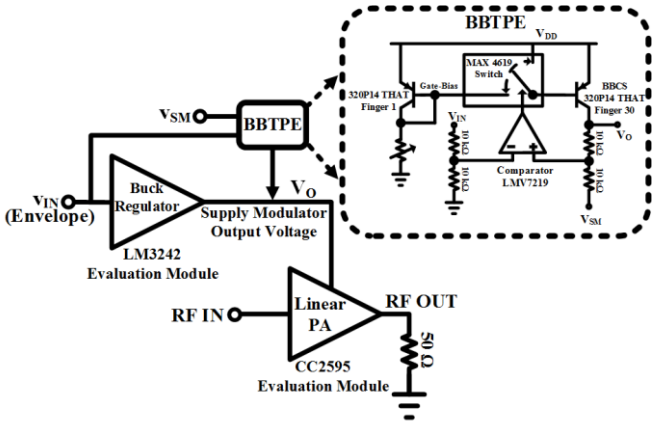

Fig. 14. RF Frequency Implementation Setup

B. A Low-Frequency System Implementation and Setup

In order to verify the proposed supply modulator, a discrete components-based prototype was designed as proof of concept. Due to the limitation of the frequency response of discrete components, the frequency of operation was limited to 50 kHz in system testing. The discrete implementation setup of the employed system is shown in Fig. 12. The dynamic buck regulator was designed for 15% of the current ripple and 0.25% of the voltage ripple with a switching frequency of 50 kHz, and a loop bandwidth of 7.9 kHz. LC's Corner frequency was used at 1.96 kHz using $\mathrm{L} = 47\ \mu\mathrm{H}$ and $\mathrm{C} = 140\ \mu\mathrm{F}$. A Type III compensation network was designed to provide high low-frequency gain and stability with poles at 0, 50 kHz, and 100 kHz, and two zeros around 2.7 kHz. Furthermore, the switches S_P and S_N were realized with FQB11P06 and IRF510, respectively. The driver of these switches was designed using MAX4427. The PWM modulator employs a 50 kHz clock frequency. The non-overlapping clock circuit for the present system is a typical circuit as shown in Fig. 12. In this implementation, BBTPE has three modules: an error signal generator, a bang-bang controller, and the BBCS. The error signal generator was implemented with the help of an op-amp based subtractor, and the controller was realized employing a conventional voltage comparator. In the present prototype version, the BBCS is implemented with a single PMOS device (FQB11P06). To maintain it as a current source, voltage levels at the gate, drain, and source of the device are managed such that the device is in the saturation region while operating in Region I. The PA was modeled as a resistive load to the modulator. For linearity testing, a linear amplifier is used as a load to the supply modulator as shown in Fig. 12. Here, the envelope detector was realized using a textbook circuit employing an opamp, diode, and resistor.

C. RF-Frequency System Implementation and Simulation Setup

To justify achievable modulation speed with the presented approach, the proposed supply modulator was also designed using TSMC 40nm and tested with 16-QAM LTE standard which has a bandwidth of 5 MHz at carrier frequency of 2.4 GHz. In the circuit implementation, a dynamic buck regulator with conventional architecture consists of a compensation network, a PWM, a non-overlapping clock circuit, switches, and its driver along with an inductor and a capacitor. A typical folded-cascode opamp was used in the compensation network. The compensation network, which was Type III, had zeros at 0.16 and 0.18 MHz, and poles at 0, 3.3, and 6.7 MHz. The size of the switches S_P and S_N were 40.55 mm/460 nm and 13.98 mm/550 nm, respectively. The inductor and capacitor values are 69.6 µH, and 21.12 nF, respectively. The dc gain, unity gain frequency, and phase margin of the regulator loop were 53 dB, 0.8 MHz and 60º, respectively. The PWM clock frequency was set at 4 MHz. The frequency was decided based on the common design practice of keeping the switching frequency around 5-10 times away from the unity gain frequency of the dynamic buck regulator loop [1], [44]. However, as discussed in Section II, the higher value of the switching frequency comes with the lower power efficiency of the dynamic buck regulator. Hence, the switching frequency was kept at the lower side of the suggested range. The circuit diagram of BBTPE is shown in Fig. 13. Here, the delay of the comparator and inverter are in the range of 0.42 ns and 0.11 ns, respectively. In addition, the transition time of the transmission gate is in the range of 0.24 ns. In the circuit, the comparator compares input voltage v_{IN} and output voltage v_O along with safety margin (V_{SM}) with the help of a resistive adder. If the difference between output voltage and input voltage, i.e., error voltage is greater than V_{SM}, then, the transmission gate gets enabled and it biases BBCS with a generated gate-bias. Furthermore, if the error voltage is below the safety margin; then, the BBCS-OFF transistor gets enabled and the switch-off BBCS. Due to the dynamic nature of the OFDM signal, the need for a hysteresis comparator was not observed. However, frequent switching of BBCS can be reduced to some extent with the adoption of a hysteresis comparator. The used supply for the BBTPE was 3.3 V. The slew rate of the BBTPE needs to be faster than that of the envelope signal to meet a particular standard. For a 25 dBm output power, the slew rate of the envelope peak transition is ~13 V/us which is much faster for the rest all other time constants embedded in the dynamic buck regulator; the BBTPE shows the slew rate of 15.4 V/us.

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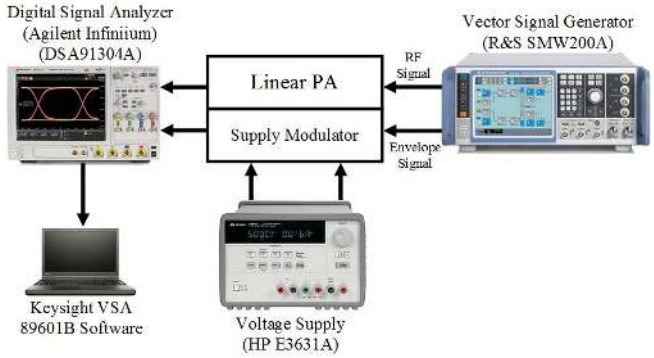

Fig. 15. RF Frequency Measurement Setup

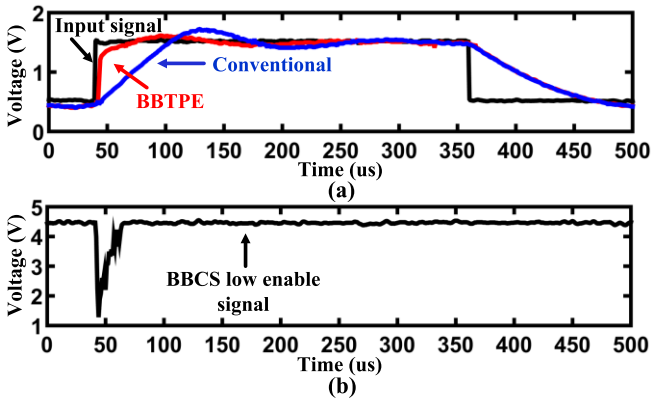

Fig. 16. Measured response of supply modulator for rectangular wave input signal (a.) input signal, output with and without BBTPE and (b.) BBCS low enable signal

TABLE III
RF FREQUENCY DISCRETE IMPLEMENTATION SETUP PART#

Blocks		Part#
	Linear PA	CC2595 Evaluation Module
	Buck Regulator	LM3242 Evaluation Module
BBTPE	Comparator	LMV7219
	Switch	MAX 4619
	BBCS	320P14 THAT

The linear power amplifier was having a cascode configuration [46]. The sizes of the bottom and cascode transistor were set as 5 µm/60 nm and 20 µm/270 nm, respectively, with 6144 fingers. The effective load to the linear amplifier is 4/3 Ω. The impedance transformation was achieved with the help of a cascaded L-matching network (0.37 nH, 11.25 pF, 1.64 nH and 1.33 pF).

D. RF-Frequency System Implementation and Measurement Setup

An RF-frequency prototype was implemented as a proof of concept. The system was designed for the LTE 16-QAM with 5 MHz bandwidth at the RF frequency of 2.4 GHz. The implemented system setup is shown in Fig. 14. The dynamic buck regulator was implemented using the LM3242 evaluation board which has a PWM frequency of 6 MHz with a 0.5 µH inductance and 0.47 µF capacitance. Here, the PWM clock frequency source is built-in and cannot be directly modified by a user. The linear power amplifier was employed with a CC2595 evaluation board. This is a two-stage power amplifier with an L-type matching network implemented with 1.2 nH inductance and 1.5 pF capacitance. Its supply is connected to

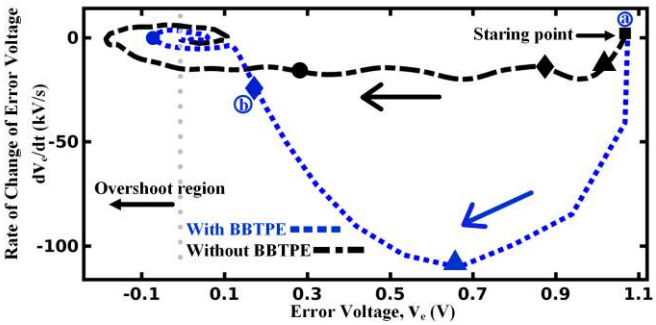

Fig. 17. Measured rate of error voltage vs. error voltage with and without BBTPE. Here, time mapping symbols ■,▲,♦ and ● represent 0, 5, 10 and 49 µs respectively.

TABLE IV
TESTING CONFIGURATION WITH RESISTIVE LOAD IN DISCRETE PROTOTYPE MEASUREMENT

Parameters	Test Case
Input Signal (v_{IN})	1 V_{PP} Square wave at 2 kHz with 1 V offset
Safety Margin Voltage (V_{SM})	100 mV
Closed Loop Dominant Poles	Complex conjugates

the supply modulator via a 12 nH choke inductor. The BBTPE architecture is shown in Fig. 14. In this, the BBCS gets activated when the supply modulator output voltage (v_O) is lower than the input envelope signal v_{IN} by the margin (V_{SM}). It was implemented with the help of a comparator, switch and current source. Here, the comparator's delay is around 7 ns, and the transition time of the switch is around 7.2 ns. In practice, the envelope is generated in a digital domain (baseband processor) and its delay is equated with an in-phase (I) and quadrature (Q) baseband signal [2]. The manual compensation of the delay mismatch between envelope and baseband signals includes visual check in oscilloscope and performance check of both EVM and ACPR in the spectrum analyzer. Besides this, there are several other approaches reported in the literature that include a timing alignment loop to correct the delay mismatch [47]–[49].

The employed component list is given in the Table III. The measurement setup for the discussed system is shown in Fig. 15. Here, VSA 89601B software was used for the measurement of ACPR and EVM. The wireless signal along with its envelope signal was generated with the help of the vector signal generator R&S SMW 200A.

E. Experimental Results for a Low-Frequency Prototype

The system response with and without BBTPE were measured for the test case shown in Table IV. For these tests, the linear amplifier was replaced by a resistive load.

Fig. 16 shows the measured response of a discrete components-based system for the test case having a 50 Ω load and 100 mV V_{SM} with complex conjugates closed loop dominant poles. As shown in Fig. 16a, the output with the BBTPE system is not only faster compared to the conventional system but it also decreases both overshoot and settling time. Here, the BBTPE incorporated modulator showed improvement by a factor of almost five, from 48 µs down to

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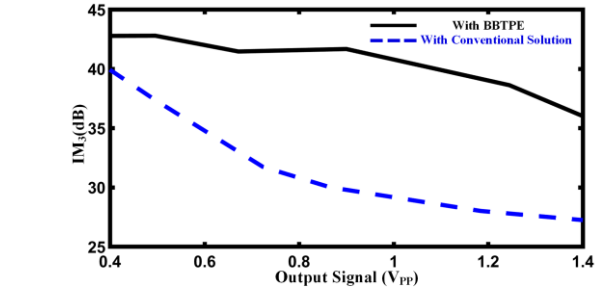

Fig. 18. Measured PA Output IM3 versus Output Signal

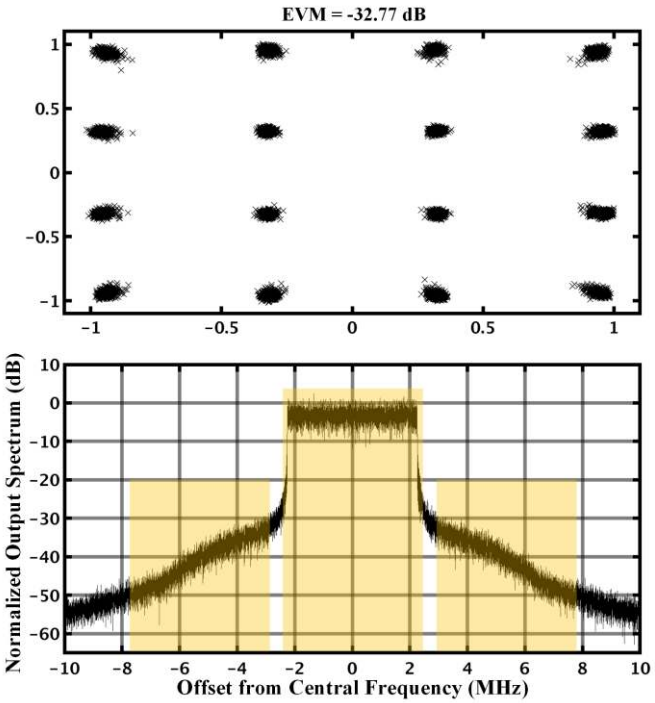

Fig. 19. Simulated EVM and output spectrum for 16-QAM LTE data

TABLE V
t_{rise} AND V_{ov} VARIATION WITH AUXILIARY CURRENT

I_{LX}	t_{rise}(µs)	V_{ov} (mV)
0 (conventional system)	48.0	210
$2*I_{LX0}$	32.0	184
$6*I_{LX0}$	15.7	145
$10*I_{LX0}$	10.0	80

10 µs in rise time. Furthermore, overshoot and 5% settling time were reduced by around 60% from 210 mV and 185 µs down to 80 mV and 72 µs, respectively. Settling time can be further reduced if a smaller safety margin voltage V_{SM} is used (e.g., 50 mV). In the current case, $t_{s,eff}$ is reduced by a factor of 13.7, from 179 µs down to 13 µs. Fig. 16b shows the BBCS low enable signal, which was activated during the rising edge of the input signal. As the error voltage gets closer to the safety margin voltage V_{SM}, the BBCS starts turning off. As shown, when the input signal slew rate is faster than the modulator slew rate, the BBTPE takes care of it, and when the error voltage reaches the safety margin i.e., $v_e \sim V_{SM}$, the BBCS operates like a bang-bang system (on and off) until the inductance current is closer to the current demanded by the load. The measured phase portrait is shown in Fig. 17, which shows the rate of change of the error voltage, dv_e/dt vs. error voltage v_e, for an input step. As shown, the BBTPE is activated from point (a) to (b). With the help of BBTPE, the rate of change of error increases drastically compared to the without BBTPE scenario, which helped to decrease the error voltage quickly. For corresponding time instances (■▲♦●), the BBTPE incorporated modulator showed lesser error voltage than that in the conventional system. The figure also demonstrates the improvement in the overshoot voltage with the help of BBTPE. Table V showed the variation of measured rise time and overshoot voltage with the auxiliary current source. Here, I_{LX0} is 1.1 A. As discussed in Section III, the rise time and the voltage overshoot decrease with the increment in the auxiliary current, I_{LX}. For the measured test case shown in Fig. 16, the auxiliary current source was $10*I_{LX0}$. In addition, the measured rise time versus voltage ripple and switching frequency are shown in Table VI and Table VII, respectively. Here, the rise time decreases with the increment in voltage ripple and switching frequency, which is aligned with the Section II.

TABLE VI
t_{rise} VARIATION WITH VOLTAGE RIPPLE

VOLTAGE RIPPLE (%)	t_{rise}(µs)
0.25	48.0
0.5	31.6
0.75	25.0
1.0	21.2

TABLE VII
t_{rise} VARIATION WITH SWITCHING FREQUENCY

SWITCHING FREQUENCY (kHz)	t_{rise}(µs)
12.5	193
16.6	144
25	96
50	48

To measure the impact of BBTPE on the PA linearity performance, a linear amplifier was used instead of a resistive load as shown in the implementation setup in Fig. 12. The amplifier was built using a 2N1711 with a 120 Ω load, and for testing two tones at 106 and 107 kHz were used. The linearity (IM_3) of the amplifier with a conventional solution and the BBTPE included modulator versus output signal are shown in Fig. 18. Here, we can see that, when the output signal is small, the difference in linearity is also small because the conventional solution was able to track the envelope signal closely. However, as the output signal amplitude increased hence the slew rate of the envelope signal, the conventional solution was not able to track the envelope signal, and its linearity started degrading as shown in the figure. Additionally, the BBTPE incorporated supply modulator was

TABLE VIII
PERFORMANCE COMPARISON WITHOUT AND WITH BBTPE CONFIGURATION

Parameters	Without BBTPE	With BBTPE
ACPR (dB)	-24.42	-32.1
EVM (%)	8.07	2.82
PAE (%)	20	25.3
Modulator Efficiency (%)	83.9	76.1

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TABLE IX
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RESULTS

Ref.	Modulation	Signal BW (MHz)	Frequency (GHz)	PAPR (dB)	Modulator Efficiency (%)	ACPR (dBc)	EVM (%)
[3]	LTE 16-QAM	5	0.78	7.5	73	–31.1	3.7
[20]	LTE 16-QAM	5	2.4	–	82.5*	–	5
[26]	WiBro 16QAM	5	1.88	10.75	–	–	3.64
[27]	LTE 16-QAM	5	1.9	7.5	78.5*	–	4.9(1.1♦)
[28]	WiMAX 64QAM	5	1.88	8.6	75	–	2.98
[29]	HSUPA R6	5	–	6.7	80%	–40	<2%
This work	LTE 16-QAM	5	2.4	9.38	76.1 (80.3†)	–32.1	2.82

*estimated ♦at 6-dB back-off †without including BBTPE Controller

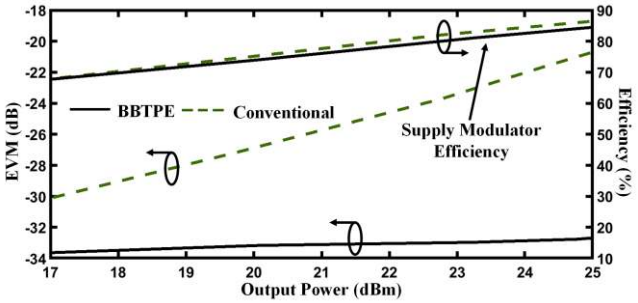

Fig. 20. Simulated EVM and power efficiency vs output power for supply modulator with and without BBTPE

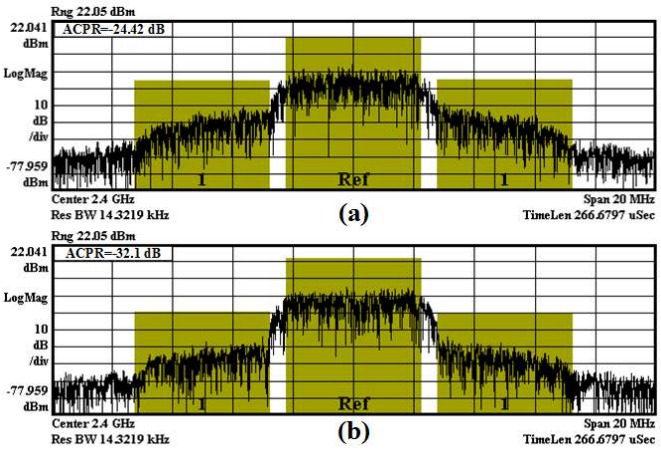

Fig. 21. Measured output spectrum (a) without BBTPE and (b) with BBTPE

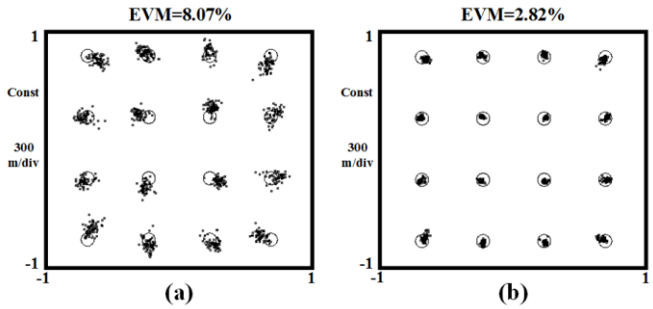

Fig. 22. Measured EVM (a) without BBTPE and (b) with BBTPE

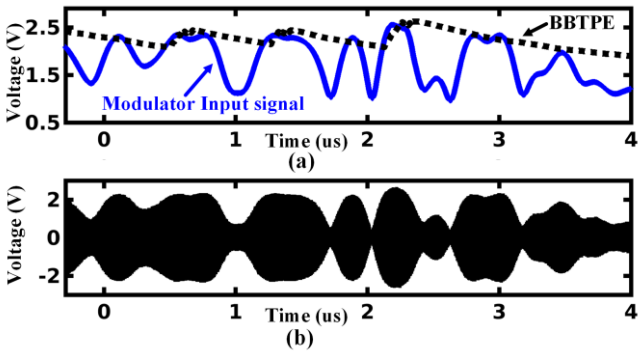

Fig. 23. Measured response with BBTPE (a) supply modulator input signal, as well as output, (b) Power amplifier's output signal

able to track the envelope signal and provided a linearity enhancement by ~11 dB in the middle region of the figure. As the input signal kept increasing, the linearity with the BBTPE incorporated solution started degrading marginally, mainly due to the PA linearity degradation rather than by the functionality of the supply modulator.

F. Simulation Results with an RF-PA

The cadence-based system simulation for an output power of 25 dBm is shown in Fig. 19. The simulated ACPR and EVM were −34.1 dBc and −32.77 dB respectively with the help of the BBTPE included modulator, which satisfied the standard requirement.

To consider switching noise coupling from the BBTPE, the contribution of switching noise in the main channel power and adjacent channel was measured. Basically, it is the processing of voltage ripple and the BBTPE switching noise that lied on the carrier frequency through the transfer function of the path from the supply modulator to the RF out. For the case of 25 dBm output power, in-band switching noise power due to BBTPE increased by less than 1 dB from −91.74 dBm to −90.92 dBm. Besides the marginal increment in the switching noise power, the absolute value is quite small compared to the main channel and adjacent channel power. Considering the performance of the PA, the impact of switching noise on ACPR and EVM was not noticeable.

With the increment of output power, the peak of output voltage increases and demands more agility in the supply modulator. As shown in Fig. 20, as the output power increases, the EVM degrades in the case of a conventional solution; however, with the help of the BBTPE included modulator, EVM remained below −32 dB for output power ranging from 17 to 25 dBm. For output power of 25 dBm, the improvement in EVM was 12 dB. As the transition from PBO to the peak power level is not frequent for wireless standards, the impact of using BBTPE on the modulator efficiency, which is 84.5%, is as minimal as ~2% at 25 dBm PA output power, and the difference becomes smaller and smaller as the

output power decreases. Here, the BBTPE controller's power consumption is 4.51 mW, which is 0.53% of the modulator input power.

G. Experimental Results with an RF-PA

The ACPR and EVM for both configurations (with and without BBTPE) are shown in Fig. 21 and Fig. 22, respectively. Here, the ACPR and EVM are improved by 7.68 dB and 65.1% (from 8.07% to 2.82%), respectively.

In addition, the time-domain input and output signals of the BBTPE incorporated supply modulator are presented in Fig. 23a. Due to the BBTPE, the modulator output voltage always remains equal or higher than the input envelope signal. The corresponding RF output signal of the PA is shown in Fig. 23b. The system's performance summary with and without BBTPE is shown in Table VIII. Due to the addition of the BBTPE system including the peripherals, the modulator efficiency degraded from 83.9% to 76.1%, in which 4.2% degradation is due to the BBTPE controller. The power consumption of the BBTPE controller is 6.83 mW. The impact of the switching noise on the PA output spectrum was not noticeable in both scenarios. A further comparison with a state-of-the-art performance with bandwidth of 5 MHz is shown in Table IX. The designs reported in [3], [20], [26]–[29] belong to the category of the architectures based on the parallel combination of linear and switching amplifier [2]–[10], [50]. In current work, the modulator efficiency and linearity performance are better than [3] and [28]. Compared to [20] and [27], this work shows a far better linearity performance. With respect to [29], which is having better linearity and efficiency, the current work processes a very demanding PAPR, which has a degrading impact on power efficiency and linearity. A further improvement in the modulator efficiency can be achieved with a faster dynamic buck regulator, which can reduce BBCS activity, and an optimized BBTPE controller with power efficient switch and comparator.

V. Conclusions

This paper presented an agile supply modulator with enhanced transient performance for envelope tracking purposes in linear PA systems. The proposed supply modulator is comprised of BBTPE along with a dynamic buck regulator. The transient performance enhancer provided an on-demand current to output in order to improve tracking of the input signal during sharp input rising transition along with improvement in overshoot and settling time. In this way, the BBTPE was able to provide additional degrees of freedom to the buck regulator design by relaxing its requirement for transient performance. The proposed selective envelope tracking also provides an efficient and simplified solution for envelope tracking in linear PA systems. In a test scenario, the proposed architecture showed an 80% improvement in rise time with a 60% reduction in overshoot and settling time. The effective settling time for the test scenario was reduced by 93%. When compared with the results for the PA system using the conventional dynamic buck regulator, the experimental results with a 16-QAM LTE 5 MHz at 2.4 GHz standard showed improvement of 7.68 dB and 65.1% in ACPR and EVM, respectively.

Finally, the benefits over improvement of overshoot and settling time along with rise time can be extended for other solutions that use auxiliary elements in parallel with switching regulators to handle fast input transition.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2934364, IEEE Transactions on Power Electronics

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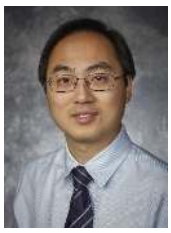

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