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An All-Digital Fast Tracking Switching Converter with a Programmable Order Loop Controller for Envelope Tracking RF Power Amplifiers

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Abstract

This paper presents a step down, switched mode power converter for use in multi-standard envelope tracking radio frequency power amplifiers (RFPA). The converter is based on a programmable order sigma delta modulator that can be configured to operate with either 1st, 2nd, 3rd or 4th order loop filters, eliminating the need for a bulky passive output filter. Output ripple, sideband noise and spectral emission requirements of different wireless standards can be met by configuring the modulator's filter order and converter's sampling frequency. The proposed converter is entirely digital and is implemented in 14nm bulk CMOS process for post layout verification. For an input voltage of 3.3V, the converter's output can be regulated to any voltage level from 0.5V to 2.5V, at a nominal switching frequency of 150MHz. It achieves a maximum efficiency of 94% at 1.5 W output power.

I. Introduction

Radio-frequency power amplifiers (RFPA) account for over 60% of the total power consumption in hand held devices and are prime target for efficiency improvements. The use of high peak-to-average power ratio (PAPR) signaling in 3G/4G LTE networks, combined with fixed power supply operation accounts to considerable losses as illustrated in Fig. 1(a). To address this issue, envelope tracking (ET) supplies have been proposed (Fig. 1(b)). ET operation enables considerable power savings by varying the RFPA supply voltage ($V_{DD, ET}$) according to the envelope of the base-band signal [1].

Due to their high efficiency, switch-mode DC-DC power converters (SMPC) make a good choice for ET power supply implementation [2]. However, they present a multitude of design tradeoffs that impact their performance at the wireless system level. SMPCs output voltage ripple for instance can mix into the RF spectrum and cause interference with adjacent channels.

Latest wireless standards have high envelope bandwidths, requiring the SMPC to have a fast dynamic response, and consequently a high switching frequency, which lead to s lower

efficiency. A common solution for switching frequency reduction, to lower losses, while maintaining low ripple operation is to use high-order passive output filtering. Recent work making use of 4th and higher order LC filtering to meet different wireless standards (GSM, EDGE, UMTS, LTE) has been reported [3,4], however, passive filtering is not an optimal solution due to cost, space, and power loss considerations. Additionally, passive filtering does not allow for cost effective multi-standard operation, hence separate SMPCs, each tailored for a specific standard have been used to power the different RFPAs found in typical handsets. The recent emergence of multimode, multi-standard RFPAs makes it desirable to power the RF stage using a single customizable SMPC, capable of catering to all supported wireless standards [5]. To this end, this paper presents a programmable SMPC that can be configured according to the wireless network's ripple, noise and spectral emission requirements without the need for high order passive filtering.

The rest of the paper is organized as follows, section II describes the proposed architecture whereas implementation is provided in section III. Transistor level simulations are presented in section IV, and finally conclusions in section V.

II. Proposed Architecture

A block diagram of the proposed buck converter is shown in Fig. 2. The digital controller consists of digitizers ΣΔFDC1 and ΣΔFDC2, PID compensator, and ΣΔ modulator. V_{IN} is the unregulated battery supply. In order to meet the ripple and noise energy requirements set by the different FCC spectral emission masks, a programmable order ΣΔ modulator is used.

It can be configured to operate as either a 1^{st}, 2^{nd}, 3^{rd} or 4^{th} order modulator depending on the dynamic system requirements. Another degree of programmability is the use of load dependent, variable switching frequency (f_s) (not shown) which directly impacts ripple amplitude and SMPC switching losses. The SMPC configuration controller (SCC) receives control input and master clock (CLK) from the application platform (for e.g. cell phone's application processor), and configures the ΣΔ modulator order, as well as the control loop's switching frequency accordingly.

A typical application for the proposed SMPC would be a cell phone transitioning from a 2G (GSM) to 4G (LTE) network. Based on the GSM emission mask, the RFPA output spectrum should remain below −46 dBm for frequencies greater than 1.8 MHz offset from the carrier frequency, and below −51 dBm for offset frequencies between 600 kHz–1.8 MHz, whereas the LTE (E-UTRA) mask dictates emissions to remain below −73 dBm for offset frequencies between 15 – 30 MHz from carrier and below −85 dBm for offset frequencies greater than 30 MHz from carrier [6].

To meet the GSM standard, the SCC configures the ΣΔ modulator to operate in 2^{nd} order, whereas it configures it to operate in 4^{th} order to meet the LTE standard. F_s is scaled based on load requirements which are a function of the platform conditions (i.e, power-back off status, distance to base-station,… etc).

The SMPC's control loop operates as follows; the scaled output (V_{fb}) and reference (V_{ref}) voltages are digitized using ΣΔFDC1 and ΣΔFDC2 respectively, the digital difference (V_{err})

is processed by the proportional-integral-differential (PID) compensator. The output of the PID compensator is fed to the digital ΣΔ modulator which generates the duty cycle command (PWM signal) that drives the power stage drivers.

III. Implementation

In what follows, discussion of the design details of the main blocks for this proof of concept implementation is presented.

Although the SMPC is designed as a closed loop, voltage controlled converter, the control loop can be used in open loop, current mode regulation with the addition of a current sensing block. Design of the PID and power stage follows standard work in [7], whereas implementation of the SCC controller and (f_s) scaling are application/platform specific and not the scope of this paper.

A. Programmable Order ΣΔ Modulator

The proposed fully digital modulator is shown in Fig. 3. It is composed of four integrators in a feed forward topology (CIFF) [8]. First and third stage integrators are delaying, whereas the second and fourth are none delaying for stability and response speed considerations. Loop filter coefficients are implemented as single or double bit shifts on incoming bus lines. Coefficients ($A_{i=1,2,3,4}$) take values of 1, 0.5 or 0.25 which correspond to no data shift, single bit shift and double bit shifts respectively. The values the coefficients take depend on the order the modulator is configured in as dictated by the SCC control unit. To configure the modulator to operate as 2nd order for e.g, $A_{3,4}$ are set to zero (GND) whereas A_1 and A_2 are set to 1 and 0.5 respectively. Optimal loop coefficient values are listed per modulator order in table 1. Multiplexers are used to implement bit shifting and order reduction.

The input bus line is connected to the subtractor (Δ) along with the feedback output bus (OUTPUT) which is formed by discarding the LSB bits and padding the remaining MSBs (6 for this implementation) with zeroes. Typically, an *n*-bit realization of the modulator should use adders, registers, and multiplexers that are *n*-bit wide. In order to reduce implementation complexity and gate count, the bus length is reduced from integrator to integrator along the signal path. Truncation errors resulting from inter-stage bus reduction are masked below the filtered quantization error of the last stage provided relation (1) applies [9]:

$$2^{4-n_i}\sum_{i=2,3,2}\left(2^{2(k-n_i+4)}/(2\pi)^2\right)^{5-i} \quad (1)$$

This allows the 22 bit implementation ($n_{1,2,3,4}$) to be reduced from an all stage 22 bit design to 22 – 17 – 13 – 9 for n_1, n_2, n_3, and n_4 bus lines respectively and an effective word (k) 18 bits wide. The extra 4 bits are used for sign and overflow protection.

A CIFF design is chosen for the loop filter implementation because it provides a unity signal transfer function (STF) which simplifies loop compensation and only introduces a fixed delay component that is a function of the switching frequency. This is critical since both

group delay and STF attenuation at the switching frequency impact the supply envelop distortion. However, a frequency dependent loop filter group delay would directly distort the RFPA signal being transmitted, while poor switching frequency attenuation would cause spectral broadening and out-of-band noise.

B. ΣΔ Frequency Discrimination Analog to Digital Converters

To enable a fully digital implementation, A/Ds are required at the input to the control loop. Compared to other nyquist rate architectures, ΣΔFDCs offers simple, area and power efficient choice. They are digital none feedback modulators, that are inherently linear since they use a single bit comparator [10]. Implementation of the 1st order ΣΔFDCs used in this work is shown in Fig. 4. A single, ΣΔFDC is composed of a voltage controlled oscillator (VCO), two D flip flops and one XOR gate. Resolution of the SDFD (n_{adc}) is given by:

$$n_{adc}=int\left[\log_2\left(\frac{V_{max.adc}}{V_{ref}}\cdot\frac{V_{fb}}{\Delta V_{fb}}\right)\right] \quad (2)$$

Where, V_{ref} is the reference voltage, V_{fb} and ΔV_{fb} are the scaled output voltage and regulation error respectively, and $V_{max,\,adc}$ is the full scale voltage of the ADC. As depicted in Fig. 4, two ΣΔFDCs are used to digitize V_{fb} and V_{ref}, the difference of the two signals forms a single bit stream that is down sampled and filtered by the decimator.

IV. Simulation

The SMPC is implemented in 14nm bulk digital CMOS process (supply voltage 3.3 V I/O, 1.05V Digital) and validated with post layout (Fig. 5) simulations. For an input voltage of 3.3V, the supply voltage can be regulated to any level between 0.5V to 2.5V, with a nominal value of 1.5V. The implemented converter can deliver a peak supply power of 1.5 W and achieves an efficiency of 94% at 800 mA at fs = 150 MHz. Spectral and transient results reported here are based on post layout simulations. Fig. 6 demonstrates the noise shaping capability of the programmable modulator configured in different orders with fs fixed at 100MHz. 20,40, 60 and 80 dB/decade noise shaping is observed for the first, second, third, and fourth order modulators respectively. Fig. 7 presents the SMPC's output power spectral density for the different modulator orders with fs fixed at 150 MHz and a constant load current of 750mA. The output noise power is well below emission requirements for 2G/3G and 4G standards and affords a significant margin for added noise floor and spectral leakage introduced by the RFPA nonlinearity products. Fig. 8 demonstrates the envelope tracking response of the converter using a 4.2 Ω resistive load corresponding to 31.5 dBm output power. The SMPC is able to track the 10MHz LTE test envelope signal while configured in 4th order and Fs = 80MHz. Key performance metrics are provided in Table 2.

V. Conclusion

A fully digital switched mode power converter for multi-standard envelope tracking RFPA applications is presented. It features a 22-bit, reduced complexity, programmable order, digital sigma delta modulator that can be configured to operate with either 1st, 2nd, 3rd or 4th

order loop filters for meeting different output ripple and spectral noise requirements of varying wireless standards without high order, output passive filtering. The design is implemented in 14nm bulk CMOS process and verified with post layout simulations.

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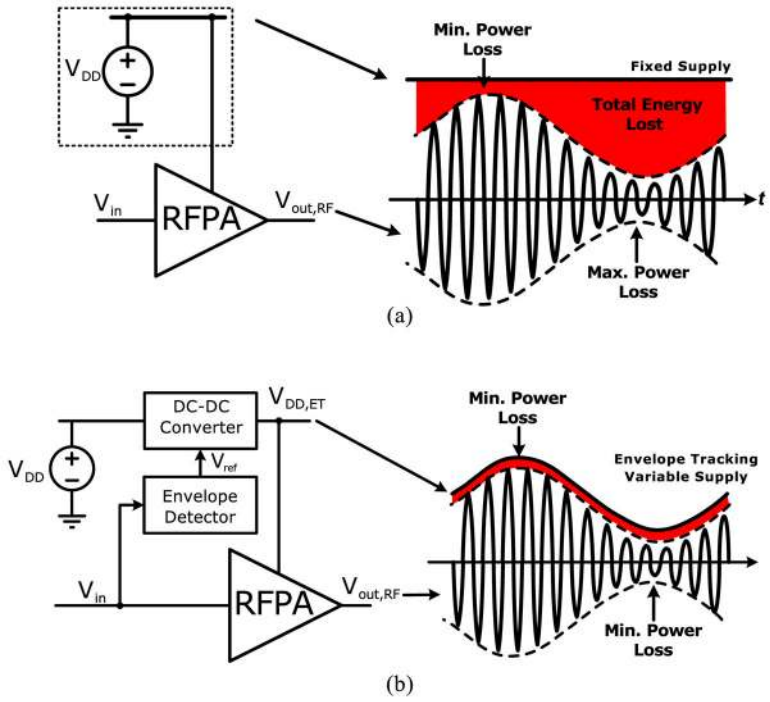

Fig. 1.

(a) Fixed power supply (b) supply modulation scheme in RF PAs.

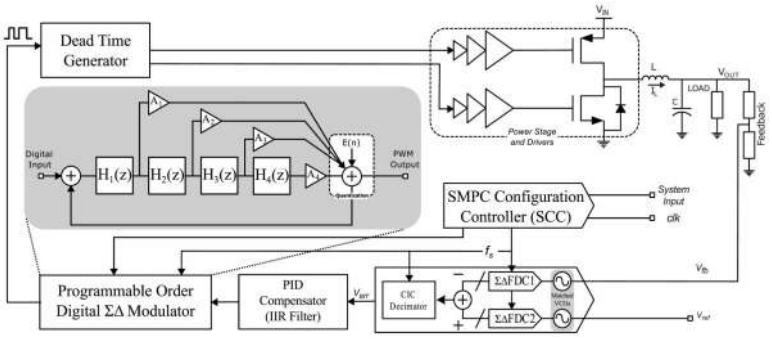

Fig. 2.

Proposed architecture of the programmable order, ΣΔ controlled, digital buck DC-DC converter.

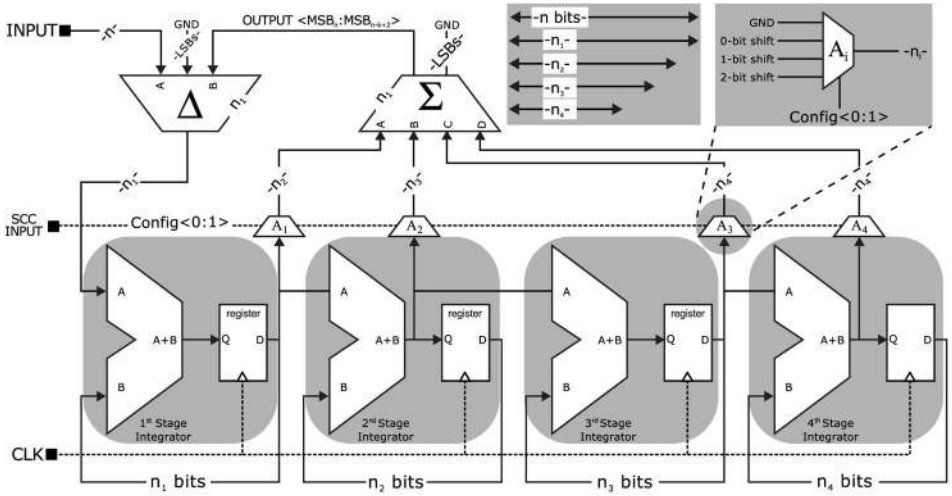

Fig. 3.
Proposed programmable order CIFF ΣΔ modulator

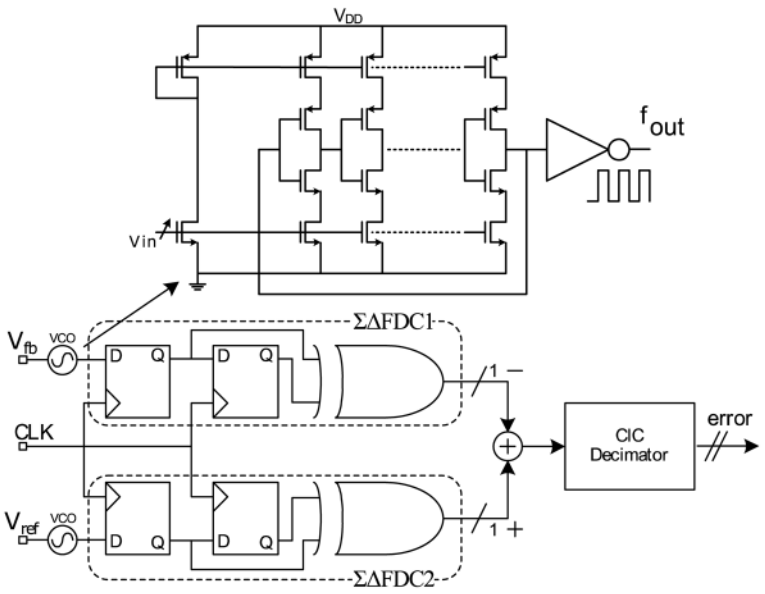

Fig. 4.

Gate level implementation of V_{fb} and V_{ref} digitizers. Current-starved VCOs are used as voltage-to-frequency converters.

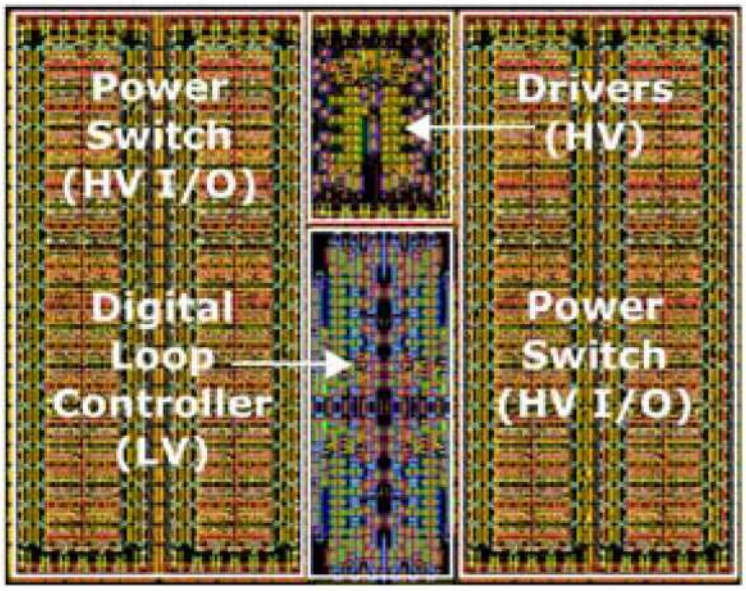

Fig. 5.
Layout of the proposed digital converter.

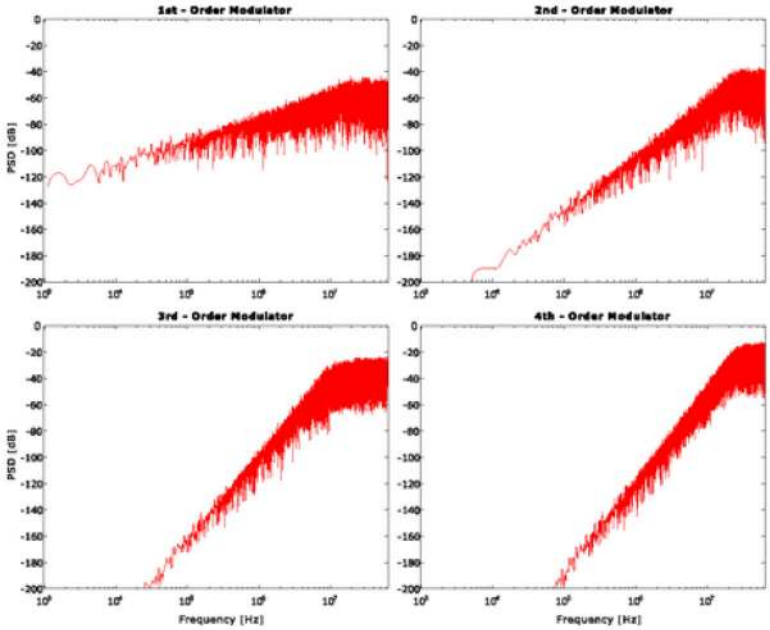

Fig. 6.
Simulated output PSD of the programmable order ΣΔ modulator, f_s = 100MHz.

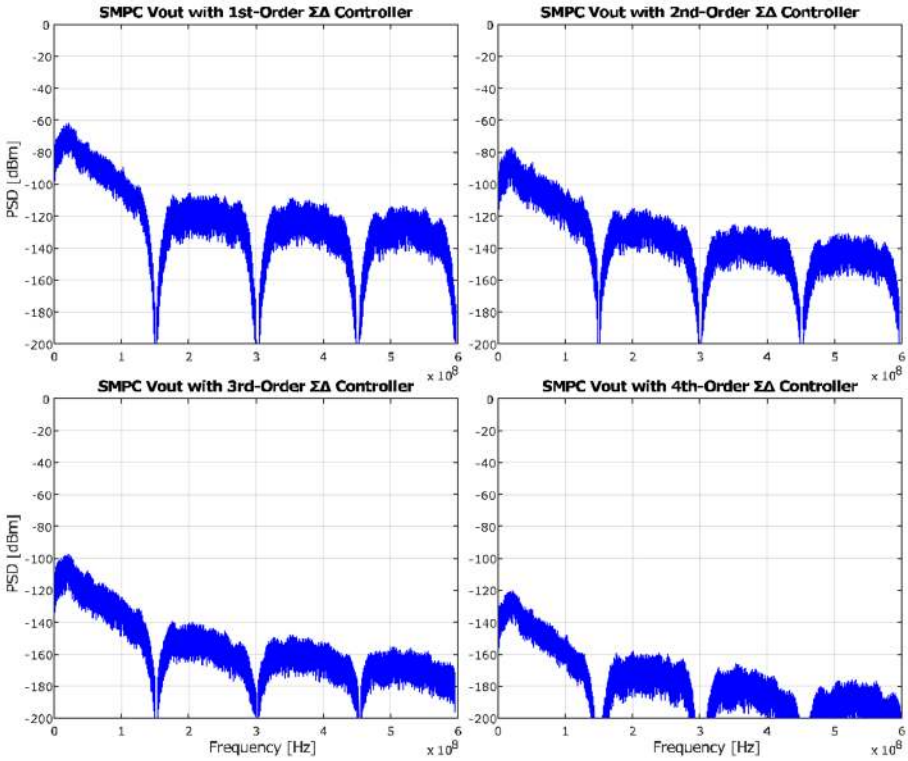

Fig. 7.

PSD of the converter's output for different ΣΔ modulator orders, f_s = 150MHz.

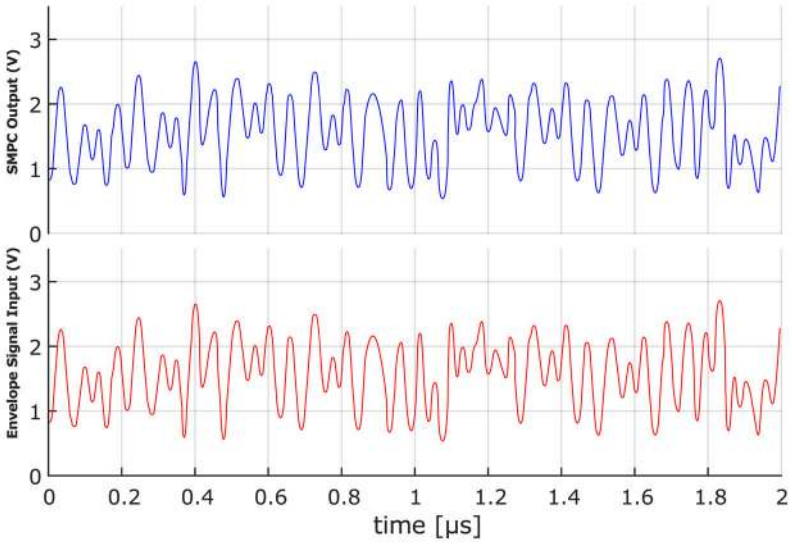

Fig. 8.

Transient tracking response for a 10MHz LTE test envelope signal, programmable ΣΔ set to 4th order, fs = 80MHz.

Table 1

Programmable ΣΔ modulator loop filter coefficients

Modulator Order	Loop Filter Coefficients (Ai=1,2,3,4)
1st	1 – 0 – 0 – 0
2nd	1 - 0.5 – 0 – 0
3rd	0.25 – 0.25 – 0.5 – 0
4th	0.25 – 1 – 1 – 0.25

Table 2

Performance Summary

Process	**14nm HV CMOS**
Layout Area (μm)	220 × 190
Supply Voltage (V)	3.3 I/O, 1.05 Digital
ΣΔ Max. Sampling Frequency (MHz)	150
Max. Efficiency (%)	94%
Regulated Output (V)	0.5 – 2.5
Max Load Current (A)	1.0
Max Output Power (W)	1.5