An all-inversion-region g_m/I_D based design methodology for radiofrequency blocks in CMOS nanometer technologies

ABSTRACT

This chapter presents a design optimization methodology for analog radiofrequency (RF) blocks based on the g_m/I_D technique and on the exploration of all inversion regions (from weak inversion or sub-threshold to strong inversion or above threshold) of the MOS transistor in nanometer technologies. The use of semi-empirical models of MOS transistors and passive components, as inductors or capacitors, assure accurate designs, reducing time and efforts for transferring the initial block specifications to a compliant design. This methodology permits the generation of graphical maps to visualize the evolution of the circuit characteristics when sweeping both the inversion zone and the bias current, allowing reaching very good compromises between performance aspects of the circuit (e.g. noise and power consumption) for a set of initial specifications. In order to demonstrate the effectiveness of this methodology, it is applied in the design of two basic blocks of RF transceivers: low noise amplifiers (LNAs) and voltage controlled oscillators (VCOs), implemented in two different nanometer technologies and specified to be part of a 2.4 GHz transceiver. A possible design flow of each block is provided; resulting designs are implemented and verified both with simulations and measurements.

1. INTRODUCTION

The variety of wireless applications in areas as diverse as medicine, entertainment or environment have originated a wide spectrum of wireless standards and therefore, of circuit specifications. This diversity in the circuit characteristics together with the shrinking time to market results in design challenges. To keep pace with this innovation, RF designers, as never before, need reliable optimization tools helping them from the beginning of the design process.

Some RF standards are very demanding in terms of power consumption but they have relaxed performance requirements e.g. in terms of channel bandwidth or noise and frequency synthesizer spectral purity, as in the case of IEEE 802.15.4 standard (on which ZigBee is based) and low-energy Bluetooth (IEEE 802.15.1-2002). Power consumption constraints the transceiver design and forces to assign carefully the power budget of each block of the chain. It also has a strong influence on the noise, linearity, gain and other characteristics. A well known trade-off is especially noticeable between power and inherent noise of blocks as LNAs, mixers or VCOs. To take advantage of this compromise, the designer needs a deep and accurate knowledge of the block behavior and its devices to reach an optimized design, especially when using nanometer technologies.

The trade-offs between consumption and noise, among other performances, are strongly determined by the characteristics of the active element: the MOS transistor. These characteristics change as a function of the inversion region in which the MOS transistor is biased: strong inversion (above threshold), moderate inversion (approximately "around" threshold) and weak inversion (sub-threshold). In Section 2 a summary of the characteristics and the implications of working in each of these zones are presented.

When working in radiofrequency, the MOS transistor has been traditionally biased in strong inversion. It is because in this region the transistor has a smaller size and drives a higher current than in moderate or weak inversion. This leads to a reduction of parasitic capacitances and an increment in the transconductance. Therefore, as the MOS transition frequency f_T is proportional to the transconductance and to the inverse of its parasitic capacitance, the maximum frequency of operation increases in strong inversion region. However, as it will be shown later, this increased maximum frequency of operation is obtained at the expense of a very low ratio between transconductance and bias current (below 5 V^{-1} instead of the 38 V^{-1} achievable with a bipolar transistor at ambient temperature). The effect of moving from strong inversion through weak inversion implied a considerable current reduction, but in contrast, parasitic capacitances are higher as transistor dimensions increase. For example, for sub-micrometer technologies the high frequency design in moderate was limited up to one gigahertz (Barboni, Fiorelli & Silveira , 2006).

However, the tremendous channel length reduction to below 100 nm, and the improvement in passive components, i.e. inductors and capacitors, are opening the path to feasible implementations. So, nowadays it is possible to use CMOS technology without increasing the consumption and even reduce it much more by working in the moderate and weak inversion in the range of several gigahertz for minimum length transistor. This can be achieved even considering the MOS transistor working below the quasi-static limit of one tenth of f_T (Tsividis, 2000, p. 492) and therefore greatly simplifying the circuit analysis.

Many implementation examples working in moderate and weak inversion are found in literature. Porret, Melly, Python, Enz and Vittoz (2001) and Melly, Porret, Enz, and Vittoz (2001) presented the design of a receiver and a transmitter, respectively, for 433 MHz in CMOS, working in moderate inversion. Ramos et al. (2004) showed the design of an LNA in 90 nm technology for 900 MHz in moderate/weak inversion. Barboni et al. (2006) utilized the moderate inversion to implement an RF amplifier and a VCO at 900MHz, Shameli and Heydari (2006) designed a CMOS 950 MHz LNA in moderate inversion. Lee and Mohammadi (2007) designed a 2.6 GHz VCO in weak inversion in CMOS. To provide a final example, Jhon, Jung, Koo, Song and Shin (2009) designed a 0.7 V - 2.4 GHz LNA in deep weak inversion. All these works show how, in the last decade, the design in moderate and weak inversion in CMOS at RF became consolidated. Nevertheless, there is a lack of studies that analyze the performance of an RF design in all the inversion regions of the MOS transistor.

In this chapter, we present an RF design systematic approach for all-inversion regions starting from the data provided by the nanometer technology foundries and leading to successfully measured circuits. The basis of this method is the use of the g_m/I_D based tool of the MOS transistor (Silveira, Flandre & Jespers, 1996). As it will be discussed later on, the g_m/I_D ratio is an intrinsic MOS characteristic slightly dependent on the transistor aspect ratio and directly related to the inversion level of the transistor. The inversion level is directly associated with the normalized current or current density, defined as $i=I_D/(W/L)$, and g_m/I_D is one-to-one related with i. Biasing the transistor in strong inversion means low g_m/I_D values and high i currents while working in weak inversion is translated to high g_m/I_D figures and low i values.

Several factors make useful the g_m/I_D parameter. Firstly, the ease to write circuit design expressions as a function of this parameter, since generally the transconductance and the current are part of them. Secondly, its value gives a direct indication of the inversion region and of the efficiency of the transistor in translating current consumption into transconductance. Finally, its variation is constrained to a very

small range, efficiently covered with a grid of some tens of values of g_m/I_D (e.g. from 3 V^{-1} to 28 V^{-1} in nanometer bulk CMOS). Utilizing this variable in the circuit expressions and sweeping the g_m/I_D value allows obtaining a set of design space maps. For example, circuit characteristics as noise, gain, consumption, among others, can be displayed as function of g_m/I_D. This graphical representation helps the designer to study the evolution and trade-offs of some of these characteristics when working in any of the three regions.

Along this chapter, we will state a very general RF design methodology for all inversion regions of the MOS transistor suitable for RF circuits as diverse as LNAs or VCOs. To develop this design methodology, four general steps should be followed.

Firstly, the DC behavior of MOS transistor has to be captured in curves or expressions of g_m/I_D, g_{ds}, and intrinsic capacitances versus i. This requires a MOS transistor model accurately characterized in all-inversion regions. In addition, good short-channel MOS noise model and their correspondent parameters should be known. All this will be detailed in Section 2.

Secondly, follows the extraction of passive component models, as will be discussed in Section 3.

In third place comes the modeling of the RF block with a set of equations modified in order to express them in terms of g_m/I_D or i.

Finally, it is necessary to establish a design flow to arrange the computations, the application of the technological data collected in the two first steps, and the relations between them and the decisions fixed by block specifications and technological constraints. These two last steps are described in Section 4 through two application examples. The electrical simulation and measurement results of the implementations of these examples, an LNA and a VCO, are also presented in order to show the usefulness and effectiveness of the design methodology.

2. MOS TRANSISTOR ANALYSIS AND GM/ID TOOL

2.1 MOS operation and modeling

2.1.1 MOS transistor inversion regions

The simplest, strong inversion model of the MOS transistor considers that when the gate-bulk voltage is lower than the threshold voltage, there is no significant inversion channel in the transistor and therefore the drain current I_D is zero. In practice the inversion charge in the channel is gradually reduced as the gate voltage decreases, as seen in Fig. 1(a), where the current I_D versus V_G is plotted in a logarithmic scale. Below the threshold voltage V_{thres} the current is not zero and has an exponential relation with the gate voltage; this current is often referred to as sub-threshold current.

In this sub-threshold region the main current conduction mechanism is through diffusion, where the current is proportional to the charge concentration gradient. The diffusion current component, negligible in the above-threshold operation, is also the main mechanism in a bipolar transistor, which shares with the MOS sub-threshold region the characteristic of having an exponential voltage to current characteristic. Above the threshold, the dominating current conduction mechanism is drift, where the current is proportional to the inversion charge concentration, leading this mechanism to the classic quadratic relationship between gate voltage and drain current.

Summarizing, depending on the value of V_G, three behavioral regions of the saturated MOS transistor, can be distinguished, as Fig. 1(a) shows:

- Strong inversion (S.I.): when V_G is higher than approximately 100 mV of the threshold voltage V_{thres}, the inversion channel is strongly established, the drift current is the dominant. Here it is the well-known classic quadratic I_D-V_G MOS equations.

- Weak inversion (W.I.): for low V_G voltages, far below V_{thres}, the number of free charge is very small, so the inversion in the channel is weak. Here the dominant method of conduction is diffusion and the current I_D has an exponential relationship with V_G ($I_D \propto \exp(V_G/(nU_T))$; that is why $\log(I_D)$ in Fig. 1(a) has a constant slope in this zone. Parameter n is called the slope factor and U_T is the thermal voltage.

- Moderate inversion (M.I.): when V_G is around V_{thres} both conduction mechanisms are significant and the final effect is a mixture of both. The mathematical expression in this zone is neither quadratic nor exponential.

2.1.2 g_m/I_D characteristic

As mentioned in the Introduction, the g_m/I_D ratio is a MOS characteristic which is directly related with the inversion region of the transistor. Let us show why this happens.

The coefficient g_m/I_D is the slope of the curve I_D versus V_G in a logarithmic scale because:

$$\frac{g_m}{I_D} = \frac{\partial I_D / \partial V_G}{I_D} = \frac{\partial \log(I_D)}{\partial V_G} \tag{1}$$

As Fig. 1(a) shows, the maximum slope of the curve, that is, the maximum g_m/I_D ratio, appears in the weak inversion region, decreasing until reaching strong inversion. Firstly, this means that the weak and moderate inversion regions are more adequate for low power efficient designs. In these regions, the values of gate voltage V_G (around 100 mV below the threshold voltage) and the saturation drain voltage V_{Dsat} (from 100 mV to 150 mV) are very low, which make these zones very adequate for low supply voltage operation.

The g_m/I_D ratio is a measure of the efficiency to translate I_D into the transconductance g_m, because the greater g_m/I_D value the greater transconductance which can be obtained at a constant current value. The inset of Fig. 1(a) shows the g_m/I_D curve as a function of I_D (which is the variable used for MOS biasing). The maximum value of g_m/I_D is approximately $1/nU_T$; for the technology used to generate Fig. 1(a), this value is approximately 28 V^{-1}; for g_m/I_D higher than 17 V^{-1} the transistor is in weak inversion; for g_m/I_D lower than 8 V^{-1}, it is in strong inversion, and for g_m/I_D in the midst of this range, it is in moderate inversion.

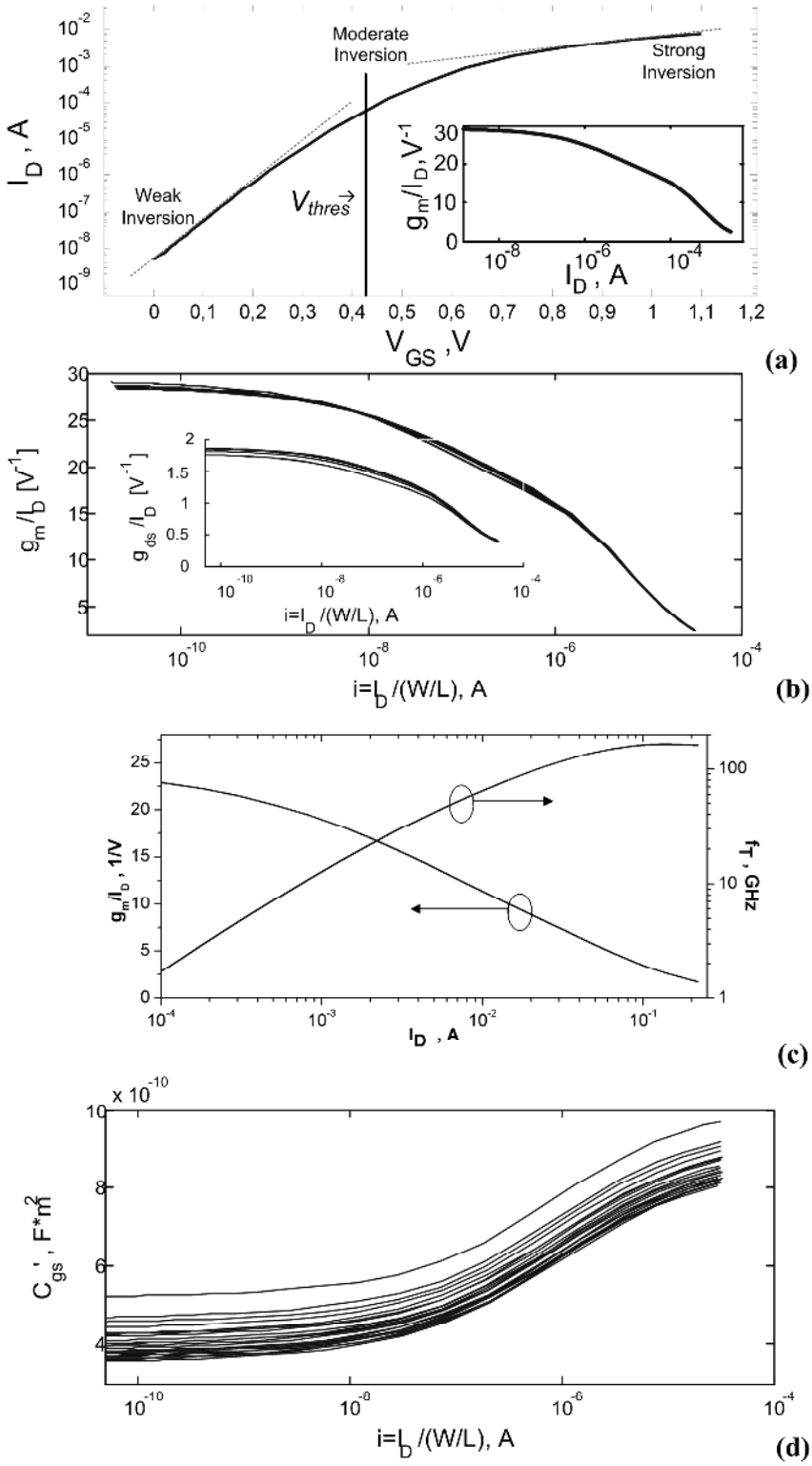

Fig.1 (a) Drain current I_D versus V_{GS} and g_m/I_D vs. I_D (inset) for an nMOS transistor with an aspect ratio of W/L=6μm/100nm. (b) g_m/I_D vs. normalized current i and g_{ds}/I_D vs. i (inset) for a set of 100nm nMOS transistors with widths in the range of [6μm, 320μm]. (c) Transition frequency f_T and g_m/I_D versus I_D. (d) Intrinsic capacitance C_{gs}' vs. i.

g_m/I_D versus transistor size

For a specific transistor size, if an increment in the f_T is needed, as $f_T \approx g_m/(2\pi C_{gs})$, the transconductance g_m (and so I_D) should be raised, meaning a reduction in g_m/I_D. But g_m can also be changed modifying the transistor size.

From a general expression of the MOS drain current

$$I_D = \frac{W}{L} f_1(V_G, V_S, V_D; L)\,, \tag{2}$$

where the dependence of the function f_1 (usually named normalized current $i=I_D/(W/L)$) with the transistor length L is explicitly considered only for short channel MOS.

The transistor transconductance is

$$g_m = \partial I_D / \partial V_G = \frac{W}{L} \frac{\partial f_1(V_G, V_S, V_D; L)}{\partial V_G} \tag{3}$$

then

$$g_m / I_D = \frac{\partial f_1 / \partial V_G}{f_1} = \frac{\partial\left(\log f_1\right)}{\partial V_G} = \frac{\partial\left(\log\left(I_D/(W/L)\right)\right)}{\partial V_G} = f_2(I_D/(W/L)) = f_2(i)\,. \tag{4}$$

Because $i=f_1$ does not depend on the transistor width W, the g_m/I_D ratio vs. i curve is a constant for MOS transistors with equal length, as shown in Fig. 1(b). Really that is true if you do not consider very narrow devices, which, usually are not applied for transconductance generation in radiofrequency, especially in moderate and weak inversion. Moreover, for short channel devices, it is necessary to consider the slight variation of g_m/I_D with L due to its implicit dependence on i according to (2).

So, to increase g_m while maintaining a good current efficiency, W should be increased maintaining constant $I_D/(W/L)$ (and consequently g_m/I_D), while increasing I_D. As a drawback, increasing W means increasing the parasitic capacitances, which implies reducing the transistor f_T. These two opposing factors (maintaining or improving g_m/I_D when increasing both W and I_D but increasing the parasitic capacitances) show the existence of an optimum in the compromise bandwidth-consumption (f_T - I_D) which generally appears in moderate inversion. These dependences are shown in Table I where, for a given transconductance of 5 mS, the impact of operating in strong, moderate or deep weak inversion is shown. The table exemplifies how working in moderate inversion region allows decreasing consumption while keeping acceptable frequency and die area characteristics.

g_m=5 mS	S.I.	M.I.	W.I.
g_m/I_D, V^{-1}	4	14	25
I_D, A	1.25 m	357 µ	200 µ
i, A	17.8 µ	0.79 µ	12 n
W, m	7 µ	45 µ	1.59 m
f_T/10, GHz	16	3	0.2
V_G, V	0.85	0.56	0.36

Table I. nMOS characteristics for S.I, M.I and W.I.

The curve g_m/I_D versus $i=I_D/(W/L)$ is a technological characteristic, and will be our fundamental design tool. As mentioned before, it is strongly related to the performance of analog circuits and gives an indication of the transistor region of operation. Also, the g_m/I_D vs. i curve provides a tool for calculating transistor dimensions, as will be discussed in Section 3. This curve slightly varies with the transistor

width and length, and only changes appreciably for narrow or very short channels. For the final design examples of this chapter, this curve is extracted for the minimum transistor length (100 nm) and a set of widths {1, 10, 100, 320} μm. This small range is enough for covering very well the variations of g_m/I_D vs. i in the whole transistor region. Because of this slight variation in the curve g_m/I_D vs i with the transistor dimensions, the methodology presented here makes sense. In Fig. 1(b), for a 90 nm technology, the behavior of g_m/I_D vs. i when the width of a minimum length transistor changes from W=6 μm to W=320 μm is observed, depicting how little is the change of the g_m/I_D curve for different MOS widths.

g_m/I_D versus f_T

As well as the g_m/I_D versus i is used to calculate the transistor dimensions, when used together with the transistor gate capacitances versus i, the frequency f_T versus i can be found, as Fig. 1(c) shows. This curve gives an idea of the frequency limits of the technology used when different inversion zones are considered. As Fig. 1(c) stands, when working with nanometer technologies and in strong inversion, f_T frequencies can reach hundreds of gigahertz whereas in deep weak inversion those frequencies drop down to levels of hundreds of megahertz. For the example of Fig. 1(c) and Table I, and considering again the very restrictive quasi-static limit for the working frequency of one tenth of f_T, for a g_m/I_D around 4 V^{-1} the operating frequency can be up to the tens of gigahertz, whereas with a g_m/I_D around 25 V^{-1} the operating frequency falls to the gigahertz. This simple check lets the designer to know the limitations of the technology in terms of frequency in each level of inversion.

2.1.3 Output conductance g_{ds} and g_{ds}/I_D

Another small signal parameter required in our methodology to describe the MOS behavior is the output conductance g_{ds}. It dramatically increases in nanometer transistors with respect to micrometer ones, due to the shortening of the channel length L (Tsividis, 2000, page 372). This effect must be taken into account because it begins to influence on certain RF blocks. For example, in an LC tank-VCO the conductance g_{ds} affects the value of the final g_m chosen, and hence the bias current and the phase noise; in a Common-Source LNA it changes the maximum gain of the circuit. Therefore, a ratio similar to g_m/I_D can be applied (Jespers, 2010) which is the g_{ds}/I_D ratio; it is also very technology dependent. The inset of Fig. 1(b) shows the behavior of g_{ds}/I_D versus i, for W in the range of [6, 320] μm. As happens with the g_m/I_D curve, its variation is subtle when changing the width. The variation between strong and weak inversion is small, and similarly to the curve g_m/I_D vs. i, it also decreases when moving towards strong inversion (Tsividis, 2000, page 380).

2.1.4 Intrinsic Capacitances

When working in the radiofrequency range, it is absolutely required the consideration of the transistor intrinsic capacitances. Considering again that the working frequencies are below one tenth of f_T, it is enough to consider the following intrinsic capacitances: C_{gs}, C_{gd}, C_{gb}, C_{bs} and C_{bd}, disregarding the other four capacitances and transcapacitances as well as non-quasistatic effects. These capacitances change with the inversion level, as Tsividis (2000) shows (page 405); and obviously they change with the transistor size. In this work, in order to simplify the modeling, the intrinsic capacitances are considered to be proportional to the gate area (WL). This can be done because these capacitances are proportional to the gate oxide capacitance Cox which is, at the same time, proportional to WL (Tsividis, 2000, page 391). Hence, each normalized capacitance C_{ij}'=$C_{ij}/(WL)$ is considered to be equal for all transistors in the width range of interest. With this assumption, the intrinsic capacitances are extracted for one representative transistor and normalized to its area. Afterwards, normalized capacitances are applied to estimate the capacitances of other transistors in the considered width range.. For example, in Fig. 1(d) shows the behavior of the normalized capacitance C_{gs}' versus i for a set of widths in a 90 nm technology. As observed, the error is below ±20% of the mean value considering the widths varying between 8 μm and 320 μm, which is acceptable for this methodology. For C_{gd}' and C_{gb}' the error is lower than ±3% of the mean value.

2.1.5 Semi-empirical modeling

Analytical compact models —as PSP (Gildenblat et al., 2006), BSIM (BSIM Research Group, 2011), EKV (Enz and Vittoz, 2006) o ACM (Cunha, Schneider and Galup-Montoro, 1998)— have a set of equations more or less complex, consistent in all regions of operation, which describes the MOS transistor. Semi-empirical models use measurement or simulation data to obtain numerically certain characteristics and to build a look-up table.

Despite in the methodology presented here both approaches are valid and can be used indistinctively, in this work we have decided to apply a semi-empirical MOS model, as it jointly considers second and higher order effects which appear in nanometer technologies and it is easily obtained by extracting MOS characteristics via DC simulation. We discarded the use of analytical compact models, as the fitting of parameters is very time consuming. The semi-empirical model is extracted via an electrical simulator; which, in turn, uses the BSIM (or PSP) model, suitable for RF. The parameters used are provided by the foundry, which means that they are strongly validated. In addition, they are used by designers as the standard verification framework.

MOS data acquisition scheme

As already introduced, for the proposed methodology, three basic characteristics must be considered as a function of the normalized current i: (a) the transconductance to current ratio g_m/I_D, (b) the output conductance to current ratio g_{ds}/I_D and (c) the normalized MOS capacitance $C_{ij}' = C_{ij}/(WL)$. To acquire this information, a very simple scheme is utilized: both transistor gate and drain nodes are connected to a DC voltage source, while source and bulk nodes are connected either to ground (nMOS transistor) or to the supply voltage (pMOS transistor). Then, the gate voltage V_G is swept extracting I_D, g_m, g_{ds} and C_{ij}'. For small-signal circuits, the drain voltage is set around its expected DC value. To get a very complete dataset the same simulation must be run for a set of widths (for example, for 1 μm, 10 μm and 100 μm), when a fixed transistor length value is used. Otherwise, following the same idea, a small set of lengths (e.g. 100nm, 1 μm, 10 μm) should be chosen.

2.1.6 Noise in MOS transistors

In this section the MOS noise sources used in this chapter to deduce the equations that describe the noise characteristics of the radio-frequency blocks are presented. These sources are the drain current noise (consisting of the white noise and the flicker noise) and the induced gate noise, presented by Galup-Montoro, Schneider and Cunha (1999) and, after by Tsividis, (2000), (Section 8.5); and more recently, for RF models, by Shi, Xiong, Kang, Nan and Lin, (2009).

For the drain-noise current power spectral density two zones are clearly recognized, the white noise zone and the flicker noise zone. The white noise is due to random fluctuations of the charge in the channel; whereas the flicker noise is the result of trapping and detrapping of the channel carriers in the gate oxide. The corner frequency f_c is the frequency of the asymptotic limit between these two zones.
The white noise, for all inversion regions, is generally expressed as:

$$\overline{i_{d,wn}^2} = 4k_B T\gamma g_{d0}\Delta f = 4k_B T\gamma \frac{g_m}{\alpha}\Delta f \tag{5}$$

where k_B is the Boltzmann constant, T is the absolute temperature, γ is the excess noise factor, α is equal to $\alpha = g_m / g_{d0}$, with g_{d0} the output conductance evaluated at V_{DS}=0 where the white noise is maximum for all the inversion regions.

The flicker noise is written as:

$$\overline{i_{d,1/f}^2} = \frac{K_F' g_m^2}{WL} \frac{1}{f} \Delta f \tag{6}$$

with K'_F the flicker noise constant, W and L are the transistor width and length, and f is the frequency of study.

The total drain-noise current power spectral density is the sum of (5) and (6), as no correlation is supposed to exist between the white noise and the flicker noise sources.

Finally, for high frequency operation, the induced gate noise must also be considered. This noise appears because random fluctuations of the carriers (generated by the white noise) cause a gate current to flow through the gate, even if no signal current exists. The induced gate noise is written as:

$$\overline{i_g^2} = 4k_B T \delta \frac{C_{gs}^2}{5g_{d0}} 4\pi^2 f^2 \Delta f = \frac{16}{5} k_B T \delta \alpha \pi^2 \frac{C_{gs}^2}{g_m} f^2 \Delta f \tag{7}$$

where δ is the gate noise coefficient.

The gate noise is partially correlated with the drain noise due to the white noise, with a correlation coefficient c given by Van der Ziel (1986):

$$c = \frac{\overline{i_g i_{d,wn}^*}}{\sqrt{i_g^2 i_{d,wn}^2}} \tag{8}$$

For long channel MOS transistors biased in strong inversion γ is around 2/3, δ is two times γ, α approximately equal to 0.6 and |c| around to 0.4. These variables change its values when working in short-channel devices and when working in moderate and weak inversion. However, in order to simplify the explanation of the methodology, in this work these constants are fixed around the mentioned values. But, to improve the methodology results, the designer should express these constants versus g_m/I_D. Further reading on these topics can be found in the studies presented by Manghisoni, Ratti, Re, Speziali and Traversi (2006) and Scholten et al. (2004). These works quantify the constants of the power spectral densities of MOS noise sources particularly for nanometer technologies.

3. PASSIVE COMPONENT ANALYSIS

In radiofrequency design, the on-chip passive components need to be correctly characterized, as they are fundamental in the performance of the circuit. For example, in a VCO design, if it is considered an inductor model with a parasitic parallel resistor much lower that the actual one, the VCO could even not oscillate. This section briefly introduces the models and parameters of the passive components we have used in the design examples of Section 4.

We use semi-empirical models extracted from electrical simulations, the same way we do with the MOS transistor. Depending on the level of accuracy and the available technological information, we use the models provided by the foundry or the ones obtained with electromagnetic simulators as ADS Momentum™ or ASITIC (Niknejad, 2000). The two main drawbacks of electromagnetic simulators are: 1) they need the process technological data and unfortunately this information is not fully available in many cases; and 2) the large computational time. In this work, for the sake of efficiency, the former method is utilized; the library cells supplied by the foundry are simulated using AC analysis at the working frequency obtaining their equivalent complex impedance.

For the design methodology presented in this chapter, simple passive component models, as an ideal inductor in series with a parasitic resistor for on-chip inductors, will be used. Biunivocal relations between the model parameters of the component, as between the inductance and its parasitic serial resistance, are very useful to generate a simple design flow.

The extraction of these models depends on the topological location of the component, for example, if the device has an AC grounded terminal or if it is fully differential. The analysis performed with the electrical simulator logically has to reflect this fact.

Inductor modeling

In this work, inductors cells provided by the foundry are used. The extracted inductor model consists on an equivalent ideal inductor with a parasitic resistor for a particular working frequency f_0. For example, for an inductor with an AC grounded port and using the AC analysis, its serial network is found. It has a complex series impedance $R_{s,ind} + jX_{ind}$., where $R_{s,ind}$, is the series resistance and X_{ind} is its series reactance which divided by $\omega_0=2\pi f_0$, is the equivalent series inductance L_{ind}.

Depending on the function of the inductor in the circuit, a serial or a parallel resistance is chosen to describe it. For the previous example, the serial network can be transformed into a parallel network by means of the series quality factor $Q_L = X_{ind} / R_{s,ind}$. The equivalent inductance of the parallel network is $L_{p,ind} = L_{ind}(1+1/Q_L^2)$ and the parasitic resistance of the parallel network is $R_{p,ind} = R_{s,ind}(1+Q_L^2)$. For real on-chip inductors with $Q_L \geq 4$, $L_{p,ind} \approx L_{ind}$. The electrical analysis used have to be run for a large set of inductors to obtain a complete database, including L_{ind}, Q_L, $R_{s,ind}$, and $R_{p,ind}$. It is important to bear in mind that these values will change when the frequency changes or other technology corner is considered, so more than one table should be needed if any of the situations must be taken into account.

To illustrate the modeling procedure in a standard CMOS 90 nm process, extracted L_{ind}, $R_{p,ind}$, and $R_{s,ind}$ are plotted in Fig. 2, when both coil conductor width and internal diameter (hence sweeping the number of turns) are swept. The data in these plots show that in this technology the highest parasitic parallel resistances come with the largest inductor values.

Because in this work, we have considered that a good inductor is the one it has a low series resistance or a high parallel resistance, depending on its function in the circuit, we have established some particular biunivocal relations between the data of each simulated inductor in the inductor database, as the highlighted in thick line in Fig. 2. In this way, by means of computational routines, it is possible to find, for a given inductance value, the nearest inductor included in the database with the lowest series resistance or the highest parallel resistance.

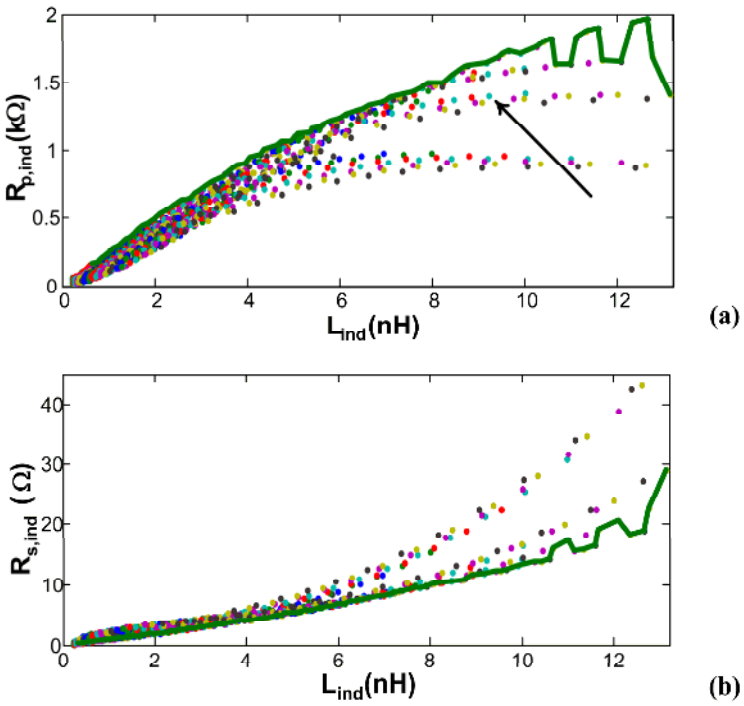

Fig. 2. (a) Parasitic parallel resistance $R_{p,ind}$ versus equivalent inductance L_{ind} varying internal inductor radius and inductor coil width and (b) Parasitic serial resistance $R_{s,ind}$ versus L_{ind} corresponding with inductors in (a).The bold line highlights the inductors with (a) the highest $R_{p,ind}$ and (b) the lowest $R_{s,ind}$.

Capacitor and Varactor modeling

As well as inductors, capacitors and varactors can be modelled as serial networks which consists of a complex series impedance $Z_{s,cap(\mathrm{var})} = R_{s,cap(\mathrm{var})} + jX_{s,cap(\mathrm{var})}$. Again, AC analysis is used to characterize these components.

For practical capacitors used in RF designs, as metal-insulator-metal type, their quality factors are considerably high –above 100 for the technology used here- when we compared them with monolithic inductors, so generally their parasitic resistances will be discarded in the initial design.

On the other hand, varactors, which are generally based on semiconductor devices, have lower quality factor -they can be comparable with high-Q on-chip inductors- and their parasitic resistances suffer from variations when the bias voltage changes the effective capacitance. As a result, an AC behavior study should be done for different biasing conditions. Because the quality factor of the varactor varies with the bias voltage, a conservative yet simple approach is to consider the lowest reachable quality factor value when the bias is swept.

4. PROPOSED DESIGN METHODOLOGY

The core of the proposed design methodology intends to give a simple way to size MOS transistors and passive components and to visualize the compromises involved in the design of an RF block. The sizing of the MOS transistors is performed by the g_m/I_D tool which uses the g_m/I_D vs. i characteristic of the transistor.

The basic idea is that each g_m/I_D is one-to-one related with a normalized current i value (Fig. 1(b)). Then, let us consider the range of g_m/I_D between 3 V^{-1} (deep strong inversion) and 25 V^{-1} (weak inversion) and, that for each g_m/I_D the drain current I_D is swept in a range of interest. So for each defined pair (g_m/I_D, I_D) the normalized current i, the transconductance g_m and the transistor W/L are known and, because the transistor length is set, for example to the technological minimum, the width W is also deduced.

This technique has been successfully applied both in simple designs with a few transistors (Shameli & Heydari, 2006; Fiorelli, Peralías & Silveira, 2011) as in complex structures (Flandre, Viviani, Eggermont, Gentinne & Jespers, 1997; Aguirre & Silveira, 2008; Tanguay & Sawan, 2009).

Despite these examples show the efficient use of the g_m/I_D tool, they lack of a systematic methodology suitable to be employed in RF blocks.

As it was sketched at the end of the chapter Introduction, four steps have to be followed to apply our design methodology for an RF block:

1. DC behavior of MOS transistor has to be captured in curves or expressions. It is necessary to measure or simulate the DC MOS characteristics (g_m, g_{ds}, I_D, C_{ij}) for a small set of transistor sizes and for all-inversion levels to generate the curves g_m/I_D, g_{ds}/I_D and C_{ij}' versus *i and W*. The parameters corresponding to the noise models should be also extracted.
2. Extracting of parameters of practicable passive components (e.g. parasitic resistances and capacitances, quality factors, effective inductances, capacitances, and resistances for inductors, capacitors, and resistors, respectively). The objective is to have one-to-one relations to get the best feasible device from its nominal value. The qualifier "best device" could be in the sense of, for example, its best quality factor or, its lowest series parasitic resistance.
3. Modeling of the most important characteristics of the RF block and then, perform the necessary modifications to the found equations in order to introduce the parameters described in the previous steps for the involved transistors, as g_m/I_D and g_{ds}/I_D.
4. Create a design flow where it is arranged the relations between the block equations, the extracted parameters and the decisions, all intended to fulfill the particular specifications of the block and technological process constraints.

The final step is the inclusion of characteristics of the circuit, modeled in a set of equations. In this way a complete design flow can be developed. In this chapter two examples are provided: a VCO and an LNA. These circuits present a small number of transistors and passive components, so it helps in developing a simple design flow to simplify the reader's comprehension.

Each example begins presenting the relevant equations of the block with no deductions because it is not the scope of this chapter; nevertheless relevant references where these circuits are carefully studied are

provided. Where necessary, equations have been modified in order to express them in terms of g_m/I_D and/or g_{ds}/I_D.

The design flows and real implementations in nanometer technologies to work under the 2.4 GHz band of the IEEE 802.15.1 and IEEE 802.15.4 standards are presented. With the design flows, implemented in a computational program, a set of design space maps are displayed in order to visualize the trade-offs between consumption and noise and to pick a design point to be fabricated. Implemented circuit simulation data and measurement results are given to show their similarity with the data provided with the methodology.

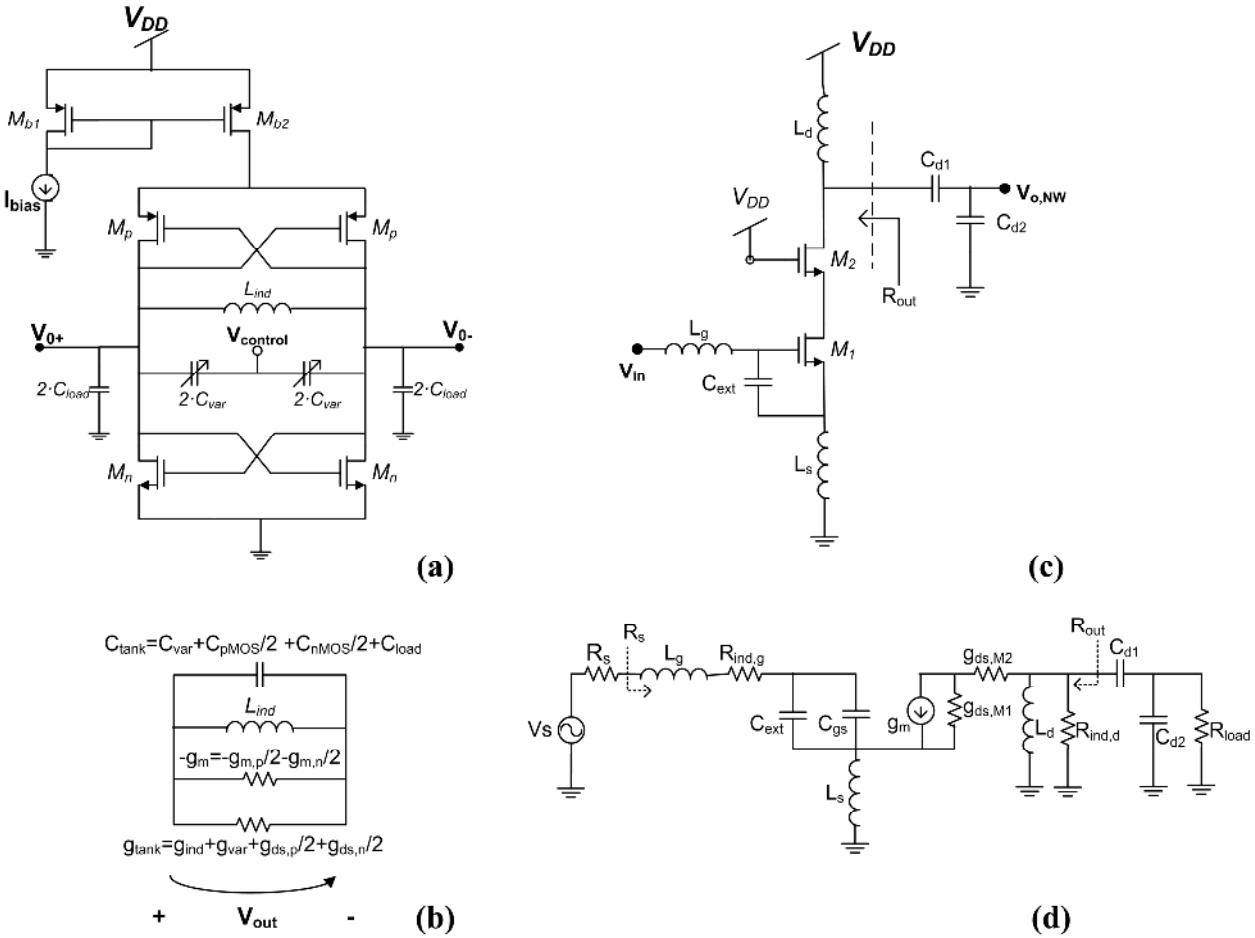

Fig. 3. (a) Complementary cross-coupled LC-VCO. (b) LC-VCO small-signal schematic. (c) Inductively degenerated CS-LNA schematic. (d) CS-LNA small-signal schematic.

4.1 VCO Example

4.1.1 VCO modeling

The VCO topology used in this example is depicted in Fig. 3(a). It shows a cross-coupled complementary VCO with an inductor-capacitor tank (LC-VCO), biased with a pMOS current mirror (M_{b1},M_{b2}). Cross-coupled transistors provide the needed negative feedback whereas a pMOS-nMOS complementary structure increases the VCO transconductance while consuming the same quiescent I_D current (with $I_{bias}=2 \cdot I_D$). A complete study of this block is developed in the work of Hershenson, Hajimiri, Mohan, Boyd and Lee (1999).

A small-signal simplified model of this LC-VCO is given in Fig. 3(b). It comprises: the effective inductance at ω_0 of the differential inductor L_{ind}, the varactor capacitance C_{var}, the parasitic capacitances of the nMOS and pMOS transistors C_{nMOS} and C_{pMOS} and the load capacitance C_{load}. The nMOS and pMOS transconductances, $g_{m,p}$ and $g_{m,n}$ are arbitrarily matched to g_m. Therefore, transistors sizing is adjusted to achieve this.

The well-known oscillation frequency and oscillation condition expressions are respectively:

$$\omega_0 = \frac{1}{\sqrt{L_{ind} C_{\tan k}}} \tag{9}$$

and

$$g_{\tan k} \leq g_{m,p}/2 + g_{m,n}/2 = g_m \tag{10}$$

where

$$C_{\tan k} = C_{var} + \frac{C_{pMOS} + C_{nMOS}}{2} + C_{load} \tag{11}$$

and

$$g_{\tan k} = g_{ind} + g_{\text{var}} + g_{ds,p}/2 + g_{ds,n}/2 \tag{12}$$

where $g_{ds,p}$ and $g_{ds,n}$ are the output parallel conductances of the nMOs and pMOs transistors; g_{ind} and g_{var} are the parasitic parallel conductances of the inductor and varactor respectively. If the MOS transistor intrinsic gain A_i is considered —defined as the ratio between g_m and g_{ds}, i.e. $A_i = g_m/g_{ds} = g_m/I_D/g_{ds}/I_D$ — and as generally g_{var} is negligible compared to g_{ind}, (12) can be rewritten as

$$g_{\tan k} \approx g_{ind} + g_{ds,p}/2 + g_{ds,n}/2 = g_{ind} + \frac{g_m}{2}\left(\frac{1}{A_{i,p}} + \frac{1}{A_{i,n}}\right) \tag{13}$$

Inequality (10) can be transformed into equality using an oscillation safety margin factor k_{osc}, which is added to guarantee the VCO oscillation despite technology or current variations. Generally, k_{osc} goes between 1.5 and 3.

$$g_m = k_{osc}\, g_{\tan k} \tag{14}$$

Merging (13) and (14), it is obtained

$$g_m = g_{ind}\left(\frac{1}{k_{osc}} - \frac{1}{2A_{i,p}} - \frac{1}{2A_{i,n}}\right)^{-1} = k'_{osc}\, g_{ind} \tag{15}$$

The differential output voltage at the tank, V_{out}, is a function of g_m/I_D and it is estimated as (Hajimiri & Lee, 1999):

$$V_{out} \approx \frac{8}{\pi}\frac{I_D}{g_{\tan k}} = \frac{8}{\pi}\frac{k'_{osc}}{g_m/I_D} \tag{16}$$

The tank quality factor is estimated as

$$Q = \frac{g_{\text{tank}}}{2\pi f_0 L_{ind}} \tag{17}$$

Phase noise (PN) is a fundamental characteristic of the VCO that describes the spectral purity around the VCO oscillation frequency f_0 (Leeson, 1966). Considering the frequency offset Δf around f_0, three asymptotic zones are currently defined: very near f_0, in the named $1/f^3$ region, the phase noise decreases proportionally to $1/\Delta f^3$ and it is directly related to the flicker noise of MOS transistors. Then appears the $1/f^2$ region where PN is inversely proportional to Δf^2, caused fundamentally by the white noise of VCO elements. Finally, far from f_0 there is a flat zone, the VCO floor noise, where the external noise sources dominate. Generally it is in the $1/f^2$ zone where the VCO phase noise is specified. The expression of the phase noise in the $1/f^2$ region, derived from the work of Hajimiri and Lee (1999) and modified to express it in terms of the g_m/I_D ratio is presented:

$$PN_{1/f^2} = 10 \cdot \log\left(k_B T \frac{\pi^2}{64} \left(\frac{\gamma}{\alpha_{eq}} + \frac{1}{k_{osc}} \right) \frac{1}{Q^2} \frac{g_m / I_D}{I_D} \left(\frac{f_0}{\Delta f} \right)^2 \right) \tag{18}$$

where k_B is the Boltzmann constant, T is the absolute temperature, Q is the tank quality factor obtained from (17), γ is the excess noise factor, and α_{eq} is defined as $\alpha_{eq} = g_m / (g_{d0,n} + g_{d0,p})$, with g_{d0} the output conductance at V_{DS}=0.

Derivation of (18) and a corresponding expression for the $1/f^3$ region can be found in Fiorelli, Peralias & Silveira (2011).

The flicker corner frequency, the asymptotic limit between $1/f^2$ and $1/f^3$ zones, is given by

$$f_{c,1/f^3} \simeq \frac{k_0}{2\pi} \frac{K'_F \alpha_{eq}}{4 k_B T \gamma} \frac{g_m}{I_D} i \frac{1}{L^2} \tag{19}$$

with $k_0 = \Gamma_{av}^2 / (2\Gamma_{rms})^2$, where Γ_{av} and Γ_{rms} are the average and the root-mean-square values of the impulse sensitivity function Γ defined in Hajimiri and Lee (1998).

4.1.2 VCO design methodology

Now that the basic equations of the VCO model have been listed, the design flow of the VCO is presented through the scheme of Fig. 4(a). Each step is itemized below:

Step 1: Lets start fixing a set of initial parameters and limits: the minimum transistor channel length L_{min}, the oscillation safety margin factor k_{osc}, a maximum equivalent inductance $L_{ind,max}$, a minimum varactor capacitance $C_{var,min}$ and C_{load}. Next, set the VCO specifications: the oscillation frequency f_0, a maximum current $I_{D,max}$, a maximum phase noise in the white noise zone $PN_{\max}$ at an offset Δf and, a minimum output voltage $V_{out,min}$.

Step 2: Pick a pair of values, an inductance L_{ind} and a g_m/I_D ratio from the technological database of inductors and transistors, which are assumed previously collected.

Step 3: From inductor database, derive the g_{ind} of the selected inductor, assuming that we have the relationship between the maximum parallel resistance versus inductance ($R_{p,ind}^{\max}$ vs. L_{ind}). Obtain

the normalized currents of nMOS and pMOS i_n and i_p as well as g_{ds}/I_D, from the picked g_m/I_D and the characteristic curves (g_m/I_D vs. i) and (g_{ds}/I_D vs. i). Calculate the intrinsic gains $A_{i,n}$ and $A_{i,p}$. Extract the transistors equivalent capacitance from C'_{nMOS} vs. i and C'_{pMOS} vs i tables.

Step 4: Deduce g_m from (15), k_{osc}' and g_{ind},. With g_m and g_m/I_D calculate the bias current I_D, and with (16) compute V_{out}. Then calculate the transistors widths W_n and W_p from i_n and i_p and I_D. Then, compute C_{nMOS} and C_{pMOS} . With (9) and (11), solve for C_{var}. Calculate the flicker frequency corner $f_{c,1/f3}$ using (19).

Step 5: If $I_D > I_{D,max}$ or $V_{out} < V_{out,min}$ or $C_{var} < C_{var,min}$ or $f_{c,1/f3} > \Delta f$, return to *Step 2* and change one or both of the values chosen; otherwise continue.

Step 6: Compute Q with (17). Then calculate the phase noise PN using (18) at the frequency offset Δf. If it surpasses PN_{max} return to *Step 2*, otherwise the design is finished.

Following these steps, we have implemented a computational routine both to obtain a VCO design and to study graphically the behavior of the current consumption and PN when we vary the inversion region (i.e. g_m/I_D) and L_{ind}. A 90 nm CMOS technology is used, and the noise parameters are set to α=0.65 and γ=0.6. Figure 4(b) presents an example of the plots obtained from the routine. This shows the behavior of the drain current I_D for different inversion zones and for a constrained set inductor values. A reduction in the drain current occurs when g_m/I_D increases, that is, when moving to weak inversion. It happens because g_m is fixed for a fixed inductor and an increment in g_m/I_D means a reduction in I_D. Figure 4(c) displays the phase noise (at an offset of 400 kHz) for different g_m/I_D and inductors values. As expected from (18), PN increases when working in moderate and weak inversion as well as when the quality factor of the tank is low.

Figures 4(b) and 4(c) show the power of this methodology, as choosing the g_m/I_D and the inductor it can be obtained jointly the I_D and the phase noise; easily visualizing their trade-offs. Another view of this idea is given in Table II where the results of designing in strong, moderate or weak inversion for a hypothetical specification of PN of -114 dBc/Hz affects the consumption, transistors and inductor size. In particular it can be seen that a minimum of consumption exists in the moderate inversion region.

PN=-114 dBc/Hz @ 400 kHz	S.I.	M.I.	W.I.
g_m/I_D , V^{-1}	7	14	23
L_{ind}, nH	11.2	4.2	1.8
R_p, kΩ	2.0	1.1	0.24
I_D, μA	410	320	840
W_n, μm	4.7	29	3400
W_p, μm	18	35	64000

Table II. Parameter values of the VCO in S.I., M.I. and W.I.

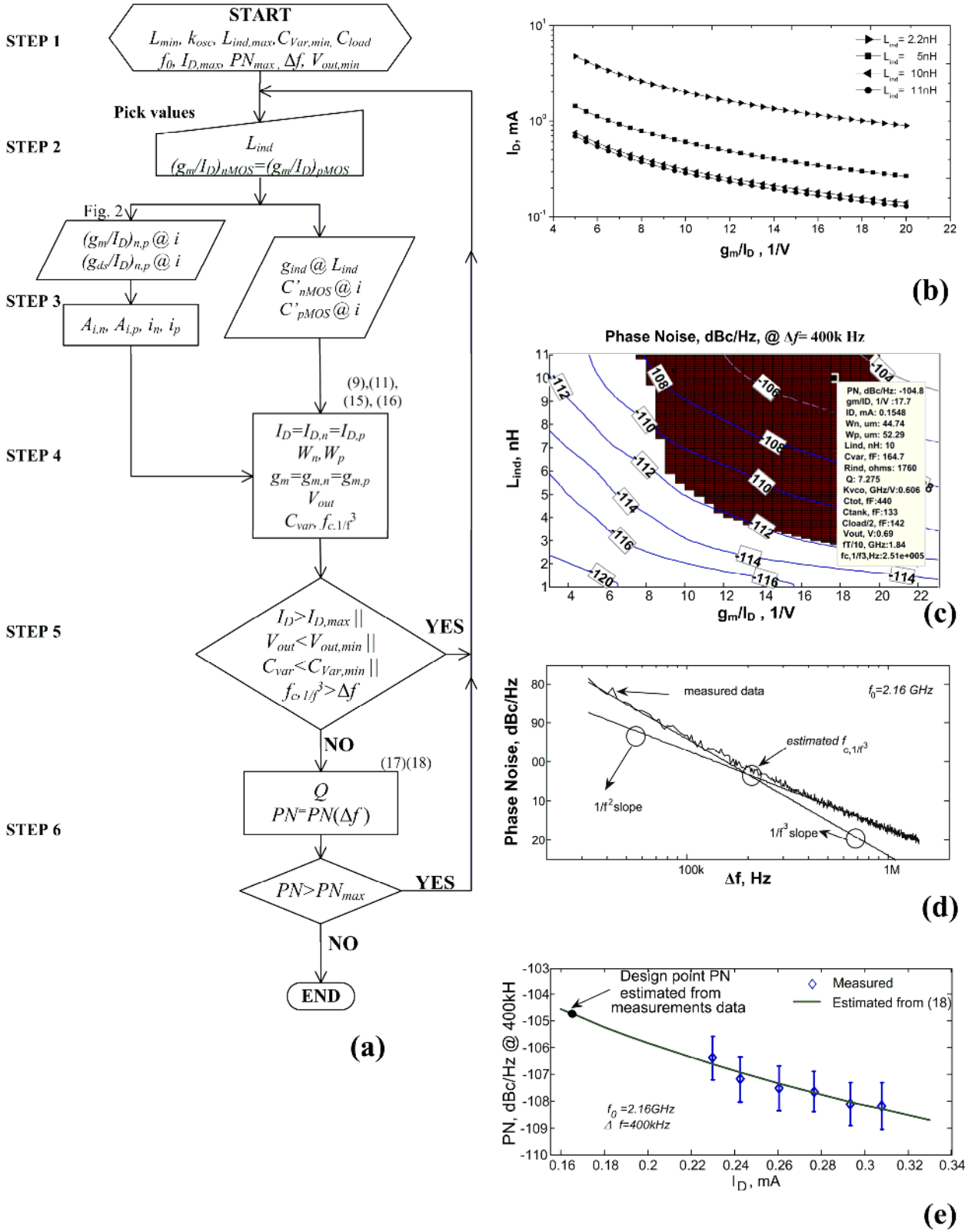

Fig. 4. (a) LC-VCO design flow. (b) I_D vs g_m/I_D for four inductor values. (c) Design space of PN at 400 kHz offset versus g_m/I_D and L_{ind}. (d) Measured PN at a central frequency of 2.16 GHz. (e) Measured PN at 400 kHz offset varying the current I_D.

4.1.3 Application example and experimental results

With the VCO methodology presented, a 2.4 GHz LC-VCO has been implemented in a 90 nm CMOS technology. An on-chip differential-pair buffer is included in the design in order to fix C_{load}. To follow the design flow presented in Section 4.1.2 the technology database (MOS data and inductor data) has been previously collected.

Using the design space of Fig. 4(c) the design displayed in the text box has been implemented. The election of this design point was focused on generating a VCO with a PN lower than -100 dBc/Hz at an offset of 400 kHz from the carrier and a total bias current I_{bias} lower than 600 μA, with $I_{bias}=2I_D$. The shadowed area shows the zone where I_{bias} complies with the latter requirement. The picked point drives an I_{bias} of 310 μA (I_D=155 μA).

With the data provided by the chosen design point, the necessary electrical simulations are performed to do small design adjustments to adapt the design to the desired oscillation frequency and oscillation condition. After the adjustments, the LC-VCO consumes an I_{bias} of 330 μA (I_D=165 μA) with phase noise of -104.3 dBc/Hz at 400 kHz from the 2.4 GHz carrier frequency. The final component sizing is: W_p=54 μm and W_n=46 μm; C_{var}=350 fF and L_{ind}=10 nH.

Measurements

A set of phase noise measurements has been done to the fabricated chip. Due to external interference with the measurement setup, the minimum bias current utilized in the measurements was I_{bias}=440 μA (I_D=220 μA). For this current, the phase noise versus the offset frequency, with the carrier at 2.16 GHz is shown in Fig. 4(d). It also shows the measured $1/f^3$ corner frequency, $f_{c,1/f3}$ which is 203 kHz, while the analytical expected one at g_m/I_D = 17.6 V^{-1} is 257 kHz.

The current I_D was also swept up to 310 μA and a set of phase noise measurements at 400 kHz from the carrier were performed, as depicted in Fig. 4(e), considering again a carrier frequency around 2.16 GHz (with slight variations due to minor changes in the parasitic capacitances of the MOS). The experimental data were fitted considering γ=0.65, α=0.55 and k_{osc} = 3. The fitted model is extended up to the nominal I_D current of 165 μA, obtaining an extrapolated *PN* value of -104.6 dBc/Hz.

4.2 LNA example

4.2.1 LNA modeling

In order to describe the methodology proposed for RF LNAs implemented in nanometer technologies, the design of an inductively degenerated common-source low noise amplifier (CS-LNA) is utilized, as shown in the schematic of Fig. 3(c). The LNA includes an external gate-source capacitor C_{ext} to provide an additional degree of freedom in the design (Andreani & Sjland, 2001). The input stage is composed by the gate inductor L_g, the source inductor L_s, the capacitor C_{ext} and the MOS transistor M_1; whereas the output stage consists of the cascode transistor M_2 and the load inductor L_d. To couple the LNA output resistance R_{out} with the load R_L it is used a matching network, consisting of capacitors C_{d1} and C_{d2}.

This design follows the idea formulated in the work of Belostotski and Haslett (2006). Here, only the parasitic series resistance of the gate inductor $R_{ind,g}$ is considered. The parasitic resistance of the source inductor, as well as the gate-bulk C_{gb} and gate-drain C_{gd} parasitic capacitances are discarded for the sake of facilitating the explanation, as the expressions are considerably simplified and the slight deviation is easily corrected with a minor adjustment in the gate inductance value (Belostotski & Haslett, 2006). To

increase as much as possible the circuit gain, the load inductor L_d is chosen to have a very high parallel resistance.

Defining C_t=C_{gs}+C_{ext} and L_t=L_g+L_s, the input impedance of the LNA is

$$Z_{in}(s) = R_{ind,g} + sL_t + \frac{1}{sC_t} + L_s\frac{g_m}{C_t} \tag{20}$$

Equation (20) can be divided into real and imaginary parts and evaluated for $s = j\omega_0$, where ω_0 is the working frequency. Assuming matching impedance between the LNA input and the purely resistive input voltage source, i.e. Z_{in}=R_s, the following expressions are obtained:

$$R_s = R_{ind,g} + L_s\frac{g_m}{C_t} \tag{21}$$

and

$$\omega_0 = 1/\sqrt{L_tC_t} \tag{22}$$

With (21) and (22) a second order equation with C_t as its unique unknown is found:

$$(R_s - R_{ind,g})\omega_0^2C_t^2 + \omega_0 g_m L_g C_t - g_m = 0 \tag{23}$$

The effective transconductance of the input stage, evaluated at ω_0, is:

$$G_{eff} = \left|G_{eff}(s)\right|_{s=j\omega_0} = \frac{g_m}{\omega_0\left(R_{ind,g}C_t + L_s g_m\right)} \tag{24}$$

Then the LNA voltage gain is

$$G = G_{eff}\frac{R_{out}}{2} \tag{25}$$

The noise factor expression in ω_0 is (Belostotski & Haslett, 2006):

$$F = \frac{R_{ind,g}}{R_s}\left(1 + \frac{\omega_0\gamma C_t}{2G_{eff}\alpha}\chi\right) \tag{26}$$

with

$$\chi = 1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\frac{C_{gs}^2}{C_t^2} + \frac{\delta\alpha^2}{5\gamma}\left(1 + \frac{1}{\omega_0^2C_t^2R_{ind,g}^2}\right)\frac{C_{gs}}{C_t} \tag{27}$$

where $|c|$, δ, α and γ are defined in Section 2.1.6.

Finally, the Noise Figure (NF) is NF_{dB} = 10 log(F).

4.2.2 LNA design methodology

The proposed design flow optimizes the Noise Figure, considering a power consumption constraint. Its objectives are the correct biasing and sizing of the MOS transistor and the dimensions of L_g, L_s and C_t.

The design flow covers all the possible pairs (g_m/I_D, I_D) with I_D below the maximum acceptable $I_{D,max}$. For each pair, it is necessary to find the gate inductor that minimizes the noise figure among all of a predetermined subset of inductors $\Lambda_L = \{L_{ind,1}, \ldots, L_{ind,j}, \ldots, L_{ind,N}\}$. For this inductor, C_{ext}, L_s and G are computed. To build Λ_L the inductors that have the highest parallel resistance are chosen from the whole set of extracted inductors.

Following the above idea, the flow diagram of the methodology is presented in Fig. 5(a). It is organized in the following steps:

Step 1: Start by setting the constraints of a minimum transistor length $L_{\min}$ and the inductor subset Λ_L, and the specifications: the working frequency ω_0, a maximum transistor bias current I_D^{max}, a maximum noise factor F_{max} and, a minimum gain G_{min}, .

Step 2: Pick a pair of I_D and g_m/I_D values, using the transistor technology database, which is assumed previously collected. Pick an inductor L_d included in Λ_L with a high parallel resistance $R_{ind,d}$.

Step 3: With the pair (g_m/I_D, I_D), and the transistor technology database (characteristic curves g_m/I_D vs. i, g_{ds}/I_D vs. i and C_{gs}' vs. i) obtain the normalized current i, the transistor width W, the output conductance g_{ds}, and C_{gs}. Calculate R_{out} with $R_{ind,d}$ and $1/g_{ds}$.

Step 4: Consider each inductor $L_{ind,j}$ of Λ_L as a possible gate inductor L_g. For each $L_{ind,j}$ evaluate its serial resistance $R_{ind,j}$ and apply (21), (24), and (26) to obtain $C_{ext,j}$, $L_{s,j}$ and NF_j. Then, consider as the gate inductor for the selection of *Step 2* the one which provides with the lowest value of NF: $NF_{\min} = \min_j \{NF_j\}$ & $j^* = \{j \mid NF_{\min} = NF_j\}$. That is $L_g = L_{ind,j^*}$, $C_{ext} = C_{ext,j^*}$

If NF_{min} is higher than NF_{max} return to *Step 2*, otherwise continue.

Step 5: Being j^* the index of the selected gate inductor in Λ_L, find in the collection Λ_L the inductor with the nearest inductance to L_{s,j^*} and with the lowest series resistance. If the source inductor is not found in Λ_L, return to *Step 2*.

Step 6: Compute the gain G using (25). If G is lower than G_{min} then return to *Step 2* and choose another pair (g_m/I_D, I_D). Otherwise, end the design.

In order to assess the performance of this design flow, we have implemented it in computational routines. In this way, we can obtain numerically the optimum noise figure for the available range of g_m/I_D versus a wide range of I_D.

We have used the database obtained from a 90 nm CMOS technology. We fix the operating frequency to 2.445 GHz, γ=4/3, δ=0.6, L_{min}=100nm, R_s=50Ω, R_{Load}=50Ω, and Λ_L a subset of the inductors of Fig. 2.

In Fig. 5(b) it is depicted the Noise Figure characteristic and the gain versus g_m/I_D and I_D. As expected, the optimum of Noise Figure respect to the power consumption is in moderate inversion. This trade-off is presented in Table III, where three design points are compared.

I_D=0.6 mA	S.I.	M.I.	W.I.
g_m/I_D, V^{-1}	5	14	19.5
W, µm	4.3	32.4	278
NF, dB	2.6	1.9	9.1
G, dB	0.4	6.6	6.6

Table III. Parameter values of the LNA in S.I., M.I. and W.I.

4.2.3 Application example and experimental results

To validate experimentally this LNA design methodology, a differential CS-LNA has been implemented in a 90 nm CMOS technology to be used in a fully differential 2.4 GHz ZigBee receiver. As initial specifications we considered I_D lower than 0.6 mA, G around 10dB, a NF lower than 5 dB, and a 1-dB compression point (P1dB) higher than -15 dBm for 100 Ω input and output impedances. To design a differential circuit based on the method proposed, we obtain the single ended design following the design flow of Fig.5(a), then we mirror the circuit to generate a differential structure. In our differential LNA we employ a differential source inductor; but the L_s calculated by the procedure is single ended; thus we use the double of this value to find a near value differential inductor included in the technology set.

To pick the final design point we use the Noise Figure-Gain space map of Fig. 5(b). The displayed text-box lists the computed components sizing, C_t value, current consumption, noise figure, gain, among others. These data were used to implement and simulate the circuit in Cadence SpectreRF.

The final simulation results of the LNA, after minor adjustments in the component sizing, show that it consumes 573 µA, has a voltage gain of 10.7 dB and a NF of 4.5 dB. The nMOS width is 92 µm, C_t/C_{gs} is 4.4, L_g is 11 nH, L_d is 10.5 nH and L_s is 1.5 nH. As expected, under post-layout conditions, only minor adjustments in component sizing were needed to reach the specifications.

Measurements

The measured S-parameters are shown in Fig. 5(c) and 5(d). The input and output networks resonant frequencies have a shift around 150MHz, visualized in traces S_{11} and S_{22}, where $|S_{11}|<$ -10 dB and $|S_{22}|<$ -10dB. These shifts reduce the gain in approximately 1 dB and increase the NF value. The LNA isolation is correct as S_{12} is below -35 dB. The gain of the LNA, represented by S_{21} in Fig. 5(c), is higher than 9dB in the specified band.

Figure 5(e) depicts the Noise Figure at the band between 2.2 GHz and 2.5 GHz. At 2.445 GHz it shows a value of 5.2 dB, with a minimum of 4.8 dB in the band of interest. This minimum is close to the expected NF value of 4.5 dB obtained in SpectreRF.

Finally, the input third order intermodulation point (IIP3) as well as the 1-dB compression point are measured. The P1dB is found to be -13 dBm. For the IIP3, we measured the amplitude of the fundamental and third order intermodulation tone, where two tones separated 1 MHz with variable amplitude are injected. Extrapolating these curves, the IIP3 is -3.5 dBm.

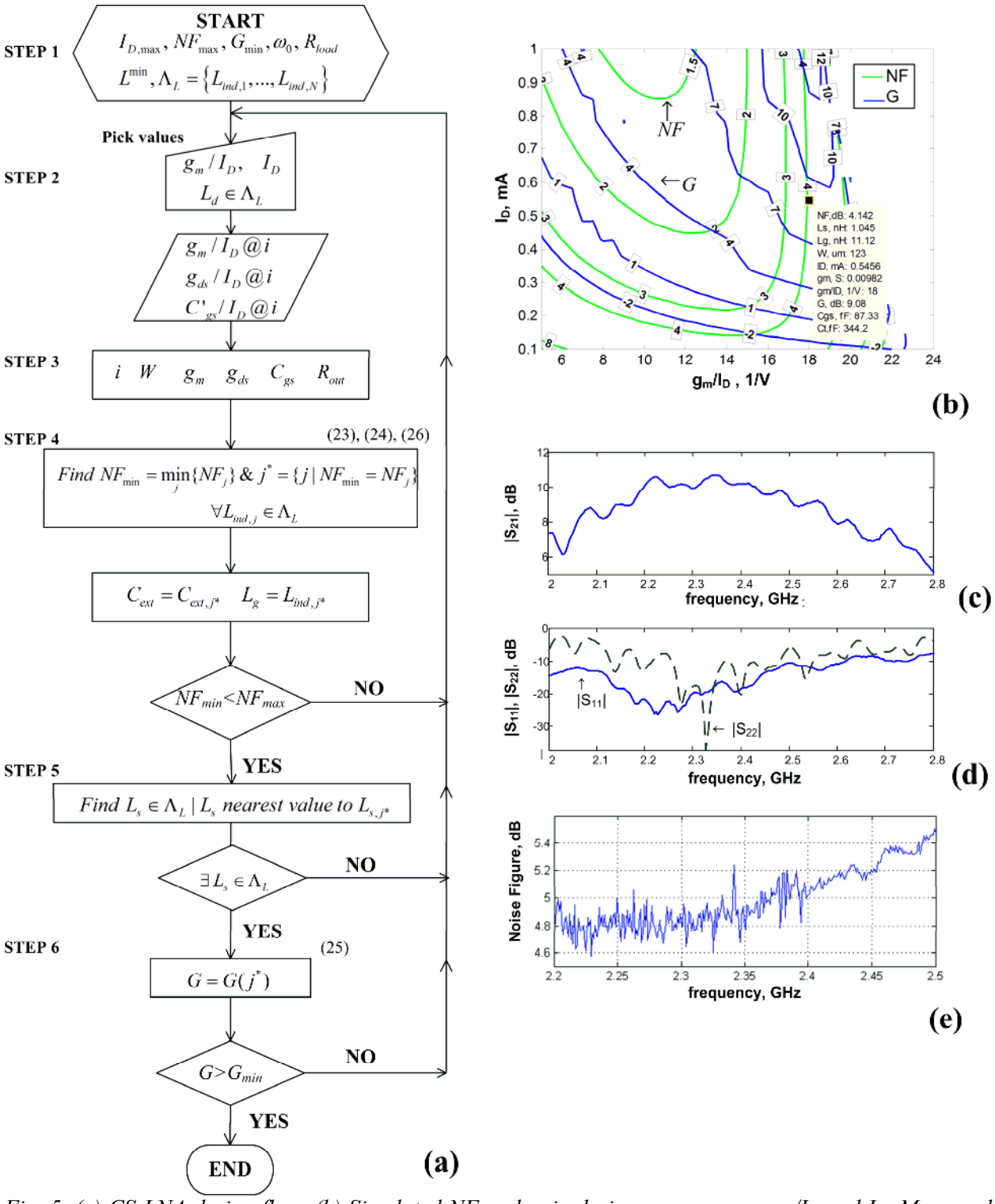

Fig. 5. (a) CS-LNA design flow. (b) Simulated NF and gain design space versus g_m/I_D and I_D. Measured S-parameters: (c) LNA gain characteristics, (S_{21}), (d) LNA matching characteristics S_{11} and S_{22}, and (e) LNA Noise Figure.

5. CONCLUSIONS

In this chapter we present a design methodology for analog radiofrequency blocks, focused to nanometer technologies and based on the g_m/I_D tool. We review the MOS model in all inversion regions, studying the curve g_m/I_D versus i and the behavior of f_T when the bias point moves from weak inversion to strong inversion. We show the importance, already highlighted by other works, of working with a MOS transistor model that covers all inversion regions of operation and therefore exploiting to its maximum the MOS transistor potential and the performance trade-offs. We show that for RF circuits integrated in nanometer technologies, the best trade-off occurs in many cases in the moderate region.

Moreover, this methodology easily presents the trade-offs involved in each particular design and the consequences of modifying the parameters of the RF block. The use of the proposed methodology reduces the design time, as little adjustments are needed after the election of the design point.

We present two examples of RF blocks in which the method is applied. We derive the specific design methodologies for a CS-LNA and an LC-VCO. The key equations of each block were adjusted to express them as a function of the g_m/I_D ratio.

For each circuit, we present how the characteristics change when we utilize a design in weak, moderate or strong inversion.

Considering particularly the VCO, we show graphically the design compromises with respect to the inversion region or the inductor choice. We see that designing in moderate and weak inversion leads to a current reduction and a Phase Noise increment; on the other hand an increment of the inductor value (and hence a raise in its parasitic parallel resistance) contributes to an improvement in the VCO spectral purity.

For the case of the LNA, the design space map is shown displaying the Noise Figure when we vary the inversion level and the drain current. Here we can also appreciate that working in moderate inversion permits to obtain a good compromise between noise figure and gain for a fixed current.

The particular design methodologies of each block are verified in measured prototypes, which show a good agreement between measurements, simulated values and computed results in the design flow.

6. REFERENCES

Aguirre, P. & Silveira, F. (2008). CMOS op-amp power optimization in all regions of inversion using geometric programming, *21st Symposium on Integrated Circuits and System Design,. SBCCI*. 152–157.

Andreani, P.& Sjland, H. (2001). Noise optimization of an inductively degenerated CMOS low noise amplifier. *IEEE Transactions on Circuits and Systems*. 48(9). 835–841.

Barboni, L., Fiorelli,R. & Silveira, F. (2006). A tool for design exploration and power optimization of CMOS RF circuit blocks. *IEEE International Symposium on Circuits and Systems, ISCAS*. 2961-2964.

Belostotski, L & Haslett, J. (2006). Noise figure optimization of inductively degenerated CMOS LNAs with integrated gate inductors. *IEEE Transactions on Circuits and Systems*. 53(7). 1409–1422.

BSIM Research Group (2009). *BSIM3v3 and BSIM4 MOS Model*. From http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html

Cunha, A., Schneider, M & Galup-Montoro, C. (1998). An MOS transistor model for analog circuit design. *IEEE Journal of Solid-State Circuits*. 33(10). 1510–1519.

Enz, C. and Vittoz, E. (2006). *Charge*-based *MOS transistor modeling*. John Wiley and Sons.

Enz, C. C., Krummenacher, F. & Vittoz, E. A. (1995). An analytical MOS transistor model valid in all regions of operation and dedicated to low voltage and low-current applications. *Analog Integrated Circuits Signal Process.*8. 83-114.

Flandre, D.,Viviani, A. Eggermont, J-P., Gentinne, B. & Jespers, P. (1997). Improved Synthesis of Gain-Boosted Regulated-Cascode CMOS Stages Using Symbolic Analysis and gm/ID Methodology. *IEEE Journal of Solid-State Circuits*. 32(7). 1006-1012.

Fiorelli, R., Peralías, E., Silveira, F. (2011), LC-VCO design optimization methodology based on the g_m/I_D ratio for nanometer CMOS technologies. *IEEE Transactions on Microwave Theory and Techniques*. 59, ISSN 0018-9480, DOI: 10.1109/TMTT.2011.2132735, (In press).

Galup-Montoro, C., Schneider, M & Cunha, A. (1999). A Current-Based MOSFET Model for Integrated Circuit Design. In E. Sánchez-Sinencio and A. Andreou (Ed), *Low Voltage/Low Power Integrated Circuits and Systems* (pp. 7-55). IEEE Press.

Gildenblat, G., Li, X., Wu, W., Wang, H., Jha, A., van Langevelde, R., Smit, G., Scholten, A. & Klaassen, D. (2006). Psp: An advanced surface potential- based MOSFET model for circuit simulation. *IEEE Transactions on Electron Devices*. 53 (9). 1979–1993.

Girardi, A. & Bampi, S. (2006). Power constrained design optimization of analog circuits based on physical gm/ID characteristics. *19th Symposium on Integrated Circuits and System Design, SBCCI*.

Jespers, P.G. (2010). The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits. Springer.

Jhon H.-S., Jung H., Koo M., Song I. & Shin, H. (2009). 0.7 V Supply Highly Linear Subthreshold Low-Noise Amplifier Design for 2-4GHz Wireless Sensor Network Applications. *Microwave and Optical Technology Letters*. 51(5).

Hajimiri, A. & Lee, T. (1998). A general theory of phase noise in electrical oscillators. *IEEE Journal of Solid-State Circuits*, 33(2). 179–194.

Hajimiri, A. & Lee, T. (1999). Design issues in CMOS differential LC oscillators. *IEEE Journal of Solid-State Circuits*. 34(5). 717–724.

Hershenson, M., Hajimiri, A., Mohan, S. Boyd, S. and Lee, T., (1999). Design and optimization of LC VCO oscillators. *IEEE/ACM International Conference on Computer-Aided Design*. 65-69.

Lee, H. & Mohammadi, S. (2007). A subthreshold low phase noise CMOS LC VCO for ultra low power applications. *IEEE Microwave and Wireless Component Letters*. 17(11).796–799.

Leeson, D. (1966). A simple model of feedback oscillator noise spectrum. *Proceedings of the IEEE*. 54. 329–330.

Manghisoni, M. , Ratti, L., Re, V., Speziali V., & Traversi, G. (2006). Noise characterization of 130nm and 90nm CMOS technologies for analog front-end electronics. *IEEE Nuclear Science Symposium Conference* .214–218.

Melly, T., Porret, A.-S., Enz, C., & Vittoz, E. (2001). An ultralow power UHF transceiver integrated in a standard digital CMOS process: Transmitter," *IEEE Journal of Solid-State Circuits*. 36(3). 467–472.

Niknejad, A. (2000). *Analysis of Si inductors and transformers for IC's (ASITIC)*. From http://rfic.eecs.berkeley.edu/ niknejad/asitic.html

Porret, A.-S., Melly, T., Python, D., Enz, C. & Vittoz, E. (2001). An ultralow -power UHF transceiver integrated in a standard digital CMOS process: Architecture and receiver. *IEEE Journal of Solid-State Circuits*, 36(3), 452–464.

Ramos, J., Mercha, A., Jeamsaksiri, W., Linten, D., Jenei, S., Rooyackers, R., Verbeeck, R., Thijs, S., Scholten, A., Wambacq, P., Debusschere, I. & Decoutere, S. (2004). 90nm RF CMOS technology for low-power 900MHz applications. *Proceedings of 34th European Solid-State Device Research conference, ESSDERC*. 329-332.

Shameli, A. & Heydari, P. (2006). A novel power optimization technique for ultra-low power RF ICs. *International Symposium on Low Power Electronics and Design, ISLPED*.

Shi, J., Xiong, Y. , Kang, K. ,Nan, L., & Lin, F. (2009). RF noise of 65-nm MOSFETs in the weak-to-moderate-inversion region. *IEEE Electron Device Letters*. 30(2) .185–188.

Scholten, A., Tiemeijer, L., van Langevelde, R., Havens, R., Zegers-van Duijnhoven, A., de Kort, R. & Klaassen, D. (2004). Compact modelling of noise for RF CMOS circuit design. *IEE Proceedings Circuits Devices Systems*. 151(2).

Silveira, F., Flandre, D., & Jespers, P. G. A. (1996), A gm/ID based methodology for the design of CMOS analog circuits and its applications to the synthesis of a silicon-on-insulator micropower OTA. *IEEE Journal of Solid-State Circuits*. 31(9). 1314–1319.

Tanguay, L-F. & Sawan, M. (2009). An ultra-low power ISM-band integer-N frequency synthesizer dedicated to implantable medical microsystems. *Analog Integr Circuits and Signal Processing*. 58. 205–214

Tsividis, Y. (2000). *Operation and Modelling of the MOS Transistor* (2nd ed.). Oxford University Press.

Van der Ziel, A., (1986). *Noise in Solid State Devices and Circuits*. New York: Wiley.

7. KEY TERMS & DEFINITIONS

Radiofrequency: Frequency working-band of the electromagnetic spectrum used in radio-communications.
Low power circuits: Circuits consuming power around or below the milliwatt.
All-inversion regions: All the MOS transistor channel inversion levels.
Sub-threshold: The bias zone of the MOS transistor channel below the threshold voltage.
Design Methodology: Systematic method used to design a system.
VCO: Voltage controlled oscillator.
LNA: Low Noise Amplifier.
CMOS: Complementary Metal Oxide Semiconductor.
Phase noise: Figure of merit to qualify the spectral purity of oscillators.
Noise figure: Figure of merit to qualify the intrinsic noisy behaviour of analog RF-blocks.
RF IC Design: design of radiofrequency integrated circuits
Transconductance: ratio between the output current of a circuit and its input voltage.
Transition frequency: the frequency where MOS current gain falls to unity.
Zigbee: communication standard defined in the standard IEEE 802.15.4
Bluetooth: communication standard defined in the standard IEEE 802.15.1.