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AN ANALYSIS OF CARRY TRANSMISSION IN COMPUTER ADDITION

Since all arithmetic operations reduce ultimately to addition, the basic consideration in designing a high speed computing automaton is fast addition; and the basic difficulty in achieving fast addition is the carry problem, inasmuch as a single carry may propagate through an entire addition. The carry problem is particularly serious in binary addition. To see why, we observe that there are four basic situations:

$$\begin{array}{r} 1 \\ 1 \\ \hline 10 \end{array} \qquad \begin{array}{r} 0 \\ 0 \\ \hline 00 \end{array} \qquad \begin{array}{r} 0 \\ 1 \\ \hline 01 \end{array} \qquad \begin{array}{r} 1 \\ 0 \\ \hline 01 \end{array}$$

The first two will not propagate carries; the second two will propagate but will not originate carries; and only the first will originate carries. Hence the probability that a randomly chosen stage in a binary addition will generate a carry is 1/4, but the probability that a randomly chosen stage will propagate a carry is 1/2. More generally, in a radix R system, there are R^2 possible situations (2^2 in binary, as we have seen) of which $1 + 2 + \ldots + R-1$ will originate carries. If we sum this arithmetic progression, we see that carries can originate in $R(R-1)/2$ ways, giving the probability $R(R-1)/2R^2$ or $(R-1)/2R$ that a randomly chosen stage will originate a carry. A carry will be propagated if and only if the units digit is R-1, which can be the sum of two digits in R different ways, so that the probability that a randomly chosen stage will propagate a carry is R/R^2 or $1/R$. A carry will, of course, be 0 or 1 regardless of the radix, because the worst possible case is $(R-1) + (R-1) = 2R - 2 = R + (R-2)$ so that the carry digit will be at most a 1, and

in that case the units digit will be at most R-2.

The probabilities that a random stage of an addition in radix R will originate a carry or propagate an incoming carry make it clear that, as the radix increases, carry generation is essentially unchanged as it approaches the limit 1/2, while carry propagation approaches 0 as 1/R. Binary addition thus gives the worst possible carry situation.

Inasmuch as computer construction generally calls for the use of binary arithmetic on account of high storage efficiency and easy mechanization, we shall consider methods of facilitating carry transmission in binary addition. To do this, we first introduce some operations of the classical two-valued logic, in which events are either "true" or "false," a pair of steady states which can be represented by 1 and 0 respectively. The operands of our logical representations will correspond to signals (0 or 1) on wires in the electronic circuitry of the computer. The operations which we wish to consider are:

Logical Operation	Logical Representation	Interpretation
1. Conjunction	$a \cdot b$ (or, ab)	a "and" b
2. Negation (Inversion)	$\bar{a}$	"not" a
3. Inclusive disjunction	$a \vee b$	a "or" b
4. Exclusive disjunction	$a \not\equiv b$	a "or" b but not both.

The arithmetic interpretation of these operations is demonstrated by the so-called truth table definitions of the operations.

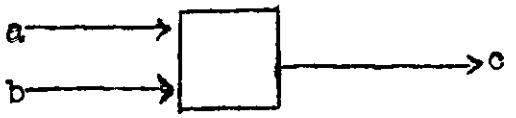
	a=o	a=1
b=o	a·b=o	a·b=o
b=1	a·b=o	a·b=1

a	$\bar{a}$
0	1
1	0

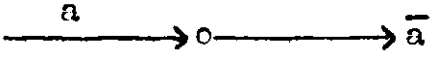
	a=o	a=1
b=o	avb=o	avb=1
b=1	avb=1	avb=1

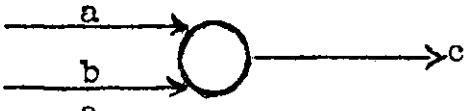
	a=o	a=1
b=o	$a \not\equiv b=o$	$a \not\equiv b=1$
b=1	$a \not\equiv b=1$	$a \not\equiv b=o$

In electronic circuitry, we shall represent these logical operations by the following diagrams:

1. Conjunction 

c=a·b

2. Negation (Inversion) 

3. Inclusive disjunction 

c=avb

4. Exclusive disjunction 

$c=a \not\equiv b$

These are the diagrams of "and", "complement", "or", and "excl-or" gates respectively. Although exclusive disjunction is usually given as a combination of other operations, we have chosen to use it as a basic operation for convenience, inasmuch as "excl-or" gates of simplicity comparable to the other gates may now be built. The logical design of a computing automaton may be described with these diagrammatic symbols.

At any given stage s_i of a binary addition, a bit (binary digit) u_i of the sum and an outgoing carry c_i (0 or 1) are developed from the corresponding bits of the augend and addend, a_i and b_i, and the incoming carry c_{i+1}. (The possibilities for such stages are subsequently tabulated). Addition may be accomplished logically in several apparently different ways, but we choose the following logical functions to define u_i and c_i:

$$u_i\ (a_i,\ b_i,\ c_{i+1}) \ = \ (a_i \not\equiv b_i) \ \not\equiv c_{i+1}$$
$$c_i\ (a_i,\ b_i,\ c_{i+1}) \ = \ a_i b_i \quad \vee \quad (a_i \not\equiv b_i)\ c_{i+1}$$

Inasmuch as the truth value tables of these logical functions correspond exactly to values for c_i and u_i given below in Table 1, the functions correctly define the carries and the bits of the sum. These logical functions are reflected in the circuit diagram for an addition unit s_i in Figure 1.

In order to add two n-bit numbers, we need either n of the individual addition units connected linearly (in parallel) as in Figure 2, or suitable delay mechanism such that one addition unit of the type shown in Figure 1 could develop the bits u_i at successive moments of time (with the a_i and b_i changing at each moment of time and the c_i of one moment being fed back in as the c_{i+1} of the next moment). The former course is much more desirable in accomplishing rapid addition. The signals a_i and b_i are then applied steadily until the number representing the sum, $u_1u_2u_3.....u_n$, reaches a steady state.

We should like to note briefly that binary subtraction may be accomplished by the unit in Figure 3 which is sufficiently similar to our addition unit that borrow transmission with our subtraction unit partakes of the same general transformations subsequently to be developed in this paper for carry transmission. Again the validity of the logical functions embodied in the circuitry may be demonstrated by truth table analysis.

A clear picture of what the carry situation is suggests alternative solutions. On one extreme, the easiest way out is simply to allow enough time for a complete carry of n places; the most difficult is to adopt a system of simultaneous carry for all digits, which

will be shown to involve a very large amount of equipment, but which will speed up the addition process considerably. Between these extremes are various other possibilities, including simultaneous carry within each successive group of m digits (where n/m is an integer) and immediate transmission of carries entering major stages S_1 (composed of several adjacent minor stages s_1) when the incoming carry will be propagated through the entire stage S_1. Thus, a sort of carry sensing is involved in the latter, to be accomplished by what we shall call "grouped" circuitry. Various other more complex methods of handling carry transmission will present themselves as we progress. For several methods of handling carries, we shall give a circuitry diagram and also seek an expression of the effective transformation as to the number of places traveled which carries undergo in such a circuitry. The effective number of places traveled by carries is, in one sense, an expression of the rapidity of an addition. For example, consider a parallel asynchronous adder in which addition times vary from t_1 to $t_1 + t_2$; essentially t_1 is the time required for an addition in which there are no carries and t_2 is the time required for a full n stage carry. Then, reducing the longest carry from n to k by some carry transformation will reduce addition time approximately to $t + \frac{k}{n} t_2$; that is, the reduction will be by $t_2 \left(\frac{n-k}{n}\right)$.

Assume that parallel addition circuitry is grouped as shown in Figure 4, each group of m addition units having an (m+1)-fold "and" gate to facilitate the transmission of carries. A carry of j places in ordinary non-grouped parallel addition circuitry becomes effectively a carry of only R places with the grouped circuitry given in Figure 4. That is, $c_j \longrightarrow c_R$.

For convenience in analysis, let us provide that $j = mk + p$,

where p is always less than m. The point of origination of a carry within some stage (or group) S_i will be denoted by σ. For origination at the first addition unit (to the left) in S_i, $\sigma = 1$; for origination at the second, $\sigma = 2$; etc. For origination at the $(m-1)$st addition unit, $\sigma = m-1$. But we shall temporarily provide that origination at the mth addition unit in S_i be denoted by $\sigma = 0$ rather than by $\sigma = m$.

For given values of J and σ, the value of R may be determined by consideration of the circuitry. Such values are given in Table 2, for the general case. The general case may be made specific by assigning a value to m. For purposes of illustration, we have given the addition circuitry and the corresponding table for m = 4. (See Figure 5 and Table 3).

It is obvious that R must be a function of j and σ; that is, $R = R(j,\sigma)$. Examination of the tables shows that we may define R thus:

$$R(j,\sigma) = j \quad \text{for} \quad j \leq m$$

$$R(j,\sigma) = R(j-1,\sigma) + 1 - (m-1)\delta_{\sigma,P_j} \quad \text{for} \quad j > m,$$

where δ_{σ,P_j} is the Kronecker delta function and p_j is that part of j which is not a multiple of m. ($j = mk + p$, $p < m$).

Inasmuch as application of this recursive formula to obtain a numerical value for R may be somewhat cumbersome, we shall simplify the functional definition of R as follows:

$$\begin{aligned} R(j,\sigma) &= 1 - (m-1)\,\delta_{\sigma,P_j} + R(j-1,\sigma) \\ R(j-1,\sigma) &= 1 - (m-1)\,\delta_{\sigma,P_{j-1}} + R(j-2,\sigma) \\ R(j-2,\sigma) &= 1 - (m-1)\,\delta_{\sigma,P_{j-2}} + R(j-3,\sigma) \end{aligned} \qquad j > m$$

$$\vdots$$

$$\vdots$$

$$R(m+1,\sigma) = 1 - (m-1)\delta_{\sigma,P_{m+1}} + R(m,\sigma)$$

$$R(m,\sigma) = m$$

Adding these equations, we obtain:

$$R(j,\sigma) = (j-m)(1) + m - (m-1)(\delta_{\sigma,P_j}+\delta_{\sigma,P_{j-1}}+\delta_{\sigma,P_{j-2}} + \cdots + \delta_{\sigma,P_{m+1}}).$$

Empirical consideration of Table 2 reveals that exactly

$$\left[\frac{j-\sigma}{m}\right]$$

of the above Kronecker delta functions have the value unity, where the brackets indicate that only the integral part of the number $\frac{j-\sigma}{m}$ is to be taken, and where we now let σ take on the value m for origination of a carry at the m-th addition unit in S_1.

The non-recursive definition of R is given, then, as:

$$R(j,\sigma) = j \qquad \text{for } 0 \leq j \leq m$$

$$R(j,\sigma) = j - (m-1)\left[\frac{j-\sigma}{m}\right] \qquad \text{for } m < j < n.$$

We may disallow the value zero for j and define R more simply as

$$R(j,\sigma) = j - (m-1)\left[\frac{j-\sigma}{m}\right] \qquad \text{for } 1 \leq j \leq n.$$

Taking the amount of time necessary for a carry to travel through one addition unit as a unit of time, we state that a j place carry is speeded up by some multiple of (m-1) units of time when the addition units are grouped, m units to a group, as shown in Figure 4, and $j - \sigma \geq m$.

Assuming that m is an integral factor of n, a carry with j = n (and σ = m, necessarily) becomes a carry of

$$n - (m-1)\left[\frac{n-m}{m}\right] \text{ or } \frac{n}{m} + m - 1 \text{ places,}$$

while a carry with $j = n-1$ and $\sigma = m$ becomes a carry of

$$(n-1) + (m-1)\left\lceil \frac{n-1-m}{m} \right\rceil \text{ or } \frac{n}{m} + 2m - 3 \text{ places,}$$

which is the longest possible carry under the given carry transformation (grouped circuitry transformation), provided that $m > 2$.

Another method of facilitating carry transmission may be found in simultaneous "wiring" of the addition circuitry. A completely simultaneous circuitry would provide the fastest carry transmission but would require many more component parts, thus entailing much greater expense and possibility of mechanical failure than the less rapid circuits. A completely simultaneous adder for $n = 4$ is shown in Figure 6a. For n addition units, this type of circuit requires $n(n-1)/2$ multi-fold "and" gates in addition to the 5n two-input gates necessary for addition with linear carry transmission (i.e., 2n "and" gates, 2n "excl-or" gates, and n "or" gates).

The simultaneous carry principle may be effectively used in another way, however. The n addition units of an adder may be divided into n/m stages, each stage having simultaneous carry transmission within that stage. This type of circuitry provides all the benefits of the grouped circuitry (Figure 4) and in addition gives more rapid carry transmission within the individual stages. A diagram of a simultaneous carry stage is given in Figure 6.

Let us say that a carry of j places in ordinary linear circuitry becomes effectively a carry of N places with circuitry having simultaneous stages (linearly connected). Once again, we introduce σ, a position variable, to indicate the point of origination of a carry within a given stage: $1 \leq \sigma \leq m$. Some of the values of σ and j are systematically tabulated in Table 4 for general m and in Table 5 for

$m = 4$.

By empirical consideration of these tables, we define N as follows:

$$N(j,\sigma) = N(j-1,\sigma) + \delta_{\sigma,P_{j-1}} \qquad \text{for } j>m,$$

where $\delta_{\sigma,P_{j-1}}$ is the Kronecker delta function and P_{j-1} is that part of $(j-1)$ which is not a multiple of m. (As before, $j = mk + p$, $p<m$);

$$N(j,\sigma) = 2 + \sum_{x=2}^{j-1} \delta_{\sigma,x} \qquad \text{for } 2<j\leq m,$$

and $$N(j,\sigma) = j \qquad \text{for } 0\leq j<2.$$

To obtain a non-recursive definition of N over the range $m<j\leq n$, we observe that:

$$\begin{aligned}
N(j,\sigma) &= N(j-1,\sigma) + \delta_{\sigma,P_{j-1}} \\
N(j-1,\sigma) &= N(j-2,\sigma) + \delta_{\sigma,P_{j-2}} \\
N(j-2,\sigma) &= N(j-3,\sigma) + \delta_{\sigma,P_{j-3}} \\
N(j-3,\sigma) &= N(j-4,\sigma) + \delta_{\sigma,P_{j-4}} \\
&\vdots \\
N(m+1,\sigma) &= N(m,\sigma) + \delta_{\sigma,P_m} \\
N(m,\sigma) &= 2 + \sum_{x=2}^{m-1} \delta_{\sigma,x} \quad .
\end{aligned}$$

Adding these equations, we obtain

$$N(j,\sigma) = 2 + \sum_{y=m}^{j-1} \delta_{\sigma,P_y} + \sum_{x=2}^{m-1} \delta_{\sigma,x} \qquad \text{for } j>m.$$

An alternative empirically formed definition of N for $j>m$ is

$$N(j,\sigma) = 3 - \delta_{\sigma,1} + \left[\frac{j-\sigma-1}{m}\right],$$

where the brackets indicate that only the integral part of the

number $\left[\frac{j-\sigma-1}{m}\right]$ is to be taken. Since the latter is the more convenient formula to apply, we shall use the following definition of the simultaneous-stage carry transformation:

$$N(j,\sigma) = j \qquad 0 \leq j \leq 2$$

$$N(j,\sigma) = 2 + \sum_{x=2}^{j-1} \delta_{\sigma,x} \qquad 2 < j \leq m$$

$$N(j,\sigma) = 3 - \delta_{\sigma,1} + \left[\frac{j-\sigma-1}{m}\right] \qquad m < j \leq n.$$

Having considered the basic stages S_1, let us now briefly consider macro-stages Σ_β, each composed of q of the S_1. The effectiveness of such a macro-stage lies, of course, in its ability to transmit relatively long carries very rapidly. The type of analysis needed to define the carry transformation from a table of its values is already familiar. However, we must introduce a new position variable, τ, to denote the S_1 of Σ_ϕ within which a carry originates. For origination in the first S_1 to the left in Σ_ϕ, $\tau = 1$. etc. $1 \leq \tau \leq q$.

Let us take q grouped stages S_1 and combine them into a grouped macro-stage Σ_ϕ. We shall designate the resulting carry transmission circuitry as grouped grouped (giving first the type of macro-stage and then the type of component stages). This type of circuitry is shown in Figure 7, and values of its characteristic carry transformation are given in Table 6 for the general case. This general case may be specifically illustrated by assigning values to q and m. A carry of j places in ordinary linear circuitry becomes a carry of T places in grouped grouped circuitry, and T is obviously a function of j, σ, and τ. That is, $T = T(j,\sigma,\tau)$.

From empirical consideration of Table 6, we observe that the following recursive function gives the appropriate values of T:

$$T(j,\sigma,\tau) = T(j-1,\sigma,\tau) + 1 - (m-1)(1 - \delta_{\tau-1,k}) - (m+q-2)\,\delta_{\tau-1,k}\,\delta_{\sigma p} \qquad j > m$$

$$T(m,\sigma,\tau) = m$$

where $\sigma = o$ for carry origination at the mth unit in S_1

We may derive a non-recursive definition in the manner previously demonstrated. A non-recursive definition of T is, then:

$$T(j,\sigma,\tau) = j - (m-1)\left[\frac{j-\sigma}{m}\right] - (q-1)\left[\frac{j-(\tau-1)\,m-\sigma}{mq}\right] \qquad \begin{matrix} j > 0 \\ 1 \leq \sigma \leq m. \end{matrix}$$

It is quite apparent that we may form a grouped macro-stage in which the S_1 are simultaneous stages and a simultaneous macro-stage in which the S_1 are either simultaneous or grouped. That is, we may construct grouped simultaneous, simultaneous simultaneous, and simultaneous grouped carry transmission circuits as well as the grouped grouped circuitry, making use of macro-stages Σ_ρ. Other possibilities include the construction of hybrid macro-stages in which some S_1 are grouped, some simultaneous, and/or some linear as well as the construction of even larger stages consisting of some combination of macro-stages Σ_ϕ. * In each case, we might follow the type of analysis used heretofore: after drawing the circuitry, we could construct tables characterizing the carry transformation embodied in the circuitry and then obtain an empirical formulation of that transformation.

* Note: In the construction of hybrid stages mentioned above, a probabilistic analysis of the carry problem is invaluable in determining the strategic location of the various types of stages along the carry transmission line, so as to facilitate a profitable compromise between rapidity of addition and economy of construction of the

After considering these transformations, we should also note that the speed of computer addition may be increased by a sensing device for the completion of all carries. In the case of an asynchronous parallel adder with addition times varying between t_1 and $t_1 + t_2$ (as previously considered), this procedure would reduce the average time in terms of the longest expected carry to $t_1 + \{t_2 \cdot (\log_2 n/n)\}$ since the longest expected carry in binary addition is less than $\log_2 n$ for n bits. This is a rather pessimistic bound for the average time; with forty bits the actual figure is about $t_1 + 1.15t_2$. Thus some of our carry transformations are virtually equivalent to sensing completion of carries, and some of them are better. The transformations have the further advantage that there is much less dispersion about the average value when they are used; with carry sensing there can still be from 0 to n carries while with carry transformations $c_n \rightarrow c_x$ and X is the longest possible carry.

Actually, the two approaches may be combined, in which case the longest possible carry now becomes c_x where $c_n \rightarrow c_x$ under the transformation. If the longest expected carry for the system is C_E, then the transformation sends $C_E \rightarrow C_j$, so that C_j is the longest expected carry in the transformed system. Since $4 < E < 5$ for most reasonable binary computers, the transformation tables included with this paper show what happens when a combination of carry transformation and carry sensing is used; addition time becomes $t_1 + t_2 (Cj/n)$.

(Note - continued)

circuit. Such an analysis is briefly undertaken in S. G. Campbell's Numerical Analysis, now being prepared for prepared for publication. One particularly interesting result of this analysis gives the probability that a carry will be emitted from any given stage of an addition, whether from origination in that stage or from propagation of a carry originated in some previous stage. Thus, it is shown that, in radix R, adding two n digit numbers with circuitry having each m

Finally, we should like to note that such results as are developed in this paper make it possible to transform immediately any information about ordinary binary carry into equivalent information about any transformed circuit. For this reason, the analysis of carry transformations is quite valuable in approaching the general problem of carry transmission in computer addition.

Some characteristics of some of the carry transforming circuits which we have mentioned in this paper are tabulated below.

(Note - continued)

of the basic addition units combined into a stage S_i, with σ the position variable as heretofore used and i the number of the major stage, $1 \leq i \leq n/m$, the probability of carry emission from the $(\sigma+1)$st unit of the ith stage is

$$\frac{1 - R^{m(i-1) + \sigma - n}}{2}$$

Transformation	Longest Possible Carry Under the Transformation	Amount of Equipment
Linear $c_j \rightarrow c_j$	$j = n$	2n "excl-or" gates 2n "and" gates n "or" gates
Grouped $c_j \rightarrow c_R$	$R = 2m - 3 + n/m$	2n "excl-or" 2n "and" n "or" n/m (m+1)-fold "and"
Completely simultaneous $c_j \rightarrow c_1 \vee 2$	2	2n "excl-or" 2n "and" n "or" n(n-1)/2 multi-fold "and"
Simultaneous stages $c_j \rightarrow c_N$	$N = 1 + n/m$	2n "excl-or" 2n "and" n "or" n(m-1)/2 multi-fold "and"
Grouped Grouped $c_j \rightarrow c_T$	$T = 2m + 2q - 5 + n/mq$	2n "excl-or" 2n "and" n "or" n(q+1)/mq multi-fold "and"
Simultaneous Simultaneous $c_j \rightarrow c_V$	$V = 3 + n/mq$	2n "excl-or" 2n "and" n "or" n(m-1)/2 + n(q-1)/2m multi-fold "and"

$$R(j,\sigma) = j - (m-1)\left[\frac{j-\sigma}{m}\right] \quad \text{for } 1 \leq j \leq n$$

$$N(j,\sigma) = j \quad \text{for } 0 \leq j \leq 2$$

$$N(j,\sigma) = 2 + \sum_{x=2}^{j-1} \delta_{\sigma,x} \quad \text{for } 2 < j \leq m$$

$$N(j,\sigma) = 3 - \delta_{\sigma,1} + \left[\frac{j-\sigma-1}{m}\right] \quad \text{for } m < j \leq n.$$

$$T(j,\sigma,\tau) = j - (m-1)\left[\frac{j-\sigma}{m}\right] - (q-1)\left[\frac{j-(\tau-1)m-\sigma}{mq}\right] \text{ for } 1 \leq j \leq n$$

TABLE 1

Augent	0	0	0	0	1	1	1	1
Addend	0	0	1	1	0	0	1	1
Carry	0	1	0	1	0	1	0	1
	00	01	01	10	01	10	10	11

(First digit in each pair is the outgoing carry; second is the units digit of the sum in the given position.)

TABLE 2

$j = nk + p$		$\sigma = 1$	$\sigma = 2$	. . . . .	$\sigma = m-1$	$(\sigma = 0)$ $\sigma = m$
$k = 0$	$p = 0$	$R = 0$	$R = 0$		$R = 0$	$R = 0$
	1	1	1		1	1
	2	2	2		2	2
	.					
	.					
	$m-1$	$m-1$	$m-1$	. . . . .	$m-1$	$m-1$
$k = 1$	$p = 0$	m	m	. . . . .	m	m
	1	2	$m+1$		$m+1$	$m+1$
	2	3	3		$m+2$	$m+2$
	.					
	.					
	$m-1$	m	m	. . . . .	m	$m+m-1$
$k = 2$	$p = 0$	$m+1$	$m+1$	. . . . .	$m+1$	$m+1$
	1	3	$m+2$		$m+2$	$m+2$
	2	4	4		$m+3$	$m+3$
	.					
	.					
	$m-1$	$m+1$	$m+1$	. . . . .	$m+1$	$m+m$
$k = 3$	$p = 0$	$m+2$	$m+2$	. . . . .	$m+2$	$m+2$
	1	4	$m+3$		$m+3$	$m+3$
	2	5	5		$m+4$	$m+4$
	.					
	.					
	$m-1$	$m+2$	$m+2$	. . . . .	$m+2$	$m+m+1$
.						
.						
.						
.						
.						
$k = \frac{n}{m} - 1$	$p=0$	$m+\frac{n}{m}-2$	$m+\frac{n}{m}-2$	. . . . .	$m+\frac{n}{m}-2$	$m+\frac{n}{m}-2$
	1	n/m	$m-1+n/m$		$m-1+n/m$	$m-1+n/m$
	2	$1+n/m$	$1+n/m$		$m+n/m$	$m+n/m$
	.					
	.					
	$m-1$	$m-2+\frac{n}{m}$	-----	. . . . .	-----	-----

m = 4

TABLE 3

$j = 4k + p$	$\sigma = 1$	$\sigma = 2$	$\sigma = 3$	$(\sigma = 0)$ $\sigma = 4$
$k = 0$ $p = 0$	R = 0	R = 0	R = 0	R = 0
1	1	1	1	1
2	2	2	2	2
3	3	3	3	3
$k = 1$ $p = 0$	4	4	4	4
1	2	5	5	5
2	3	3	6	6
3	4	4	4	7
$k = 2$ $p = 0$	5	5	5	5
1	3	6	6	6
2	4	4	7	7
3	5	5	5	8
$k = 3$ $p = 0$	6	6	6	6
1	4	7	7	7
2	5	5	8	8
3	6	6	6	9
.				
.				
.				
.				
.				
.				
$k = 9$ $p = 0$	12	12	12	12
1	10	13	13	(13)
2	11	11	(14)	(14)
3	12	(12)	(12)	(15)

TABLE 4

$j = nk + p$	$p<n$	$\sigma = 1$	$\sigma = 2$	.....	$(\sigma = 0)$ $\sigma = n$
$k = 0$	$p = 0$	$0 = N$	$0 = N$	.....	$0 = N$
	1	1	1		1
	2	2	2		2
	.				
	.				
	$n-1$	2	3		2
$k = 1$	$p = 0$	2	3	.....	2
	1	2	3		3
	2	3	3		3
	.				
	.				
	$n-1$	3	4		3
$k = 2$	$p = 0$	3	4	.....	3
	1	3	4		4
	2	4	4		4
	.				
	.				
	$n-1$	4	5		4
$k = 3$	$p = 0$	4	5	.....	4
	1	4	5		5
	2	5	5		5
	.				
	.				
	$n-1$	5	6		5
$k = 4$	$p = 0$	5	6	.....	5
	1	5	6		6
	2	6	6		6
	.				
	.				
	$n-1$	6	7		6
.				.....	
.					
.					
.					
.					
.					
.					

TABLE 5

$j = 4k + p$ $p < n$	$\sigma = 1$	$\sigma = 2$	$\sigma = 3$	$(\sigma = 0)$ $\sigma = 4$
$k = 0$ $p = 0$	$N = 0$	$N = 0$	$N = 0$	$N = 0$
1	1	1	1	1
2	2	2	2	2
3	2	3	2	2
$k = 1$ $p = 0$	2	3	3	2
1	2	3	3	3
2	3	3	3	3
3	3	4	3	3
$k = 2$ $p = 0$	3	4	4	3
1	3	4	4	4
2	4	4	4	4
3	4	5	4	4
$k = 3$ $p = 0$	4	5	5	4
1	4	5	5	5
2	5	5	5	5
3	5	6	5	5
$k = 4$ $p = 0$	5	6	6	5
1	5	6	6	6
2	6	6	6	6
3	6	7	6	6
	.	.	.	.
	.	.	.	.
	.	.	.	.
	.	.	.	.
	.	.	.	.

$\tau = 1$ TABLE 6 $\tau = 2$ . . .

h	k	p	$\sigma = 1$	$\sigma = 2$	. .	$\sigma = m$	$\sigma = 1$	$\sigma = 2$	. .	$\sigma = m$	. .	. .
0	0	0	0	0	. . .	0	0	0	. . .	0	. .	. .
0	0	1	1	1		1	1	1		1		
0	0	2	2	2		2	2	2		2		
.	.	.	.	.		.	.	.		.		
0	0	m-1	m-1	m-1	. . .	m-1	m-1	m-1	. . .	m-1	. .	. .
0	1	0	m	m	. . .	m	m	m	. . .	m	. .	. .
0	1	1	2	m+1		m+1	2	m+1		m+1		
0	1	2	3	3		m+2	3	3		m+2		
.	.	.	.	.		.	.	.		.		
0	1	m-1	m	m	. . .	m+m-1	m	m	. . .	m+m-1	. .	. .
0	2	0	m+1	m+1	. . .	m+1	m+1	m+1	. . .	m+1	. .	. .
0	2	1	3	m+2		m+2	3	m+2		m+2		
0	2	2	4	4		m+3	4	4		m+3		
.	.	.	.	.		.	.	.		.		
0	2	m-1	m+1	m+1	. . .	m+m	m+1	m+1	. . .	m+m	. .	. .
.	.	.	.	.		.	.	.		.		
0	q-1	0	m+q-2	m+q-2	. . .	m+q-2	m+q-2	m+q-2	. . .	m+q-2	. .	. .
0	q-1	1	q	m+q-1		m+q-1	q	m+q-1		m+q-1		
0	q-1	2	q+1	q+1		m+q	q+1	q+1		m+q		
.	.	.	.	.		.	.	.		.		
0	q-1	m-1	m+q-2	m+q-2	. . .	2m+q-3	m+q-2	m+q-2	. . .	2m+q-3	. .	. .
1	0	0	m+q-1	m+q-1	. . .	m+q-1	m+q-1	m+q-1	. . .	m+q-1	. .	. .
1	0	1	2	m+q		m+q	q+1	m+q		m+q		
1	0	2	3	3		m+q+1	q+2	q+2		m+q+1		
.	.	.	.	.		.	.	.		.		
1	0	m-1	m	m	. . .	2m+q-2	m+q-1	m+q-1	. . .	2m+q-2	. .	. .
1	1	0	m+1	m+1	. . .	m+1	m+q	m+q	. . .	m+q	. .	. .
1	1	1	3	m+2		m+2	3	m+q+1		m+q+1		
1	1	2	4	4		m+3	4	4		m+q+2		
.	.	.	.	.		.	.	.		.		
1	1	m-1	m+1	m+1	. . .	m+m	m+1	m+1	. . .	2m+q-1	. .	. .
1	2	0	m+2	m+2	. . .	m+2	m+2	m+2	. . .	m+2	. .	. .
1	2	1	4	m+3		m+3	4	m+3		m+3		
1	2	2	5	5		m+4	5	5		m+4		
.	.	.	.	.		.	.	.		.		
1	2	m-1	m+2	m+2	. . .	m+m+1	m+2	m+2	. . .	m+m+1	. .	. .
.	.	.	.	.		.	.	.		.	.	.
.	.	.	.	.		.	.	.		.	.	.
.	.	.	.	.		.	.	.		.	.	.
1	q-1	0	m+q-1	m+q-1	. . .	m+q-1	m+q-1	m+q-1	. . .	m+q-1	. .	. .
1	q-1	1	q+1	m+q		m+q	q+1	m+q		m+q		
1	q-1	2	q+2	q+2		m-q-1	q+2	q+2		m+q-1		
.	.	.	.	.		.	.	.		.		
1	q-1	m-1	m+q-1	m+q-1	. . .	2m+q-2	m+q-1	m+q-1	. . .	2m+q-2	. .	. .

TABLE 6 (Continued)

$\tau = 1$ $\tau = 2$

h	k	p	$\sigma = 1$	$\sigma = 2$	. .	$\sigma = m$	$\sigma = 1$	$\sigma = 2$	. .	$\sigma = m$	. .	. .
2	0	0	m+q	m+q	. .	m+q	m+q	m+q	. .	m+q	. .	. .
2	0	1	3	m+q+1		m+q+1	q+2	m+q+1		m+q+1		
2	0	2	4	4		m+q+2	q+3	q+3		m+q+2		
.	.	.	.	.		.	.	.		.		
.	.	.	.	.		.	.	.		.		
2	0	m-1	m+1	m+1	. .	2m+q-1	m+q	m+q	. .	2m+q-1	. .	. .
2	1	0	m+2	m+2	. .	m+2	m+q+1	m+q+1	. .	m+q+1	. .	. .
2	1	1	4	m+3		m+3	4	m+q+2		m+q+2		
2	1	2	5	5		m+4	5	5		m+q+3		
.	.	.	.	.		.	.	.		.		
.	.	.	.	.		.	.	.		.		
2	1	m-1	m+2	m+2	. .	m+m-1	m+2	m+2	. .	m+m+q	. .	. .
.	.	.	.	.		.	.	.		.	.	.
.	.	.	.	.		.	.	.		.	.	.
.	.	.	.	.		.	.	.		.	.	.
3	0	0	m+q+1	m+q+1	. .	m+q+1	m+q+1	m+q+1	. .	m+q+1	. .	. .
3	0	1	4	m+q+2		m+q+2	q+3	m+q+2		m+q+2		
3	0	2	5	5		m+q+3	q+4	q+4		m+q+3		
.	.	.	.	.		.	.	.				
.	.	.	.	.		.	.	.				
3	0	m-1	m+2	m+2	. .	2m+q	m+q+1	m+q+1	. .	2m+q	-	-
3	1	0	m+3	m+3		m+3	m+q+2	m+q+2		m+q+2	. .	. .
3	1	1	5	m+4		m+4	5	m+q+3		m+q+3		
3	1	2	6	6		m+5	6	6		m+q+4		
.	.	.	.	.		.	.	.		.		
.	.	.	.	.		.	.	.		.		
3	1	m-1	m+3	m+3		m+m+2	m+3	m+3		2m+q+1	. .	. .
.	.	.	.	.		.	.	.		.	. .	. .
.	.	.	.	.		.	.	.		.	. .	. .
.	.	.	.	.		.	.	.		.	. .	. .

$k < q$
$p < m$
$j = mqh + mk + p$

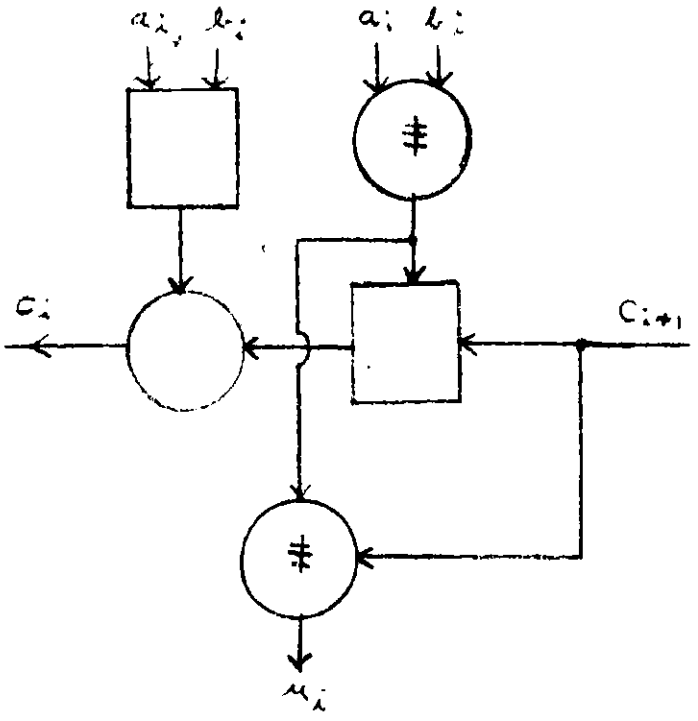


FIGURE 1
Addition Unit

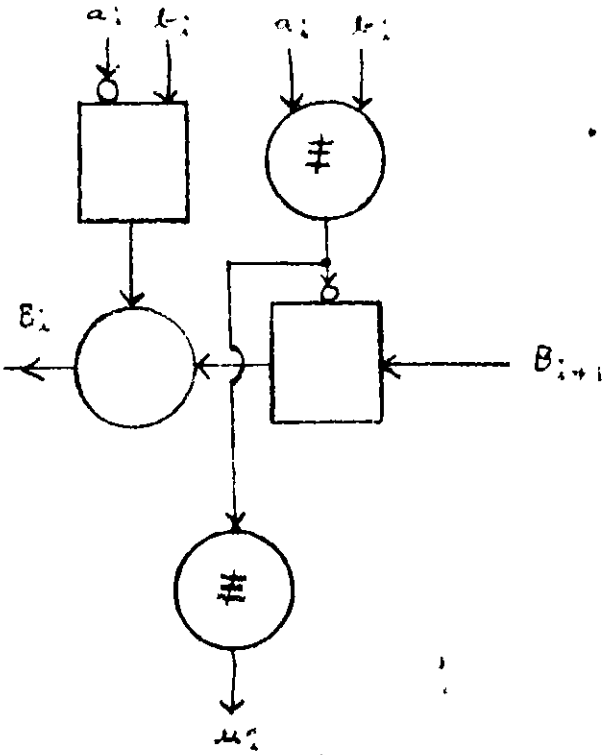


FIGURE 3
Subtraction Unit

Note: because of the similarity of Figure 1 to Figure 3, the carry of Figure 1 is the same as the borrow of Figure 3 for the same inputs a_i, b_i; hence the analysis of this paper applies equally well to both borrow transmission in subtraction and carry transmission in addition, and in general, any analysis of carry probabilities becomes automatically an analysis of borrow probabilities.

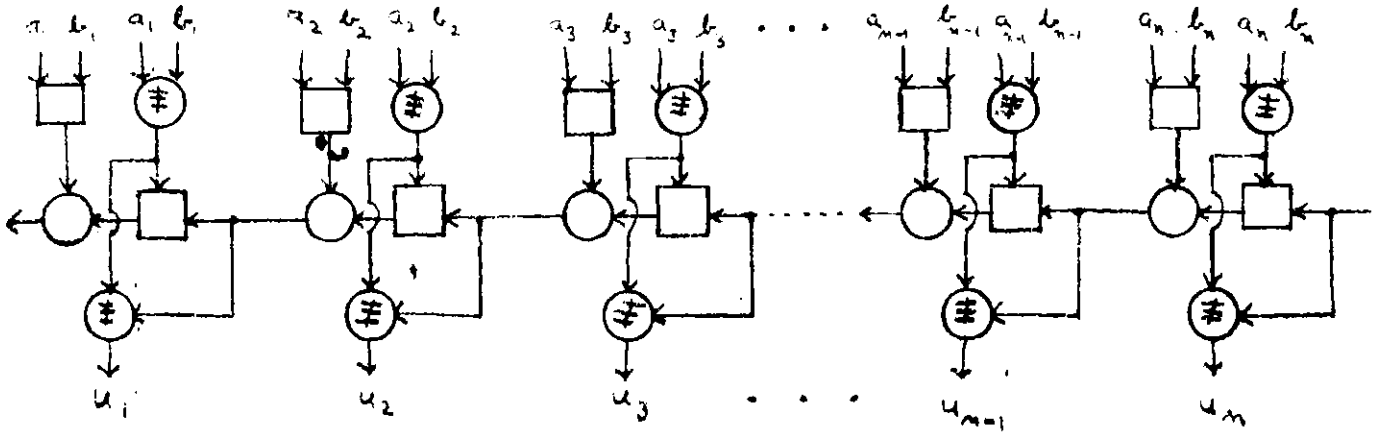


FIGURE 2 Addition Units — Linear

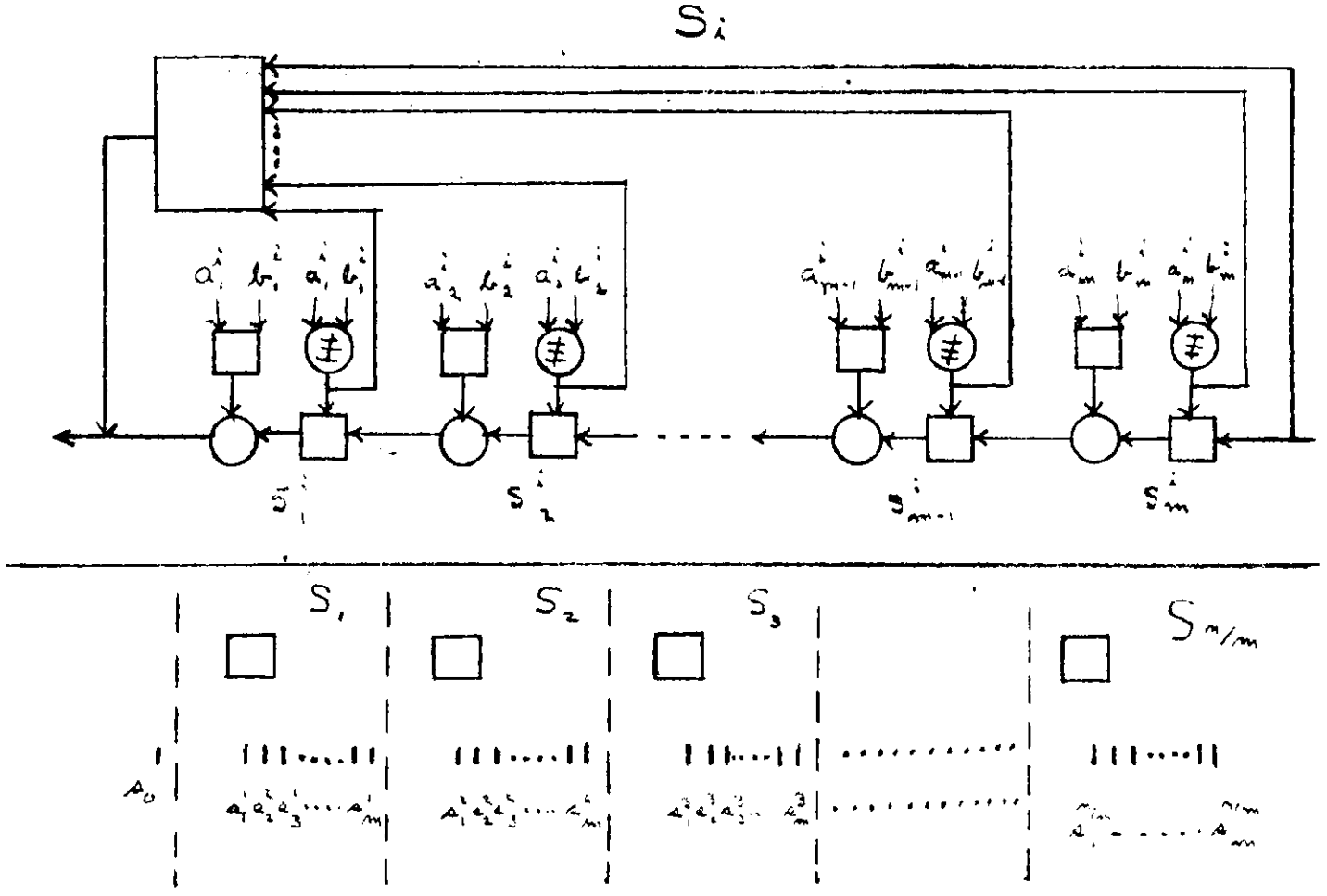


Figure 4

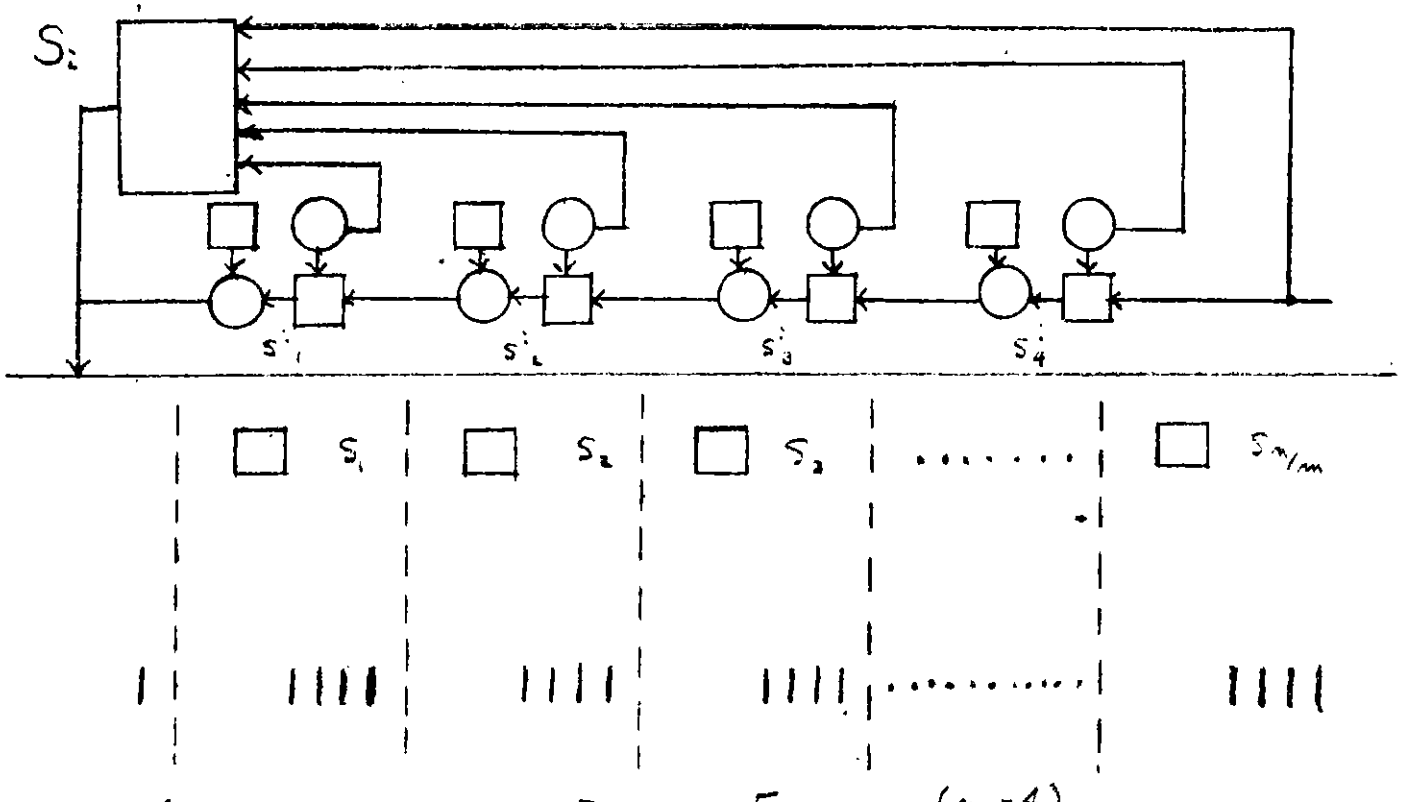


Figure 5 ($m = 4$)

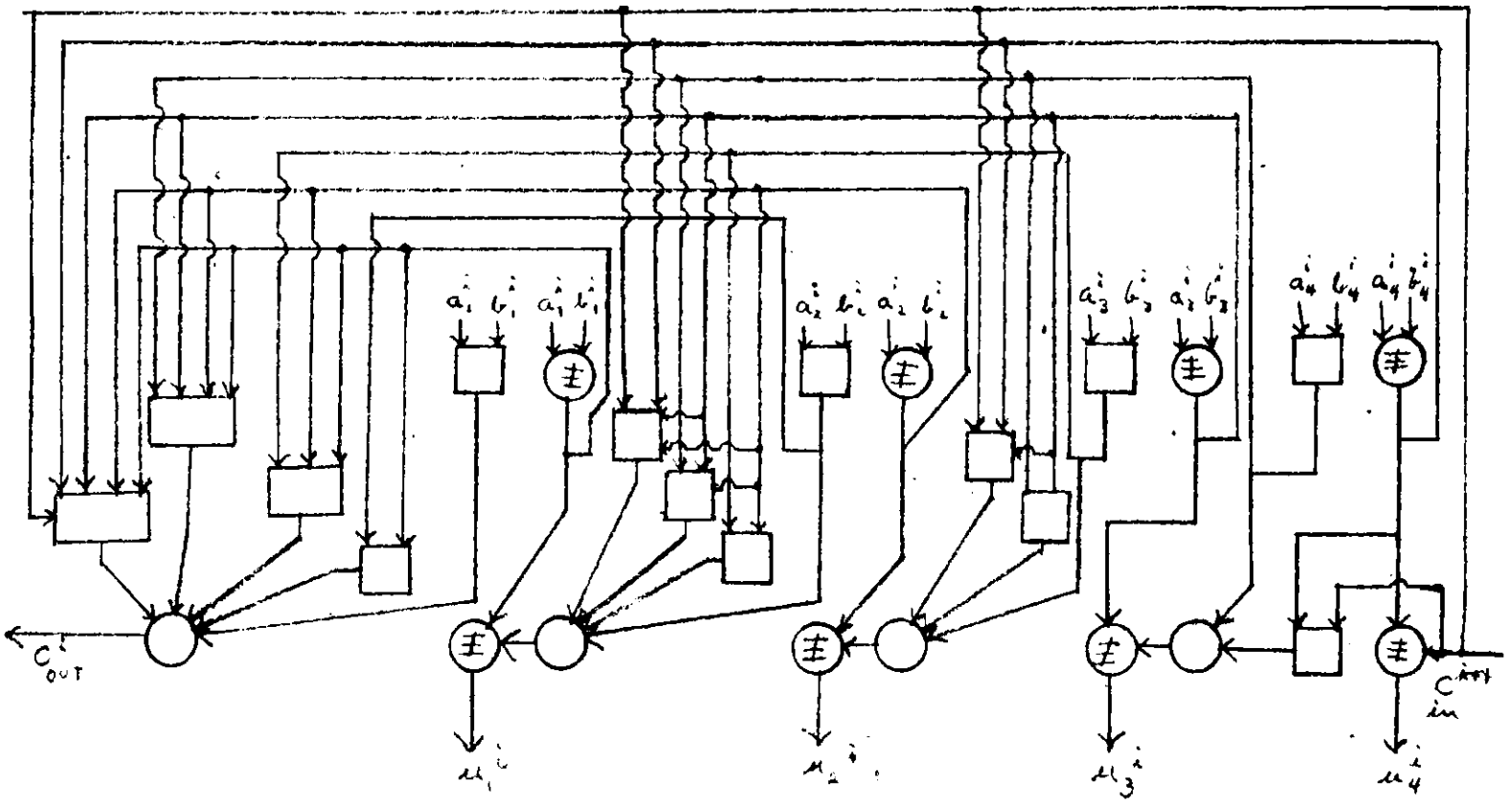


Figure 6a Carry Transmission in a Simultaneous Adder (n = 4)

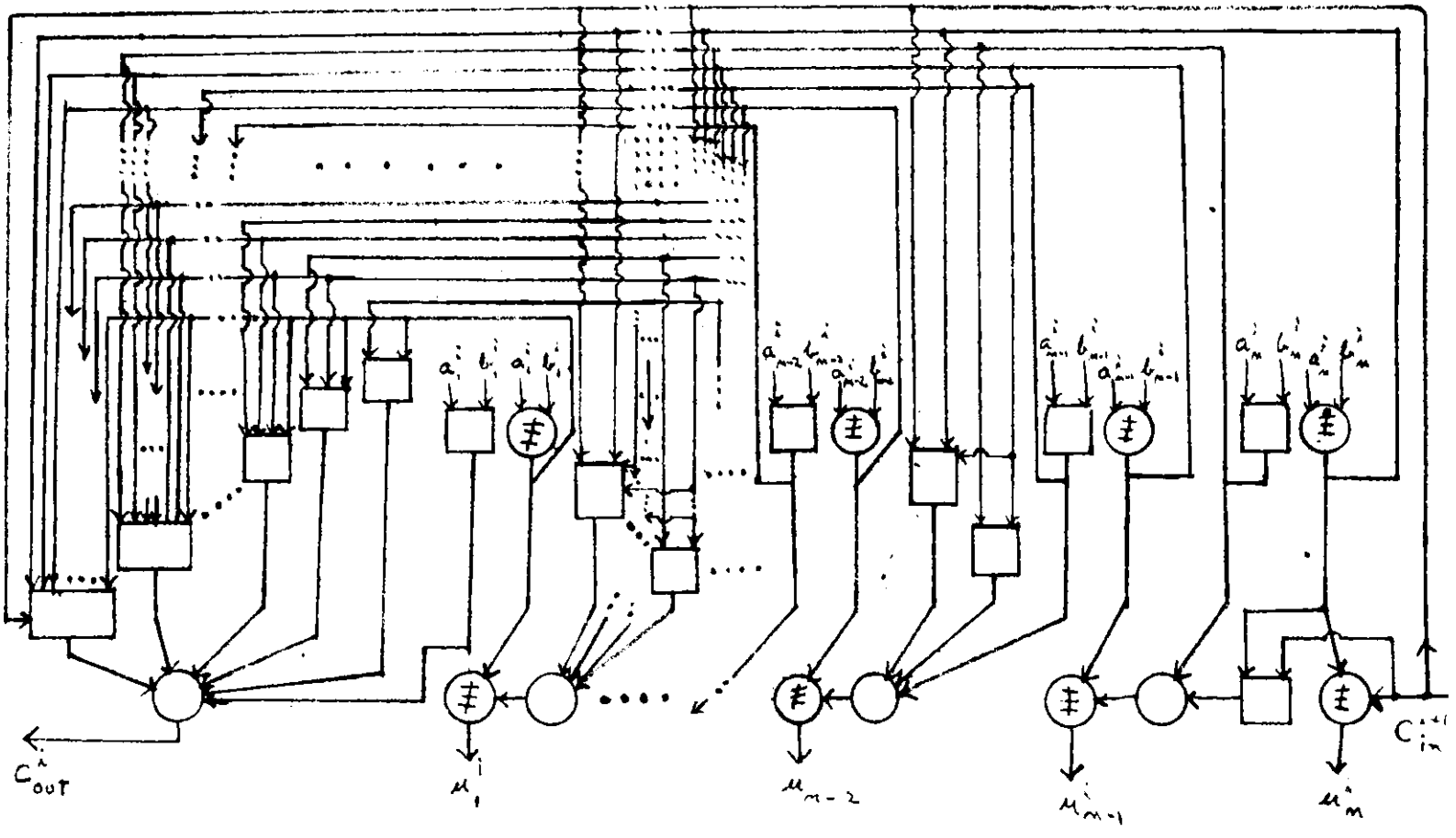


Figure 6 Representation of Simultaneous Stage

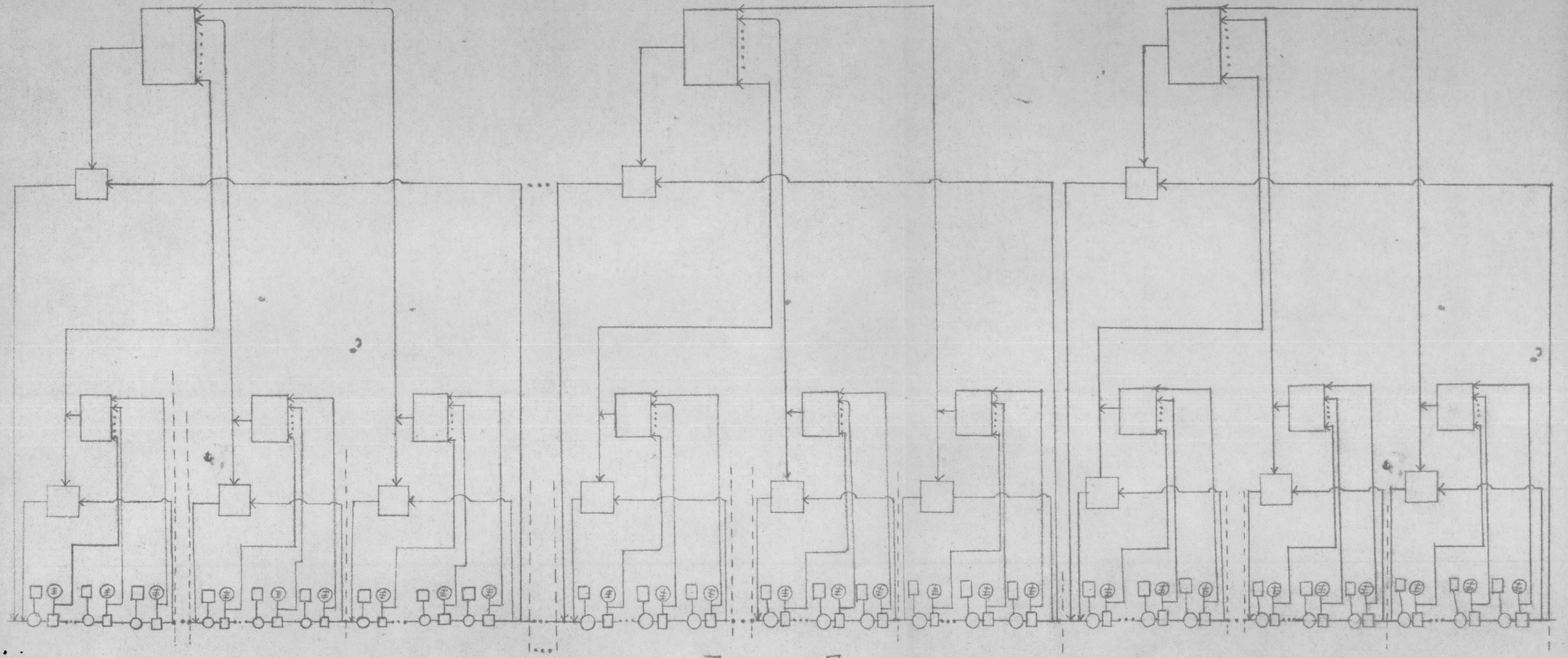


FIGURE 7

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