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# An Analytical Approach for Memristive Nanoarchitectures

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***Abstract*—As conventional memory technologies are challenged by their technological physical limits, emerging technologies driven by novel materials are becoming an attractive option for future memory architectures. Among these technologies, Resistive Memories (ReRAM) created new possibilities because of their nano-features and unique $I$-$V$ characteristics. One particular problem that limits the maximum array size is interference from neighboring cells due to sneak-path currents. A possible device level solution to address this issue is to implement a memory array using complementary resistive switches (CRS). Although the storage mechanism for a CRS is fundamentally different from what has been reported for memristors (low and high resistances), a CRS is simply formed by two series bipolar memristors with opposing polarities. In this paper our intention is to introduce modeling principles that have been previously verified through measurements and extend the simulation principles based on memristors to CRS devices and hence provide an analytical approach to the design of a CRS array. The presented approach creates the necessary design methodology platform that will assist designers in implementation of CRS devices in future systems.**

***Index Terms*—Complementary resistive switch, Memristor, Memistive device, Resistive RAM, Memory, Nanoarchitectures.**

## I. Introduction

EMERGING memory technologies based on new materials have been widely accepted as alternatives to the current CMOS technology. These technologies are mainly classified in three subclasses: Magnetoresistive Random Access Memory (MRAM), Phase Change RAM (PCRAM), and Resistive Memory (ReRAM) [1]. Memory applications motivate the need for an evaluation of these technologies in terms of READ and WRITE bandwidth, latency, and energy dissipation. The International Technology Roadmap for Semiconductors [1], highlights that the performance characteristics of these emerging technologies are rather promising when compared with the curent large memory arrays based on Static RAM (SRAM) constructs, particularly for large memory capacities. This suggests that emerging technologies, except PCRAM, will overtake advanced conventional Complementary Metal Oxide Semiconductor (CMOS) technology. We define a figure of merit as $E_{\mathrm{R}}E_{\mathrm{W}}\tau_{\mathrm{R}}\tau_{\mathrm{W}}N_{\mathrm{W,ref}}$ for comparing these technologies—with greater emphasis on the access time—the parameters represent READ and WRITE energy ($E_{\mathrm{R}}$, $E_{\mathrm{W}}$), READ and WRITE latencies ($\tau_{\mathrm{R}}$, $\tau_{\mathrm{W}}$), and the number of refresh cycles ($N_{\mathrm{W,ref}}$). This figure of merit indicates around 96%, 91%, and 79% improvement for ReRAMs, MRAMs, and PCRAMs, respectively, over SRAMs for large memory capacities ($>1$ GB) [1]. The READ and WRITE access times of MRAMs show around 41% more and 48% less processing time than ReRAMs. ReRAMs introduce smaller cell size, $4F^2$/bit, where $F$ is the lithographic feature size, see Fig. 1(c), with comparable endurance in comparison with the other memory technologies. Although a number of strategies that utilize diode and/or transistor cross-point devices are proposed, their fabrication is relatively more complex than a ReRAM crossbar [2].

The mathematical foundation of the memristor[1], as the fourth fundamental passive element, has been expounded by Leon Chua [3] and later extended to a more broad class of memristors, known as memristive devices and systems [4]. This broad classification today includes all resistance switching memory devices such as ReRAMs [5]. Realization of a solid-state memristor in 2008 [6] has generated realization of both large memory arrays as well as new opportunities in the neuromorphic engineering domain [7]–[13].

Although the memristor has introduced new possibilities for memory applications within the simple and relatively low cost crossbar array architectures, the inherent interfering current paths between neighboring cells of an addressed cell impose limitations on the scalability, a necessary condition for large memory arrays [14].

The imposed limitation was addressed by Linn *et al.* [14] through adaptation of two series memristive elements connected with opposing polarities. This structure is referred to as Complementary Resistive Switch (CRS) as shown in Fig. 2. The unique aspect of this device is in using a series

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[1]The term *memristor* is a portmanteau of *memory* and *resistor*.

of high resistance states (HRS), $R_{\rm HRS}$, and low resistance states (LRS), $R_{\rm LRS}$, to introduce logic "0" and logic "1". As an example, a LRS/HRS combination represents "1" and a HRS/LRS state represents "0". Using this approach, the net resistance of the device is always around the HRS, $R_{\rm LOGIC}$, which helps in reducing sneak-path currents and at the same time main path currents. The advantage of using a CRS as a fundamental element originates from its excellent READ voltage margin, even with small HRS to LRS ratios. Moreover, it facilitates a comparable WRITE margin [15]. There is also a lack of SPICE model verification for CRS devices and a statistical analysis considering the mentioned operational uncertainties. Here, we address these issues using a Verilog-A implementation for memristor dynamics within a memristor macro-model for SPICE simulation.

Contributions in this paper can be categorized in five parts:

- CRS device modeling and verification using available functionality information from [14].
- Comprehensive mathematical framework for a memristive array for assisting designers to identify the impacts of stored memory pattern, parasitic resistances, and sneak-path currents on the array performance. In addition, we develop a system of linear equations to extract the voltage pattern across an array regardless of the READ or WRITE scheme. This mathematical framework can be used for different emerging memory devices.
- Characterization of a comprehensive framework for a CRS array and identifying an optimal value for load resistors in a CRS array.
- Highlighting the importance of the WRITE scheme and array size in the total power dissipation through an analysis of the number of half-selected cells in array for memristive-based and CRS-based arrays.
- It is also shown that the existence of a long tail distribution in LRS resistance, after several thousand operation cycles, process variation, temperature effects, and uncertainties related to the nanowire parasitic resistances have significant impact on a memristor cross-point array than a CRS array.

Along with addressing the parasitic current path issue, the importance of parasitic resistors also increases as $F$ reduces. In a practical memory design, the line resistance of a nanowire can be calculated with $R_{\rm line} = \rho_{\rm metal}(0.2n/F)$, where $n$ is the number of cells in the line and $\rho_{\rm metal}$ is the resistivity of metal, which is a function of $F$ [16]. Therefore, a mathematical model is developed to consider the nanowire parasitic resistances in a matrix based analysis of cross-point arrays.

In this paper, the preliminaries of memristor technology and modeling approach based on a fabricated Metal-Insulator-Metal (MIM) structure is presented in Section II. Then a practical model of the CRS device is developed and created in SPICE as a macro-model. This is described in Section III. Section IV shows the analytical cross-point model and mathematical model as well as simulation results and discussions.

## II. Memristors

Memristive device modeling is a necessary step for CRS device modeling. Therefore, we first present the memristive element characteristics, which can be defined using two equations,

$$\begin{cases} I = g(w,V)\cdot V \\ \frac{{\rm d}w}{{\rm d}t} = f(w,V)\ , \end{cases} \tag{1}$$

where $w$ is a physical variable indicating the internal memristor state that in theory is such that $0 < w < L$, where $L$ is the thickness of transient material oxide (TMO) thin-film. The parameters $I$ and $V$ represent current and applied voltage, respectively. The second expression of Eq. (1) defines velocity of this movement. Considering an ionic conduction mechanism, this part can be redefined as an ionic drift velocity. The function $f(\cdot)$ captures the highly nonlinear characteristics of the memristor as function of the applied voltage [17]–[19]. The $I$-$V$ curve relationship, as in Eq. (1), has already proposed by several groups [20]–[23], however, an accurate reproduction of the characteristics in simulation is an area of intense research. An appropriate $f(\cdot)$ function seems to be either a double exponential or related forms [19], [22], or a $\sinh(\cdot)$ function [18], which defines intrinsic threshold voltages. Here we apply a commonly accepted $f(\cdot)$ function to our experimental data. The memristor state variable is identified through time integral of the $f(\cdot)$ function and then it is applied to the $g(\cdot)$ function. The outcome shows a good agreement between the measured data and the modeled $I$-$V$ hysteresis.

To address this modeling problem we use the Mott *et al.* [24, Chap. 2] model of ionic conduction in terms of the theory of lattice defects that has been already used in several studies in this area [15]. In this case,

$$\frac{dw}{dt} = \upsilon_0 e^{-\frac{U}{kT}} \sinh(\frac{\rho V}{kT})\ , \tag{2}$$

where $\upsilon_0$ is initial velocity, $U$ is the potential barrier height, $k$ represents the Boltzmann constant, $T$ temperature, and $V$ applied voltage in eV. The parameter $\rho = a/2L$, which is a dimensionless parameter related to the distance between adjunct lattice positions, $a$, and TMO thickness $L$. For approximating the effective electric field in the equation, $\rho$ should be a function of $w$ in the way that $\rho = a/2(L-w)$. Quantities are summarized in Table I.

The relationship between the drift velocity and device thickness, $\upsilon \propto \sinh(1/L)$, clearly shows the reason that memristive behavior appears strictly at nano scale dimentions. A detailed comparison between the model and experimental data is given by Heuer *et al.* [25].

The virgin device needs an electroforming step that acts like a soft breakdown condition and creates a conductive channel through the TMO material ($TiO_2$ in our case).

Then the applied voltage polarity identify the channel orientation [26]–[28]. In our case, the forming step is carried out by applying an electric field around 6.2 MV/cm across $TiO_2$. This forming step creates a difference in atomic percentage ratio of oxygen in $TiO_2$ close to one of the electrodes. The conducting mechanism is then carried out through a channel known as a conducting filament (CF). The conducting filament is highly localized (e.g. for a cylindrical CF, $A_{\rm CF} \approx 10$ nm$^2$) compared to the metalic contact area, $A$, and the filament (ON) resistance $R_{\rm ON}$ is proportional to $A_{\rm CF}^{-1}$ [29]. This shows that controlling the filament area is very important for controlling the programming current in an array of ReRAM elements. Controlling $A_{\rm CF}$ is possible through a set of operations. It is also reported that the SET threshold smoothly increases as $R_{ON}$ increases, $V_{\rm SET} \propto R_{ON}^{0.25}$, whereas a significant decrease in $I_{\rm SET} \propto R_{ON}^{-0.75}$ was reported [29].

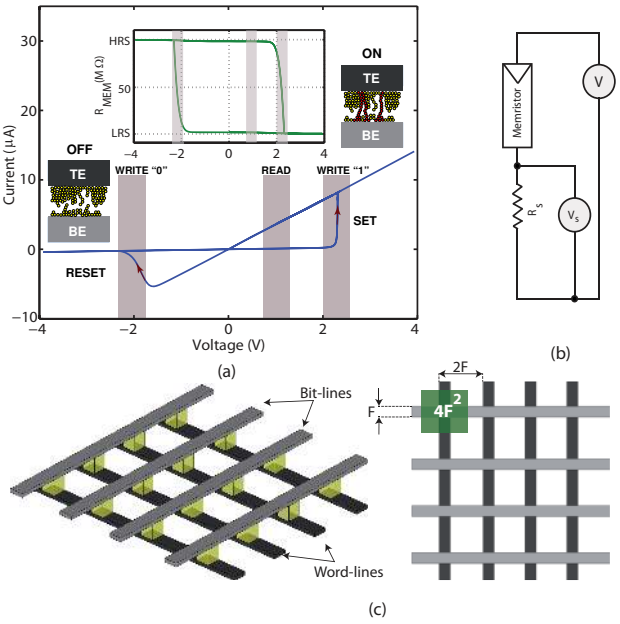


Fig. 1. Memristor cross-point implementation and array presentation. (a) Memristor model result verified by experimental data of a fabricated Ag/$TiO_2$/$TiO_{2-x}$/ITO [22]. Inset shows memristor device resistance *vs* applied voltage. TE and BE are stand for top-electrode and bottom electrode, respectively. The reason for choosing $-4$ V to 4 V is related to CRS device functionality that is explained in Section III. The curve shows asymmetric characteristics. The measurement data was collected using a Keithley 4200 semiconductor characterization system. Red paths (inset (a)) show filament paths. The probability that a conductive path is broken can be calculated through a set of (independent) Boltzmann probabilities [16]. To avoid complexity, data for linear parts are not shown here. Due to the internal dynamics of the memristor, we applied similar voltage (triangular) signal to the model and device. The digram (b) conceptually shows the measurement setup. The arrays in (c) illustrate 3D and 2D representations of a ReRAM (memristive) array.

A Verilog-A implementation of this model is used as a macro-model in Cadence. The macro-model implements the $g(\cdot)$ function as $I = (w/L)I_{\rm ON} + (1 - w/L)I_{\rm OFF}$. Our experiments show that a linear $I_{\rm ON}$-$V$ is in agreement with measurement results for an area of $100 \times 100$ $\mu$m$^2$ [22]. Further reduction of the device feature size, $F$, is possible. However, issue related to crosstalk and tunneling between neighboring cells should be taken into account [16], [30], [31]. The OFF current can be defined as $I_{\rm OFF} = \chi_1 e^{(\gamma_1 V)} - \chi_2 e^{(-\gamma_2 V)}$, where $\chi_1$, $\gamma_1$, $\chi_2$, and $\gamma_2$ are fitting parameters. Different $I$-$V$ equations for ON and OFF states have been also reported in [32] and [33]. For instance, Inoue *et al.* [33] reported $I_{\rm OFF} \propto \sinh(\cdot)$ and $I_{\rm ON} \propto \sinh^{-1}(\cdot)$. Section IV-C includes a discussion on using the nonlinearity of the memristor characteristics for increasing $R_{\rm ON}$ at a given READ operation voltage.

TABLE I
PHYSICAL PARAMETERS

| Parameter | Value | Units | Reference |
|---|---|---|---|
| $a$ | 1.5 | Å | [18] |
| $f_{\rm e}$ | $10^{13}$ | attempts/s | [18] |
| $E_{\rm ai}$ | 1.1 | eV | [34] |
| $\upsilon_0$ | 1500 | m/s | calculated |
| $L$ | 22 | nm | fabricated |
| $\rho$ | 0.0034 | no units | calculated |
| $k_{\rm th}$ | 1.5 | W/(Km) | [35] |
| $A$ | $100 \times 100$ | $\mu$m$^2$ | fabricated |
| $A_{\rm CF}$ | 10 | nm$^2$ | [29] |
| $R_{\rm th}$ | $4.5 \times 10^6$ | K/W | calculated |

Fig. 1 illustrates the modeling results for a memristor based on experimental data from a Silver/Titanium dioxide/Indium Thin Oxide (Ag/$TiO_2$/$TiO_{2-x}$/ITO) measurement implementation [22]. This is a novel combination for an ReRAM implementation in using $TiO_2$ as the TMO material according to Table 1 in [30]. This implementation yields a bipolar cell with nearly 200 successful cycles. Besides asymmetry, recent studies shows that the inherent Joule heating effect is responsible for (RESET) switching mechanism in a way that sufficient heat induces a crystallization of the oxide surrounding the channel [26], [36]. This crystallization time frame is exponentially related to temperature [26]. The exact equation can be extracted from [29]. Therefore, as Joule heating increases in the hysteresis, the CF diameter (hot spot) shrinks and this effect would lead to a reset. We include this effect in our macro-modeling approach using a relationship introduced in [37],

$$T - T_0 = PR_{\rm th} \ , \tag{3}$$

where $T_0 = 300$ K, $R_{\rm th} = L/(8k_{\rm th}A_{\rm CF})$ is the thermal resistance, $P = IV$ is Joule dissipation at reset, and $k_{\rm th}$ is $TiO_2$ thin film thermal conductivity. According to experimental data, as $A_{\rm CF}$ decreases, RESET current decreases, so the RESET threshold voltage would increase [36].

In order to increase simulation convergence Eq. (2) can be rewritten as,

$$\frac{dw}{dt} = \upsilon_1 V + \upsilon_3 V^3 + \upsilon_5 V^5 + \dots \ , \tag{4}$$

where $\upsilon_1$, $\upsilon_3$, and $\upsilon_5$ are low-field and higher order coefficients. This approach also combines the effects of Joule heating and $L - w$ (on the effective electric field) in $\upsilon_i$

coefficients. Note that $dw/dt = v_1 V$ usually defines a pure memristive behavior, as described in [3].

These properties then raise the following questions, (i) how to address the asymmetric characteristic in WRITE and READ operations, (ii) what is the impact of using more realistic model for cross-point array evaluation, and (iii) what is the effect of different device level $I$-$V$ characteristics on the array performance? Here we are aiming to answer the first two questions using the explained model and the answer to the third question is currently under review by the our research group and will be the topic of another paper. The second question can be answered using a worst-case consideration for $R_{\mathrm{ON}}$. In this case, this paper compares a memristor array with a CRS-based array.

Using the developed model of the memristor that accurately models the nonlinear behavior of the device, we can model the CRS as explained in the following section.

## III. Complementary Resistive Switch

A CRS is a resistive switching device that is built using two memristor devices connected in series with opposite polarities [14]. Fig. 2(c) illustrates the modeling results. The figure's inset illustrates a CRS based cross-point array. Each memristor in the figure follows a $I$-$V$ curve relationship that is shown in Fig. 1(a). The minimum applied voltage for a switch is around ±2.0 V. Considering the CRS structure as a simple voltage divider, for a LRS/LRS situation[2] minimum ±2 V is applied across either of the memristors. Please refer to Table III for the crossbar memory array parameters. CRS's ON state resistance is $R_{\mathrm{CRS,LRS}} = R_{\mathrm{ON}} \approx 2R_{\mathrm{LRS}}$, where $R_{\mathrm{LRS}}$ represents memristor's LRS and CRS's high resistance, $R_{\mathrm{CRS,HRS}} = R_{\mathrm{LOGIC}} \approx R_{\mathrm{HRS}}$, where $R_{\mathrm{HRS}}$ indicates memristor's HRS (see Table II). Fig. 3 highlights the resistance switching of the CRS device. The initial state is programmed to be slightly below $R_{\mathrm{CRS,HRS}}$, so there is a difference at the initial curve and the rest of the sweeps. In a memristor device, logic "0" and "1" are represented with $R_{\mathrm{HRS}}$ and $R_{\mathrm{LRS}}$, respectively, whereas a CRS device represents logic "0" and "1" using a combination of low and high resistances which results in overall resistance of $R_{\mathrm{HRS}}$ ($R_{\mathrm{OFF}}$) for the both logical values.

A fresh CRS device shows a HRS/HRS resistance for memristors A and B. This combination occurs only once (this is not shown in the figure) [27]. After applying a positive or negative bias, depending on the polarity of memristors, the device switches to either the "0" or "1" state. In Fig. 2(c), red lines are threshold voltages for SET $V_{\mathrm{th,S1}}$ and $V_{\mathrm{th,S2}}$ and for RESET $V_{\mathrm{th,R1}}$ and $V_{\mathrm{th,R2}}$. In an ideal CRS device, $V_{\mathrm{th,SET}} = V_{\mathrm{th,S1}} = |V_{\mathrm{th,S2}}|$ and $V_{\mathrm{th,RESET}} = V_{\mathrm{th,R1}} = |V_{\mathrm{th,R2}}|$. Here $V_{\mathrm{th,SET}} = 2.4$ V and $V_{\mathrm{th,RESET}} = 3.6$ V. A successful READ operation occurs if $V_{\mathrm{th,SET}} < V_{\mathrm{READ}} < V_{\mathrm{th,RESET}}$. For a successful WRITE,

[2]This situation is defined as the ON state. This is not a stable state so it does not represent a logic state but plays an important role in the switching, READ, and WRITE processes.

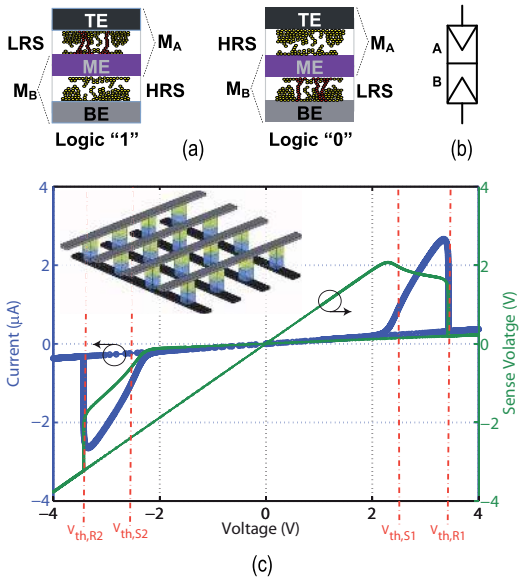


Fig. 2. CRS functionality using the described memristor model. (a) Fundamental behavior of switching between logic "0" and logic "1". Here, TE, BE, and ME are the top, bottom, and middle electrodes, respectively. The reading procedure can be carried out by sensing ME. Note that $M_A$ and $M_B$ are memristors A and B. (b) A symbol for the CRS device. (c) $I$-$V$ sense voltage curve of the simulated device that shows the characteristics described in [14]. The inset shows a 3D schematic of a CRS array. Note that the middle electrode (ME) should not be connected to any point, otherwise it creates new sneak current paths.

$V_{\mathrm{th,RESET}} < V_{\mathrm{WRITE}}$. Consequently, every voltage below $V_{\mathrm{th,SET}}$ should not contribute any change in the device state. Possible state transitions are shown in Table II, where $R'$ shows the next resistance state, $R$ illustrates the initial resistance state, and output is a current pulse or spike. In this table, H represents high resistance (either logic states, Logic "" or Logic "1"), and L indicates low resistance.

The simplest analytical model of a CRS can be defined in a relative velocity form, when $\mathrm{d}w/\mathrm{d}t = \mathrm{d}w_{\mathrm{A}}/\mathrm{d}t + \mathrm{d}w_{\mathrm{B}}/\mathrm{d}t$ and the two memristors (A and B) form a voltage divider. Therefore, depending on the combination, the difference between $V_{\mathrm{A}}$ and $V_{\mathrm{B}}$ can be identified.

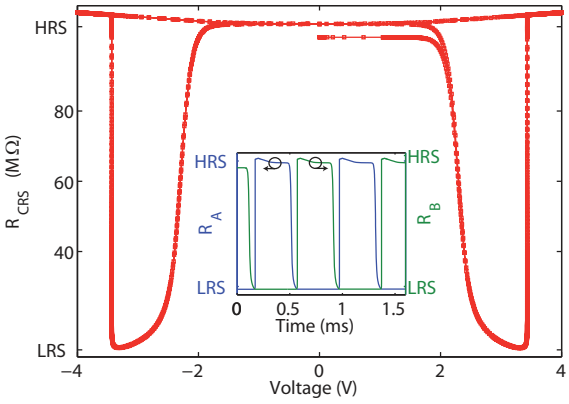


Fig. 3. CRS effective resistance for a triangular applied voltage. The inset clearly shows the switching mechanism for memristors A and B. The initial state is slightly less than $R_{\mathrm{OFF}} (= R_{\mathrm{HRS}} + R_{\mathrm{LRS}})$.

TABLE II
STATE TRANSITIONS IN CRS

| $R$ | $\Delta V$ | $R'$ | Output |
|---|---|---|---|
| H ("1") | $V_{\text{th,S1}} < \Delta V < V_{\text{th,R1}}$ | L (ON) | pulse |
| H ("1") | $V_{\text{th,R1}} < \Delta V$ | H ("0") | spike |
| H ("0") | $V_{\text{th,R2}} < \Delta V < V_{\text{th,S2}}$ | L (ON) | pulse |
| H ("0") | $\Delta V < V_{\text{th,R2}}$ | H ("1") | spike |
| L (ON) | $V_{\text{th,R1}} < \Delta V$ | H ("0") | – |
| L (ON) | $\Delta V < V_{\text{th,R2}}$ | H ("1") | – |

The first feature that appears from the CRS simulation, and device fabrication [14], [38], is a perfectly symmetric $I$-$V$ curve out of an asymmetric memristor $I$-$V$ curve. The device is programmed initially at logic "1", LRS/HRS, ($R_{\text{A}} \approx$LRS and $R_{\text{B}} \approx$HRS). An appropriate READ pulse creates a high potential difference across $R_{\text{A}}$ while the voltage difference across $R_{\text{B}}$ is not beyond its memristive threshold. Therefore, $R_{\text{A}}$ switches to LRS and an ON current (pulse) passes through the CRS device. After a resting time, a negative WRITE pulse is applied to restore "1", which can be defined as refreshing procedure. Fig. 4(b) shows that the $R_{\text{CRS}}$ settled close to HRS with a logic "1" stored in the device. Then a positive WRITE pulse tends to write logic "0", which can be defined as programming step. Depending on the switching speed of the memristors, a short term ON state occurs that causes a relatively large current spike (encircled by red dots in Fig. 4(a)). There are other functional characteristics that have to be met. For instance, a HRS/HRS state should not appear in any of the situations that are demonstrated by the presented simulation [15].

The CRS device shows several advantages over a single memristor element for memory applications. This work highlights these advantages for nano crossbar memories.

## IV. Crossbar Memory Array

A crossbar structure as shown in Fig. 5(a) is used. This hybrid nano/CMOS implementation is a 3D implementation that the nano domain is stacked on top of the CMOS domain [39]. The cross-point element could be either a CRS device or a memristor. In order to read any stored bit in $R_{i,j}$, similar to many other reported schemes [2], [40]–[42], here we apply $V_{\text{pu}} = V_{\text{READ}}$ to the $i^{\text{th}}$ bit-line, $j^{\text{th}}$ word-line is grounded, and all other word and bit lines are floating. A direct benefit of this approach is the pull-up resistor ($R_{\text{pu}}$) can be implemented in nano domain [41]. The stored state of the device then can be read by measuring voltage $V_{\text{o}}$ that is performed by using CMOS sense amplifiers (SAs). Reading "1" creates a current pulse, and as a consequence, a voltage pulse appears on the middle electrode. Note that the CRS read-out mechanism does not rely on sensing the middle electrode (ME) and this electrode is floating. The read-out mechanism detects the affect of this current pulse on the bit-line's nanowire capacitor and senses it with the SA array.

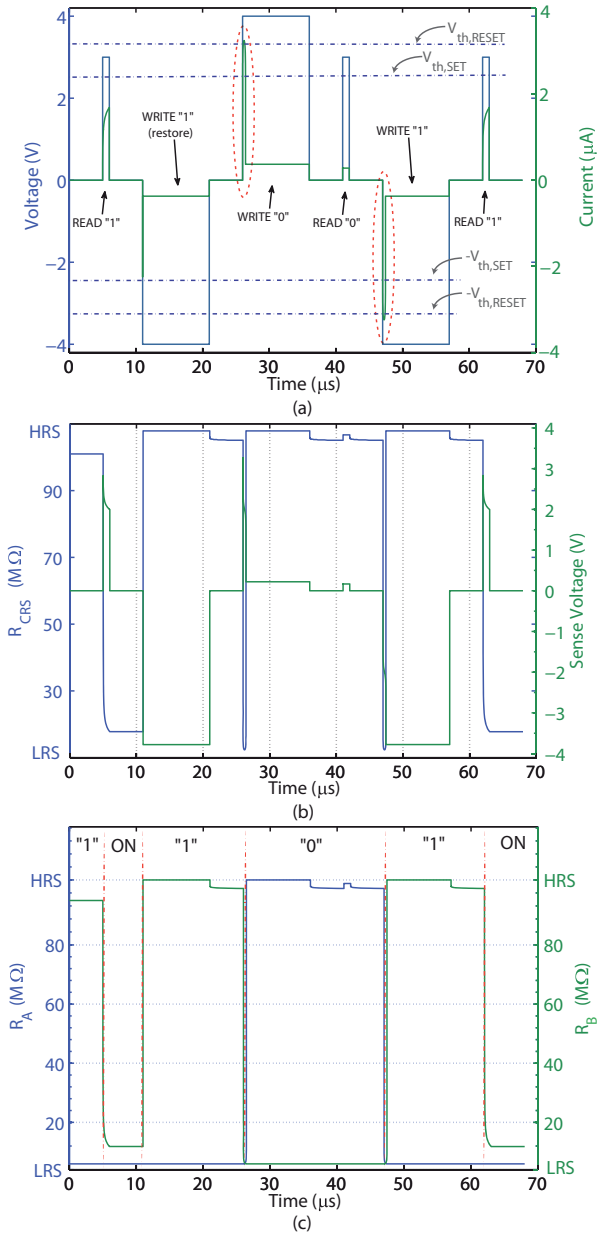


Fig. 4. CRS response to a sequence of pulses for READ and WRITE operations. (a) Current response to applied voltage pulses. The dashed lines indicate threshold voltages. The 1 $\mu$s READ pulses lie between the $V_{\text{th,SET}}$ and the $V_{\text{th,RESET}}$. A 5 $\mu$s WRITE pulse provides a voltage amplitude beyond $V_{\text{th,RESET}}$. (b) Illustrates the total CRS resistance and sense voltage (sensing from middle electrode). As can be seen from the figure, for most of the time $R_{\text{CRS}} \approx$HRS. (c) Shows the logic in terms of memristive state for A and B memristors. memristors. Appropriate READ and WRITE pulse widths have been already discussed by Yu *et al.* [15].

The WRITE scheme that is used is the common accessing method in which the $i^{\text{th}}$ bit-line is pulled up, the $j^{\text{th}}$ word-line is grounded, and the other lines are all connected to $V_{\text{w}}/2$, where $V_{\text{w}}$ is the WRITE voltage. This voltage should be high enough to create sufficient voltage difference across the target cell and at the same time having no unwanted affect on the other cells that

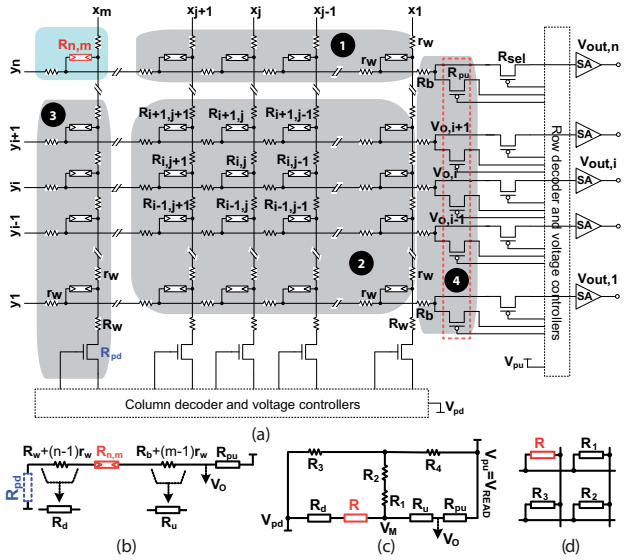


Fig. 5. Typical $n \times m$ crossbar array. (a) A hybrid nano/CMOS circuit. Columns show word-lines and rows identify bit-lines. Each $R_{i,j}$ show resistive elements that can be a memristor or a CRS device. Nanowire segment resistance is shown by $r_{\rm w} = R_{\rm line}/n$ (if $n = m$) and the connection between the nanowire and word-line is shown using $R_{\rm w}$. Similarly the bit-line resistance indicated by $R_{\rm b}$. According to the model discussed in Section I, unit cell resistance of a bit/word line (nanowire) for $F = 100$ nm and $n = 64$ is around 1 Ω while it is increased to 32 Ω if $F$ reduces to 5 nm, which is consistent with the unit cell resistance that is reported in [1] (1.25 Ω). The segment resistance of $r_{\rm w} = 1.25$ Ω is taken in our simulations. The pull-up resistors (dashed box in red), $R_{\rm pu}$, can be implemented in nano domain and in this paper we assumed them as part of the nano domain. The triangular shape at the output shows a CMOS amplifier that is assumed to have an acceptable sensitivity ($\Delta V$ or $\Delta I$) range of $>$ 100 mV. While READ process is in progress appropriate signals provided by decoders directs $V_{{\rm o},i}$ to $V_{{\rm out},i}$. Stored pattern in groups (1), (2), and (3) can be identifed by $R_{\rm X1}$, $R_{\rm X2}$, and $R_{\rm X3}$, respectively. (b) The ($n^{\rm th}$,$m^{\rm th}$) cell that can be identified in red color is the worst case possible cell for any READ and WRITE schemes. This circuit does not consider sneak-path current. The pull-down resistors, $R_{\rm pd}$ are implemented as part of the CMOS domain and their effects are neglected as the read-out are related to pull-up resistors. (c) Equivalent circuit for the READ scheme with sneak-path and parasitic nanowire resistors considerations. (d) Schematic of a $2 \times 2$ array that is a good approximation to the array according to the grouping.

mainly see a $V_{\rm w}/2$ voltage difference.

Although the WRITE operation in memristors dominates because of its relatively high voltage/current, for CRS device the READ current dominates the current level. Therefore, in our case, the READ operation analysis for energy consumption and performance characteristics is more critical than WRITE operation. Consequently, we discuss the READ and WRITE simulation results here. Table III highlights the cross-point junction and array parameters.

To analyze the structure, we need to provide a simplified equivalent circuit for the crossbar structure, as can be seen in Fig. 5(b) and (c). Note that $V_{\rm MEM,READ} < V_{\rm CRS,READ}$ and $V_{\rm th,SET} < V_{\rm CRS,READ} < V_{\rm th,RESET}$. Fig. 5(c) illustrates the equivalent circuit considering sneak-path currents for the both memristive and CRS-based array. For

TABLE III
PARAMETERS OF THE MEMRISTIVE AND CRS CROSS-POINT JUNCTIONS AND ARRAY STRUCTURE.

| Parameter | Value | Array* | Description |
|---|---|---|---|
| $R_{\rm LRS}$ | 100 kΩ | (M) | low resistance state |
| $R_{\rm LRS}$ | 200 kΩ | (C) | low resistance state |
| $R_{\rm HRS}$ | 100 MΩ | (B) | high resistance state |
| $r$ | $10^3$ | (M) | resistance ratio |
| $R_{\rm b}$ | 100 Ω | (B) | input resistance of SA† |
| $R_{\rm w}$ | 100 Ω | (B) | pull-down resistance▷ |
| $R_{\rm pu}$ | $R_{\rm LRS}$ | (B) | pull-up resistor‡ |
| $r_{\rm W}$ | 1.25 Ω/□ | (B) | parasitic resistor |
| $V_{\rm th,SET}$ | 2.2 V | (M) | SET threshold |
| $\lvert V_{\rm th,RESET}\rvert$ | 1.8 V | (M) | RESET threshold |
| $V_{\rm READ}$ | 1 V | (M) | READ voltage |
| $V_{\rm WRITE}$ | 2 V | (M) | WRITE voltage |
| $\lvert V_{\rm th,SET}\rvert$ | 2.4 V | (C) | SET threshold |
| $\lvert V_{\rm th,RESET}\rvert$ | 3.6 V | (C) | RESET threshold |
| $V_{\rm READ}$ | 2.8 V | (C) | read voltage |
| $V_{\rm WRITE}$ | 3.8 V | (C) | write voltage |

* Array type: (M) Memristor-based, (C) CRS-based, (B) Applicable for both.
† We assumed that bit-lines are directly connected to sense amplifiers (SAs) and there is no $R_{\rm sel}$ in between.
‡ It is assumed that these resistors are implemented in nano domain. Transistors in Fig. 5 are used to express a more general form of a hybrid nano/CMOS memory.
▷ Lumped parasitic resistance of an activated pull-down.

the sake of simplicity, two series resistors, $R_1$ and $R_2$, are evaluated separately.

The resistor value for the memristive-based and CRS-based circuit can be written as,

$$R_1 = \frac{R_{\rm X1}}{(m-1)} + r_{\rm w}\ , \tag{5}$$

$$R_2 = \frac{R_{\rm X2}}{(m-1)(n-1)} + r_{\rm w}\ , \tag{6}$$

$$R_3 = \frac{R_{\rm X3} + R_{\rm d}}{(n-1)}\ , \tag{7}$$

$$R_4 = \frac{R_{\rm pu} + R_{\rm u}}{(n-1)}\ , \tag{8}$$

where $R_{\rm X}$ represents the array's stored pattern in three different groups as seen in Fig. 5(a). For the worst case READ or WRITE in a memristive array $R_{\rm X1} = R_{\rm X2} = R_{\rm X3} = R_{\rm LRS}$ and for a CRS array $R_{\rm X1} = R_{\rm X2} \equiv$ logic "1" or logic "0", whereas $R_{\rm X3} \equiv$ logic "1". Although a worst case cell selection is considered here, due to the harmonic series behavior of the overall parallel parasitic resistance, increasing $R_{\rm LRS}$ and/or decreasing the array size, $n = m$, results in better agreement with the analytical approximation for $R_1$ and $R_2$. These equations then can be used for evaluating the impact of parasitic current paths and parasitic nanowire resistors on the array performance.

The worst case pattern is assumed to be applied when $R_{\rm LRS} \equiv$ logic "1" for either memristive or CRS array. In this case, we have the most significant voltage drop because of the both parasitic paths and elements. Therefore, a pattern of either logic "0" or "1" for all the elements except those on $j^{\rm th}$ word-line ($x_j$) is assumed, which is roughly equivalent to a HRS resistance for a CRS device, $R_{\rm CRS,HRS} = R_{\rm HRS} + R_{\rm LRS}$. A close look at Fig. 4(a)

and (c) shows if the stored logic in all the CRS devices along $x_j$, which may or may not include $R_{i,j}$, is "1" (LRS/HRS), so applying a $V_{\rm READ}$ can change their states to an ON condition (LRS/LRS). Therefore, during the READ time, $n-1$ devices along $x_j$ comprise the ON resistance, $R_{\rm ON} = 2R_{\rm LRS}$, in our simulations. Therefore, for a CRS array, $R_{\rm X1} = R_{\rm X2} = R_{\rm HRS} + R_{\rm LRS}$ and $R_{\rm X3} = 2R_{\rm LRS}$.

Sizing of the pull-up resistor, $R_{\rm pu}$, as part of the nano domain implementation is a very important factor. For instance, low $R_{\rm LRS}$ devices, e.g. magnetic tunneling junctions (MTJs), interconnection impedance should be also taken into account, whereas in ReRAMs, the LRS resistance is normally $\gtrsim 100$ kΩ [23]. Therefore, our approach provides a generalized analytical form for a nanocrossbar array. In other words, if $R_{\rm LRS} \gg (n+m)r_{\rm W}$, the nanowire overall resistance will be negligible. These considerations along with taking low output potential, $V_{\rm OL}$, and high output potential, $V_{\rm OH}$, lead to an optimal value for $R_{\rm pu}$. We first follow the conventional approach without considering parasitic currents and the nanowire resistors. Note that in a more precise analysis, the sense amplifier's sensitivity is also important to be considered [16]. In this situation have,

$$V_{\rm OL} = \frac{R_{\rm L}}{R_{\rm L}+R_{\rm pu}}V_{\rm pu}\ , \tag{9}$$

$$V_{\rm OH} = \frac{R_{\rm H}}{R_{\rm H}+R_{\rm pu}}V_{\rm pu}\ , \tag{10}$$

where for a memristive array $R_{\rm L} = R_{\rm LRS}$ and $R_{\rm H} = R_{\rm HRS}$, whereas for a CRS array $R_{\rm L} = 2R_{\rm LRS}$ and $R_{\rm H} = R_{\rm HRS} + R_{\rm LRS}$. These equations are applicable for both of the arrays (memristive and CRS array). Read margin (RM) is defined as $\Delta V = V_{\rm OH} - V_{\rm OL}$. An optimal value of $R_{\rm pu}$ can be extracted from $\partial\Delta V/\partial R_{\rm pu} = 0$. For a memristive array, $R_{\rm pu,MEM} = R_{\rm LRS}\sqrt{r}$, where $r = R_{\rm HRS}/R_{\rm LRS}$. Taking parasitic resistors into account (e.g. MJTs), and neglecting sneak-paths, results in $R_{\rm pu,MEM} = \sqrt{rR_{\rm LRS}(R_{\rm LRS}+(n+m)r_{\rm W})}$ as an optimal value for the load resistor. For a CRS array,

$$R_{\rm pu,CRS} = R_{\rm LRS}\sqrt{2(1+r)}\ . \tag{11}$$

A generalized form can be achieved by solving two Kirchhoff's current laws (KCLs) for the equivalent circuit (Fig. 5(c)). Therefore, if $R_{12} = R_1 + R_2$ and

$$x = \frac{R_{12}}{R_4} + \frac{R_{12}}{R_3} - 1\ , \tag{12}$$

$$y = \frac{1}{R+R_{\rm d}} + \frac{1}{R_{\rm pu}+R_{\rm u}} - \frac{1}{R_{12}}\ , \tag{13}$$

$$V_{\rm M} = \frac{R_{12}(xR_4 - (R_{\rm pu}+R_{\rm u}))}{R_4(1+xyR_{12})(R_{\rm pu}+R_{\rm u})}V_{\rm pu}\ , \tag{14}$$

$$V_{\rm O} = \frac{R_{\rm u}}{R_{\rm pu}+R_{\rm u}}(V_{\rm pu}-V_{\rm M})\ , \tag{15}$$

where $R$ is a memristor or CRS device to be read. This is similar to the ideal condition, $R_{\rm LRS} \Rightarrow V_{\rm OL,MEM}$, $2R_{\rm LRS} \Rightarrow V_{\rm OL,CRS}$, $R_{\rm HRS} \Rightarrow V_{\rm OH,MEM}$, and $R_{\rm HRS} + R_{\rm LRS} \Rightarrow V_{\rm OH,CRS}$. A numerical approach helps designers to identify an optimal value for $R_{\rm pu}$. The significance of this analytical model can be highlighted using a comparison between the optimal values for $R_{\rm pu}$ calculated through Eqs. (9) and (10) and the optimal value calculated via Eq. (15) (and if parasitic resistors are negligible then via Eq. (14)). The optimal value for a memristive array, neglecting sneak currents and parasitic resistors, is around 3.16 MΩ using data from Table III. This parameter is a strong function of array size ($n$ and $m$) and $R_{\rm LRS}$. In practical designs, $R_{\rm pu}$ optimal increases as $n$ ($= m$) increases. This rate of change can be significantly reduced by a high $R_{\rm LRS}$. This study shows $R_{\rm LRS} > 3$ MΩ results in a significant reduction in dependency of the optimum value to the array size. This analytical approach also indicates that in our case $R_{\rm pu} \approx R_{\rm LRS}$ for CRS and memristive arrays.

In this paper we calculated the voltage pattern using $2mn$ linear equations from a $n \times m$ array. This mathematical framework can be easily implemented using KCL equations in a matrix form. Fig. 6 demonstrates the schematic of how KCL equations work in the two plates. Basically, it shows that for $1 < (i \text{ and } j) < n$ $(n = m)$,

$$g_{\rm w}V_{{\rm B1},i} + g_{\rm w}V_{{\rm B2},i} = G_{i,j}V_{i,j}\ , \tag{16}$$

$$g_{\rm w}V_{{\rm W1},j} + g_{\rm w}V_{{\rm W2},j} = -G_{i,j}V_{i,j}\ , \tag{17}$$

where $g_{\rm w} = 1/r_{\rm W}$, $G_{i,j} = 1/R_{i,j}$, $V_{{\rm B1},i} = V_{{\rm B},i,j+1} - V_{{\rm B},i,j}$, $V_{{\rm B2},i} = V_{{\rm B},i,j-1} - V_{{\rm B},i,j}$, $V_{{\rm W1},j} = V_{{\rm W},i+1,j} - V_{{\rm W},i,j}$, $V_{{\rm W2},j} = V_{{\rm W},i-1,j} - V_{{\rm W},i,j}$, and $V_{i,j} = V_{{\rm B},i,j} - V_{{\rm W},i,j}$. Therefore, we have $2mn$ unknowns and $2mn$ equations. Depending on the READ scheme, the first and last rows (word-line) and columns (bit-line) should be treated differently. Therefore, we can have a control over the voltage pattern and the amount of voltage drop for READ and WRITE operations considering parasitic resistors.

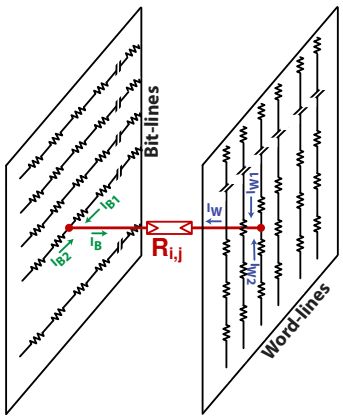


Fig. 6. A schematic of an interconnection network in a crossbar array to illustrate the two KCL equations that can be achieved from both bit-line and word-line plates. Generally, current flow through a cross-point device from the $i^{\rm th}$ bit-line is $I_{{\rm B},i} = I_{{\rm B1},i} + I_{{\rm B2},i}$, similarly for the $j^{\rm th}$ word-line is $I_{{\rm W},j} = I_{{\rm W1},j} + I_{{\rm W2},j}$.

Although, the impact of multiple parasitic currents and nanowire resistors are studied in the literature [2], [43], a

comprehensive analytical approach to address these issues, for the both memristive and CRS arrays, is lacking and it is this issue that is addressed in this paper.

### *A. Simulations of crossbar array*

Extensive analytical studies have been carried out in the area of nano crossbar memory design [2], [40]–[43]. Here we extend these studies and also the comprehensive analytical framework, introduced early in this section, to the simulation of the memristive and CRS-based arrays.

For simulations in this paper we consider a range of rectangular array sizes from $n$ = 4,16, and 64 ($n = m$) and three input patterns, the best case, the worst case, and a random pattern for sneak-path current, or interference from neighboring cells, considerations. All patterns are identical for memristor-based and CRS-based arrays. Parameter values can be found in Table III and the simulations results are as reported in Table IV for the memory patterns that are given in Fig. 8. If $\Delta V \geq 100$ mV is acceptable for the CMOS amplifiers, $\Delta V/V_{\rm pu} \geq 10\%$ for memristors and $\Delta V/V_{\rm pu} \geq 3.6\%$ for CRS are acceptable. Only acceptable case for memristor array is the best stored pattern ($16 \times 16$) while all the results for a CRS array are acceptable. This study shows that a memristive array needs substantial improvement in the static power dissipation to be an appropriate candidate for the future memory applications, if $R_{\rm LRS}$ values are in the order of kΩ.

For a worst case pattern in a CRS-based array, the $(16 \times 16) - 1$ bits are initially programmed at their LRS/HRS state ($R_{\rm X1}$, $R_{\rm X2}$, and $R_{\rm X3}$), which is effectively equivalent to a HRS state. There is only 1 bit on the selected word-line that is programmed with a different logic value and this is for reading $V_{\rm OH}$ and $V_{\rm OL}$ at the same time via different bit-lines. Fig. 7 illustrates how a worst case happens by applying appropriate READ voltage (here 2.8V) and 15 CRS devices switch to their $R_{\rm ON}$ state, which makes a significant difference in terms of the maximum amount of current that can pass through the device. Consequently, this is the main source of power dissipation for a CRS array. A similar scenario is observed for a $64 \times 64$ array.

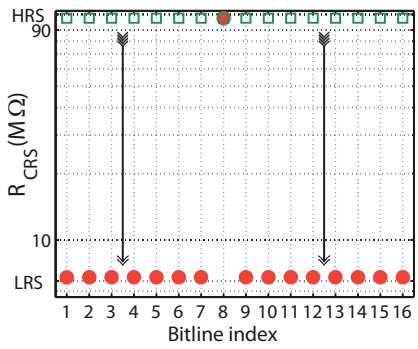


Fig. 7. Resistance switch in a column of CRS devices, green rectangular and red circles are the resistance states before and after READ operation, respectively.

Fig. 9 illustrates voltage pattern for a $64 \times 64$ CRS array for reading 32$^{\rm th}$ word-line. The magnitude of the voltage peak above the settled voltage surface for unselected cells shows a successful READ process. A similar approach can be taken for the WRITE process to show that the minimum requirement (at least the programming threshold voltage) is met on the selected cell(s).

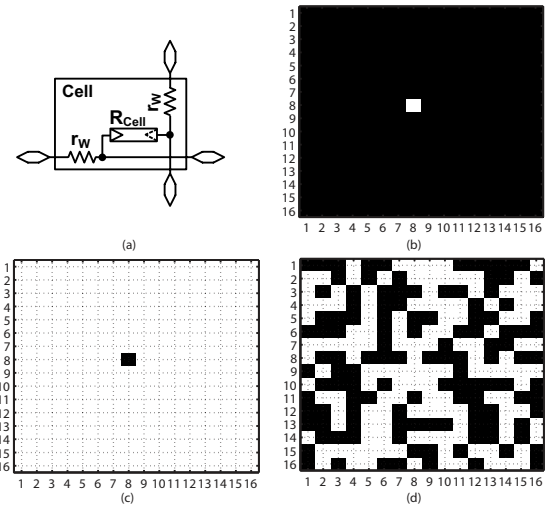


Fig. 8. Crossbar memory stored patterns for SPICE simulations. (a) Cross-point unit cell. Horizontal line shows bit-line and vertical wire illustrates word-line. (b) A possible best case in terms sneak-paths for reading 8$^{\rm th}$ word-line. We assume a pattern that all the 16 bits in this word are programmed at their OFF state and there is only one bit with ON state resistance (LRS). The worst case possible is to read from or write in the last word-line. (c) A possible worst case. (d) A random pattern. In all cases, we read the 8$^{\rm th}$ column. We initially program one bit with different logic to be able to analyze read margin efficiently. Note that these cases are all relative worst and best cases for comparing the two technologies. A worst case for reading "1" occurs if selected word line contains only cells with $R_{\rm HRS}$ and the rest of the array are at $R_{\rm LRS}$. Worst case for reading "0" and writing happen when all the resistive elements are at their $R_{\rm LRS}$ state. For a CRS array, if the array under test is initially programmed to store "0" for all the cells on selected word line and "1" for the rest of the array, worst case for reading "1" occurs, otherwise if the array stores only "1" logic then the worst case for WRITE operation and reading "0" occurs.

TABLE IV
CROSSBAR SIMULATION RESULTS

| Array | $\frac{\Delta V}{V_{\rm READ}}$ (%) | | Energy (pJ) | $V_{\rm READ}$ |
|---|---|---|---|---|
| MEM (> 10%) | | | | |
| 16 × 16 | Worst | 2.3 | 32.1 | 1 V |
| 16 × 16 | Best | 52.6 | 4.0 | 1 V |
| 16 × 16 | Random | 5.5 | 26.9 | 1 V |
| 64 × 64 | Worst | 0.45 | 127.0 | 1 V |
| CRS (≥ 3.6%) | | | | |
| 16 × 16 | Worst | 19.8 | 119.9 | 2.8 V |
| 16 × 16 | Best | 24.3 | 20.8 | 2.8 V |
| 16 × 16 | Random | 21.2 | 89.0 | 2.8 V |
| 64 × 64 | Worst | 9.5 | 483 | 2.8 V |

By analyzing the results for a range of array from $4 \times 4$ to $64 \times 64$, it is observed that to gain an appropriate and nondestructive READ, $V_{\rm READ} = 1$ V, for memristors.

This is an intermediate voltage and is low enough to avoid significant change in the device internal state and is high enough to drive a 64×64 array for the last or worst case selected cells. Our simulations indicate that a relatively high LRS ($> 3$ MΩ, as reported in [43]) guarantee enough read margin as well as sufficient potential across a selective cell for a successful WRITE operation when $r > 2$. Therefore, the negative contributions of nanowire parasitic resistors and parasitic (sneak) path currents that are responsible for voltage drop on the selected lines can be both significantly mitigated to a negligible level by increasing $R_{\mathrm{LRS}}$ and maintaining $r$ at a level to guarantee a distinguishable high and low state outputs, whether in terms of $\Delta V$ or $\Delta I$.

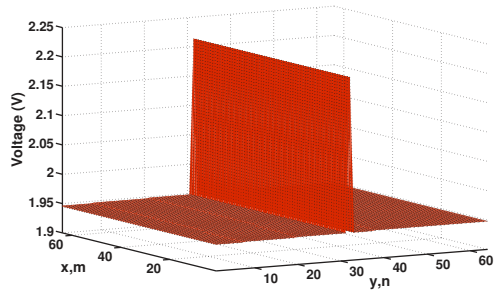


Fig. 9. Voltage pattern across a 64 × 64 CRS cross-point array.

Endurance requirement[3] in the CRS will be relaxed by utilizing a nondestructive and scalable read-out technique, which significantly reduces the total number of refreshing cycles. A nondestructive readout approach can be found in [44].

### *B. Statistical analysis*

Recent study on memristive switching behavior indicates that there is also a lognormal (long tail) distribution associated with LRS switching (SET) [23]. This certainly reduces the impact of interconnection resistors due to the fact that a significant portion of low resistor states have higher values than the nominal $R_{\mathrm{LRS}}$, however, the impact of such distribution on the device switching speed is significant. The lognormal distribution has been also seen in the switching time ReRAMs [45]. However, despite extensive research about the mechanism that causes the lognormal distribution this area is still under intensive discussion [45].

An analysis has been carried out on a 4 × 4 memristive and a 16 × 16 CRS arrays through 1000 Monte Carlo simulations to observe the impact of the uncertainty associated with $R_{\mathrm{LRS}}$, device process variation, spatial randomness of the initial state programming, and unfixed applied voltages. The ON state lognormal distribution data is extracted from [23] while a Gaussian distribution is assumed for the the line edge roughness (LER) for devices, nanowires, and variation on the applied voltages. According to [46], $(-3\sigma, +3\sigma) = (-5.4\%, 4.1\%)$ LER and $(-5.5\%, 4.8\%)$ thickness fluctuations is assumed for the both $R_{\mathrm{LRS}}$ and $R_{\mathrm{HRS}}$. We also assumed a normal distribution for initial state programming with $|\pm 3\sigma| = 5\%$. Fig. 10 demonstrates that the CRS array's output is less sensitive to the overall uncertainty, whereas the memristive array is widely spread out. Minimum value for CRS and memristor arrays are 15% and 1%, respectively. As discussed earlier, $\Delta V/V_{\mathrm{pu}} \geq 3.6\%$ for the CRS cross-point and $\geq 10\%$ for the memristor array are acceptable. Table IV has already shown that CRS array stored data pattern sensitivity is much (11 times) less than the memristive array. Similarly here, while a memristive array read margin is far less than 10%, a CRS array guarantee 12% margin.

In [46] the impact of such variations defined as $R_{\mathrm{XRS}} \cdot \theta_{\mathrm{Th}}/\theta_{\mathrm{LER}}$, where $R_{\mathrm{XRS}}$ is either LRS or HRS resistance and the $\theta_{\mathrm{Th}}/\theta_{\mathrm{LER}}$ define the thickness fluctuations over LER variation. The HRS resistance in a $TiO_2$-based memristor is less affected by the overall variation, whereas LRS variation shows a significant deviation from its nominal value. Likewise, since CRS overall resistance of the (unstable) ON state is $2R_{\mathrm{LRS}}$, so it is less affected by such variation.

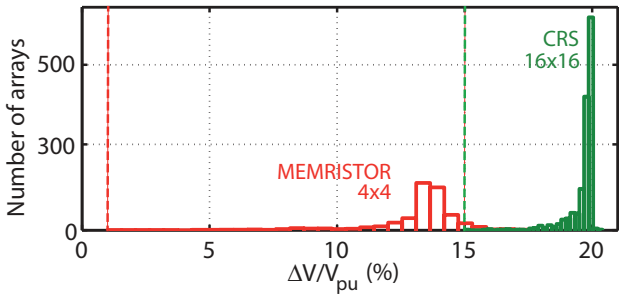


Fig. 10. The uncertainty associated with LRS, nanowires process variation, and nonideal initial state programming impact on memristor and CRS array by 1000 simulation runs, so 1000 arrays. The red and green lines illustrate minimum read margin for the memristive cross-point and CRS array, respectively.

### *C. Discussion*

Results of simulations indicate that the most important parameter that should be increased to achieve higher array sizes for a memristive array is $R_{\mathrm{LRS}}$. This research verify that a high $r(= R_{\mathrm{HRS}}/R_{\mathrm{LRS}})$ does not necessarily improve the substantial amount of parasitic path currents, while a higher $R_{\mathrm{LRS}}$ value guarantee a successful READ and WRITE operations.

In a CRS-based cross-point, the results is more significant since for a high $R_{\mathrm{LRS}}$ the effective resistance of HRS and LRS are significantly increased. Assuming a high

[3]An endurance of $10^{15}$ is required to replace SRAM and DRAM [1]. There is also an inverse relationship between endurance and data retention. To support reliable large array products, memory technologies must be able to retain data over a long lifetime ($> 10$ years at 85°C) with a low defect rates.

$R_{\rm LRS} = 3$ MΩ, $R_{\rm HRS} = 12$ MΩ ($r = 4$), and $V_{\rm READ} = 1$ V, READ operation results in a $\Delta V > 300$ mV. Analytically, the read margin (RM) does not depend on LRS or HRS resistances and it can be calculated using,

$$\mathrm{RM}_{\rm MEM} = \frac{1 + r - 2\sqrt{r}}{r - 1} \ , \tag{18}$$

which means for a 100 mV limitation $R_{\rm HRS}/R_{\rm LRS}$ ratio should be $\geq 1.3$. Similarly the simulations results show that such high value assumption for $R_{\rm LRS}$, RM is

$$\mathrm{RM}_{\rm CRS} = \frac{(r-1)\sqrt{2(1+r)}}{4(1+r) + (3+r)\sqrt{2(1+r)}} \ , \tag{19}$$

which results $r \geq 1.15$ ($> 3.6\%$) minimum requirement for a successful READ.

Our study also shows that for similar WRITE and READ access time and a high $R_{\rm LRS}$ value, energy dissipation ratio of a CRS array over a memristive array constantly increases. This ratio increases rapidly for $2 < r < 500$ and (practically) saturates for $500 < r < 3 \times 10^3$. The total (static and dynamic) power dissipation for an operation can be calculated using

$$P_{\rm total} = P_{\rm nano} + P_{\rm cmos} \ , \tag{20}$$

$$P_{\rm nano} = P_{\rm sel} + P_{\rm unsel} + P_{\rm pars} \ , \tag{21}$$

where $P_{\rm nano}$, $P_{\rm cmos}$, $P_{\rm sel}$, $P_{\rm unsel}$, and $P_{\rm pars}$ are the nano domain, CMOS domain, selected cells, unselected cells, and parasitic elements (nanowires) power dissipations, respectively. We assume that $P_{\rm cmos}$ for memristive and CRS arrays are comparable and $P_{\rm pars}$ is negligible. The unselected cells power dissipation can be identified by READ and WRITE schemes and can be divided into two (or more) subclasses of half-selected or unselected cells. This approach helps to identify the memory pattern dependency of the total power dissipation assuming a high $R_{\rm LRS}$.

The READ scheme that is discussed earlier, is used as the first READ scheme. Considering such a scheme and high $R_{\rm LRS}$ the total power dissipated by unselected cells (groups (1) and (2) in Fig. 5(a), through sneak currents) is negligible. Therefore, the worst case (reading "1") power consumption for $n \times m$ cells nano in the domain can be calculated through the following equation

$$P_{\rm nano,MEM} = \frac{n V_{\rm pu,MEM}^2}{R_{\rm LRS}(1 + \sqrt{r})} \ , \tag{22}$$

while similar approach for an $n' \times m'$ CRS array results

$$P_{\rm nano,CRS} = \frac{n' V_{\rm pu,CRS}^2}{R_{\rm LRS}(2 + \sqrt{2(1+r)})} \ , \tag{23}$$

where in this work $V_{\rm pu,MEM} = 1$ V and $V_{\rm pu,CRS} = 2.8$ V. To fill the gap between the power consumption in memristor and CRS arrays and having similar array size ($n \times m$), $n' = n/c$ and $m' = mc$, where $c$ is a constant that is adjusted to achieve approximately similar power consumption for the two arrays. Here $c = 4$, so for example, 1 K bits of data can be stored either in a $32 \times 32$ memristive array or a $8 \times 128$ CRS array and have roughly similar power dissipation.

In programming (WRITE) procedure, if $V_{\rm w,MEM} = 2$ V and $V_{\rm w,CRS} = 3.8$ V, there are $n + m - 2$ cells in the both arrays that are half-selected, groups (1) and (3) in Fig. 5(a), and $(n-1)(m-1)$ cells that are not selected, ideally 0 V voltage difference, group (2) in Fig. 5(a). The worst case condition is to have all of them at LRS for memristive array and LRS/HRS (logic "1") for CRS-based crossbar. Therefore, one potential problem with the WRITE scheme is to reset one or more half-selected cross-points. These cells are categorized under unselected cells for the power calculation. Here, there are 1 V and 1.9 V potential difference across the half-selected cells in memristor and CRS arrays, respectively, that is sufficiently low to avoid misprogramming. A power consumption analysis for this scheme shows that if $n > 16$ and $r > 3.5$, the total power dissipated in the CRS nano domain is much lower than the memristive array. The main reason is the all of the half-selected cells have an effective resistance equivalent to $(1 + r)R_{\rm LRS}$, whereas the same cells have $R_{\rm LRS}$ that is significantly lower. For example, for $n = 100$ and $r = 4$ overall improvement in power dissipation is around 38% while for $r = 10$ results 70% reduction. This improvement rapidly increases if the number of half-selected cells increases. For instance, a WRITE scheme that activates all bit-lines (pull-up) and $j^{\rm th}$ word-line (grounded) and applying $V_{\rm w}/2$ on the rest of the word lines, can write $n$ bits each time and contains $n(m-1)$ half-selected cells.

This study indicates that if $R_{\rm LRS} \ll 3$ MΩ, more than 65% and 50% of the total power (and consequently the total energy) is dissipated in half-selected cells during a WRITE operation for the 1-bit WRITE and multi-bit WRITE schemes, respectively. The contribution of half-selected cells is further increased if $R_{\rm LRS} \geq 3$ MΩ. The total power consumption is also rapidly increased as the array size increases. The results also indicate that writing a word (multi-bit) is much more energy efficient than a bit, particularly for CRS-based array. Note that for the multi-bit WRITE scheme we applied a two-step WRITE operation (SET-before-RESET) introduced in [47]. The trade-off between using several WRITE schemes is still an open question.

Due to the fact that a high $R_{\rm LRS}$ would decrease the energy dissipation and the operation speed at the same time it is very important to note that the nonlinearity of the memristor characteristics plays an important role in identifying the maximum size constraint of a memristive array by identifying the effect of half-selected memory cells.

Xu *et al.* [47] proposed a nonlinearity coefficient to analyze the nonlinearity effect using static resistance values of memristor biased at $V_{\rm w}/p$ and $V_{\rm w}$ as $K_{\rm c}(p, V_{\rm w}) = pR(V_{\rm w}/p)/R(V_{\rm w})$. This factor identifies the upper limit for $n$ and $m$ in a memristive array. If parameter $\alpha$ in $I \propto \sinh(\alpha V)$ represents memristor nonlinearity, the factor emphasizes that either higher $\alpha$ or higher $p$ results in a

larger $K_c(p, V_w)$. Clearly, the later option is under the designer's control. In fact, this technique effectively creates an intermediate $R_{LRS}$, which is larger than its actual value. Note that the resistance does not necessarily increase if $p$ increases. There is some examples that do not follow similar characteristics, for instance $\sinh^{-1}(\cdot)$ behavior in [33]. In this case, larger resistances are achievable by decreasing $p$. In [47], $K_c(p, V_w)$ is used for bit- and word-lines. Considering the $V_w/2$ scheme, this approach is appropriate when $p = 2$, $K_c(2, V_w)$. For $p > 2$, however, selected word-lines current cannot be calculated with $I(V_w/p)$ since the current that passes through an unselected cells on a selected word-line is a function of $V_w(1 - 1/p)$. Hence, calculating an upper limit for $n$ is a function of $K_r(p, V_w)$ that can be defined as,

$$K_r(p, V_w) = \frac{p}{p-1} \frac{R(V_w(1 - \frac{1}{p}))}{R(V_w)} \ , \tag{24}$$

therefore, a higher nonlinearity coefficient would not necessarily result larger upper limit for memristive array. Furthermore, controlling RESET parameters, such as filament formation process, electrode material, Joule heating process, and $TiO_2$ composition, plays a key role here.

## V. Conclusion

The presented work provides a foundation and a generic analytical approach to carry out simulations in the design of future memristive-based circuits and systems in general, and CRS arrays in particular. Simulation results indicate that due to sneak-paths and leakage current, a memristive array is faced with a programming and read error rate that aggressively limit the maximum nanocrossbar array size, whereas a CRS array is less affected by these problems. The read margin in a CRS array is also more robust against technology variations such as uncertainty in initial state programming, nanowire process variation, and the associated uncertainty on low resistance state programming.

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