An Approach to Deal With Packaging in Power Electronics

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***Abstract*—Current packaging technology in power electronics is based on assembling pre-manufactured discrete components. Each component consists of a number of parts, manufactured in a variety of manufacturing processes. This has resulted in a diversity of construction parts and mutually incompatible manufacturing processes in a typical power electronic converter and has brought power electronics to the edge where it becomes extremely difficult to reduce the cost and size of power electronic converters. This also makes integration of power electronic converters difficult.**

In this paper, we present a way to improve the physical construction of power electronic converters by increasing level of integration and using multifunctional construction parts. integration and packaging are two important aspects of physical construction of power electronic converters. Both of them and their mutual relationship are discussed in the paper. Three quantities intended to evaluate integration level and volumetric utilization namely functional elements integration level, K_I; packaging elements integration level K_P; and volumetric packaging efficiency η_v are introduced. Based on these values, a number of techniques to increase the integration level are presented. A design process in the form of a flowchart intended to implement these techniques in concrete design cases is presented.

***Index Terms*—Functional elements (FEs) integration level, packaging elements (PEs) integration level, power electronic converters, volumetric packaging efficiency.**

I. Introduction

PACKAGING technology is recognized as one of the constituent technologies and frontiers in power electronics development [1]. However, due to its multidisciplinary nature, packaging technology in power electronics lacks precise and well-defined terminology. Everything that is "nonelectrical" is assigned to packaging [2]. Packaging is mostly understood as semiconductor devices packaging, which is inherited from microelectronics and is unsuitable knowing that power electronics makes use of a variety of components including passive components.

Current packaging technology in power electronic converters is based on assembling pre-manufactured discrete components. Each discrete component, beside the part that performs basic electrical function, consists of a number of additional parts that provide connections to the outside world and insure the component's integrity. On the circuit level, these components are then linked to make a power electronic converter, again using a number of parts to insure the circuit's physical integrity to the outside world. These discrete components come from different manufacturers that have been optimizing their products over years to make them cheaper and smaller. Component manufacturers use different technologies and processes for different components or even different parts of the same component. This has resulted in a diversity of different parts and mutually incompatible manufacturing processes in a typical power electronic converter. This makes the overall process labour intensive and costly. Furthermore, this makes integration of power electronic circuits difficult. This methodology has brought power electronics to the edge where it becomes extremely difficult to reduce the cost and size of power electronic converters as well as to improve electrical performance imposed by the higher level, system requirements. Therefore, it has become clear that it is necessary to develop a new philosophy of packaging power electronic converters.

In the following text, an approach to tackle these issues is presented. The terms describing the physical construction of power electronics converters are systematically introduced. Furthermore, the quantities to evaluate the physical construction, particularly integration level, are presented. Based on these quantities, the construction of three case studies is evaluated. A number of techniques intended to improve these quantities in real products are introduced and discussed. Based on these techniques a design procedure in the form of a flow chart is presented. This procedure allows for designing the physical construction of a converter in a systematic manner ensuring that the final product has as high integration level and as few parts as possible within the specified range of technologies.

II. A Packaging Theory

A. Defining Packaging

Electronic packaging is a multidisciplinary technology and in power electronics extra dimensions are added due to the advanced thermal management that is used. For this reason, the term packaging is often loosely used and a variety of definitions can be found in the literature [2]–[4]. A commonly accepted definition of electronic packaging is: "Electronic packaging is the engineering discipline that combines the engineering and manufacturing technologies required to convert an electrical circuit into a manufactured assembly" where electrical circuit is defined as "the interconnection of electrical elements and devices to perform a desired electrical function". The engineering technologies include components technology, electrical, mechanical, thermal, chemical, etc. Following the classification of fundamental functions of a power converter [1] on:

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electronic function (switching, conduction and information), electromagnetic energy exchange function and thermal management function, we modify this definition to suit better the nature of power electronics: "Power electronic packaging is the combination of engineering and manufacturing technologies required to convert an electronic and thermal circuit as well as electromagnetic design into a manufactured assembly." Since information processing and power processing have the same limits (electromagnetic, thermo-mechanical, material) [5] despite different energy levels that they handle, this definition can be applied to electronic packaging on the whole.

B. Packaging Breakdown

In order to tackle the packaging problem, a suitable breakdown of packaging is introduced [6]. As the diversity of physical construction parts and manufacturing processes associated to them is identified as the major obstacle in improving construction of power electronic converters, the physical construction parts are used as the basis of this breakdown. We split them up according to the functions that they perform. Parts that perform the fundamental functions (electronic, electromagnetic and heat exchange) are referred to as functional elements (FEs). Typical FEs are: power and IC dies as semiconductor FEs, metallized film roll as capacitive FE, wire or planar copper conductors and magnetic core as magnetic FEs. Beside the basic or fundamental functions of a power converter, a number of functions must be performed in order to ensure proper functioning of the converter and the interface with the outside world. These functions are referred to as packaging functions and are classified in a few categories.

1) Electrical interconnection (providing electrical path for power and signals).
2) Thermal interconnection (providing thermal path for the heat dissipated by the parts).
3) Electrical insulation (providing integrity of electrical signals).
4) Environmental protection (providing protection of the parts and assembly from damaging due to handling, from environmental effects, especially moisture).
5) Mechanical support (providing mechanical support, rigidity, ductility).

Parts that perform the packaging functions are referred to as packaging elements (PEs). Typical PEs are: semiconductor devices lead frames, components leads, cases, bobbins, printed circuit board (PCB) dielectric etc.

According to their physical location in a power converter, PEs can be classified in packaging levels. The extensive classification of the packaging levels can be found in the conventional literature on electronic packaging [7]. For this purpose, two packaging levels can be distinguished.

1) Component packaging level (PEs that are physically part of the component).
2) Assembly packaging level (other PEs).

C. Evaluating Packaging

Due to the complex and multidisciplinary nature of packaging, it is very difficult to evaluate power electronic converters from the packaging perspective. A large number of evaluation criteria have to be taken account in order to get to an objective result. Also, for different applications, different criteria are more critical. It is expected that for consumer applications, the weighting factor for the cost criteria will be high, while in case of military or space applications, criteria such as reliability and geometrical constraints will be predominant.

In the previous work, a packaging figure-of-merit tree with the root in the ultimate cost-performance criteria is presented [6]. This ultimate target is branched in a number of packaging criteria. Some of them are quantitative in their nature (power density, thermal density, component density etc.). The others are fairly nebulous effects (manufacturing complexity, integration level etc.) and as such have to be quantified. The method of quantifying such fairly nebulous effects by means of proxy variable that is expected to be correlated with the effect uses the mathematical apparatus of Decision theory [8] and is described in [6]. By doing so, one ends up with a number of criteria at the final end of the tree that are implemented in a function that describes the "goodness" of the packaging solution. Some of these criteria are rather intangible for a power electronics engineer, particularly the criteria related to cost. In this paper we deal with the part of this tree that can be influenced by a packaging engineer, such as integration level, manufacturing complexity, carrier system etc.

D. Integration and Packaging

The recent trend in power electronics is to pursue a more integral design approach in order to achieve more cost effective production methods and higher power densities. Furthermore, packaging and integration, being associated to physical realization of power converters are closely related and identified as dominant technology barriers toward the growth of power conversion applications [9].

Based on the breakdown we can translate the integration of the functions into physical structures. If a number of parts in the structure can be replaced by one part that performs the same functions the manufacturing of the structure should be simplified and less material should be used. This is expected to bring a cost and size reduction. Combining some of these parts or integrating them in one physical part, reduction in cost due to the less material used and simplified manufacturing process and size is expected. Depending on the subject of integration, two levels of integration can be distinguished: FEs integration and PEs integration.

1) FEs integration—where a number of FEs is substituted with one that performs the same function. Reference [10] classifies FEs integration on integration technologies where discrete devices are made in an integrated process and integrated devices, where different functions are integrated into one device. Examples of FEs integration are: monolithic integration, electromagnetic LCT integration (integrated devices) on one side, and embedded passives, thick and thin film hybrid circuits (integrated technologies) on the other side.
2) PEs integration—where a number of FEs are integrated in one package, i.e., share the same PEs, such as housing,

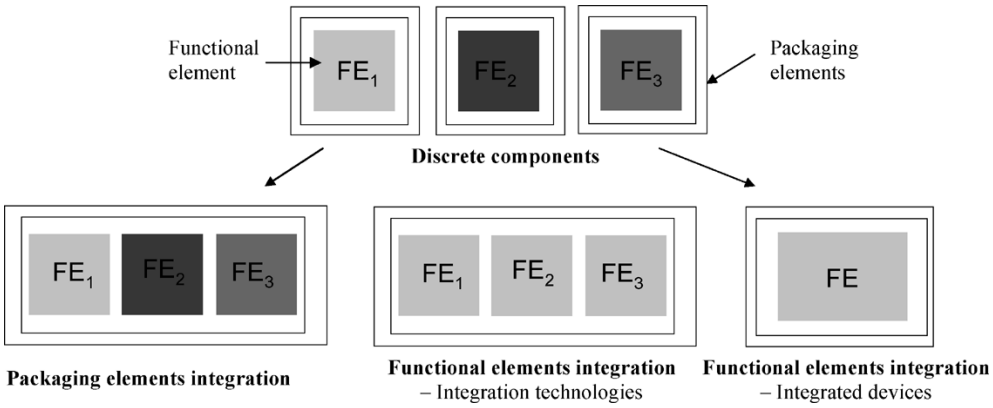

Fig. 1. Functional versus PEs integration.

mechanical support, thermal paths etc. Examples of PEs integration are: multichip modules (MCM), power modules, etc. In case of PEs integration, the number of FEs is still the same but benefits are in reduction of the number of PEs.

Fig. 1 illustrates the different types of integration. The standard approach, as already discussed, uses discrete components that each consists of one FE and a number of PEs. Different patterns in FEs symbolize different manufacturing processes. In case of PEs integration, the number of FEs remains the same but benefits are in the reduction of the number of PEs. As for FEs integration, integration technologies still have discrete FEs but made in the same manufacturing process. Finally, integrated devices technique results in one FE which gives benefits in fewer parts used, fewer manufacturing steps and smaller size.

Since the emerging packaging technologies in power electronics are mainly adapted from microelectronic packaging, the correlation between integration and packaging (or between FEs and PEs integration) can be explained by similar movements in microelectronics. Modern trends in microelectronic packaging [11] distinguish two packaging approaches: system-on-a-chip (SoC) and system-in-a-package (SiP). The first scheme designs all components on a single silicon chip, while the second includes two or more bare dies into one package. This difference is even more dominant in power electronics due to variety of components (including passives) and incompatibility of manufacturing processes of power semiconductors and control ICs. These limits (electromagnetic, manufacturing, economic etc.) determine how far integration can be pushed. It is when these limits emerge that packaging takes over.

E. Integration Level

The term "integration level" is often used in characterization of electronic systems to emphasize their benefits. Yet, it reflects different phenomena for different type of integration. In case of monolithic integration, integration level is defined as number of transistors per chip or per area unit. In case of hybrid integration, it is defined as the number of unpackaged components in a hybrid microcircuit package.

We define two quantities to describe and evaluate level of integration in power electronic converters. The quantity that describes the level of FEs integration is referred to as FEs integration level while the quantity describing PEs integration is referred to as PEs integration level. Let us first introduce the terms virtual functional and virtual PE. A FE that contributes to n circuit symbols in the discrete circuit schematic is "worth" n virtual FEs. Similarly, a PE that performs n packaging functions is "worth" n virtual PEs. In order to evaluate the level of FEs integration in a converter, a quantity FEs integration level (K_I) is defined as

$$K_I = \frac{\sum_i N_{\mathrm{FEv_i}}}{N_{\mathrm{FE}}} = \frac{N_{\mathrm{FEv}}}{N_{\mathrm{FE}}} \tag{1}$$

where N_{FE} is the total number of FEs in the converter, while $N_{\mathrm{FEv_i}}$ is the number of virtual FEs that the FE i is worth. N_{FEv} is the total number of virtual FEs in the converter. As an example, copper tracks in a planar integrated LCT element represent one FE. Since they take part in the inductance (windings), transformer (windings) and capacitance (electrodes), N_{FEv} of this element is three. In a discrete converter, each FE participates in only one schematic symbol, which gives N_{FEv} equal to N_{FE} and the integration level 1. In case of monolithic integration for, e.g., N_{FE} is equal to one as we have one chip, while N_{FEv} is equal to the number of elements in the schematic representation of the chip. The K_I value then corresponds to the definition of integration level in terms of monolithic integration. Furthermore, it is possible that a PE performs a fundamental function in which case that PE does not contribute to the total number of FEs N_{FE}, but represents one (or more) virtual FEs and thus increase the integration level value.

A quantity that evaluates level of PEs integration, PEs integration level (K_P), is defined as

$$K_P = \frac{\sum_j N_{\mathrm{PEv_j}}}{N_{\mathrm{PE}}} = \frac{N_{\mathrm{PEv}}}{N_{\mathrm{PE}}} \tag{2}$$

where N_{PE} is the total number of PEs in the converter while $N_{\mathrm{PEv_j}}$ is the number of virtual PEs that the PE j is worth. As an example, the substrate dielectric in a power module represents one PE. Since it provides mechanical support, a heat path as well as insulation, it acts as three virtual PEs, i.e., N_{PEv} of this element is three.

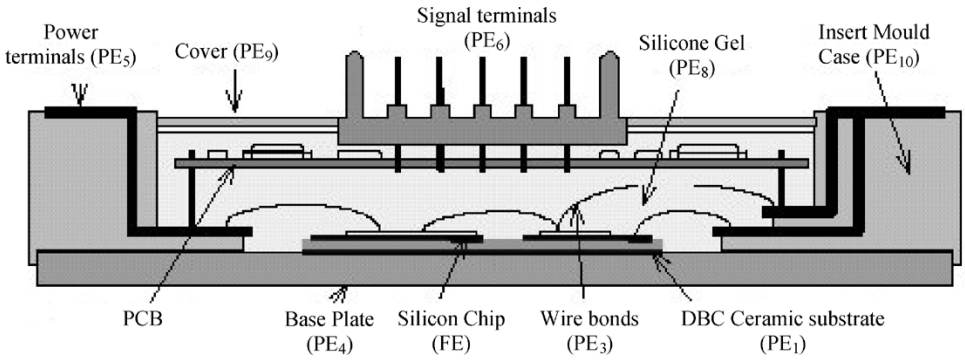

Fig. 2. Conventional intelligent power module (IPM) [15].

F. Volumetric Packaging Efficiency

Since high power densities have become a high priority target in packaging of power electronic converters, it is desirable to have the "nonfunctional" volume in a converter reduced to minimum or to package the converter as efficiently as possible. Packaging efficiency in electronic packaging is introduced as percentage of area in an interconnection substrate that is occupied by silicon [13]. Analogous to this definition and taking into account specific nature of power electronics including variety of components including passive components and importance of the third dimension or volume for power processing, volumetric packaging efficiency can be introduced as percentage of volume in a converter that is occupied by FEs [6]

$$\eta_v = \frac{V_{\mathrm{FE}}}{V_{\mathrm{TOT}}} \tag{3}$$

where V_{FE} is the volume occupied by FEs and V_{TOT} is the total converter volume.

III. Analysis of Power Modules

In the past few decades, much activity has been focussed on developing better packaging techniques in power modules, including improved interconnection techniques, advanced thermal management and larger number of integrated functions [5], [12], [14]. Other areas in power electronics product trees are much less advanced. For these reasons, three power modules that use different packaging techniques have been chosen for packaging analysis.

A. Conventional Intelligent Power Module [15]

This intelligent power module (IPM) consists of power switching insulated gate bipolar transistor (IGBT) devices with integrated drive and protection circuits. The construction of the module is shown in Fig. 2 and utilizes conventional power module technologies, thermally conductive DBC substrate and wire bonding interconnection technology. The IGBT chips are soldered onto the substrate and the substrate is soldered to the base plate. The assembling time is reduced by using the insert moulded case that has the power electrodes moulded into its sides rather than inserted after the case is moulded. The next step is interconnecting the circuitry by means of wire bonding. The gate drive and control circuits are realized on a conventional PCB and mounted above the power circuitry. The electrical connections between PCB and DBC are provided by pins. The module is encapsulated with the silicon gel for the protection purposes. The assembly is finished by inserting a plastic cover.

Let us consider the packaging characteristics of this power module. There is no functional integration since all the power semiconductors as well as the control components are in their discrete form and each of them performs only one function, i.e. $N_{\mathrm{FE}} = N_{\mathrm{FEv}}$ which gives $K_{\mathrm{I}} = 1$. As for the PEs integration, the number of PEs is $N_{\mathrm{PE}} = 10$ (designated in Fig. 2). The concept of PEs can be seen more clearly from this example. For, e.g., wirebonds are counted as one PE, although there are obviously a number of them in this power module. The reason for this is that they are made in one manufacturing step which is what determines the complexity of the physical construction and eventually the cost. In this connotation, PE is an inseparable structure made in one manufacturing process.

1) DBC ceramic dielectric provides mechanical support, thermal function and insulation, hence the number of virtual PEs that it represents is $N_{\mathrm{PEv1}} = 3$.
2) DBC copper provides electrical interconnections as well as heat spreading function $\rightarrow N_{\mathrm{PEv2}} = 2$.
3) Wirebonds electrically interconnect the MOSFETs $\rightarrow N_{\mathrm{PEv3}} = 1$.
4) Base plate acts as mechanical support and heat spreader $\rightarrow N_{\mathrm{PEv4}} = 2$.
5) Power and signal terminals electrically interconnect the module with the outside world $\rightarrow N_{\mathrm{PEv5,6}} = 1$.
6) Pins electrically connect the power module and the control PCB $\rightarrow N_{\mathrm{PEv7}} = 1$.
7) Silicone gel provides protection and electrical insulation $\rightarrow N_{\mathrm{PEv8}} = 2$.
8) Case and the top cover protect the module $\rightarrow N_{\mathrm{PEv9,10}} = 1$.

From (2) follows (4), shown at the bottom of the next page.

In this analysis only the power part of the module is considered. If the control board is taken into account the K_P value will drop, since the board is made out of discrete, packaged components.

It is important to note that, although an element theoretically performs a number of functions, only the functions that the element makes a significant contribution to, are attributed to that element. For example, the wire bonds in the above power module conduct the heat dissipated by the power semiconductor dies but their contribution is very small and hence is not included in the analysis.

B. Power Module in Embedded Power Technology [5]

Embedded Power technology has been developed for achieving high density three-dimensional (3-D) integration of quasiplanar power modules. A power module implemented in this technology consists of three levels: embedded power chips stage, a base substrate, and electronic components (gate drive, control, and protection circuitry), which are soldered together to build the final assembly. The core of the structure is the embedded power stage that comprises the ceramic frame, power chips mounted in the openings of the ceramic frame, isolation dielectrics and metallized circuit. Fig. 3 shows the cross section of a power module realized in embedded power technology with the indication of functional and PEs in the module. For the same reasoning as in the previous example, there is no FEs integration and $K_I = 1$.

The number of PEs as indicated in Fig. 3 is $N_{\mathrm{PE}} = 8$. The DCB ceramic performs mechanical, insulating and thermal function, hence, the number of virtual PEs that it represents is $N_{\mathrm{PEv1}} = 3$; the DCB copper performs heat spreading and electrical connection, $N_{\mathrm{PEv2}} = 2$; the metallization layer provides electrical interconnections and can be spread over a large area for heat removal, $N_{\mathrm{PEv3}} = 2$; the dielectric layer provides the insulation for metallization and protection of the power chips, $N_{\mathrm{PEv4}} = 2$, the ceramic frame mechanically supports the power chips, $N_{\mathrm{PEv5}} = 1$; the adhesive polymer is dispensed for mechanical support of the chips, $N_{\mathrm{PEv6}} = 1$; the power pins electrically connect the module to the outside, $N_{\mathrm{PEv7}} = 1$ and finally the housing provides protection, $N_{\mathrm{PEv8}} = 1$. Again, only the power part of the module is considered. Then, from (2), follows (5) shown at the bottom of the page.

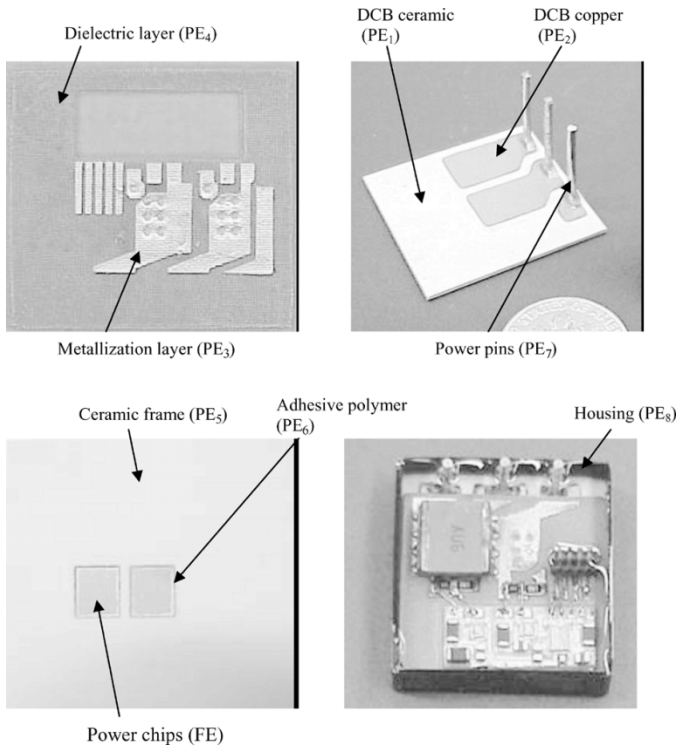

Fig. 3. Embedded power module.

C. Power Module on Lead Frame [16]

The two packaging technologies for power modules described above utilize expensive thermal conductive ceramic substrates at the same time building up the number of PEs in the assembly. The following packaging technology employs a transfer moulded lead frame design with few manufacturing steps for integrating power devices, gate drive and protection. It is intended for lower power range (up to 2 kW). Both power and control chips are mounted on a lead frame and moulded for protection. The cross section of the module is shown in Fig. 4. As there is no FEs integration, the value of $K_I = 1$. The total number of PEs is five as indicated in Fig. 4. The lead frame electrically interconnects and mechanically supports the circuitry and removes the heat, therefore $N_{\mathrm{PEv1}} = 3$, the wirebonds electrically connect the metallized semiconductor

$$\begin{aligned} K_P &= \frac{\sum N_{\mathrm{PE_{vj}}}}{N_{\mathrm{PE}}} \\ &= \frac{N_{\mathrm{PE_{V1}}}\langle \text{DBC diel.}\rangle + N_{\mathrm{PE_{V2}}}\langle \text{DBC copper}\rangle + N_{\mathrm{PE_{V3}}}\langle \text{wirebonds}\rangle + N_{\mathrm{PE_{V4}}}\langle \text{base plate}\rangle + N_{\mathrm{PE_{v5,6,7}}}\langle \text{el.terminals}\rangle}{N_{\mathrm{PE}}} \\ &\quad + \frac{N_{\mathrm{PE_{V8}}}\langle \text{sil.gel}\rangle + N_{\mathrm{PE_{V9}}}\langle \text{cover}\rangle + N_{\mathrm{PE_{V10}}}\langle \text{case}\rangle}{N_{\mathrm{PE}}} \\ &= \frac{15}{10} = 1.5 \end{aligned} \tag{4}$$

$$\begin{aligned} K_P &= \frac{\sum N_{\mathrm{PE_{vj}}}}{N_{\mathrm{PE}}} \\ &= \frac{N_{\mathrm{PE_{V1}}}\langle \text{DBC diel.}\rangle + N_{\mathrm{PE_{V2}}}\langle \text{DBC copper}\rangle + N_{\mathrm{PE_{V3}}}\langle \text{ metal.layer}\rangle + N_{\mathrm{PE_{V4}}}\langle \text{ diel.layer}\rangle + N_{\mathrm{PE_{V5}}}\langle \text{ ceramic frame}\rangle}{N_{\mathrm{PE}}} \\ &\quad + \frac{N_{\mathrm{PE_{v6}}}\langle \text{adhes.polymer}\rangle + N_{\mathrm{PE_{V7}}}\langle \text{power pins}\rangle + N_{\mathrm{PE_{V8}}}\langle \text{case}\rangle}{N_{\mathrm{PE}}} \\ &= \frac{13}{8} = 1.63 \end{aligned} \tag{5}$$

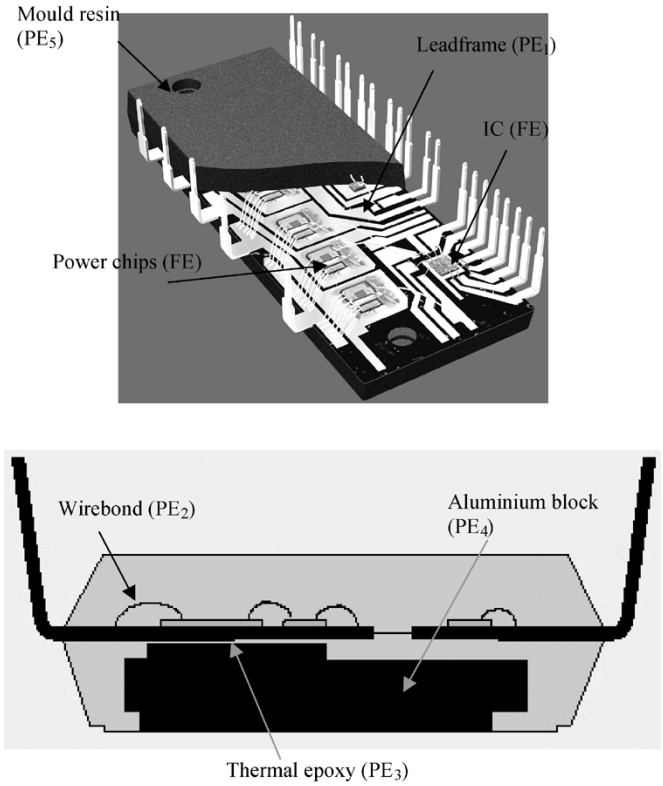

Fig. 4. Moulded lead frame power module.

terminals to the rest of the circuitry, $N_{\mathrm{PEv2}} = 1$; the thermal epoxy insulates the power chips from the heatsink and conducts the heat from the chips to the aluminum block, $N_{\mathrm{PEv3}} = 2$; the aluminum block conducts the heat to the heatsink, $N_{\mathrm{PEv4}} = 1$ and the mould resin encapsulation protects the assembly, mechanically holds it together and serves as insulation $N_{\mathrm{PEv5}} = 3$.

From (2) follows (6), shown at the bottom of the page.

The K_I and K_P values for all the three power modules are calculated and shown in Table I. From the results can be concluded that the level of functional integration in power modules is low, for the simple reason that packaging technologies used in power modules use discrete MOSFET (and IC) dies and package them together. Regarding PEs integration, conventional packaging techniques used in power modules use large number of parts and processes while the power module on lead frame has higher level of packaging integration level due to the low number of parts and their multifunctionality.

Since the dimensions of the analyzed power modules are not known to the author the volumetric efficiency values are not calculated. However, it is expected that the lead frame power module will achieve the highest value of volumetric efficiency due to the less volume occupied by the PEs compared to the other modules.

TABLE I
FUNCTIONAL AND PACKAGING INTEGRATION LEVEL OF POWER MODULES

	Conventional IPM	Embedded Power module	Power module on lead frame
K_I	1	1	1
K_P	1.5	1.63	2

IV. TECHNIQUES AND DESIGN PROCESS TO IMPROVE PACKAGING

Now that the quantities that describe integration level in power electronic converters are introduced and the main drawbacks of the present construction practice identified, the next step is to identify methods to increase these quantities and eventually implement them in real converters.

1) **FEs integration**—It is clear from (1) that the K_I value can be increased by FEs integration. The number of FEs, N_{FE}, decreases with integration. Furthermore, one FE will perform more functions which will increase N_{FEv}. Examples are silicon monolithic integration, electromagnetic integration of passives etc.
2) **Reduction of number of packaging levels**—We have identified two packaging levels in conventional discrete packaging. Components are provided with connections, mechanical support, protection and their own heat sinking. On the circuit level, these components are interconnected electrically, thermally and mechanically. Finally, the circuit is encased for protection and electrically interconnected with the outside world. By "transferring" these packaging functions from components to a higher level, e.g. the board level, the total number of PEs (N_{PE}) can be reduced. An example is using bare, unpackaged components, as seen in power modules or hybrid circuits.
3) **Sharing PEs**—In the discrete packaging approach, the components' PEs serve only one component. If more FEs share PEs (housing, mechanical support, thermal elements) the N_{PE} ratio will decrease and K_P will increase. An example is Multichip modules that make use of a common substrate that electrically interconnects and mechanically supports a number of bare semiconductors. Thermal PEs integration (the heat path is common for a number of FEs) is another example of sharing PEs. The better thermal performance is also achieved [19].
4) **Multifunctional PEs**—In order to perform one of the packaging functions, a PE must exhibit certain physical

$$K_P = \frac{\sum N_{\mathrm{PE_{vj}}}}{N_{\mathrm{PE}}} = \frac{N_{\mathrm{PEv1}}\langle\text{lead frame}\rangle + N_{\mathrm{PEv2}}\langle\text{wirebonds}\rangle + N_{\mathrm{PEv3}}\langle\text{thermal ep.}\rangle + N_{\mathrm{PEv4}}\langle\text{alum.bl.}\rangle + N_{\mathrm{PEv5}}\langle\text{mould res.}\rangle}{N_{\mathrm{PE}}} = \frac{10}{5} = 2 \quad (6)$$

properties, such as electrical or thermal conductivity, mechanical strength, moisture absorption etc. By designing a PE in a way that it fulfils more of these requirements one can make use of one element for more than one packaging function, i.e., N_{PEv} of the PE increases, which results in increasing of K_P. For e.g. a metal lead frame due to its electrical and thermal conductivity as well as mechanical strength can perform electrical interconnection, heat removal and mechanical support function.

5) **PEs and FEs duality**—Following the idea of multifunctionality, it is natural to question if the FEs can be designed to perform some of the packaging functions or, vice versa, if some properties of the PEs used in existing, commercially available technologies can be used to perform the fundamental functions. The result is that the value N_{PE} or N_{FE} decrease which, consequently, increases the values K_P or K_I. The enhanced PCB dielectric is used as the capacitive element for embedded capacitors [10]. Additionally, it has been shown that the magnetic core can be used to enclose the whole converter and for heat removal and protection [17].
6) **Geometrical packaging**—Geometrical reshaping of FEs and improved 3-D spatial layout is a way to improve the volumetric packaging efficiency (η_V). This way, the converter volume taken up by air (or other insulator) can be reduced and higher power densities achieved [18].

Fig. 5 shows the design process of implementing these methods in packaging of concrete converters. The process consists of four phases. It starts with input specifications such as electrical specifications, environmental requirements, volumetric specifications etc. After the circuit topology is chosen (with minimum feasible number of FEs), a library of available technologies that can be used to construct the converter is made. This library consists of technologies viable from manufacturing, cost and power rating viewpoints. This is where the first phase ends.

In the second phase, integration of FEs takes place (Technique 1). Depending on the circuit schematic and the technology characteristics, the FEs integration is pushed as far as the previously mentioned limits allow. At the end of this phase, all FEs (or a few possible sets of FEs) are identified. This is the end of the second phase.

The third phase deals with integration of PEs. This phase is performed for each chosen technology. The first step is to choose a carrier (mechanical support and electrical interconnections PE). In some cases, particularly in low power range, one of FEs could be used as a carrier (Technique 5). If this is not possible, then a carrier is chosen depending on the technology. Certain carriers (or their parts) can be used as FEs (Technique 5). If this is possible, the initial set of FEs can be reduced. The next step is enhancing the functionality of the carrier. The possibility of modifying the carrier to perform more packaging functions and to be shared (Techniques 3 and 4) between all the FEs (both power and control for, e.g.) is considered. Next, the possibility of using bare, unpackaged components (Technique 2) is considered. This mainly depends on mechanical and thermal properties of the carrier. If this is not possible, it is necessary

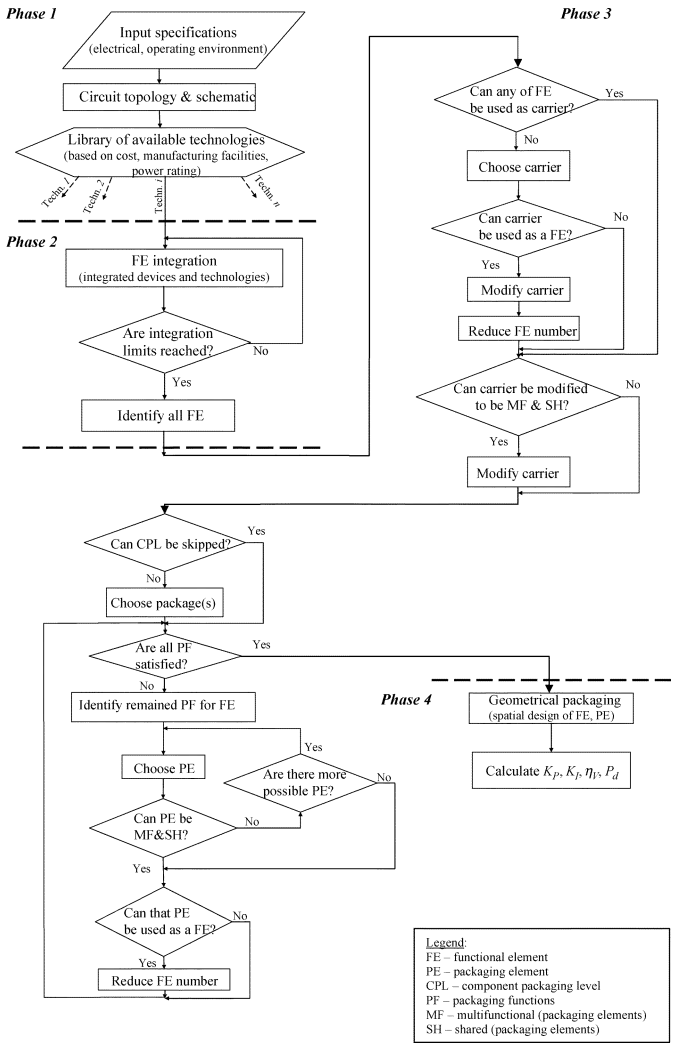

Fig. 5. Design process for improving packaging.

to choose packages for FEs (several options could be identified, e.g., SMD and through hole). After this, it is checked if all the packaging functions are satisfied, i.e. if the assembly is electrically connected, operates with the desired thermal behavior (based on results of thermal analysis), mechanically supported, electrically isolated and protected from the environment. If this is not satisfied, it means that introducing additional PEs is necessary. Again, the procedure of searching for multifunctional and shared PEs for the remained functions is repeated. Some of these PEs can be used as FEs, which reduces the set of the FEs. Once all the packaging functions are satisfied, the third phase ends.

In the fourth phase the final decisions of technologies and packages of discrete components are made and the functional and PEs are spatially designed to achieve high power densities and volumetric packaging efficiency.

Finally, all the designs (coming from different technologies at the input of the second phase are compared. The values of integration level (K_P and K_I), volumetric packaging efficiency (η_V) and power density are calculated and the best design is chosen. The implementation of this design process is shown on a case study in [20].

As the list of technologies is made in the beginning of the design process the presented procedure is limited to commercially available technologies only. During the design process, a need for new manufacturing processes and materials may appear which requires close cooperation of the designer with the manufacturing industry and material suppliers. Furthermore, even if technologies chosen in the beginning of the design process essentially lend themselves to mass production, the external factors, such as technology immaturity and limited usage can affect its cost-effectiveness compared to conventional technologies. Finally, each choice in the design procedure should be followed by the appropriate analysis in order to ensure that the fundamental functions performance is not jeopardized. This will ensure that the final product not only has a high level of integration but also that the new design with a reduced number of parts has an equally good or better performance compared to the conventional solutions.

V. Conclusion

The necessity of changing the present practice of packaging in power electronic converters is elaborated. In order to meet the future size, cost, and performance requirements, the discrete converter must be stripped down and put back together in a better way. Integration is often seen as a way to reduce the size by incorporating more components into one, and decrease cost by using the same manufacturing processes for a number of components. This type of integration is well known and in this paper is referred to as FEs integration. Yet, the implementation of this type of integration is limited by a number of factors including electromagnetic, economical, material etc. Another type of integration, referred to as PEs integration gives a lot of room for improvement. By combined use of integrated devices and technologies on one and smart, multifunctional parts on the other side we may expect positive movements in construction of power electronic converters.

This paper gives the means to evaluate the level of both types of integration as well as the methods to improve them in actual converters. In this manner, successful designs in a specific area in the power electronics product tree can indicate directions and form basis for further improvement. The presented design process can be used to improve packaging in designing any power electronic converter regardless of the specific nature of the concrete example.

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