KYOTO INSTITUTE OF TECHNOLOGY

An Area-efficient 65 nm Radiation-Hard Dual-Modular Flip-Flop to Avoid Multiple Cell Upsets

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発表概要

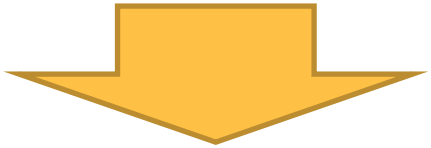
- 目的
  - 耐ソフトエラーFFの研究
  - レイアウトレベルにおけるMCU対策
- 評価方法
  - MCU対策を行った回路をチップに搭載
  - 中性子ビームを照射
- 結果
  - 非MCU対策時に比べ、8倍のMCU耐性

Outline

- Background & Motivation
- Relation between MCUs and Component Distance
- Layout Structure to Avoid MCUs
- Experimental Result
- Conclusion

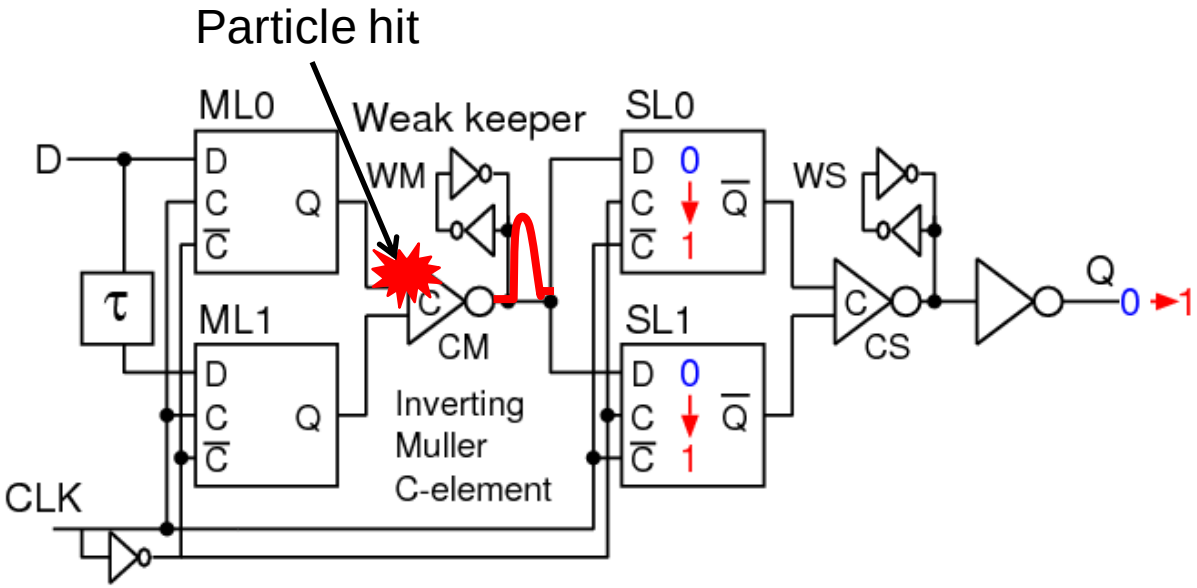
Background (1)

- LSI less reliable to soft errors by process scaling

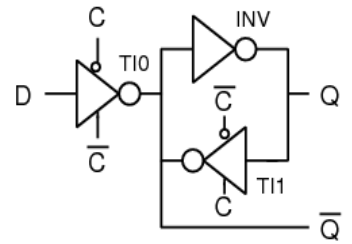


- Redundant FFs are used to reduce soft errors
  - TMR, BISER…

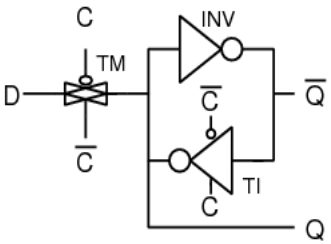
Conventional DMR (BISER) FF



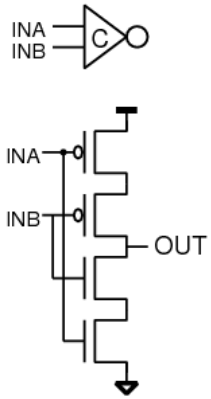
[S. Mitra et al. ITC 2006]



Master Latch
(ML0, ML1)



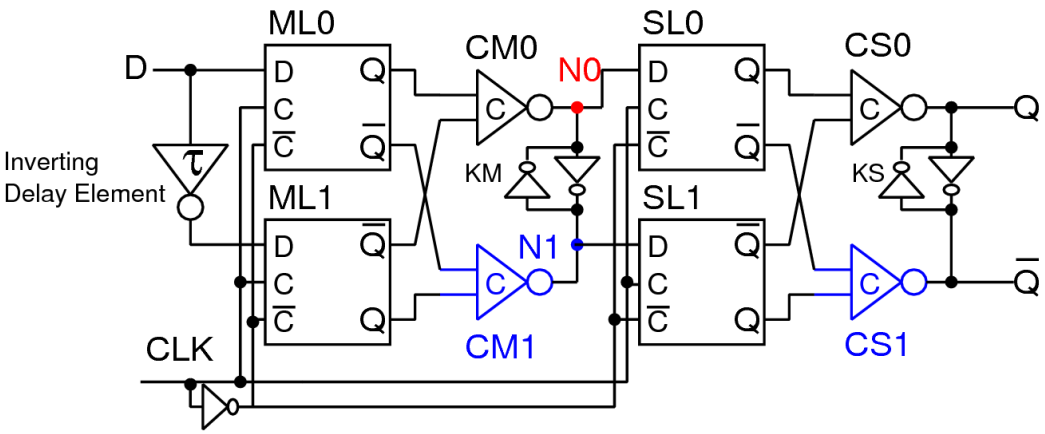
Slave Latch
(SL0, SL1)

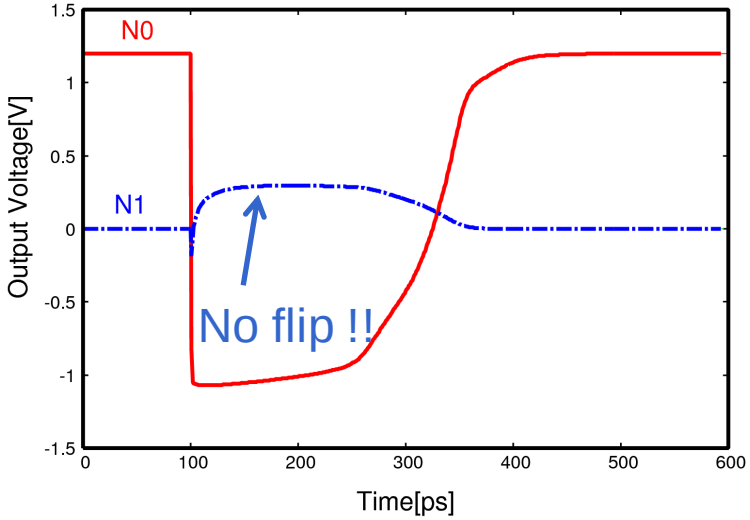


Inverting
Muller
C-element

- C-element (CM) is connected to both of slave latches
  - Weak to SET on CM
  - Higher SER at higher clock freq.

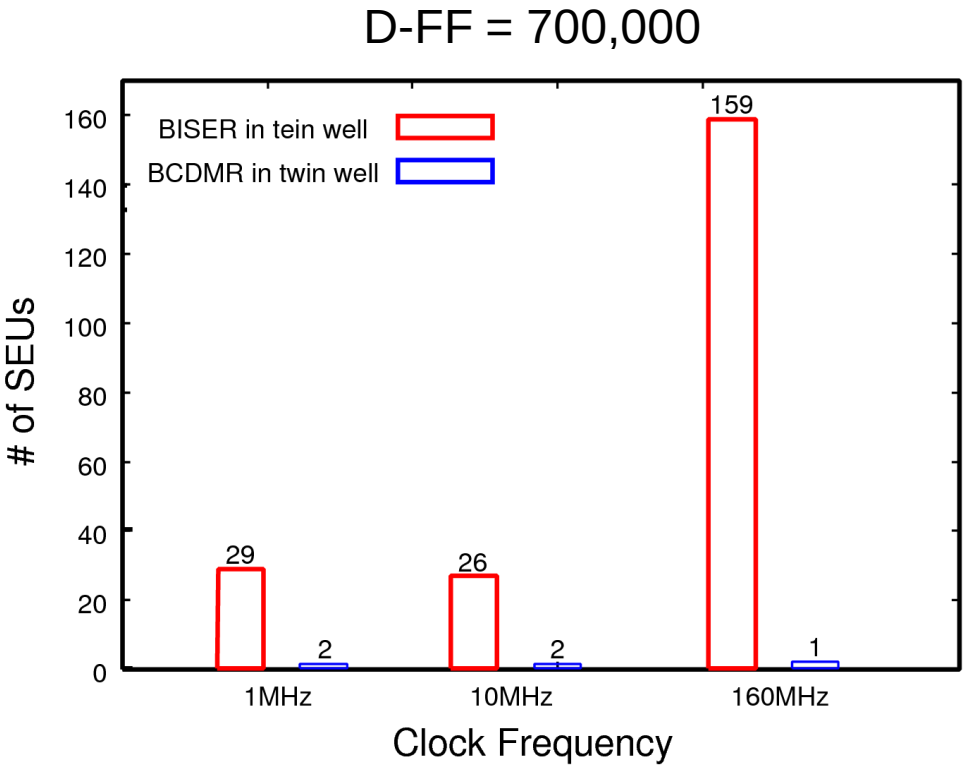
Proposed BCDMR FF





- Duplicate C-element (CM0+CM1, CS0+CS1)
- While N0 is flipped, N1 is almost stable
  - SET on CM only influences one of slave latches
  - Strong to SET on CM

SERs by Alpha-Particle Irradiation

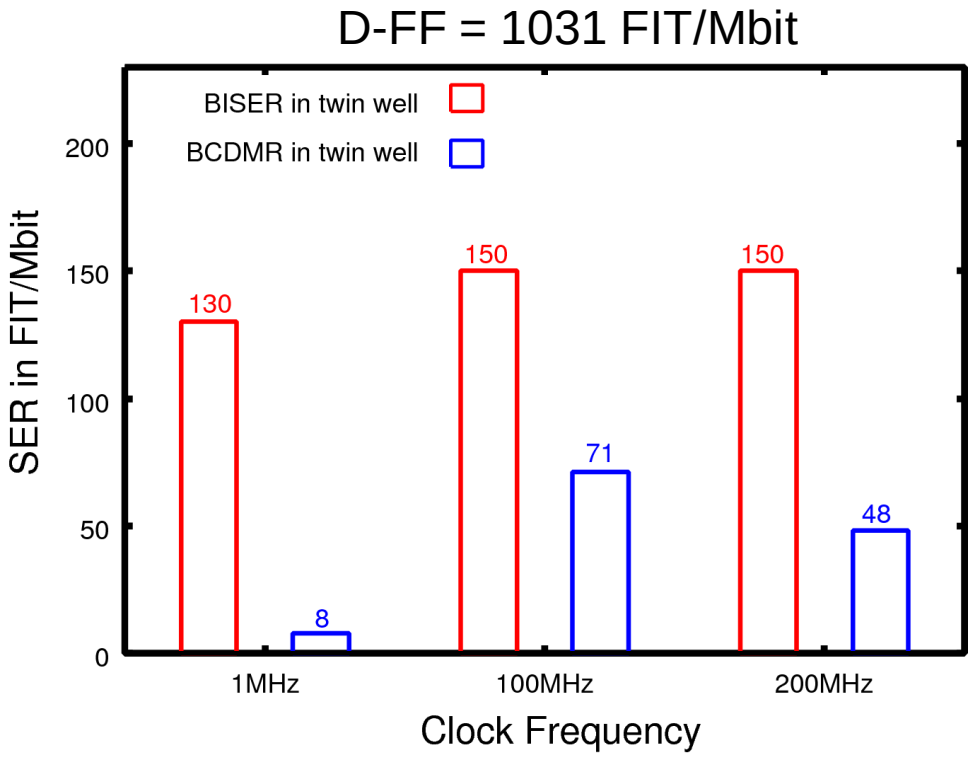


- Accelerated test using alpha source (Am-241)
- BCDMR has better resilience
  - 700,000x stronger than D-FF at 160 MHz
  - 159x stronger than BISER at 160 MHz

Background (2)

- High-energy neutrons have higher possibility of MCUs
- Process scaling makes the probability of MCUs higher because of
  - Sensitive Volume ≈ Cell Area
  - Lower Q_{crIt}
- MCUs is one of critical issues diminishing soft error resiliency of rad-hard designs

SERs by Neutron Irradiation



- Accelerated test using spallation neutron beam
  - Measured for 100 min.
- BCDMR has low resilience at 100 MHz
  - Only 10x stronger than D-FF

Outline

- Background & Motivation
- Relation between MCUs and Component Distance
- Layout Structure to Avoid MCUs
- Experimental Result
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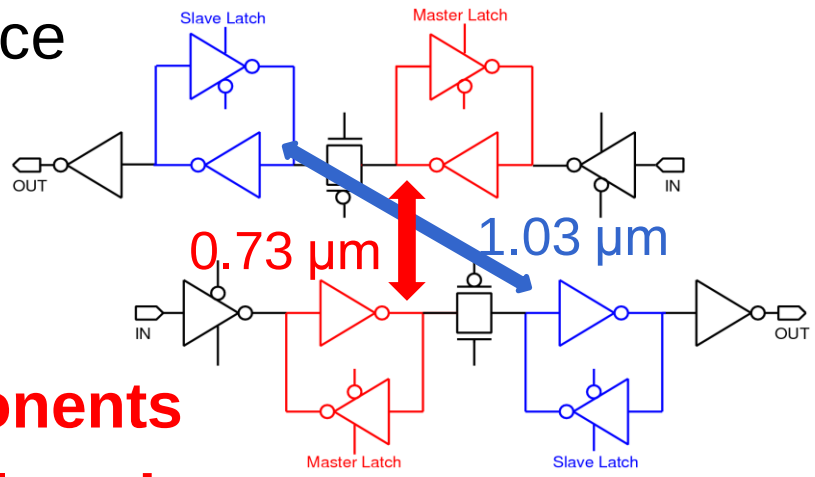
MCUs and Component Distance

D-FF array to measure MCU/SEU

- Although the difference of distance is 0.3 μm, MCU rate is 1/4
- **MCU strongly depends on component distance**
- **MCU among redundant components become dominant, if closely placed**



Latch	Min. Dis.	# SEUs	# MCUs	# M/# S
Master	0.73 μm	541	88	16 %
Slave	1.03 μm	493	19	3.8 %

+0.3 μm **1/4**

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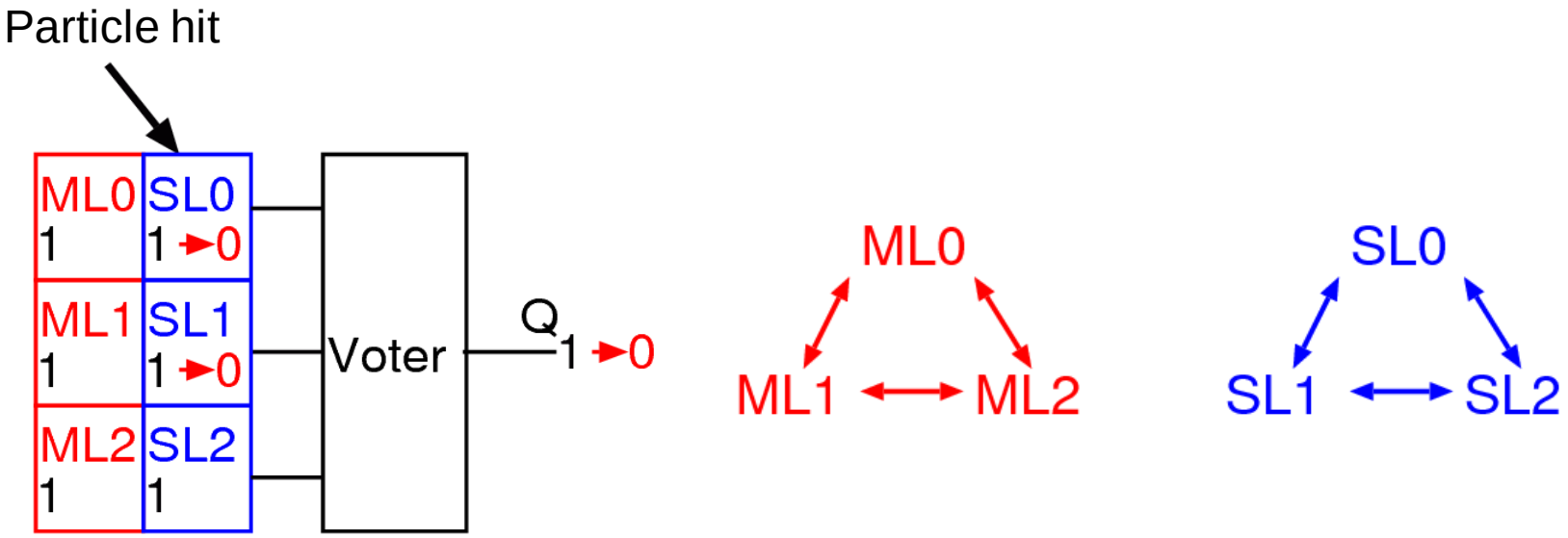
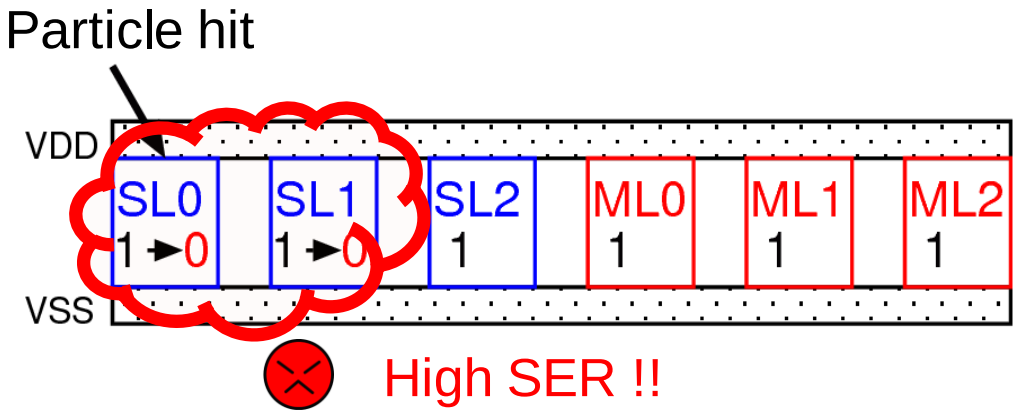
Critical Components in TMR

- Two of three MLs/SLs are flipped,
  Q become wrong
  - A pair of latches called critical components

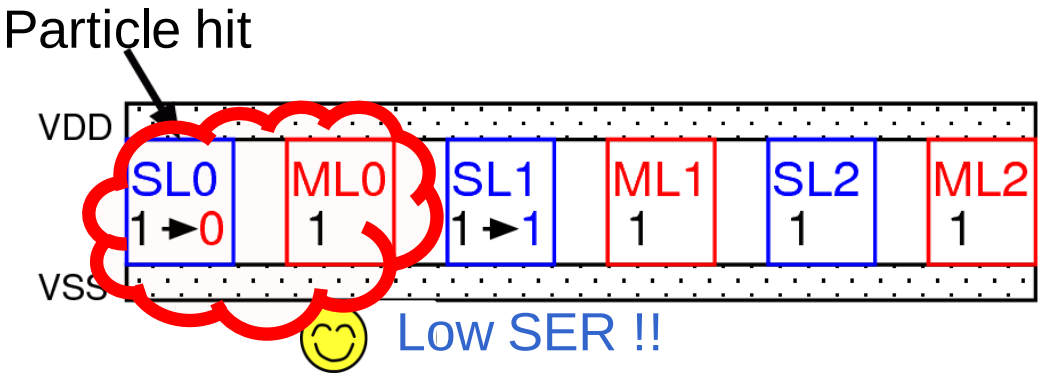


Floorplan to avoid MCUs in TMR

- If critical components are placed closely, they are flipped easily

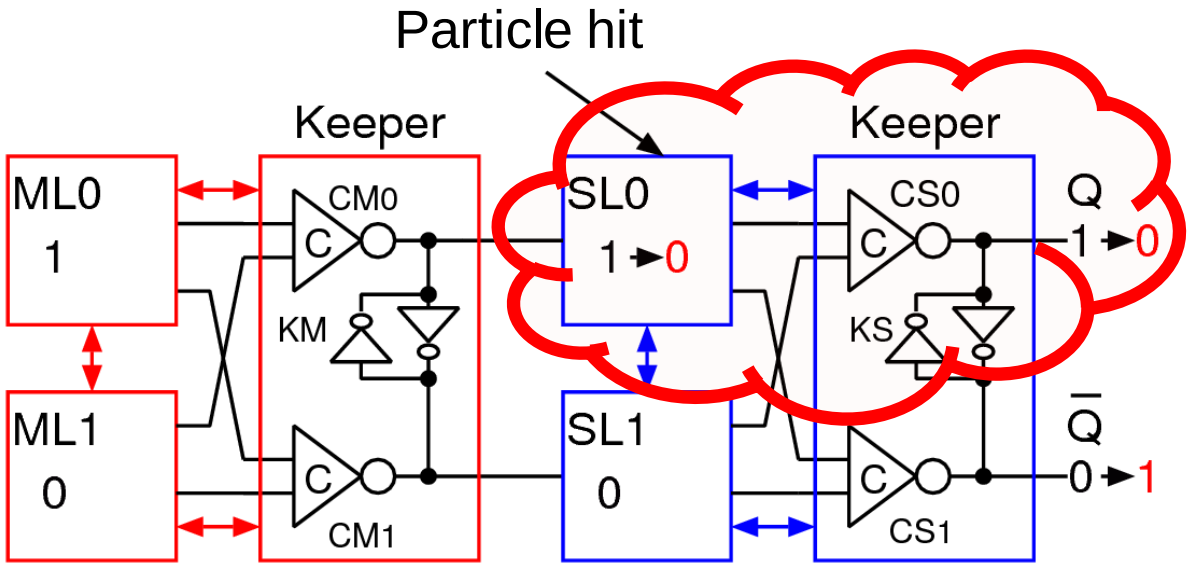


- Interleaving is very effective to prevent MCUs



Critical Components in BCDMR

- Two of MLs/SLs and keeper are flipped, Q become wrong
  - Place them as far apart as possible !!

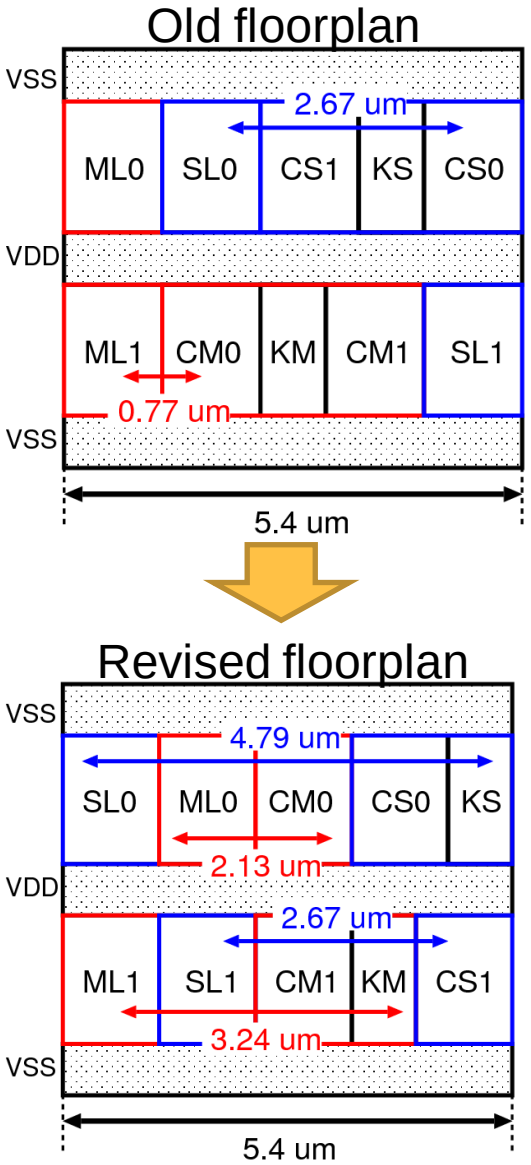


Critical components
- ML0 + ML1
- ML0 + Keeper
- ML1 + Keeper

Critical components
- SL0 + SL1
- SL0 + Keeper
- SL1 + Keeper

Floorplan to avoid MCUs in BCDMR

- In old floorplan, distance between Crit. Comp. is short
  - Lower MCUs tolerance
- In revised floorplan, place them separately
- Min. Dis. Between Crit. Comp. is 2.8x without any area overhead !!



		Min. Dis.
BCDMR FF	old	0.77 μm
	revised	2.13 μm

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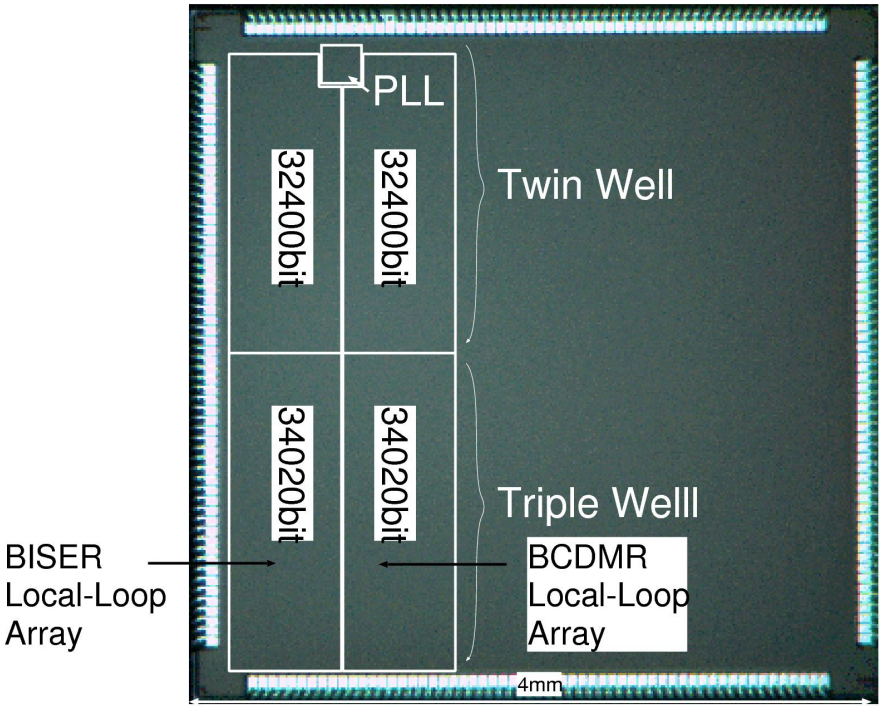
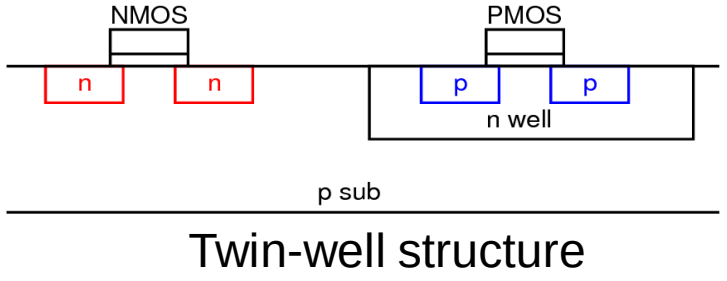
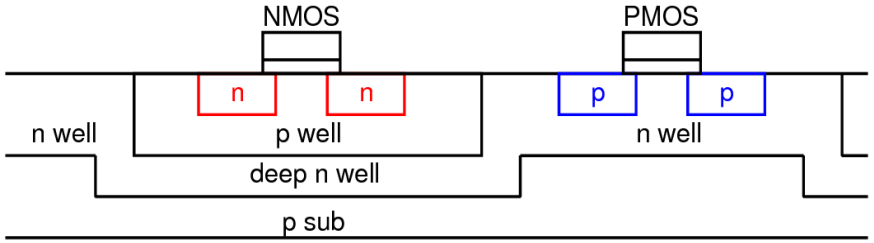
Chip Micrograph





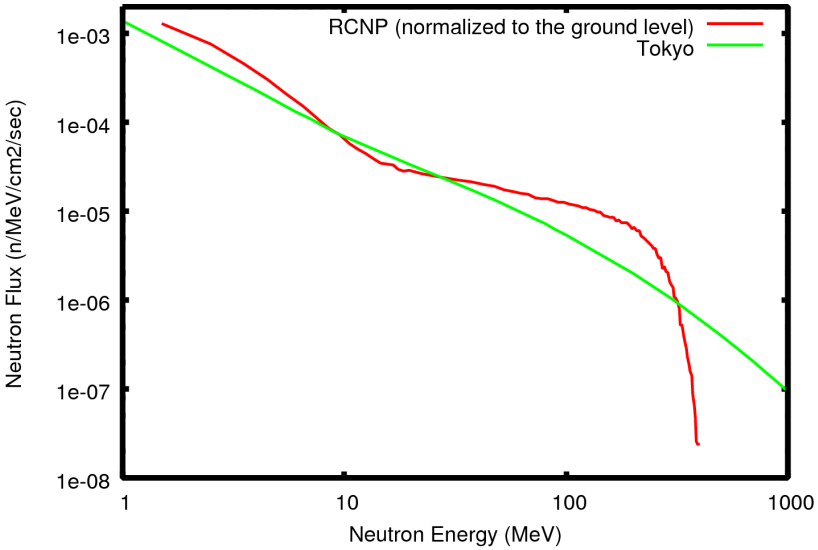
Twin-well structure

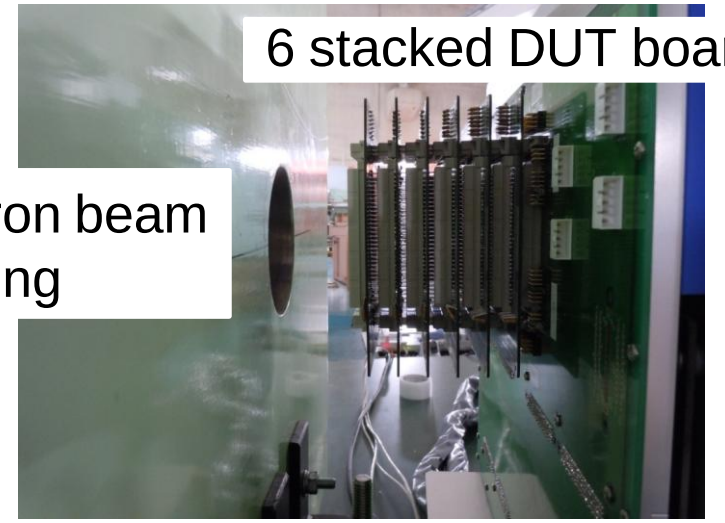


Triple-well structure

- Fabricated a 65 nm chip including two FF arrays on twin-well and triple-well structure
  - BCDMR FF array (right side), BISER (left side)

Experiment Setup

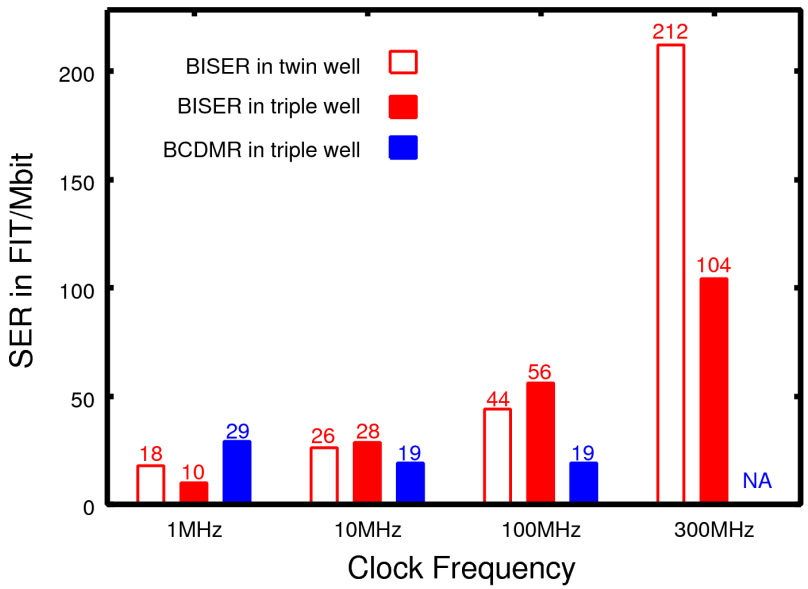




- Accelerated test using spallation neutron beam
- At Research Center for Neutron physics (RCNP) of Osaka University
- 16 test chips using 6 stacked DUT boards
  - Measured for 50 min.
  - Retrieve stored values every 5 min.

Results

D-FF = 1031 FIT/Mbit

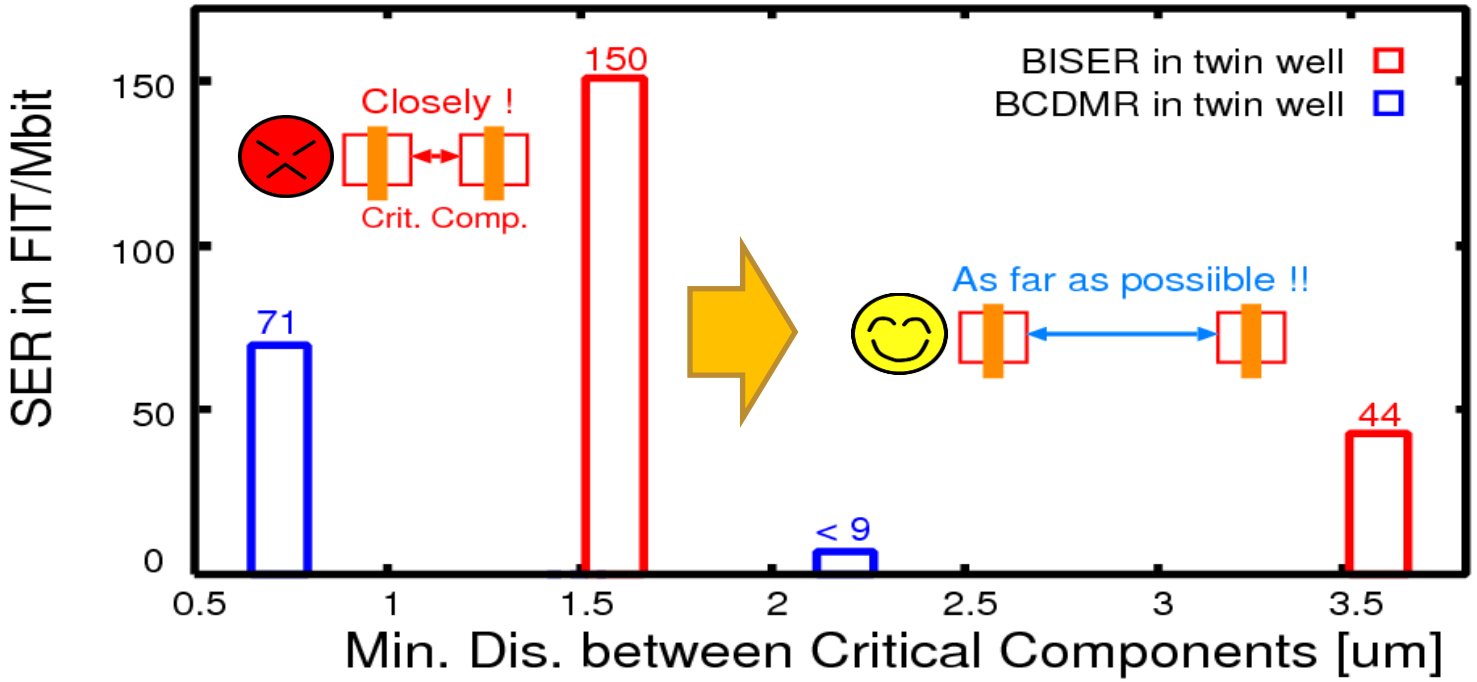


SER in FIT/Mbit

	well	Clock Freq.[MHz]			
		1	10	100	300
BISER	twin	18	26	44	212
	triple	10	28	56	104
BCDMR	twin	< 9 (No error)			-
	triple	29	19	19	-

- SER on the BISER FFs is increasing according to clock freq.
  - Weak to SET on C-element
- <9 FIT/Mbit on the BCDMR FFs in twin-well
  - Strong to SET on C-element
- Errors in the triple-well might be caused by parasitic bipolar effect

Comparison of SERs at 100 MHz



		Min. Dis.	FIT/Mbit
BCDMR	old	0.77 μm	71
	revised	2.13 μm	< 9
		2.8 x	**1/8**

		Min. Dis.	FIT/Mbit
BISER	old	1.54 μm	150
	revised	3.61 μm	44
		2.3 x	**1/3.4**

Outline

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Conclusion

- Propose a layout structure to avoid MCUs on redundant FFs
  - Separating Crit. Comp. without any area overhead
  - In BISER, 3.4x MCU tolerance by 2.3x Min. Dis
  - In BCDMR, 8x MCU tolerance by 2.8x Min. Dis

  at 100 MHz

- BCDMR FF has higher soft error resilience
  - <9 FIT/Mbit (No error) on twin-well
  - Over 100x stronger than non-redundant D-FF