AN AREA EFFICIENT THERMAL ENERGY HARVESTER WITH RECONFIGURABLE CAPACITOR CHARGE PUMP FOR IOT APPLICATIONS

A Thesis

by

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ABSTRACT

Renewable energy sources are promising alternatives to a battery. Due to the varying power profile of renewable energy sources, an energy harvester needs the different power management techniques including boosting the small input voltage. The awareness of the demand, this thesis introduces an integrated energy harvester system targeting Internet of Things (IoT) sensor applications such as a wireless temperature sensor. The proposed design extracts energy from a thermal energy generator (TEG), and provides the regulated output voltage.

To ensure the maximum power extraction, the proposed energy harvester includes multiple circuit level techniques. First, the reconfigurable capacitor charge pump distributes on-chip capacitors to required step-up stages. This approach optimizes the silicon area by utilizing 100% on-chip capacitors regardless of a charge pump conversion gain. Second, the design is capable of 3 dimensional Maximum Power Point Tracking (MPPT), matching a source impedance to input impedance of an energy harvest source. Thus, the proposed energy harvester is able to extract power from a small form factor TEG, having low source impedance (1 Ω). With the increased matching range, up to 500 μW is available at the output for IoT applications.

Experimental results show an end-to-end power efficiency of 64% @ 1 V output voltage, and the input impedance matching range of 1 Ω–5 $k\Omega$. The energy harvester was fabricated in 130 nm Complementary Metal-Oxide-Semiconductor (CMOS) standard technology, and occupies 0.835 mm^2.

DEDICATION

To my parents, advisor Dr. Edgar Sánchez-Sinencio.

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I would like to thank the Texas A&M University to allow me to have fantastic experiences. Special thanks to Dr. Edgar Sánchez-Sinencio. It is my great honor and privilege to learn how to conduct research.

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Contributors

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NOMENCLATURE

TEG	Thermal Energy Generator
CMOS	Complementary Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	n-channel MOSFET
PMOS	p-channel MOSFET
MPPT	Maximum Power Point Tracking
OCV	Open Circuit Voltage
MPP	Maximum Power Point
PMU	Power Management Unit
DCO	Digital Current starved Oscillator
CR	Conversion Ratio
SSL	Slow Switching Limit
FSL	Fast Switching Limit
IoT	Internet Of Things
SC	Switched Capacitor
DUT	Device Under Test
MIM	Metal Insulator Metal
PVT	Process, Voltage and Temperature variation
FSM	Finite State Machine
LDO	Low Drop Out voltage regulator

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1. INTRODUCTION

1.1 Motivation

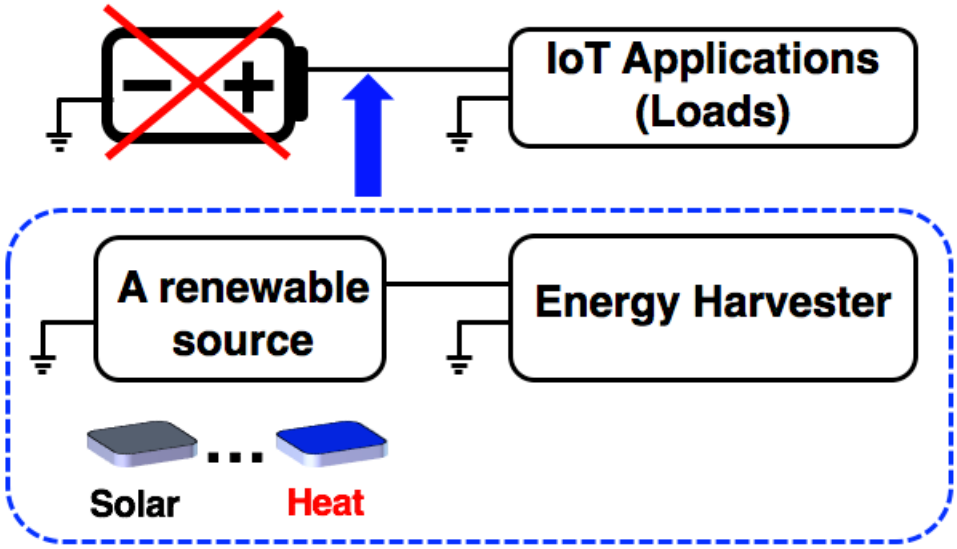


Figure 1.1: The concept of an energy harvester.

Advancement in micro sensors and scaling down of CMOS process enables consumer applications to be connected in a network. Following the concept of IoT, Figure 1.1 describes that renewable energy sources such as Thermal, Solar, Vibration, RF have emerged to power the applications rather than batteries limited size and operating cycles.

Due to the limited amount of power from an energy harvest source, an energy harvester is required to maximize the power extraction and optimize the power consumption. Realizing the design issues, this research present the novel energy harvester with the reconfigurable capacitor charge pump. In the following sections, survey of energy harvest sources, previous power management units, and open problems are discussed.

1.2 Survey of Energy Harvest Sources

	TEG [1]	Solar Cell [2]	RF [3]	Vibration [4]
Power density	1.3 W/cm^3	72.1 mW/cm^3	53.6 uW/cm^3	4.60 uW/cm^3
Sustainability	Best	Good	Better	Fair
Source Impedance	1 Ω	Non-linear	50 Ω	Non-linear
Price	Fair	Fair	Cheap	Fair

Table 1.1: Comparison of energy harvesting sources

From Table 1.1, both a solar cell and TEG have a reasonable power density to power IoT applications without a battery. However, a solar cell has two more disadvantages than a TEG. First, the available power from a solar cell significantly drops when it is partially shaded. Second, the electronic characteristic of a solar cell is non linear; matching the input impedance of a converter to the non linear source impedance is a design challenge. The electrical characteristics of both a solar cell and TEG are described in Figure 1.2.

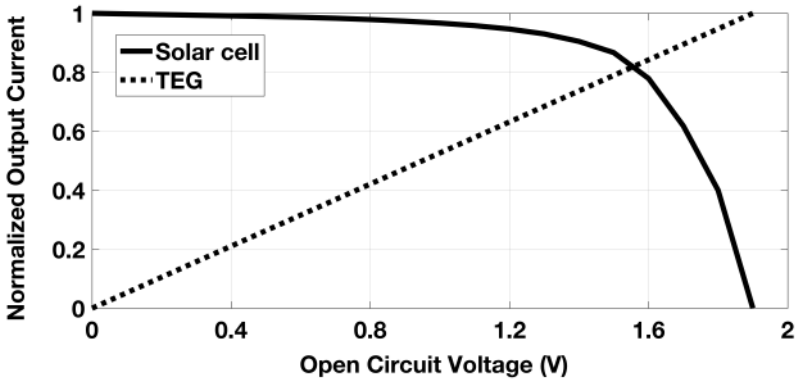


Figure 1.2: Electrical characteristics for a solar cell and TEG

1.3 Survey of Energy Harvesting Power Management Unit

The outstanding results successfully present the power management units (PMU) utilizing the renewable energy sources in micro-watts levels. However, inductor based systems [5, 6] have limitations to be integrated into a small form factor, and cost.

To extract the maximum power from renewable energy sources, an energy harvester is required to match its input impedance to a source impedance. However, tuning the parameters of an energy harvester is a difficult design challenge. The tunability of each parameter is limited. First, the conversion gain needs to be changed due to the varying power profile as a result of temperature gradient of a TEG [1]. Second, the silicon area for on-chip capacitance is suppressed by a small capacitance density. Third, increasing switching frequency leads power losses from driving switches.

Conventionally, several energy harvesting power management units have been proposed to optimize power delivery efficiency. The energy harvester presented in [7], the fixed switching frequency (60 kHz) limits the capability of MPPT for 100 kΩ source impedance. To elaborate the problem, the power management system [8] senses the output current to optimize a switching frequency. However, a current sensing is the power hungry approach which is improper in the low power scenario. Instead of a sensing output current, measuring a peak output voltage by constant on-time is presented [9] tuning the conversion ratio and switching frequency. Even with two dimensional (2D) MPPT, input impedance matching range has not been expanded and the available output power is up to 50 μW. Alternatively, the system [10] senses an open circuit voltage of an energy harvest source to compare the input voltage of the system. At the maximum power point, a half of the open circuit voltage is the same as the input voltage of an energy harvester. However, the fast switching frequency of 10 MHz for a low source impedance degrades the end-to-end power efficiency due to switching losses.

1.4 The Open Problems

To replace a battery for an IoT applications, optimizing power delivery efficiency is the main issue for an energy harvester. As discussed in the previous section, conventional energy harvesters have been trickled down, maximizing an input power of the PMU. Figure 1.3 illustrates the input power varying an energy harvester input impedance to a source impedance. However, improvement of an energy harvest source that generates more power with a small foam factor causes three problems: the tuning range of the input impedance, limited silicon area for a switched capacitor converter, and power consumption by a PMU.

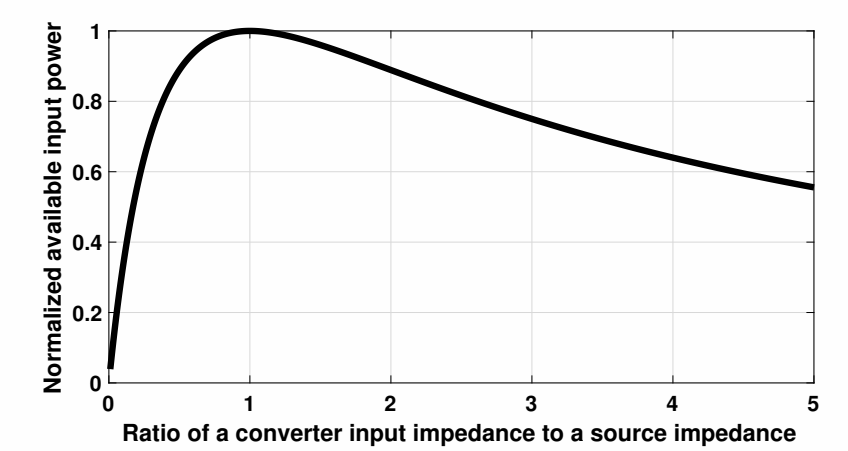


Figure 1.3: The maximum input power point condition

First, the tuning range of the input impedance has to be expanded; as a result of an improved energy harvest source, its source impedance is decreased to 1 Ω. Second, silicon area is limited to handle more power with an switched capacitor converter; half of energy is lost when charges are transferred through capacitors [11]. However, on-chip capacitance given by a technology is a few fF per micrometer square. Third, an energy harvester should optimize the power consumption to improve power delivery efficiency.

2. SWITCHED CAPACITOR CONVERTER FUNDAMENTALS

2.1 Switched Capacitor DC-DC converter

Converter	Capacitive switching regulator	Inductive switching regulator	Linear regulator
Efficiecny	Good	Best	Worst
Size (mm^3/W)	Good	Worst	Best
Cost ($\$/W$)	Good	Worst	Best

Table 2.1: Comparison of DC-DC converters

The inductive converter has been the most popular design for decades. Due to its simple configuration and the best efficiency; the boost converter needs only two switches and one inductor [12]. However, it is hard to be integrated; an on-chip inductance and quality factor of an inductor are critically limited in CMOS technologies.

In an linear regulator, the resistance of a pass transistor is varied by the output load. The ripple-less output voltage is available [13]. However, the noise rejection range is limited up to a few megahertz, and the efficiency is the worst than others. Due to the lack of boosting the input voltage, an linear regulator cannot be used alone in an energy harvester.

In a switched capacitor (SC) converter, charge pump, more switches and capacitors are required than in an inductive converter. Despite the design complexity of an SC converter, it is feasible to integrate it into a chip. Also, SC converters are progressing fast because of CMOS technology scaling and an improved capacitor density. Table 2.1 presents the comparison between different types of regulators.

2.1.1 Basics Concepts

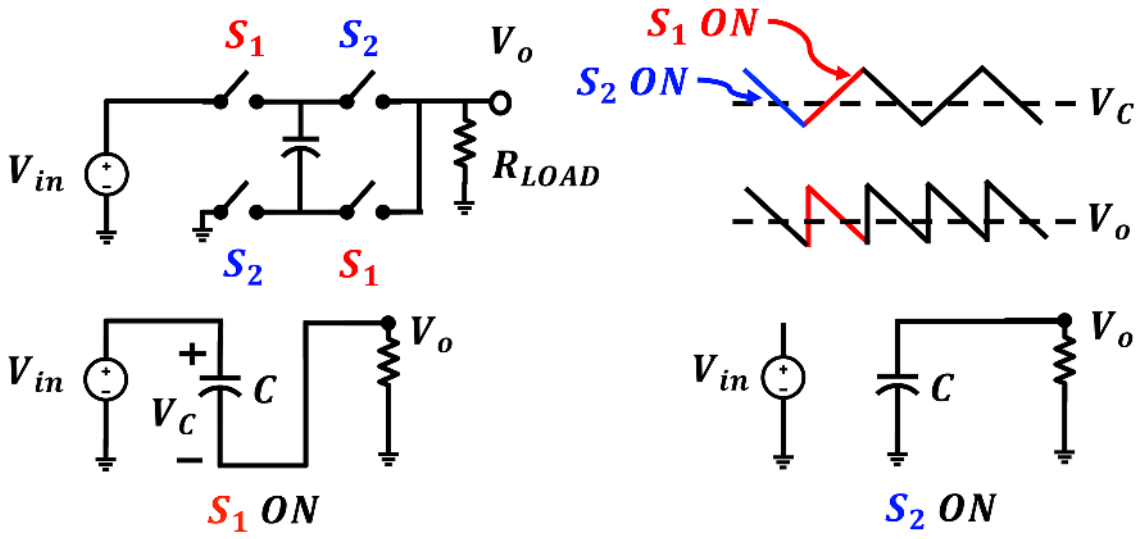


Figure 2.1: Basic operation of a switched capacitor DC-DC converter

Figure 2.1 shows the concept of an SC DC-DC converter, composed with a capacitor and switches. By the each charging (S_1 ON) and discharging phase (S_2 ON), the voltage across the capacitor, V_C, and the output voltage, V_o is also presented. For the analysis of an SC converter, the charge conservation law is described as below:

$$\sum_{i=1}^{n} Q_i = 0 \tag{2.1}$$

$$\begin{aligned} &At\ t = t_2\ (t_2 > t_1) \\ &V_{C_i} = V_{C_i}(t_2) - V_{C_i}(t_1) \end{aligned} \tag{2.2}$$

where the parameters in $Q_i = C_i V_{C_i}$, and V_{C_i} is the voltage across the capacitor, C_i.

2.1.2 Fundamental Analysis

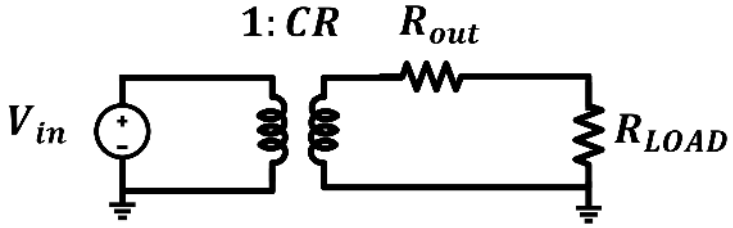


Figure 2.2: Equivalent model of a switched capacitor DC-DC converter

To analyze an SC DC-DC converter, an equivalent model is presented in Figure 2.2 including design parameters: a conversion ratio, CR; and the output impedance, R_{out}. Based on the charge conservation law, the parameters of the SC converter in Figure 2.1 is investigated. First, the ideal CR of 2:1 in the steady-state is derived from:

$$V_C = V_{in} - V_o \qquad , At\ the\ phase\ 1\ (S_1\ on) \tag{2.3}$$

$$V_o = V_C \qquad , At\ the\ phase\ 2\ (S_2\ on) \tag{2.4}$$

Second, the output impedance, R_{out}, is based on two assumptions [14]: In a charging phase, the input of an SC converter is connected to a source. In the other phase, discharging, the input is disconnected. Since the R_{out} represents the output voltage drop by I_{out}, the output impedance has two terms depending on the switching frequency, f_{sw}.

$$R_{SSL} = \sum_{i \in capacitors} \frac{(a_{c,i})^2}{f_{sw} C_i} \tag{2.5}$$

$$R_{FSL} = \sum_{i \in switches} 2R_i (a_{r,i})^2 \tag{2.6}$$

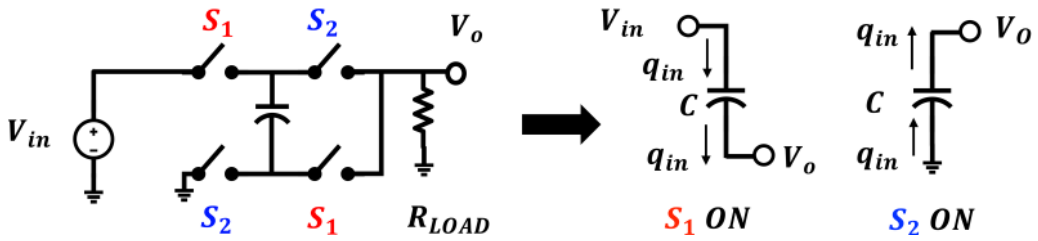


Figure 2.3: Operation of 2:1 switched capacitor converter

The slow switching limit (SSL), the finite resistance of the switches and capacitance are neglected in the slow f_{sw}. The fast switching limit (FSL), the on resistances of the switches is dominated in the fast f_{sw}. From the charge flows in Figure 2.3, charge multiply vectors, $a_{c,i}$ and $a_{r,i}$ are used to express the both parameters of the output impedance.

$$\Delta Q_C = \Delta Q_1 - \Delta Q_2 = C(V_{in} - V_o) - C(V_o) \tag{2.7}$$

$$= C(V_{in}) - 2C(V_o) \tag{2.8}$$

where the parameter ΔQ_i is the charge stored in the capacitor, C, at the phase n. From the each coefficient of ΔQ_C, both R_{SSL} and R_{FSL} are represented as follows:

$$R_{SSL} = \sum_{i \in capacitors} \frac{(a_{c,i})^2}{f_{sw} C_i} = \frac{(-1/2)^2 + (1/2)^2}{C f_{sw}} = \frac{1}{4C f_{sw}} \tag{2.9}$$

$$a_{c,i} = \frac{q_{in}}{q_{out}} = \frac{drawn\ charges\ per\ capacitor}{total\ charges\ flow\ to\ output} \tag{2.10}$$

$$R_{FSL} = \sum_{i \in switches} 2R_i (a_{r,i})^2 = 2R_i[(2(1/2)^2 + 2(-1/2)^2]^2 = 8R_i \tag{2.11}$$

$$a_{r,i} = \frac{q_{in}}{q_{out}} = \frac{flowed\ charges\ to\ swithch_{i_{th}}\ at\ phase\ n}{total\ charges\ flow\ to\ output} \tag{2.12}$$

where the parameter R_i is the on resistance of the i_{th} switch. Thus, R_{out} is described as:

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.13}$$

2.1.3 Power Losses

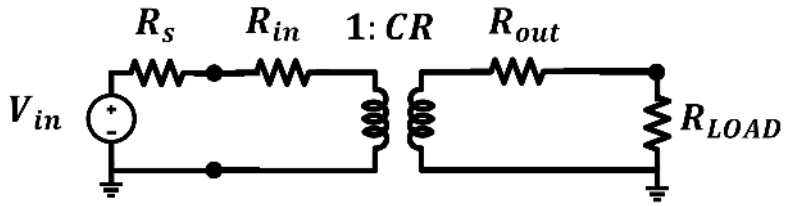


Figure 2.4: Realistic model of a switched capacitor DC-DC converter

To optimize the power losses in an switched capacitor DC-DC converter, the realistic equivalent model is illustrated in Figure 2.4; a source impedance, R_S, and input impedance of a converter, R_{in}, are included. Based on the above model, power losses in an switched capacitor DC-DC converter are summarized in Table 2.2.

Parasitic capacitors / Switching loss	Intrinsic losses
Switching $C_{par,bottom}$, $C_{par,top}$	Charge redistribution
Switching C_{gate} of the switches	On resistance of the switches
	Impedance matching ($R_S,\ R_{in}$)

Table 2.2: Power losses in a switched capacitor DC-DC converter

A switched capacitor DC-DC converter delivers charges from the input to the output by charging and discharging capacitors through metal-oxide-semiconductor field-effect transistor (MOSFET) switches. Thus, the power losses are divided into two categories: switching activities, and intrinsic losses as a result of charge transfer.

First, power losses from parasitic capacitors to stage capacitors and switching gate capacitance of switches are derived respectively as follows:

$$P_{par} = M_{par} f_{sw} C_{par} V_{DD}^2 \tag{2.14}$$

$$P_{sw} = f_{sw} V_{DD}^2 \sum_{i=1}^{n} C_{g,i} \tag{2.15}$$

where the parameters in the parasitic loss, C_{par} is the sum of the bottom and top parasitic capacitance to the power capacitance in an SC converter, M_{par} is the coefficient proportional to the number of power capacitors and voltage swing on the C_{par}, and f_{sw} is the switching frequency driving switches. In switching loss driving switches, C_g is the gate capacitance of each switch, and n is total number of switches.

Second, the intrinsic losses in an SC converter are described respectively as follows:

$$P_{redistribution} = I_{load}^2 R_{SSL} = I_{load}^2 \sum_{i \in capacitors} \frac{(a_{c,i})^2}{f_{sw} C_i} \tag{2.16}$$

$$P_{sw,on} = I_{load}^2 R_{FSL} = I_{load}^2 \sum_{i \in switches} 2 R_i (a_{r,i})^2 \tag{2.17}$$

$$P_{loss,input} = \frac{V_{in}^2}{R_S} - \frac{V_{in}^2 R_{in}}{(R_S + R_{in})^2} \tag{2.18}$$

where the parameters in equation 2.16, I_{load} is the current flows to the output. It is the power loss when two capacitors with different voltages are connected together ,and proved in Appendix B. In equation 2.17 for the power loss from switches, R_i is on resistance of switches. Equation 2.18 is the impedance mismatch between a source and the SC converter. According to equation 2.18, $P_{loss,input}$ is minimized when R_S and R_{in} are matched. Thus, the maximum power point (MPP) is defined as:

$$R_S = R_{in} \tag{2.19}$$

2.2 SC DC-DC converter Topologies

2.2.1 Dickson Charge Pump

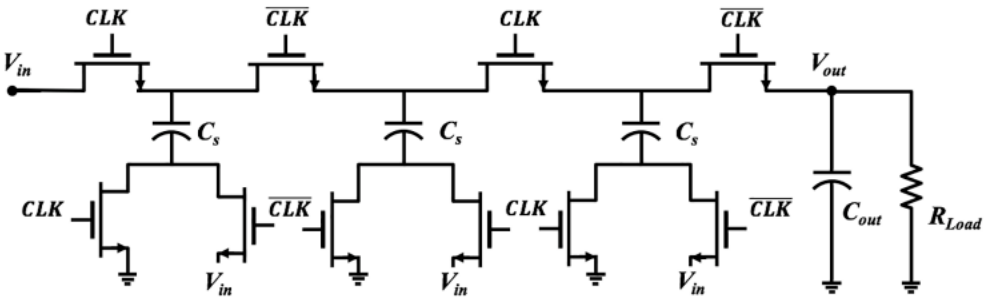


Figure 2.5: Three stages Dickson charge pump

Figure 2.5 shows a Dickson SC converter, charge pump. Each stage boosts the voltage by the input voltage, V_{in}. Assuming ideal charge transfer between switches, the actual voltage gain is as follows:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{N+1}{1+\frac{N}{C_s f_{sw} R_{Load}}} \tag{2.20}$$

where the components in N is the number of charge pump stages, I_{out} is the output current, f_{sw} is the switching frequency, and C_s is each stage capacitance. The input impedance is defined by V_{in}/I_{in}. From equation 2.20, it is described as:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{I_{out}(N+1)} = \frac{N}{(N+1)C_s f_{sw} \Delta A} \tag{2.21}$$

$$\Delta A = (N+1) - \frac{N+1}{1+\frac{N}{C_s f_{sw} R_{Load}}} \tag{2.22}$$

where ΔA is the difference between ideal voltage gain, $N+1$, and actual voltage gain.

2.2.2 Voltage Doubler Topology

As one of the popular topologies, a voltage double SC converter is presented in Figure 2.6. Similar to the Dickson charge pump, each stage boosts the input voltage, V_{in}, by the amplitude of clock: *CLK* and $\overline{CLK}$.

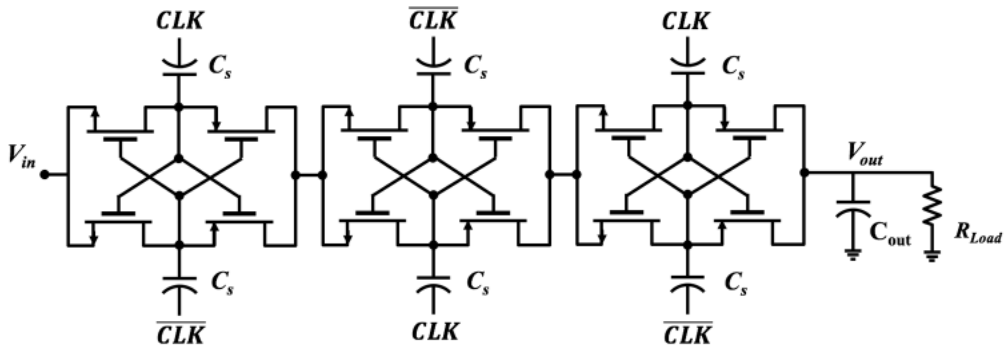


Figure 2.6: Three stages Voltage doubler charge pump

Assuming ideal charge transfer between switches, voltage gain and input impedance of the voltage doubler charge pump are described as:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{N+1}{1+\frac{N}{2C_s f_{sw} R_{Load}}} \tag{2.23}$$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{I_{out}(N+1)} = \frac{1}{\frac{(N+1)^2}{R_{Load}+\frac{1}{2C_s f_{sw}}}} \tag{2.24}$$

where the components in *N*, I_{out}, f_{sw} and C_s are the number of stages, output current, switching frequency, and stage capacitance respectively. Note that the voltage doubler charge pump has cross coupled configurations with n-channel MOSFET (NMOS) and p-channel MOSFET (PMOS). Also, the amplitude of both *CLK* and $\overline{CLK}$ are same as the input voltage of the charge pump, V_{in}.

2.2.3 Comparison of SC converters for the Energy Harvester

	Dickson charge pump	Voltage doubler topology
# of capacitors	N	$2N$
# of switches	$3N + 1$	$4N$
Voltage gain	Same	Same
Implementation difficulty	Easy	Hard

Table 2.3: Comparison of SC converters

Table 2.3 demonstrates the comparison between two charge pump topologies described in the previous sections. N is the number of stages for each SC converter topology. For the comparison, the same condition of the f_{sw}, R_{load} and total capacitance, C, are considered: $C_{s,dickson} = C/3$, and $C_{s,doubler} = C/6$. In the power scenario of energy harvesting, a Dickson charge pump has advantages over a voltage doubler topology.

First, a Dickson charge pump has fewer number of switches than in a voltage doubler topology ($N > 1$). Due to the on resistance of the switches, the conduction loss of a voltage doubler is worse as shown in equation 2.17. Second, a Dickson charge pump has single capacitor per stage; the parasitic capacitors, leading to power loss described in equation 2.14, are fewer than the other. Third, a voltage doubler topology is not suitable to deliver a few hundreds of micro-watts power. The topology uses additional buffer stages due to the directly driving power capacitors, $C_{s,doubler}$, by *CLK* and $\overline{CLK}$. Thus, the Dickson charge pump is adopted in the proposed energy harvester.

3. DESIGN OF THERMAL ENERGY HARVESTER

3.1 The Proposed Energy harvester Block Diagram

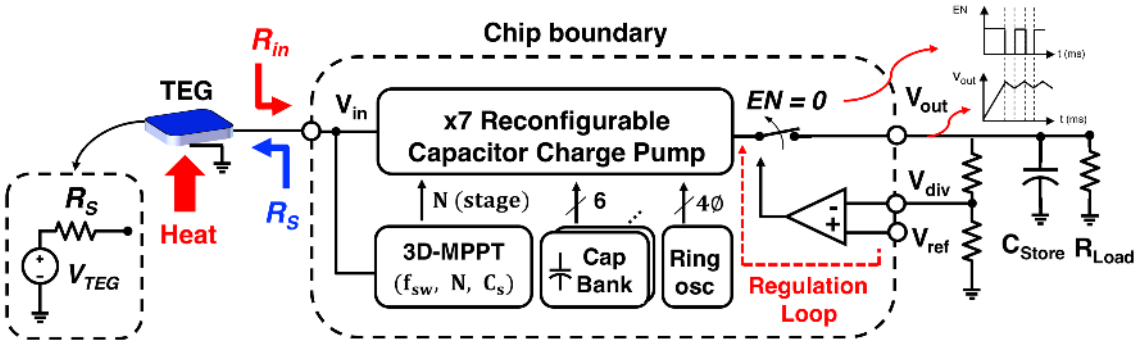


Figure 3.1: The proposed reconfigurable thermal energy harvester

This chapter presents the proposed thermal energy harvester. In Figure 3.1, power flows from TEG to output storage capacitor, C_{store}, through the charge pump. And the regulation loop maintains output voltage of the power management unit by the reference voltage. The proposed design includes four building blocks; a reconfigurable capacitor charge pump, digital controlled current starved ring oscillator, three dimensional (3D) MPPT, and a digital controller. The reconfigurable capacitor charge pump is implemented with 6 stages Dickson topology. Along with the previous section, this topology has higher power efficiency than other topologies in low power scenario [14]. The design is capable of boosting voltage from TEG (0.27 V - 1 V) to the desired voltage (1 V). And it tunes input impedance of the PMU automatically by the digital controller. As tuning the input impedance, the energy harvester can extract maximum power from a small form factor TEG having a low source impedance ($\sim 1\Omega$).

3.2 Design Procedures

To optimize the power efficiency of an energy harvester, this research proposes a novel charge pump elaborating the open problems: tuning the input impedance of the converter as low as 1 Ω due to a minimized TEG, optimizing the silicon area, and power consumption to deliver a few hundreds of micro-watts power. This section provides the design considerations for the proposed energy harvester.

3.2.1 3D Maximum Power Point Tracking

The key concept of maximum power point tracking (MPPT) is matching the input impedance of the PMU, R_{in}, to the energy harvest source impedance, R_S. From equation 2.17 for the input power losses, the MPP condition, $R_S = R_{in}$, maximizes the input power to the PMU by tuning three parameters: switching frequency, f_{sw}, a stage capacitance, C_S, and number of charge pump stages, N. Figure 3.2 illustrates the MPPT by tuning the input impedance of the PMU.

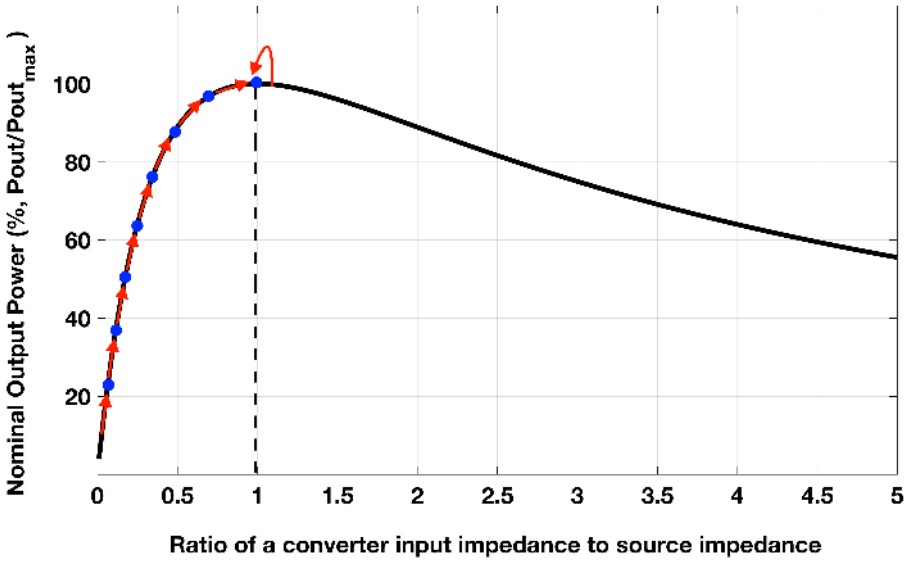


Figure 3.2: The maximum input power at the maximum power point ($R_S = R_{in}$)

To extract as much as energy from an renewable source, conventional energy harvesters [15, 9] changed the input impedance to reach the MPP; however, a small source impedance ($<$10 Ω) is not covered by those tuning ranges of the input impedance. Both input impedance equation 2.21 and 2.24 for a Dickson charge pump and voltage doubler, respectively, show the limitation of the tuning range. First, fast f_{sw} is required for a small source impedance, leading to switching power losses described in equation 2.15 and 2.14. Second, large stage capacitance reduces the input impedance, but silicon area is sacrificed.

To increase the tuning range of an input impedance alleviating the above problems, the proposed 3D MPPT dynamically tunes all of the three parameters (N, C_S, and f_{sw}) with a power efficient method. First, the input voltage of a charge pump decides N for a desired output voltage. Second, distributing all on-chip capacitors to the corresponding stage by N. Thus, effective stage capacitance, $C_{S,eff}$ is larger than the case of fixed stage capacitance. Third, f_{sw} is changed to reach an MPP ($R_{in} = R_S$). Figure 3.3 illustrates the procedures of tuning the parameters.

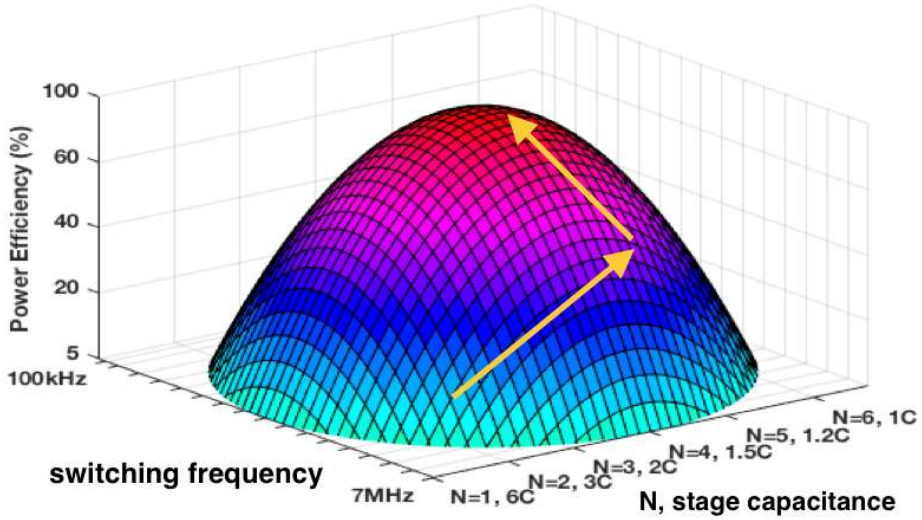


Figure 3.3: The concept of 3D MPPT

3.2.2 Reconfigurable Capacitor Charge Pump

From equation 2.21 for an input impedance of a Dickson charge pump, increasing a switching frequency, f_{sw} or stage capacitance, C_S, reduces the input impedance. However, increasing f_{sw} leads switching power losses, and on-chip capacitance is limited due to a technology. Thus, the proposed reconfigurable charge pump increases the effective stage capacitance instead of increasing f_{sw}. By distributing all on-chip capacitors to each activated step-up stages, the silicon area is also optimized. To implement the proposed solution, Table 3.1 summarizes the design parameters.

Topology	N	Total on-chip capacitance	I_{out}
Dickson charge pump	6	1.5 nF	10 μA–1 mA

Table 3.1: Design parameters of the reconfigurable capacitor charge pump

As previously mentioned, a Dickson charge pump is suitable in the power profile of energy harvesting including the design simplicity. For the number of the charge pump stages, both the technology and an energy harvest source are considered. First, the nominal supply voltage of 130 nm technology is 1.2 V. To reduce the switching stress to CMOS switches, the target output voltage is set to 1 V. Second, the expected input voltage of the charge pump is given by the small TEG [1]: the dimensions of 6 mm x 1.65 mm, and source impedance of 1 Ω. Assuming the energy harvester is operating in room temperature of 27 C°, the expected voltage from the TEG is approximately 0.2 V ($\Delta T = 5\ C^{\circ}$). Thus, 6 stages of charge pump is capable of boosting the input voltage to the target voltage, 1 V. From equation 2.20 for the voltage gain of a Dickson charge pump, the realistic gain is smaller than the ideal gain of $N + 1$.

The total on-chip capacitance, $C_{total} = 1.5\ nF$, is chosen by considering die size of 1.5 mm x 1.5 mm, and the capacitance density (<5 fF/μm^2) . Dual-layers metal insulator metal (MIM) capacitors have the minimum bottom plate parasitic capacitance minimizing power losses as described in equation 2.14. The input impedance of the proposed charge pump and the reconfigurable capacitor bank are provided. First, replacing the capacitance per stage, C_s, to C_{total}/N, the input impedance of the proposed design is described as:

$$R_{in,proposed} = \frac{V_{in}}{I_{in}} = \frac{N}{\alpha(C_{total}/N)f_{sw}N^2 + (N+1)(C_{total}/N)f_{sw}\Delta A'} \tag{3.1}$$

$$\Delta A' = (N+1) - \frac{N+1}{1 + \frac{N}{(C_{total}/N)f_{sw}R_{Load}}} \tag{3.2}$$

where the parameters in α is the ratio of bottom parasitic capacitance to the effective stage capacitance, and $\Delta A'$ is the differences between the ideal voltage gain and realistic gain. The input impedance of charge pumps are compared in Figure 3.4. The MATLAB code is provided in Appendix A.1. In the same condition, the $R_{in,proposed}$ is smaller than a conventional charge pump's input impedance due to the increased effective stage capacitance.

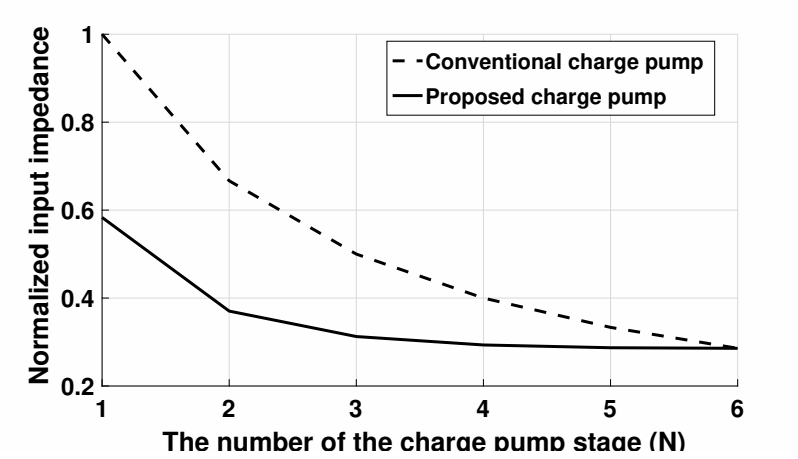


Figure 3.4: Comparison of charge pump input impedances (f_{sw}=1MHz, $I_{out} = 250uA$)

Second, the design of reconfigurable capacitor bank for stage capacitance should have the least number of unit capacitors; switches between unit capacitors reduce the power delivery efficiency as described in equation 2.17 for *on* resistance of switches. Mathematically, the least common denominator of the stages, 1–6, is 60 $(= 1 \times 2^2 \times 3 \times 5)$.

To minimize the number of unit capacitors, 60, 12 capacitors of four different capacitance are used: $C_{unit} = 250\ pF$, $0.5C_{unit}$, $0.2C_{unit}$, and $0.1C_{unit}$. When 1 step-up stage is activated, $C_{S,eff}$ is 1.5 nF. It is 6 times larger than the conventional charge pump with fixed stage capacitance of 250 pF. Table 3.2 presents the reconfiguration of 12 capacitors regarding N where the parameters in S_i is the i_{th} step-up stage.

Unit \ N	1	2	3	4	5	6
C_{unit}	S_1	S_1	S_1	S_1	S_1	S_1
C_{unit}	S_1	S_1	S_1	S_2	S_2	S_2
C_{unit}	S_1	S_1	S_2	S_3	S_3	S_3
C_{unit}	S_1	S_2	S_2	S_4	S_4	S_4
$0.5C_{unit}$	S_1	S_2	S_3	S_1	S_5	S_5
$0.5C_{unit}$	S_1	S_2	S_3	S_2	S_5	S_5
$0.2C_{unit}$	S_1	S_2	S_3	S_3	S_1	S_6
$0.2C_{unit}$	S_1	S_2	S_3	S_3	S_2	S_6
$0.2C_{unit}$	S_1	S_2	S_3	S_4	S_3	S_6
$0.2C_{unit}$	S_1	S_2	S_3	S_4	S_4	S_6
$0.1C_{unit}$	S_1	S_2	S_3	S_4	S_5	S_6
$0.1C_{unit}$	S_1	S_2	S_3	S_3	S_5	S_6
$\boldsymbol{C_{S,eff}}$	1.5 nF	0.75 nF	0.5 nF	375 pF	300 pF	250 pF

Table 3.2: Distribution of the unit capacitors by number of stages

3.2.3 Digital Controlled Oscillator

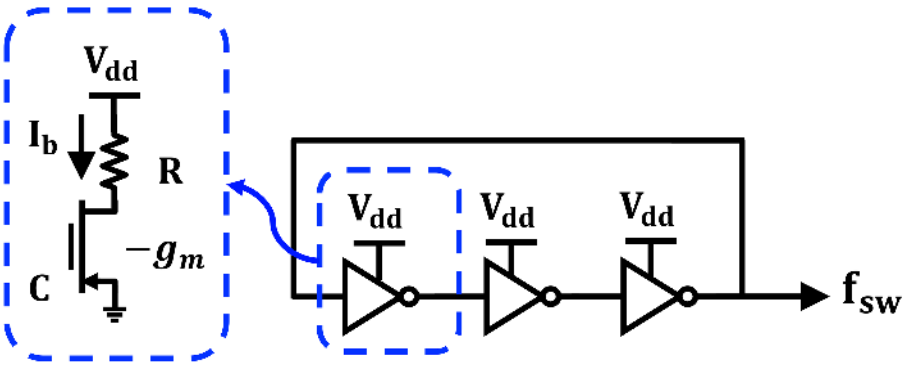


Figure 3.5: Equivalent model of a ring oscillator

The switching frequency, f_{sw}, for the charge pump, the PMU requires an oscillator with two design considerations: the wide tuning range of f_{sw}, and low power consumption. Thus, inverter based ring oscillator is chosen. As illustrated in Figure 3.5, the topology is simple and easy to tune by modulating capacitance, C. To ensure oscillation, Barkhausen criterion is described as:

$$|A_1(jw) \cdot A_2(jw) \cdots A_{2n+1}(jw)| = \left| \frac{-gm_i R}{1 + jwRC} \cdots \right| = 1 \tag{3.3}$$

where the parameters in n is the number of inverters, R is the output impedance of each inverter, and C is the input capacitance of each inverter. By the Barkhausen criterion, the minimum gain of an oscillator should be 1. For the reliability of oscillation, the gain of 2 or 3 is preferred. From the analysis of inverters ring oscillator [16], f_{sw} is as follows:

$$f_{sw} = \frac{I_b}{2n(V_{out} - V_{DS,M2} - V_{DS,M4})C} \tag{3.4}$$

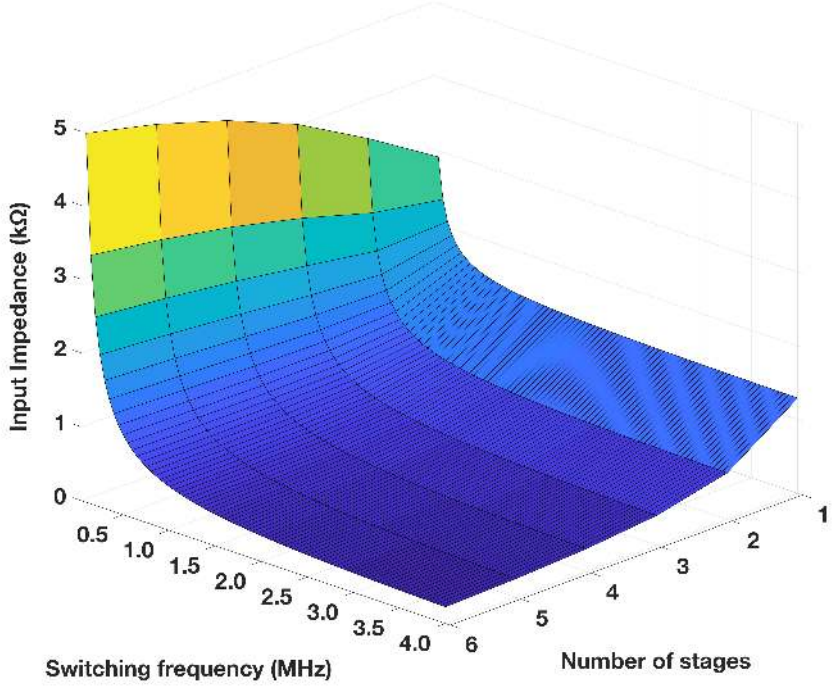
where I_b is the bias current of an inverter. Adding capacitance between an inverter, the oscillator is capable of tuning f_{sw}. For the low power consumption, minimizing I_b reduces the static power. However, too small bias current ($<$10 nA) has a possibility to distort the linearity of the frequency tuning; decreasing I_b also scales down the required C to a few fF. Due to a process, voltage and temperature variation (PVT), the small capacitance difference between each step does not guarantee the linear tuning of f_{sw}.

Based on the design considerations of an oscillator, the iterative simulation is necessary to find the optimal point between power consumption and tunability of f_{sw}. In section 3.4, details of the circuit implementation and dimensions are discussed.

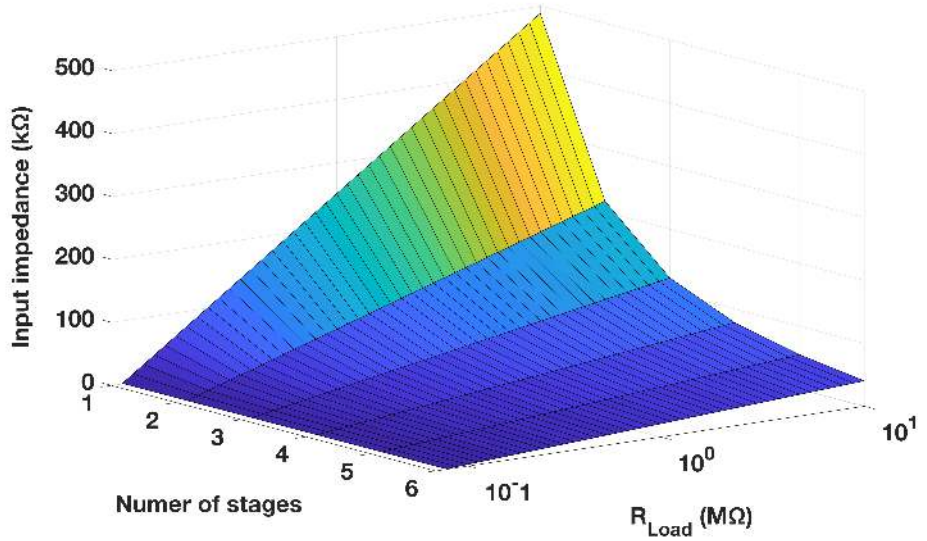
3.3 Design Trade-offs

As previously mentioned in open problems, extracting energy from a minimized energy harvest source leads two problems; equation 3.1, for the input impedance proposed charge pump, shows the demand of fast f_{sw} and more stage capacitance due to the small source impedance (<10 Ω). The proposed energy harvester mitigates the issues by reconfiguring stage capacitors. Figure 3.4 presents the comparison of the input impedance under the same condition of f_{sw} and I_{load}. Thus, this section provides the further details of design trade-offs for the implementation.

First, the input impedance of proposed PMU has correlation to f_{sw}. Assuming both a conventional charge pump and the proposed charge pump have the same amount on-chip capacitance, C_{total}, the proposed one is capable of reducing f_{sw} by 6 times for the same R_S when single step-up stage is activated; Due to the reconfiguration of stage capacitors, the proposed one has the effective stage capacitance, $C_{S,eff} = C_{total}$ rather than the fixed one, $C_{total}/6$, of the conventional charge pump. For the small source impedance, the proposed approach reduces the necessity of high f_{sw} as a result of the increased effective stage capacitance.



(a) Input impedance tuning capability by f_{sw} and N ($I_{load} = 200uA$)



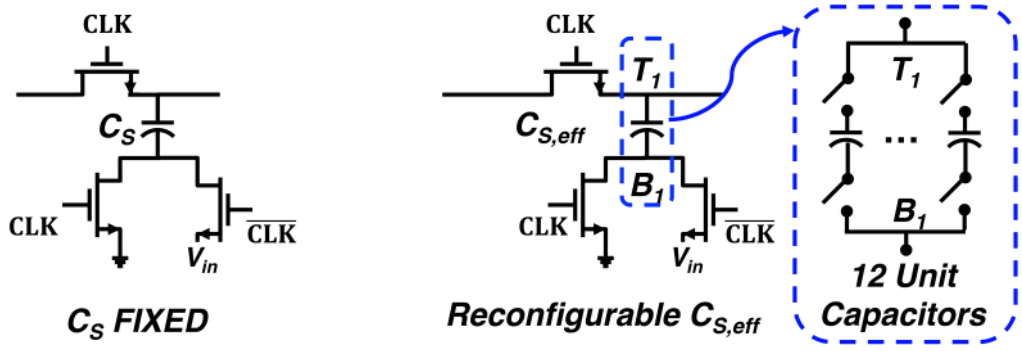
(b) Input impedance tuning capability by load resistance and N ($f_{sw} = 1MHz$)

Figure 3.6: Input impedance tuning capability

Figure 3.6a presents the input impedance of the proposed reconfigurable capacitor charge pump, $R_{in,proposed}$ with varying a switching frequency, f_{sw}, and the number of charge pump stages, N. The effective capacitance per stage, $C_{S,eff}$, is reconfigured by N. By equation 3.1 for the input impedance, $R_{in,proposed}$ is decreased as f_{sw} is increased.

Second, unfortunately, $R_{in,proposed}$ is changed by the output load resistance as shown in equation 3.1 for the input impedance of the proposed charge pump. Due to the single output path, increasing load resistance, which means reducing I_{load}, raises the effective input impedance. Thus, the capability of MPPT is suffered by the load resistance, R_{Load}. Figure 3.6b illustrates the relation R_{Load}, and N to the $R_{in,proposed}$. The MATLAB code for both Figure 3.6a and 3.6b are attached in Appendix A.2.

Third, additional switches for the reconfigurable capacitor bank lead to the power loss described in equation 2.17 for *on* resistance of the switches. In the proposed charge pump, stage capacitance is reconfigured to $C_{S,eff} = C_{total}/N$. To implement the reconfigurable capacitor bank in Figure 3.7b, more switches are necessary than the fixed stage capacitance charge pump in Figure 3.7a. Thus, the trade-off between stage capacitance reconfiguration and the power loss should be mitigated by the proper size of the switches.



(a) (b)

Figure 3.7: Comparison of stage capacitance in charge pumps (N=1)

3.4 Implementation of Circuits

3.4.1 Reconfigurable Capacitor Charge Pump

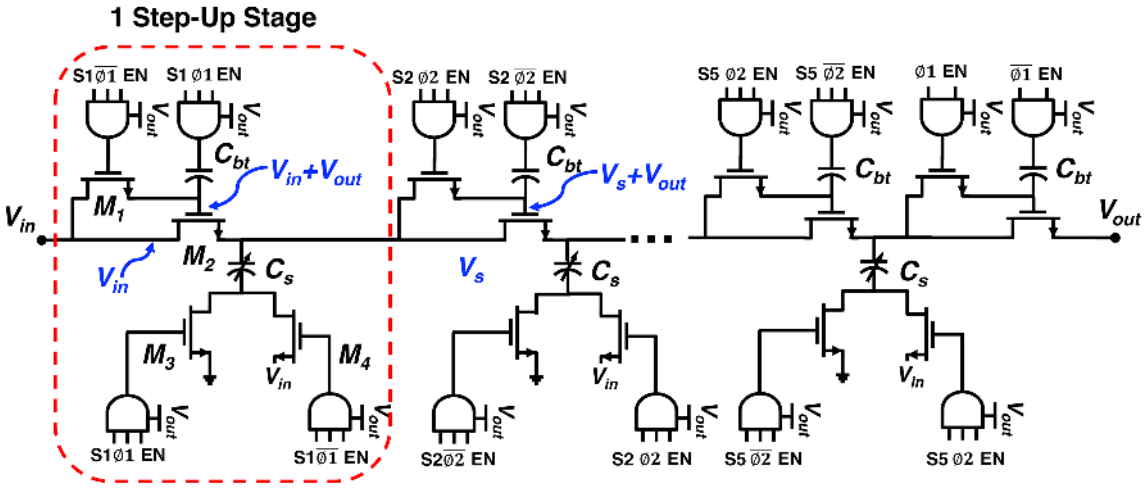


Figure 3.8: Full schematic of the proposed reconfigurable capacitor charge pump

Figure 3.8 shows circuitry of the proposed reconfigurable capacitor charge pump. Total six cascaded step-up stages are capable of boosting input voltage, V_{in}, up to seven times. However, actual voltage gain of the converter is limited by capacitance per stage, switching frequency, and load resistance as described in equation 2.20. In addition, the threshold voltage of switches limits the minimum input voltage of the charge pump around 270 mV. The dimensions of a step-up stage is presented in Table 3.3.

M1	M2	M3, M4	C_{bt}
30 μm / 120 nm	100 μm / 120 nm	60 μm / 120 nm	10 pF

Table 3.3: Implemented 1 step-up stage for the reconfigurable capacitor charge pump

To enhance the power delivery efficiency, the bootstrap technique [17, 18] is adopted. Compared to a conventional Dickson charge pump, the implemented one has an additional switch and capacitor, C_{bt}, in single step-up stage. Pre-charging an input voltage of each stage strengthens a gate-source voltage to output voltage, V_{out}. As an example, the gate-source voltage of switch M2 In the first step-up stage is described as:

$$V_{GS,M2} = V_{G,M2} - V_{S,M2} = (V_{in} + V_{out}) - V_{in} = V_{out} \tag{3.5}$$

By the bootstrap technique, gate-source voltage of the switches in the charge pump is V_{out} regardless of the stages.

3.4.2 Reconfigurable Capacitor Bank

Equation 3.1 for $R_{in,proposed}$ presents the effect of distributing all of the on-chip capacitors by number of charge pump stages; under the same power budget, f_{sw} and I_{out}, the proposed charge pump is capable of having the low input impedance.

For stage capacitance modulation, the previous energy harvester [19] simply changes each stage capacitance by parallely connected capacitors like Figure 3.9. For example, the capacitance between node A and B is tuned as $C_{AB} = C_2 + C_3$; However, C_1 just occupies the silicon area.

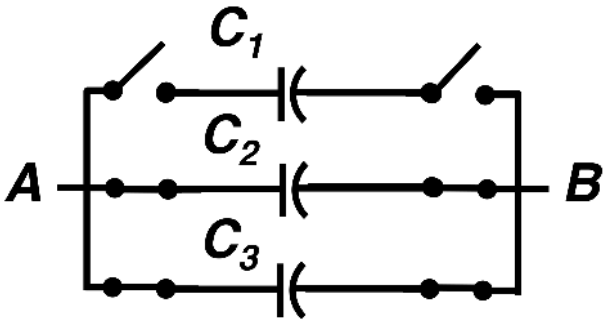


Figure 3.9: Conventional capacitance modulation

In the proposed reconfigurable capacitor charge pump, all of the on-chip capacitors are distributed to corresponding stages for the equal effective stage capacitance; $C_{S,eff} = C_{tot}/N$. The 12 capacitors of four different capacitance are used: $C_{unit} = 250\ pF$, $0.5C_{unit}$, $0.2C_{unit}$, and $0.1C_{unit}$. When 1 step-up stage is activated, $C_{S,eff}$ of 1.5 nF is connected to the first step-up stage. It is 6 times larger than the conventional charge pump with fixed stage capacitance of 250 pF.

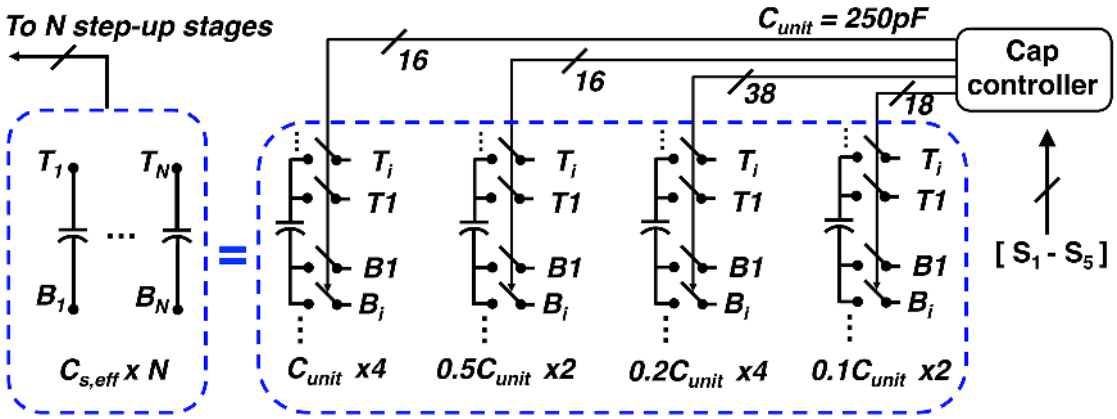


Figure 3.10: Implemented capacitor bank for the charge pump

This reconfigurable capacitor bank was implemented with transmission gates. Figure 3.10 presents the control scheme. From the charge pump stage information, S_1–S_5, *Cap controller* distributes unit capacitors to a corresponding stage parallely. Thus, each activated step-up stage has the effective stage capacitance, $C_{S,eff}$. The on-chip capacitors are configured with dual-layers MIM capacitors. Compared to other types of capacitors, MIM capacitor has less density, but minimal bottom plate parasitics. Equation 2.14 shows the power losses from parasitic capacitance.

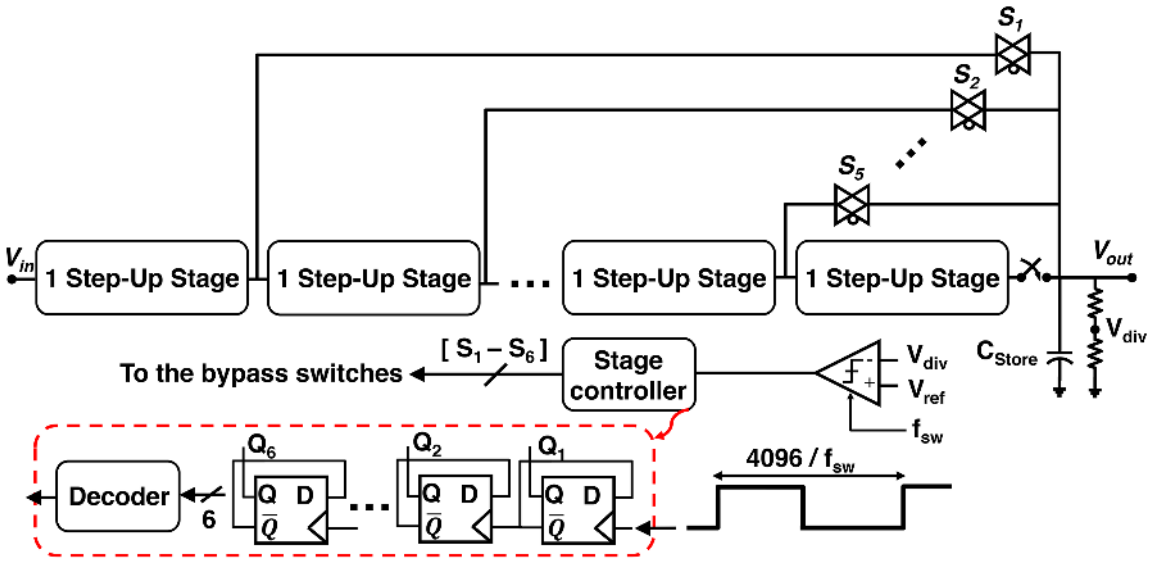


Figure 3.11: Implemented charge pump stage control scheme

3.4.3 Charge Pump Stage Control

Figure 3.11 shows the implemented charge pump stage control scheme. To eliminate static power losses, a latched comparator is adopted. Comparing the output voltage to the reference voltage, V_{ref}, the comparator triggers the 6-bits ripple counter by $4096/f_{sw}$. In the period, V_{out} is slowly changed to the conversion gain. The decoder selects one of the bypass switches, and other step-up stages are off. Table 3.4 shows the digital code from the decoder. The clock signal does not drive switches in the *off* step-up stages. The comparator makes a decision with V_{div} and V_{ref} due to the limited input voltage range.

	$N = 1$	$N = 2$	$N = 3$	$N = 4$	$N = 5$	$N = 6$
$S_1S_2S_3S_4S_5$	10000	01000	00100	00010	00001	00000

Table 3.4: Step-up stage control code

3.4.4 Digital Controlled Current Starved Ring Oscillator

Figure 3.12 presents the implemented frequency modulation scheme with a digital controlled current starved ring oscillator (DCO). The transistor sizes for the oscillator are given in Table 3.5. The long channel transistors (M1, M2) limits the current flowing to the ring oscillator reducing static power losses. 16-bits thermometer code incrementally changes the effective capacitance between inverters. By the digital code, the range of the DCO frequency is from 125kHz to 4.25MHz.

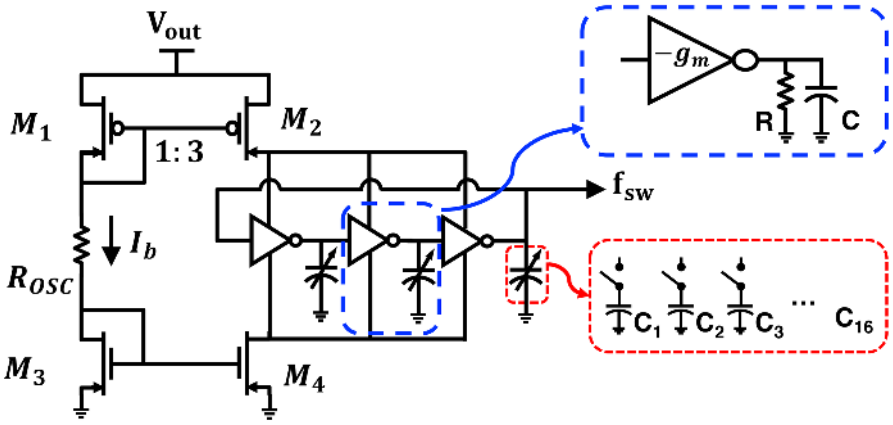


Figure 3.12: Implemented DCO with capacitive frequency tuning

M1	M2	M3	M4	R_{OSC}	Inverter (P)
W=0.3 μm L=60 μm	W=1 μm L=60 μm	W=0.6 μm L=60 μm	W=1.8 μm L=60 μm	500 kΩ	$W_p = 400\ nm$ $L_p = 120\ nm$
C_1–C_6	C_7–C_{10}	C_{11}–C_{12}	C_{13}–C_{14}	C_{15}–C_{16}	Inverter (N)
4.18 fF	9.21 fF	20.1 fF	40.3 fF	300 fF	$W_n = 300\ nm$ $L_n = 120\ nm$

Table 3.5: Dimensions of the Digital Controlled Oscillator

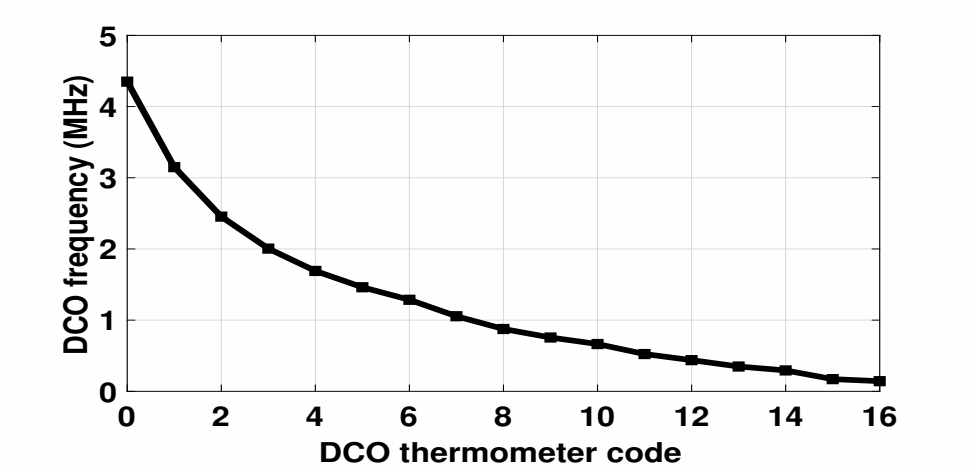


Figure 3.13: DCO frequency versus thermometer code

Figure 3.13 presents f_{sw} of the DCO by 16-bits thermometer code. Increment of the code decreases the f_{sw} as a result of the increased capacitance between inverter stages.

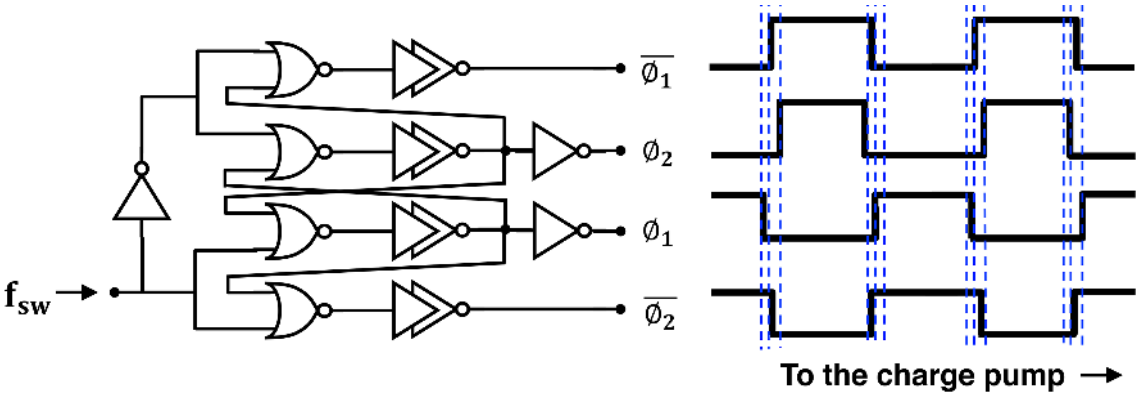


Figure 3.14: The non overlapped 4-phase clock generator

Figure 3.14 shows a non overlapped 4-phase clock generator, optimizing power consumption in the charge pump; one of the step-up stage is charging and the followed step-up stage is discharging. Thus, short paths between phases should be minimized.

3.4.5 Maximum Power Point acquisition

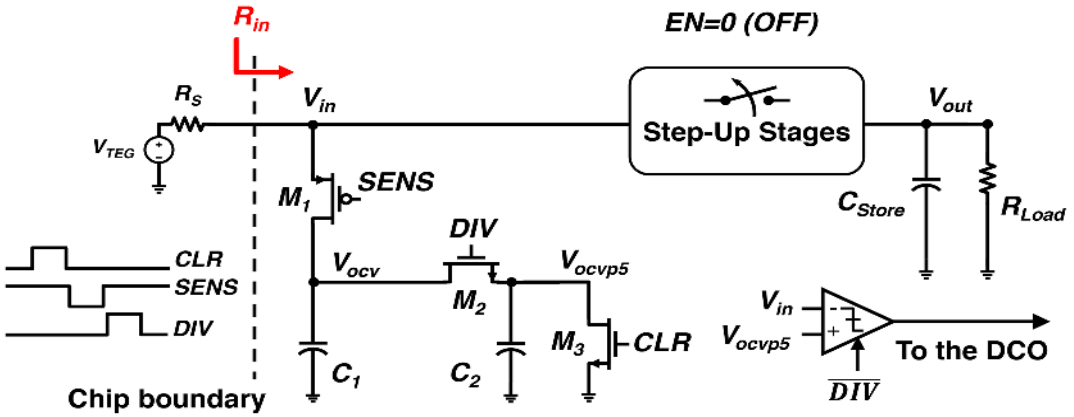


Figure 3.15: Implemented maximum power point acquisition circuitry

Figure 3.15 shows the implemented maximum power point acquisition circuitry. To sense the open circuit voltage (OCV) of an energy harvesting source, the main converter and a TEG are briefly disconnected while storing OCV to the capacitor C_1 by EN. After OCV is sampled to C_1, the V_{OCV} is divided by the capacitive network with DIV. For a short sampling and division period, both capacitance of C_1 and C_2 are 500 fF. Once the divided OCV, V_{ocvp5}, is acquired, the charge pump is enabled ($EN = 1$). Then, the latched comparator makes a decision to adjust the switching frequency:

$$V_{in} > V_{ocvp5} = R_{in} > R_S,\ Reduction\ of\ DCO\ code \tag{3.6}$$

$$V_{in} < V_{ocvp5} = R_{in} < R_S,\ Increment\ of\ DCO\ code \tag{3.7}$$

Reduction of DCO code increases f_{sw} and vice-versa. Due to the short acquisition period of 0.2 μs triggered by a digital controller, the disconnected period is negligible. The detail of triggering the acquisition circuitry will be provided in the following section.

3.4.6 Digital Controller

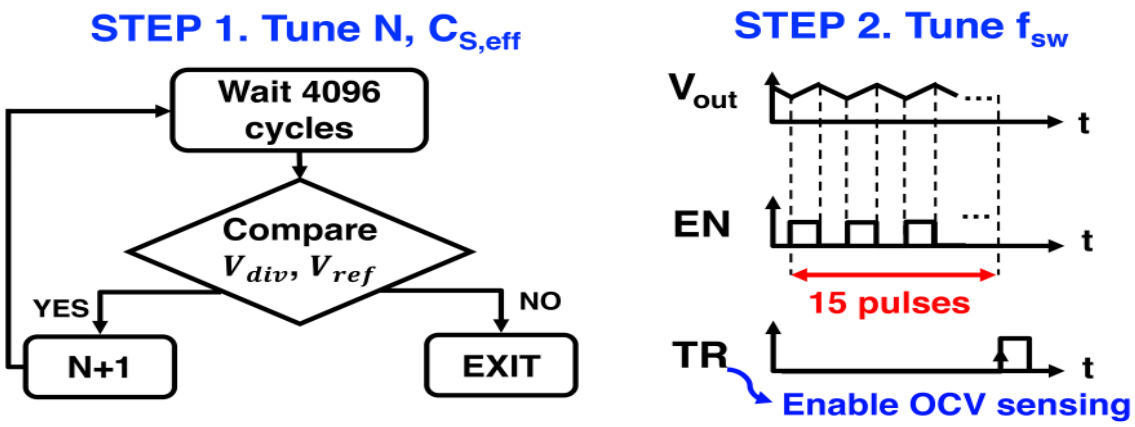


Figure 3.16: Block diagram of the digital controller

Figure 3.16 presents block diagram of the implemented digital controller managing the output voltage regulation and 3D MPPT. The controller is realized with finite state machine (FSM). Once the output buffer, C_{store}, reaches to 500mV, the proposed PMU starts with the maximum switching frequency, 4.25 MHz.

In the first step, both number of stages and the effective stage capacitance of the charge pump is tuned simultaneously. The output voltage is divided by a external resistive network, and compared to the reference voltage, V_{ref}, every 4096 cycles of f_{sw}. The resistive network has 10 times larger resistance than the maximum load resistance: $R_1 = R_2 = 5\ M\Omega$. The first step is terminated when the PMU has the minimum conversion ratio to exceed V_{ref}.

In the second step, V_{out} is regulated by the charge pump enable signal, EN. Every 15 pulses of EN, the OCV sensing circuitry is triggered by TR. The lower output load current, the less recurrence of the MPPT following the brief disconnection from a TEG. The PMU is in the second phase to prepare change of output load demand.

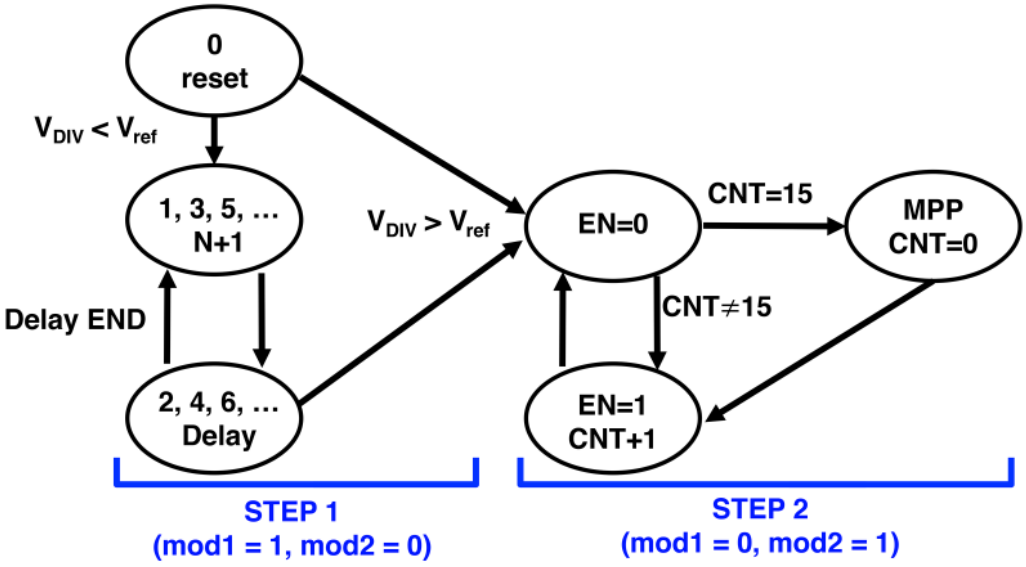


Figure 3.17: State diagram of the digital controller

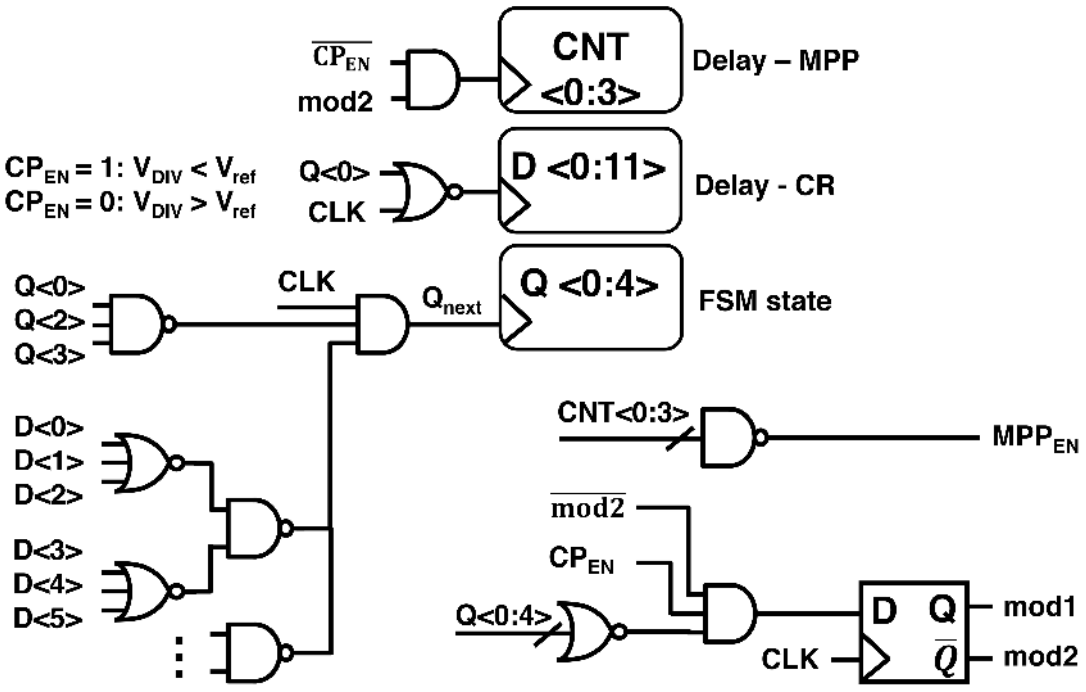


Figure 3.18: The implemented digital controller

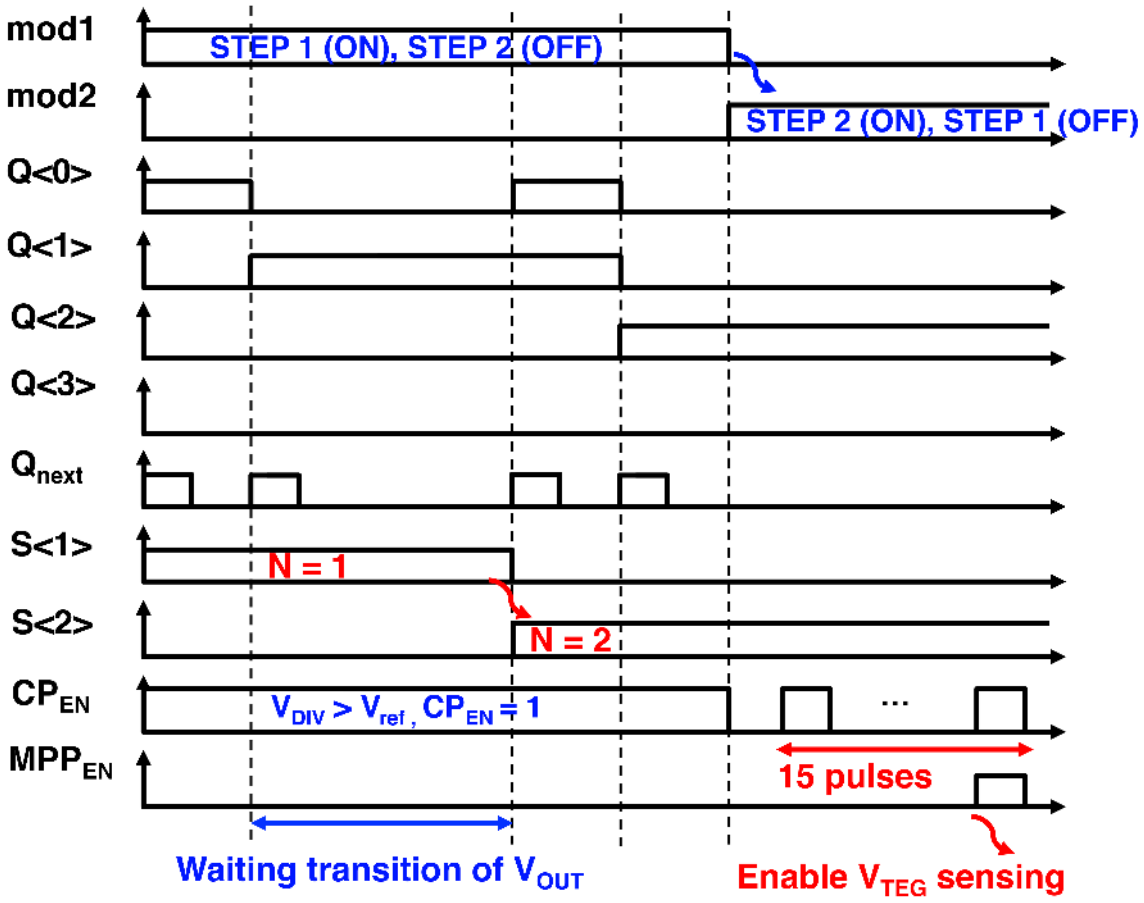


Figure 3.19: Transition of the digital controller

Figure 3.17 presents the state diagram of the FSM. In the both steps, $V_{DIV} = V_{out}/2$ is compared to V_{ref} due to the limited input voltage range of a comparator. By the comparison, $CP_{EN} = 1$ ($V_{DIV} < V_{ref}$) enables charges pump and vice versa. Figure 3.18 shows the implemented FSM with three ripple counters to minimize power consumption: Q for the states, D for the delay between transition of a conversion gain (CR), and CNT for a periodic triggering the MPP acquisition. Figure 3.19 illustrates the controller signals when $V_{TEG} = 0.5\ V$. In the first step, 4096 cycles of f_{sw} generates delay waiting transition of V_{OUT}. Once V_{OUT} reaches to a desired voltage, Q_{next} is no longer triggered. Then, $mod2$ enables the second step activating the MPP acquisition by 15 pulses of CP_{EN}.

4.1 Measurement of the proposed energy harvester

4.1.1 The Fabricated Chip

The proposed energy harvester PMU is fabricated in standard IBM 130nm CMOS technology by MOSIS. The fabricated die is 1.5 mm x 1.5 mm and occupies 0.835 mm^2 of active area. The chip is packaged with 36-pins QFN package to reduce parasitics capacitance and inductance from leads.

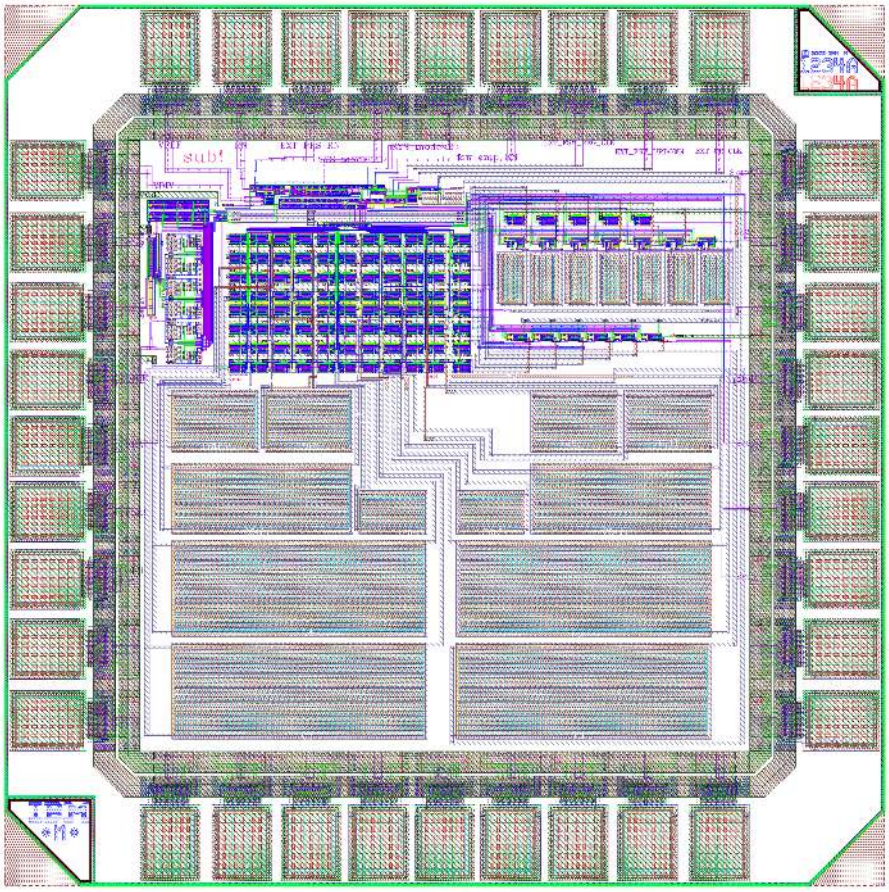


Figure 4.1: Layout of the designed energy harvester

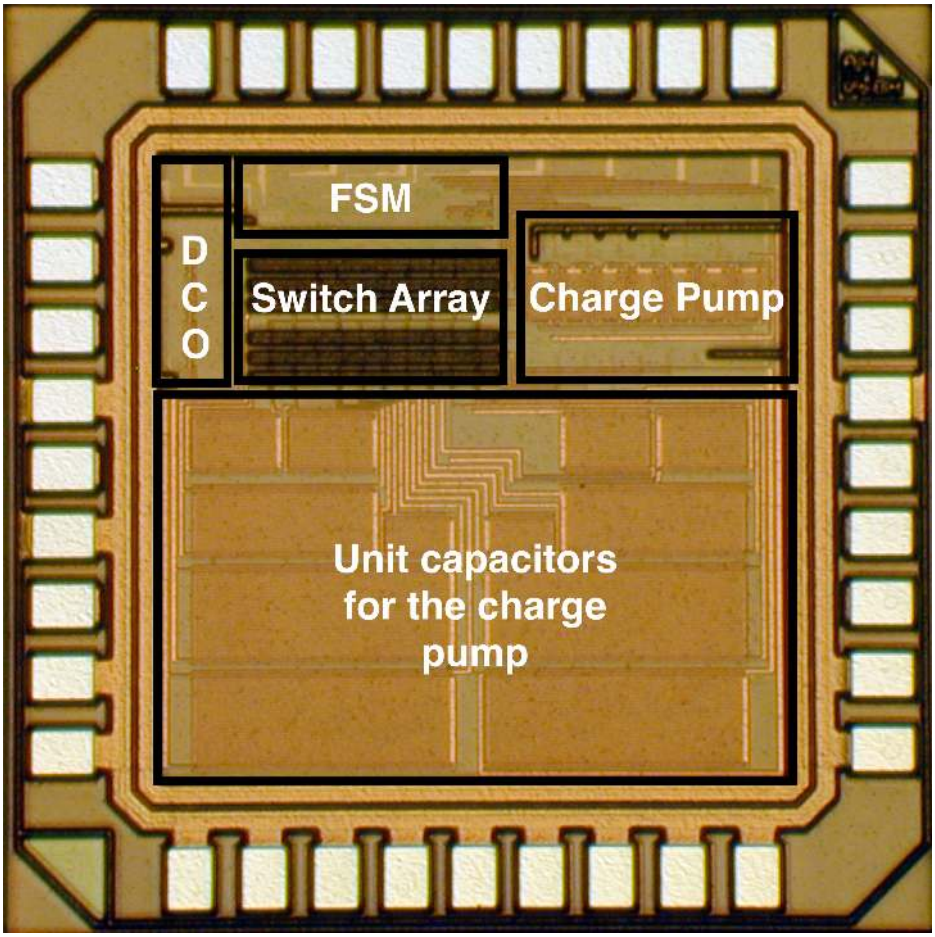


Figure 4.2: Die photograph of the fabricated energy harvester

Figure 4.1 presents the designed energy harvester layout. It is fabricated as shown in Figure 4.2. To minimize the power path routings from the input to the output, the blocks arranged horizontally. In the reconfigurable charge pump, the capacitors are realized with a dual-layers MIM capacitor: It has the minimum bottom parasitic capacitance, which reduces power delivery efficiency. As illustrated in Figure 4.2, total 1.5 nF of 12 unit capacitors are distributed to the corresponding charge pump stages by the activated step-up stages.

4.1.2 Measurement Setups

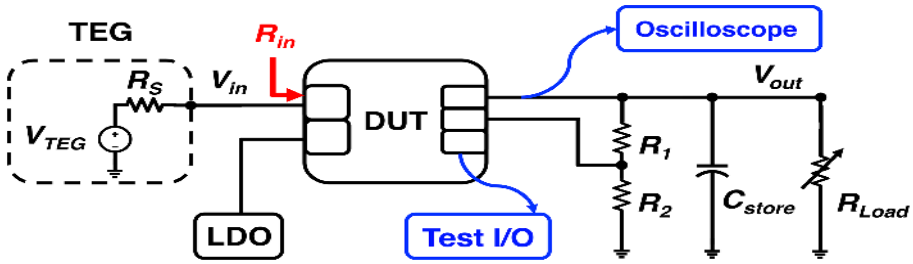


Figure 4.3: Measurement setup for the proposed energy harvester

Figure 4.3 shows the measurement setups. First, a TEG is emulated with DC power supply (Keysight E3631A) and a series connected resistor [20]. Keeping two different temperature to each TEG side needs a complicated physical setup [21] to measure the PMU performance. The input current, V_{in} and V_{out} of the device under test (DUT) are measured with a multimeter (HP 34401A) and oscilloscope (Agilent 54810A). The fabricated PCB is presented in Appendix C. Table 4.1 shows the list of external components including a commercial low drop out voltage regulator (LDO) to provide a reference voltage.

R_1, R_2	$C_{storage}$	R_{Load}	R_S	LDO
5 MΩ	1 nF	2 kΩ - 184 kΩ	1 Ω - 5 kΩ	TI-TLV70012

Table 4.1: List of external components for the measurement

Following sub sections present the overall performances of the proposed PMU: the power delivery efficiency from the input to output under varying output loads, and MPPT capability for a small energy harvester source impedance.

4.1.3 Measurement Results

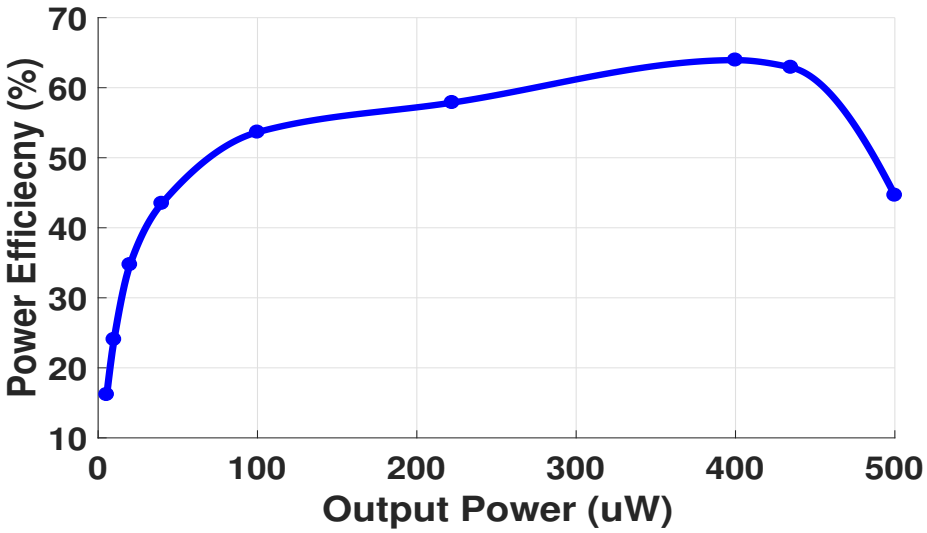


Figure 4.4: Power efficiency of the PMU with varying the output load ($R_S = 1\Omega$)

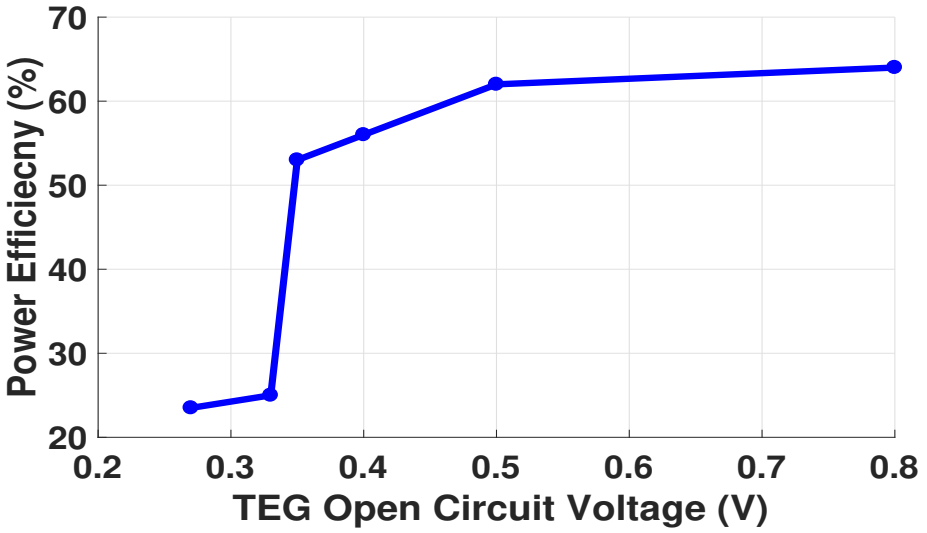


Figure 4.5: Power efficiency of the PMU with varying the TEG voltage ($R_S = 1\Omega$)

The proposed energy harvest PMU was measured with the TEG model [1]. The source impedance of 1 Ω is not available other energy harvesters: in the same switching frequency, f_{sw}, an input impedance of a conventional energy harvester is higher than the proposed PMU as shown in equation 3.1 for the input impedance of the proposed charge pump.

Figure 4.4 presents the power efficiency ($P_{out,PMU}/P_{in,PMU}$) by varying an output load in the ordinary environment; V_{TEG} = 0.8 V with Δ T=10 °C, where the temperature difference between a human and 27 °C. The measured peak power efficiency was 64% delivering 400 μW to the output. Over the peak point, conduction losses through switches in the PMU was dominated reducing the power efficiency. After 500 μW of output load current, the PMU could not maintain the desired output voltage, 1 V.

Figure 4.5 shows the power efficiency by varying a TEG open circuit voltage, V_{TEG}. As increasing V_{TEG}, the proposed PMU dynamically changes number of the charge pump stages to maintain the output voltage of 1 V. Each point represents the peak power efficiency at the corresponding charge pump stages. Expending a compatibility of the PMU to other TEGs, Figure 4.6 shows the measurement with R_S = 10 Ω and V_{TEG} = 0.8 V.

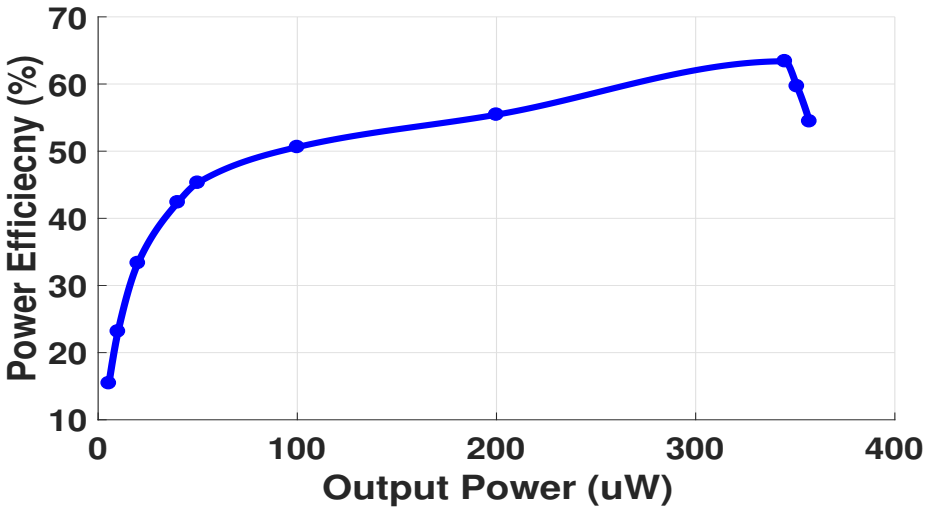


Figure 4.6: Power efficiency of the PMU with varying the output load ($R_S = 10\Omega$)

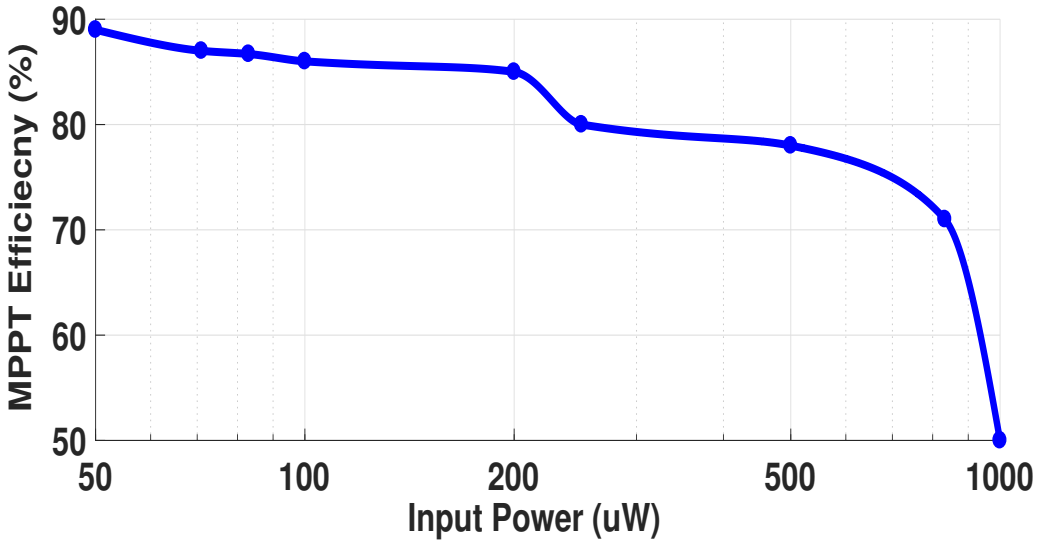


Figure 4.7: MPPT efficiency of the propose PMU with varying the input power

As described in equation 2.19 for the input power of the PMU, $V_{in} = V_{TEG}/2$ ensures the maximum input power as a result of $R_{in} = R_S$. By measuring the input voltage, the MPPT efficiency is as follows:

$$\eta_{MPPT} = \frac{V_{TEG}/2 - \Delta\epsilon}{V_{TEG}/2} \tag{4.1}$$

$$\Delta\epsilon = |V_{TEG}/2 - V_{in}| \tag{4.2}$$

Figure 4.7 illustrates MPPT efficiency of the proposed PMU with different input power conditions. With the low input power ($<$200 μW), the proposed PMU achieves at least 85% of MPPT efficiency. Under the higher input power, the MPPT efficiency is decreased due to the limitation of the maximum switching frequency, f_{sw}, of 4.25 MHz. Faster f_{sw} could increase the MPPT efficiency. However, this does not mean delivering more power to the output due to the switching power losses which is proportional to f_{sw} as described in equation 2.15.

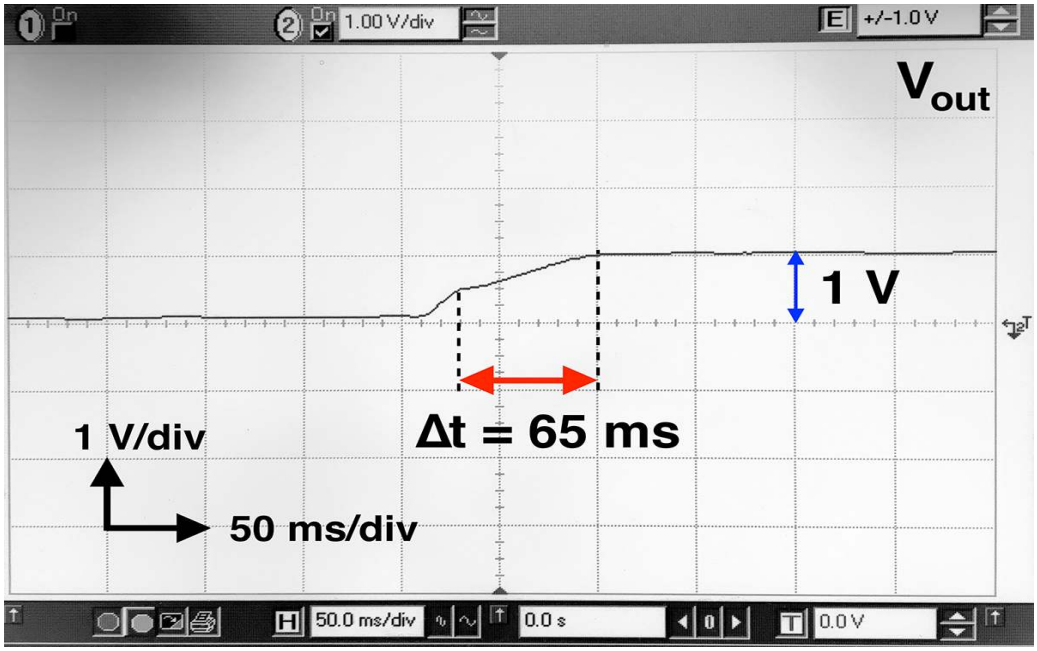


Figure 4.8: Transient response of the output voltage of the PMU

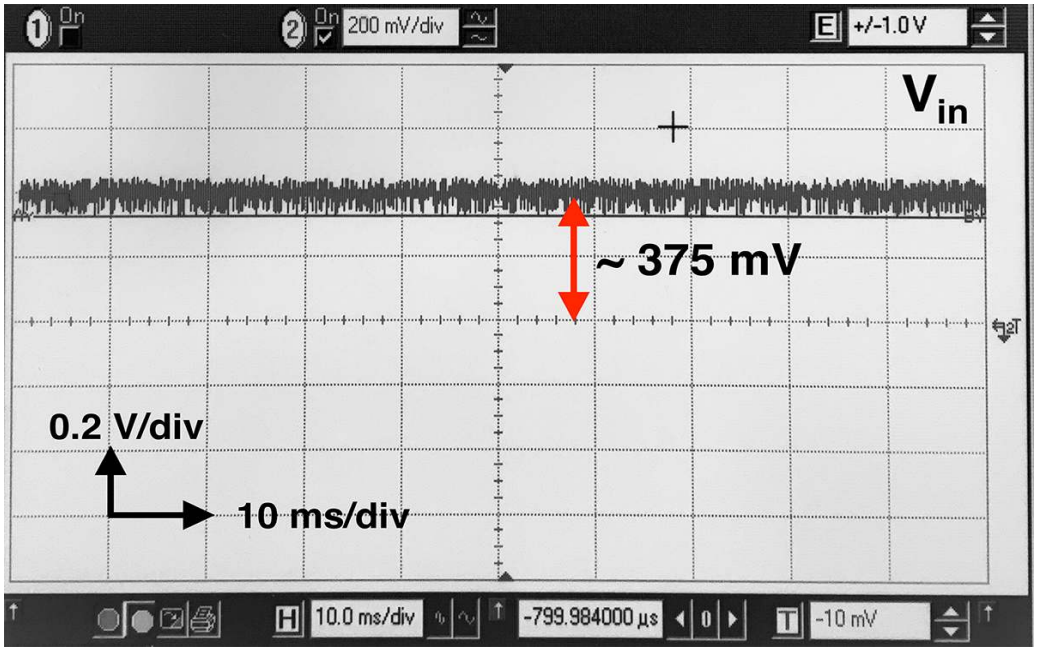


Figure 4.9: The input voltage of the PMU after MPPT

Figure 4.8 shows the transient response of the output voltage, V_{out}. Once the 1 nF output buffer, C_{store}, reaches to the cold start up voltage, 500 mV, the proposed PMU starts to optimize N, $C_{S,eff}$, and f_{sw} for the desired output voltage and MPPT. In the first step, the number of charge pump stages and the effective stage capacitance are dynamically changed until $V_{div}(= V_{out}/2)$ is larger than V_{ref}. Within the 65 ms from the initial start up, the first step is terminated. The second step excites fine-regulation of V_{out} and MPP acquisition. Regulating the output voltage of 1 V, DCO changes frequency by 16 steps.

Figure 4.9 shows the input voltage of the PMU with $V_{TEG} = 0.5\ V$, realizing 50% of MPPT efficiency by equation 4.1. Due to the limitation of the f_{sw} of 4.25 MHz, the proposed energy harvester did not reach the high MPPT efficiency. Faster f_{sw} could increase the MPPT efficiency; however, this does not mean delivering more power to the output due to the switching power losses.

4.2 Comparison of Energy Harvesters

In Table 4.2, performance of the proposed energy harvester is compared to state of the art and the commercially available chip. Each solution is responding the extended demands of replacing batteries to IoT applications. Among the academic results, this work elaborates extracting more power from a tiny energy sources for small form factor applications. Due to the reconfigurable capacitor charge pump, the proposed solution has the smallest active area while delivering power up to $500\ \mu W$. To power IoT applications, at least few hundreds of micro-watts is required because of power hungry blocks such as a transmitter. The commercial available chip, LTC3108, can extract the power from a TEG with a small source impedance. However, it does not have ability to tune the input impedance, which is changed by the input voltage. Also, a bulky transformer is the bottleneck to be integrated to small IoT applications.

Table 4.2: Performance summary

	This work	[15]	[7]	[9]	[22] *	LTC3108 **
Technology	$0.13\mu m$	$0.18\mu m$	$0.35\mu m$	$0.18\mu m$	$0.13\mu m$	NA
Topology	CP	CP	CP	CP	CP	Transformer
Energy sources	TEG	TEG/PV/MFC	TEG	TEG/PV	PV	TEG
MPPT	3D	2D	NO	2D	NO	NO
Input impedance matching range (Ω)	1–5 k	10–300 k	100 k	NA	NA	2-10
Input voltage (V)	0.27–1	0.25–1.1	1.28–5.5	1.28–3	0.27–1.4	0.02–0.5
Regulated output voltage (V)	1	1.8, 2 ***	1.5	3.3	1.4	2.2, 5.5 ***
Power delivery (μW)	< 500	< 550	NA	< 50	< 12	<3500
Peak power efficiency	64%	57%	58%	81%	58%	60%
Active area (mm^2)	0.835	2.820	3.062	1.977 ****	0.42	NA

* The converter has a fixed voltage gain of 3.
** The power efficiency drops to 20% when the input voltage is larger than 200 mV.
*** Un-regulated output voltage.
**** The active area is estimated from the scaled die photograph.

4.3 Remarks

In this work, the proposed energy harvester provides regulated 1V output from a TEG (>270 mV) to power IoT applications. Along the 7x step-up reconfigurable capacitor charge pump, the PMU is capable of extracting power from an small foam factor TEG, generating DC voltage with a low source impedance ($>1\ \Omega$). By distributing on-chip capacitance to each activated charge pump stage, the silicon area is optimized. From Table 4.2 for the performance summary, the proposed PMU has decent peak power efficiency of 64% while delivering up to 500 μW to the output.

The performance of the PMU is affected by three non-idealities: *on* resistance of switches in the reconfigurable capacitor bank, parasitic capacitance to DCO, and a short sampling period for OCV. First, the additional switches between 12 capacitors, reconfiguring charge pump stage capacitance, leads the power loss from finite *on* resistance of the switches. Second, the parasitic capacitance and PVT limits the maximum frequency of the DCO up to 4.25 MHz. Due to the limited f_{sw}, the MPPT efficiency at a source impedance of 1 Ω is degraded. Third, OCV sampling period of 0.2 μs is short when a source impedance is larger than 5 kΩ: in the design steps, sampling capacitance was set to 500 fF, but actual capacitance is more than 1 pF due to the pad and connections.

To improve the performance, five plans are expected: optimizing reconfigurable capacitor bank, scaling DCO, MPP acquisition circuitry, self start-up, and eliminating external voltage reference. First, different stage capacitance alleviates the required number of switches rather than equal stage capacitance in the design following the theoretical verification [23]. The power losses from unequal stage capacitance is negligible than *on* resistance of the switches. The improvement stage capacitance distribution is described in Table 4.3. The total number of switches can be reduced by half due to the less number of unit capacitors than in the implemented design.

Unit \ N	1	2	3	4	5	6
C_{unit}	S_1	S_1	S_1	S_1	S_1	S_1
C_{unit}	S_1	S_1	S_1	S_2	S_2	S_2
C_{unit}	S_1	S_1	S_2	S_3	S_3	S_3
C_{unit}	S_1	S_2	S_2	S_4	S_4	S_4
C_{unit}	S_1	S_2	S_3	S_4	S_5	S_5
C_{unit}	S_1	S_2	S_3	S_4	S_5	S_6
$\boldsymbol{C_{S,eff}}$	1.5 nF	0.75 nF	0.5 nF	350 pF 1.05 nF	350 pF 700 pF	250 pF

Table 4.3: Improved distribution of the unit capacitors by number of stages

Second, the maximum f_{sw} can be increased by design margins in the DCO. Figure 4.10 shows the parasitic capacitance, C_{par}, to the digital coded capacitance. As previously mentioned in section 3.3 for design trade-off, increasing the bias current of the DCO reduces a sensitivity of C_{par} to f_{sw}. Also, binary coded capacitance will provide more f_{sw} steps than the thermometer coded one under the same number of capacitors.

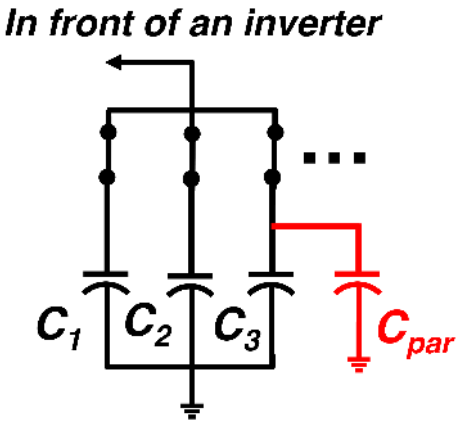


Figure 4.10: A capacitor bank in the DCO with parasitic capacitance

Third, a modified MPP acquisition circuitry in Figure 4.11 ensures sampling V_{TEG} with R_S, which is larger than 5 $k\Omega$. As increasing sampling period, the additional capacitor, C_T, seamlessly delivers charges to the output while V_{in} is disconnected from step-up stages.

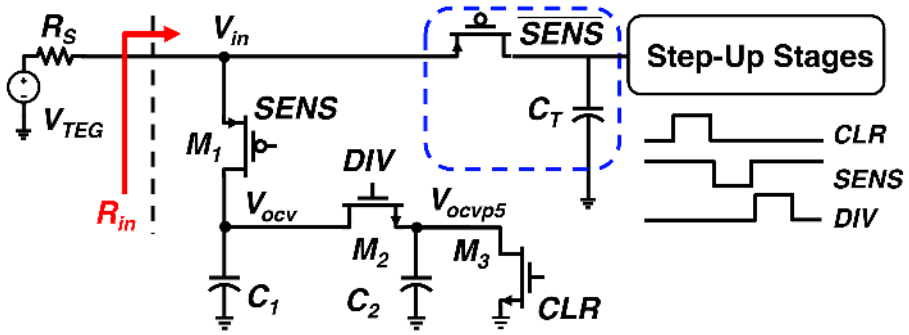


Figure 4.11: Improved MPP acquisition circuitry

Lastly, Figure 4.12 shows self-sufficient scheme with an internal voltage reference.

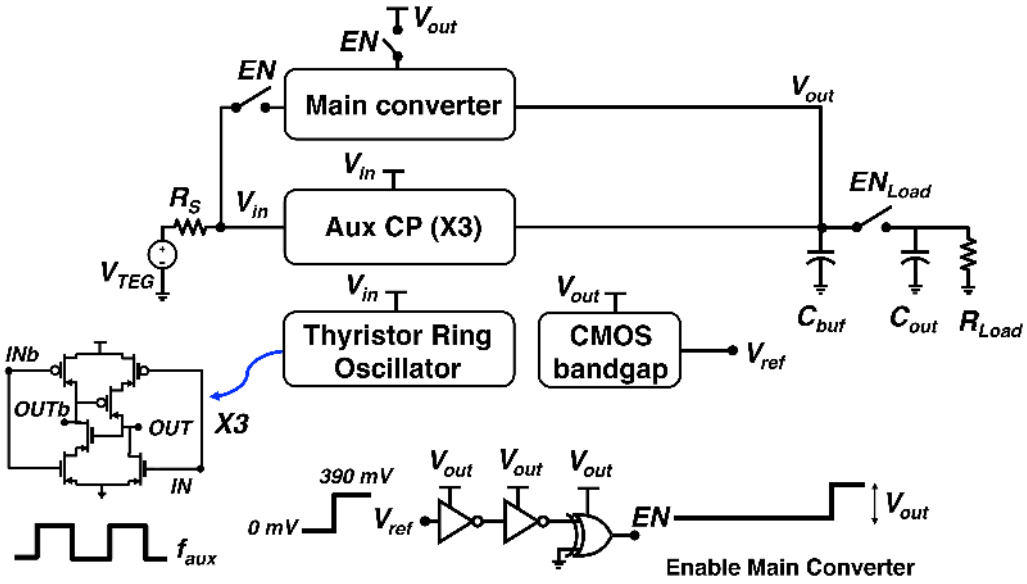


Figure 4.12: Block diagram of the self-sufficient energy harvester

For the reliability of an energy harvester, a self-start up and internal voltage reference circuitry is required. In the previously reported designs [22, 15] have the self-start up block to extract power from an energy harvest source without pre-stored charges at the output. However, both approaches are not power efficient. The design from [22] uses a comparator to check the condition to kick up an main converter. Alternatively, the PMU from [15] adopts pre-set timer to exit an auxiliary charge pump. It does not guarantee quick start-up when the input voltage is changed.

Mitigating the issues about the start-up, Figure 4.12 illustrates the improvement design eliminating an comparator and pre-set timer. The key concept is re-using CMOS band gap start-up circuitry. In the CMOS bandgap [24], a conventional start-up circuit of self-bias ensures V_{ref} of 390 mV at V_{out} of 600 mV. The EN from the combination circuit triggers the main converter. By the passive start-up, the energy harvester is capable of cold start-up when $V_{TEG} = 250$ mV. The simulation results are summarized in Table 4.4. With the best acknowledgments of the author, this is the smallest voltage excluding designs based on a transformer.

Thyristor Ring Oscillator		CMOS bandgap	
f_{aux}	P_{osc}	TC ($0C^{\circ}$–$60C^{\circ}$)	$P_{bandgap}$
114 kHz	1.18 nW	724 ppm	222 nW

Table 4.4: Simulation results of the self-sufficient energy harvester

5. SUMMARY AND FUTURE WORK

5.1 Summary

This thesis presents the energy harvester with the reconfigurable capacitor charge pump fabricated in 130nm CMOS technology. As a result of distributing on-chip capacitors to the activated step-up stages, the proposed energy harvester optimizes the silicon area. Due to the increased effective stage capacitance for the charge pump, the design is capable of 3D MPPT, dynamically tuning N, f_{sw}, and $C_{S,eff}$ to extract the power from a TEG with a small internal impedance (1 Ω). From the measurement, the energy harvester has 64% peak power efficiency delivering 400 μW to the regulated output voltage, 1 V.

5.2 Future Works

In the proposed energy harvester, a novel method is to extract power from a small foam factor energy harvest source. The maximum output power of 500 μW is reasonable to operate IoT applications by using conditionally. To extend the usage of an energy harvester, autonomous start-up, dual paths of the output, and combining multiple energy sources are are expected.

First, the proposed energy harvester requires 500 mV to initiate the operation. Thus, autonomous start-up kicks a PMU to start extracting power without small pre-stored power. Second, a LDO is capable of providing the ripple-clean output voltage to load RF applications such as a transmitter. Third, dual paths of the output power ensure the reliability of an energy harvester. When IoT applications are not in use, extra power can be stored to a super capacitor; it is smaller than the conventional batteries and safe from explosion such as Li-Ion type. Lastly, an energy harvester would simultaneously harvest power from multiple energy harvest sources (TEG, Solar, Kinetic, and RF). By the combination, an energy harvester can be the attractive solution to power every consumer applications.

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APPENDIX A

MATLAB CODE

A.1 The Comparison of Charge Pump Input Impedances

This code plots the input impedance of a Dickson charge pump and the proposed reconfigurable capacitor charge pump.

```
clear all; close all;


% Initial setup
% N  : The vector for the number of charge pump stage
% C  : Capacitance per stage
% Ct : The total on-chip capacitance (C*the maximum # of N)
% fsw: The switching frequency of a charge pump
% R  : The Load resistance at the output (Voutput = 1 V)

N=1:1:6; C=250e-12; Ct=C*6;
f=1e6; R=4E3;

% < Calculation of a conventional dickson charge pump >
% dA: the difference between a votlage gain and ideal gain
% rin_conv: An input impedance of the conventional dickson
   charge pump
% < Calculation of the proposed dickson charge pump >
% dA_new, rin_new
```

```
dA = (N+1) - ((N+1)./(1+(N./(C*f*R))));
rin_dickson = N ./ ((N+1).*C.*f.*dA);
dA_new = (N+1) - ((N+1)./(1+(N./((Ct./N)*f*R))));
rin_new = N ./ ((N+1).*(Ct./N).*f.*dA_new);

% Plot
fig_var = figure;
fig_var.Color ='white';
xlabel('The number of charge pump stage (N)');
ylabel('Normalized input impedance');
hold on
grid on

axis_var = gca;
plot_var.LineWidth = 5;
plot_var.Color = 'blue';

axis_var.FontWeight = 'bold';
axis_var.FontSize = 24;
plot(N, rin_dickson./2000); hold on;
plot(N, rin_new./2000);
```

A.2 Model of an Input Impedance

For the design of an energy harvester, this MATLAB code illustrates the relation of an input impedance to a switching frequency, f_{sw}, the number of charge pump stages, N, and an load resistance of the energy harvester, R_{load}. The first plot sweeps both f_{sw}, and N. For the second plot, R_{load} and N are changed.

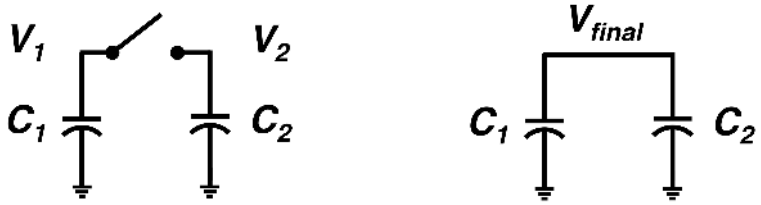
```
clear all; close all;


% Initial setting
% Vs: DC voltage from a TEG
% Rs: The source impedance of the TEG
% Rload: a load resistance of a PMU
% fsw_range: a switching frequency range of the PMU
% N_stage  : The total number of the charge pump stage
% C        : Capacitance per charge pump stage
% Ctot     : Total on-chip capacitance
Vs=0.5; Rs=1; Rload=500;
fsw_range = 100e3:50e3:10e6;
N_stage=6;
C=250e-12;
Ctot=C*N_stage;


for i=1:1:length(fsw_range)
        fsw=fsw_range(i);
        for j=1:1:N_stage
        % Reconfigurable capacitor by # of stages, j
```

```
        C=Ctot/j;
        % Design parameters from the fuction, pmu_model
        [Rin_temp, Rout, Vin, Vout]=pmu_model(j,fsw,C,Rload
           ,Vs,Rs);
        % Store scaled data
        Rin(i,j)=Rin_temp/1e3;
        end
end

% Plot 1 - Rin versus fsw and # of stages
surf(Rin);
xlabel('Stage'); ylabel('f_s_w'); zlabel('Rin (kohm)');

% For the second plot, the switching frequency is fixed
% Rload_range, load resistance for the PMU
fsw=1e6;
Rload_range=2e3:50e3:2e6;
for i=1:1:length(Rload_range)
        Rload=Rload_range(i);
        for j=1:1:N_stage
        % Reconfigurable capacitor by # of a stage, j
        C=Ctot/j;
        [Rin_temp, Rout, Vin, Vout]=pmu_model(j,fsw,C,Rload
           ,Vs,Rs);
        Rin(i,j)=Rin_temp/1e3;
```

```
        end
end
% Plot 2 - Rin versus Rload and # of stages
surf(Rin);
xlabel('Stage'); ylabel('R_l_o_a_d'); zlabel('Rin (kohm)');

function [Rinput,Routput,Vinput,Voutput] = pmu_model(num,
   frq, cap, res_load, Vsource, Rsource)
% Ideal voltage gain
Aideal=num+1;
% realistic votlage gain
Av=(num+1)/(1+num/(cap*frq*res_load));
Adiff=Aideal-Av;
Rinput=num/(Aideal*cap*frq*Adiff);
% Rout, Output Impedance
Routput = num/(cap*frq);
% Vinput, an input voltage rated to the PMU
% Voutput, an output voltage of the PMU
Vinput = Vsource * [Rinput / (Rinput + Rsource)];
Voutput= Vinput * [res_load/(res_load+Routput)]*Av;
end
```

APPENDIX B

CHARGE REDISTRIBUTION LOSSES



(a) Switch *off* (b) Switch *on*

Figure B.1: Charge delivering in a switched capacitor converter

Inherently, energy is lost while charges are redistributed between two capacitors. Figure B.1a shows the initial state of capacitors $C_1,\ C_2$ holding a voltage $V_1,\ V_2$ respectively. The stored energy for each capacitor, C_1 and C_2 are described as:

$$E_{init} = E_{C_1} + E_{C_2} = \frac{1}{2}(C_1V_1^2 + C_2V_2^2) \tag{B.1}$$

As a switch is closing in Figure B.1b, the total energy at steady-state is as follows:

$$C_1V_1 + C_2V_2 = (C_1 + C_2)V_{final} \tag{B.2}$$

$$E_{final} = \frac{1}{2}(C_1 + C_2)V_{final}^2 \tag{B.3}$$

Thus, charge redistribution losses, E_{loss} is defined as:

$$E_{loss} = E_{init} - E_{final} = \frac{1}{2}\frac{C_1C_2}{C_1 + C_2}(V_1 - V_2)^2 \tag{B.4}$$

APPENDIX C

MEASUREMENT SETUP

C.1 The Fabricated PCB

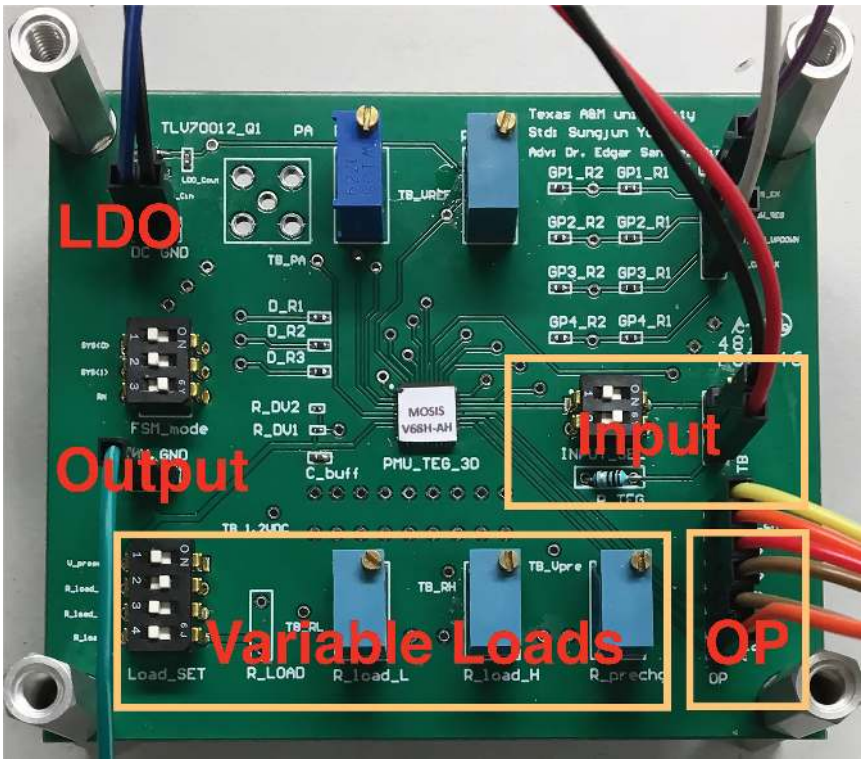
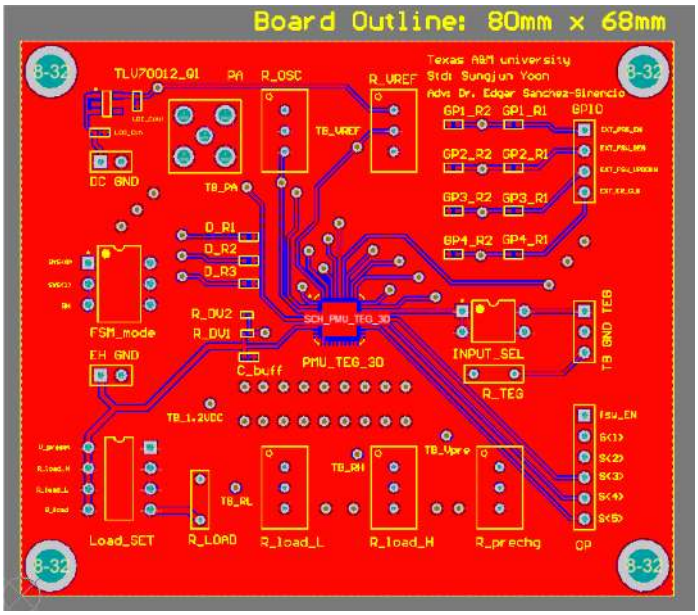


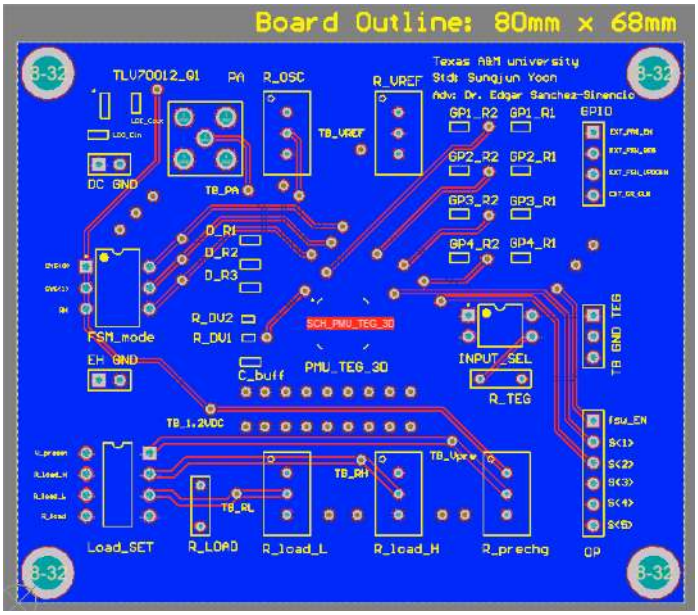
Figure C.1: The fabricated PCB for the measurement

Figure C.1 presents the fabricated PCB with the measurement setup. Figure C.2a and C.2b show the top and bottom layer of the PCB, respectively. As previously discussed, the input voltage and reference voltage were applied to the chip (PMU_TEG_3D). While changing variable loads, the output voltage and input voltage were measured with observation points (OP). The OP provided the information of the activated charge pump stages.

C.2 PCB Layers



(a) The top layer of the PCB



(b) The bottom layer of the PCB

Figure C.2: Layers of the fabricated PCB