An ASK Demodulator in CMOS Technology

Authors: Marcelo Barú, Hugo Valdenegro, Conrado Rossi and Fernando Silveira

Contact Person: Marcelo Barú.

Instituto de Ingeniería Eléctrica
Universidad de la República
J. Herrera y Reissig 565
Montevideo 11300
Uruguay
Tel: +598 2 7110974 - Fax: +598 2 7117435
E-mail: cabeza@iie.edu.uy

ABSTRACT

The design of a binary ASK noncoherent demodulator circuit in CMOS technology is described. It will be used to decode an ASK signal carrying information from an external programming device to an implantable cardiac pacemaker. The cell, currently being fabricated, has a core die area of $0.29mm^2$ on a 2.4μm standard CMOS technology with 0.85V nominal threshold voltage.

We review the characteristics of the signal and the specifications for the circuit. A non-standard topology is proposed, allowing the circuit to be fully integrated, thus, lowering the component count of the system and increasing reliability.

We detail the design to the transistor level with special consideration to the limitations associated with low supply voltage. We emphasize the careful sizing, using the (g_m/I_D) method, of transistors operating in the weak and moderate inversion regions. This allowed to lower the gate-source and saturation voltages, achieving operation for 2V even in the worst case condition of 1V maximum threshold voltage and 5 μA current consumption.

We present simulation results and the cell layout for the proposed circuit and an alternative design. Finally, we draw some conclusions.

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ABSTRACT

The design of a binary ASK noncoherent demodulator circuit in CMOS technology is described. The cell, currently being fabricated, has a core die area of 0.29mm^2 on a 2.4μm standard CMOS technology with 0.85V nominal threshold voltage. A non-standard topology and accurate sizing of the transistors for operation in the weak and moderate inversion regions allow full integration and operation down to supply voltages of 2V with consumption of 5μA.

I. Introduction

This paper describes the implementation, in a standard 2.4μm CMOS technology, of a low voltage, low power ASK demodulator circuit[1]. The circuit is part of a chip under development by the *Microelectronics Group, Universidad de la República, Uruguay* for the *Centro de Construcción de Cardioestimuladores del Uruguay (C.C.C.U.)*. It will be used to decode an ASK signal carrying information from an external programming device to an implantable cardiac pacemaker.

In section II we review the characteristics of the signal and the specifications for the circuit, section III discusses the circuit topology and section IV details the design to the transistor level with special consideration to the limitations associated with low supply voltages. Section V shows the layout and simulation results, section VI presents an alternative design, finally in section VII we draw some conclusions.

II. Characteristics of the modulated signal, constraints and specifications

Some parameters of a pacemaker need adjustment, after being implanted, according to the patient's specific needs. The information is transferred using electromagnetic coils [1], one inside the pacemaker and another inside the computerized external programming device. In this particular case, a binary ASK (amplitude-shift keying) modulation is used for transmitting these parameters. This type of modulation consists of a sequence of binary pulses where a "1" turns on a sinusoidal carrier wave and a "0" turns it off (see Fig.1).

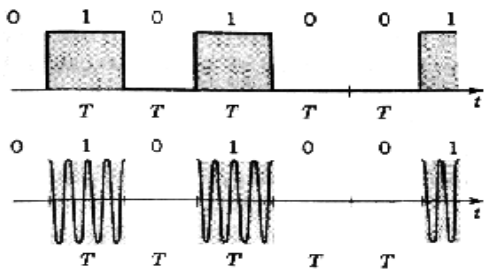

Fig.1 ASK modulation

The demodulator circuit processes the signal received from the programming device restoring a digital "1" to the pacemaker micro-controller when it senses the carrier and a "0" when it does not.

For compatibility with existing programming devices, the coil (antenna) circuit is kept from previous designs, yielding a modulated signal whose minimum amplitude is only 30mV_p around half of the supply voltage (V_{DD}/2). The carrier frequency is 27KHz and either of the bits last for 1464μs (in Fig.1, T=1464μs).

Each output bit must last at least 1000μs. Output glitches are acceptable during the remaining 464μs, which reduces the complexity of the circuit as we will see later on.

The circuit must be able to drive the capacitance of the I/O pad, wiring and the micro-controller, which was estimated to be at most 50pF.

The remaining specifications are associated to the incorporation of this cell in a pacemaker. The full charge voltage of the Lithium-Iodine battery usually supplying these devices is 2.8V, and the circuit must be fully operative for supply voltages

[1] The cell is currently being fabricated. We expect to show some results during the Workshop.

down to 2.0V . Its total consumption must not be more than 5µA to comply with the system power budget.

The target process is a standard 2.4µm analog CMOS process with double poly and double metal. This process is intended for 5V supply voltage, having a nominal threshold voltage of 0.85V with a maximum and a minimum of 1.0V and 0.7V respectively. The fulfillment of the requirements in such a process, instead of a low-voltage specialized process with lower threshold voltages, enables a broader and cheaper range of possible target processes and foundries. However, the operation with 2V supply voltage in such a process presents various challenges that are presented in the following sections as well as the means we propose to overcome them.

III. Selection of the circuit topology

Figure 2 shows the usual circuit for a noncoherent ASK demodulator.

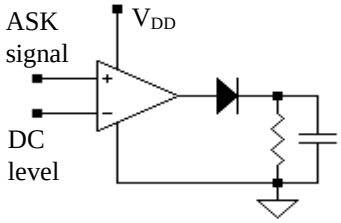

Fig.2 ASK demodulator circuit

In this circuit, the ASK signal is compared with a DC level slightly greater than its own DC level. If the carrier is present, the capacitor is charged through the diode decoding the "1". On the other hand, when there is no carrier, the capacitor is discharged through the resistance, thus decoding the "0". In this way, we reconstruct the binary sequence of pulses.

The main problems to build this circuit in a CMOS technology arise from the difficulties to use resistances and the parasitic bipolar transistors associated with floating diodes. We overcame them by using the circuit in Fig. 3.

The diode function is implemented with a PMOS transistor (M) working as a switch. We substitute the discharge resistance with a constant current source, which is much easier to build in an IC.

Finally, the two inverters drive the 50pF capacitance load (C_L).

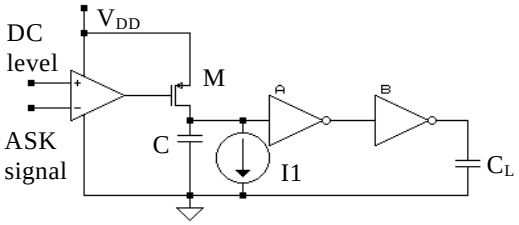

Fig.3 ASK demodulator circuit proposed

IV. Design methodology

We chose a two-stage OTA to implement the comparator (see Fig.4). In this way we achieve the needed gain.

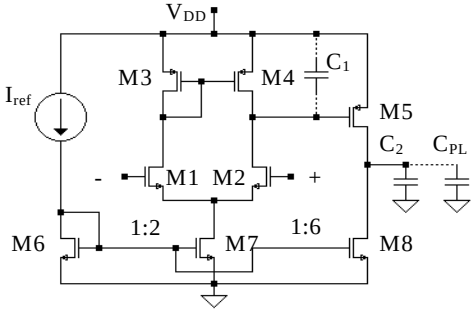

Fig.4 Proposed comparator topology

The sizing of the transistors was carried out using the method presented in [2],[3]. It is based on the relation of the transconductance over drain current ratio (g_m/I_D) to the normalized current ($I_D/(W/L)$) and allows a unified treatment of all regions of operation of the MOS transistor. An accurate sizing of the transistors can be achieved by using this method and the EKV model [4],[5] with a set of parameters extracted from measurements of the target process.

The main specifications that apply to the comparator design are the minimum input common mode level of 1.0V (for V_{DDmin} = 2.0V) and the maximum total consumption of 5µA. We designed the comparator based on these specifications and trying to minimize its die area.

Because of the minimum common mode of 1.0V, we need to place the transistors of the differential pair as deep as possible in the weak inversion region, therefore choosing a high (g_m/I_D). This will give, for a given current, a low gate-source voltage. Anyway, due to the flat characteristics of the (g_m/I_D) vs. ($I_D/(W/L)$) curve in the weak inversion region, a small increment of (g_m/I_D) requires a big increment of (W/L) increasing the parasitics and therefore slowing the comparator.

By exploring the design space through the (g_m/I_D) method, we chose the best compromise

between performance and aea which led to a $(g_m/I_D)_1$=22 while I_{D1}=500nA. This corresponds to a $(W/L)_1$=208/4. This non minimum value of 4μm for the drawn length of M1, was chosen based on reliability considerations. In the target CMOS process the final sizes are derived from the drawn sizes after a 0.8 factor shrink.

The M7 transistor is also involved in the minimum common mode parameter. The minimum common mode of the comparator in Fig.4 is (V_{GSmax}(M1) + V_{DSsat}(M7)). Therefore, in order to minimize the common mode, we need to place M7 near weak inversion, where the drain-source saturation voltage is minimum (approximately $2U_T..3U_T$, where U_T is the thermal voltage). We chose $(g_m/I_D)_7$=18. This value, together with the drain-source current of 1μA needed by the differential pair, led to two transistors in parallel, each of size $(W/L)_6$=8.7=104/12. Since M7 implements a current source, we chose L=12 so that it presents a high output impedance

After sizing M1 and M7, we can calculate the minimum common mode of the comparator. From a simulation using the EKV model, V_{DSsat}(M7)=60mV, and considering the body effect introduced by M7, V_{GSmax}(M1)=1.01V. Thus, the minimum common mode is 1.07V, slightly over 1.0V, but acceptable anyway.

The size of the mirror stage M3-M4 is determined from the minimum value of V_{DD}, which is given by the following inequation

$$\mathbf{V_{DDmin} \geq V_{DSsat}(M7)+V_{DSsat}(M1)+V_{SGmax}(M3)} \quad (1)$$

Although it is appropriate to place M3-M4 near the strong inversion region to have a better matching in the current copying, when we move toward the strong inversion region the gate-source voltages increase. In order to simultaneously satisfy the above conditions, we placed M3-M4 in the moderate inversion region with a $(g_m/I_D)_3$=12. This led to a $(W/L)_3$=47/12. The V_{SGmax}(M3) is 1.12V, so satisfying inequation 1.

For the sizing of M5, it should be observed that inequation 1 must also be satisfied if V_{SGmax}(M3) were substituted by V_{SGmax}(M5). We can place M5 nearer the strong inversion region than M3, since its current will be higher than that of M3 for the comparator to have its non dominant pole far away from the dominant one to increase speed. We chose $(g_m/I_D)_5$=5 and I_{S5}=3μA. This gives V_{SGmax}(M5)=1.4V and $(W/L)_5$=24/8. The current through M5 is fixed by M8, which is implemented with six transistors having the size of M6 in parallel.

The transistors sizes are summarized in table 1. The dimensions indicated below are drawn dimensions.

Transistor	W/L	g_m/I_D
M1	208/4	22
M3	47/12	12
M5	24/8	5
M6	104/12	18

Table 1 Transistors of the comparator. All dimensions are drawn dimensions that are shrunk by a 0.8 factor before fabrication

After the comparator, we must determine the size of M and values for I1 and C (see Fig.3). In the case of C, we chose a value of 10pF in order to avoid the effects of parasitic capacitances. The value of I1 was determined from the maximum fall time allowed in a "1-0" transition. As mentioned in section II, this time is equal to 464μs. This means that

$$\frac{\mathbf{C\ V_{DDmax}}}{\mathbf{I1}} \leq \mathbf{464\mu s} \quad (2)$$

which implies that I1≥60nA. We chose I1=100nA so as to generate it from the pacemaker internal current reference source.

For transistor M, it would be enough to choose W>>L in order to have the minimum delay in the decoding of a "1". Anyway, it is better to charge C in several steps so as to have some immunity to noise in the transmission. We applied the criterion of reaching (V_{DDmax}/2) (threshold voltage of an ideal inverter) in four carrier cycles, when the ASK signal produces the minimum differential input in the comparator. The charge gained by C in each step is proportional to the comparison window (t_{open}) as shown in Fig.5.

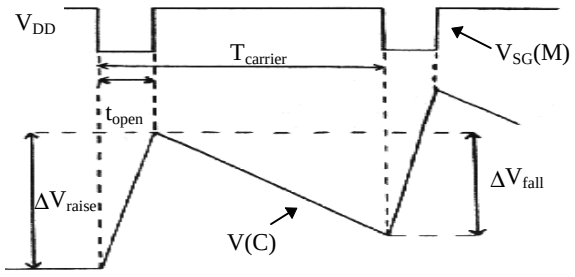

Fig.5 Voltages during the decoding of a "1"

ΔV_{raise} and ΔV_{fall} depend on t_{open} which must be found. From the sizes of the transistors of the comparator, we estimated its DC gain, the dominant pole given by C_1 and its non-dominant pole

supposed only given by the parasitic output capacitance of the comparator C_2 (see Fig.4). This last hypothesis can be applied since C_{PL}, gate-source capacitance of M, will result negligible small compared to C_2. This second order transfer function for the comparator was simulated with Matlab, with a worst case condition of an ASK signal of minimum amplitude and the maximum DC level plus a maximum comparator offset as inputs (refer to [6] for a procedure to estimate the comparator offset). The comparison window t_{open} resulted to be 3.5μs. In this way,

$$\Delta V_{fall} = \frac{I1\,(T_{carrier} - t_{open})}{C} \cong 0.33V \qquad (3)$$

and

$$(\Delta V_{raise} - \Delta V_{fall})\,4 = V_{DDmax} / 2 \qquad (4)$$

so ΔV_{raise}=0.68V. Then

$$I_S(M) - I1 = (C\,\Delta V_{raise}) / t_{open} \qquad (5)$$

From eq.5, I_S (M)≅2050nA. With this current, we can use the simplified equation for saturation in strong inversion, shown in eq.6, to size transistor M.

$$I_S(M) = \frac{\mu C_{oxp}\,(W / L)_M}{2\lambda}\,(V_{DDmax} - V_{Tmax})^2 \qquad (6)$$

From the above eq., $(W/L)_M$=4/43.

Finally, it was enough to choose the A and B inverters (see Fig.3) with minimum size in order to drive the 50pF capacitance load (this was checked by simulation).

V. Simulation results and layout

A complete simulation of a "1-0-1" decoding, for a comparison with minimum overdrive, is shown in Fig.6.

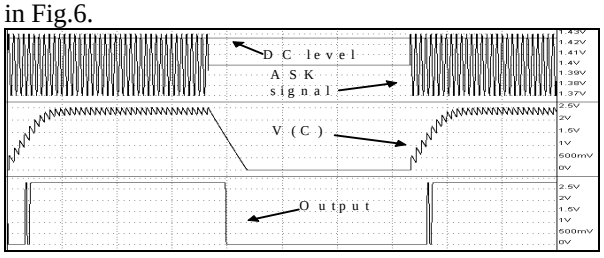

Fig.6 Complete simulation of a "1-0-1" decodification

As it can be seen in the simulation, the output of the circuit presents glitches. This is due to the charge of capacitor C in steps since we can cross the threshold voltage of the inverters more than once (see Fig.3). In the proposed circuit, a single cross can not be assured since the threshold voltage of an inverter can not be precisely known. As the glitches do not cause problems at system level, this is the circuit that we implemented.

Figure 7 shows the layout of the architecture proposed in Fig.3. It uses a die area of 0.29mm^2.

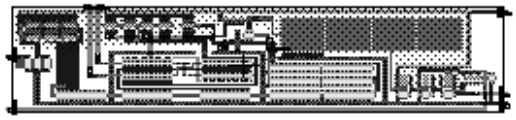

Fig.7 Layout of the ASK demodulator circuit

VI. Alternative circuit

If desired, the glitches can be avoided by implementing the function of inverter A with two current sources as schematized in Fig.8.

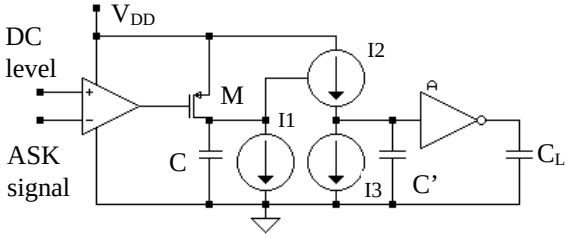

Fig.8 Decodification circuit without glitches

Here, I2 performs the pull-up function and I3 the pull-down function of an inverter. On one hand, the single cross through the threshold voltage of the A inverter has to be guaranteed by the sizing of I3. This can be done by not allowing, taking a margin of security for the switching of the inverter, C' to discharge more than ($0.35V_{DDmin}$) in a carrier cycle. On the other hand, I2 can be sized studying a "1-0" transition and imposing a charge of C' (for example to $0.65V_{DDmax}$) in the time allowed to guarantee a certain bit length required. Since I2 results to be higher than I3, it has to be controlled by the voltage in C in order to be able to perform a "0-1" decodification.

VI. Conclusions

The presented design is compatible with the requirements for demodulating the ASK signal carrying information from the external programming device to an implantable pacemaker. The circuit can operate with supply voltages down to 2V and its total consumption is less than 5μA.

The careful sizing of the transistors, operating in the weak and moderate inversion regions, by the (g_m/I_D) method allowed to lower the gate-source and saturation voltages, achieving operation for 2V even in the worst case condition of 1V maximum threshold voltage.

The proposed circuit can be fully integrated, lowering the component count of the system and, thus, increasing reliability.

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