# An Autonomous 16 mm$^3$ Solar-Powered Node for Distributed Wireless Sensor Networks

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## Abstract

*A 16 mm$^3$ autonomous solar-powered sensor node with bi-directional optical communication for distributed sensor networks has been demonstrated. The device digitizes integrated sensor signals and transmits/receives data over a free-space optical link. The system consists of three die–a 0.25µm CMOS ASIC, a 2.6 mm$^2$ SOI solar cell array, and a micromachined four-quadrant corner-cube retroreflector (CCR), allowing it to be used in a one-to-many network configuration. The CMOS ASIC includes a photosensor, integrated 3 MHz oscillator, 69 pJ/bit optical receiver, and 31 pJ/sample ADC.*

## Keywords

Smart Dust, CMOS integrated circuits, MEMS, distributed sensors, low power electronics, sensor networks, micromachined sensors, cubic millimeter mote

## INTRODUCTION

As sensors have become smaller, cheaper, and increasingly abundant, there have been commensurate reductions in the size and cost of computation and wireless communication. Extrapolating these trends we envision wireless sensor nodes becoming as small and as numerous as dust—disappearing into the environment and radically changing the way we interact with it. These devices will provide more information from more places in a less intrusive manner than ever before. The Smart Dust project [1] aims to explore the limits of system miniaturization by packing an autonomous sensing, computing, and communication node into a cubic millimeter mote[1] that will form the basis of massive distributed sensor networks, thus demonstrating that a complete system can be integrated into 1 mm$^3$. Some examples of applications that we are pursuing include defense networks that could be rapidly deployed by unmanned aerial vehicles (UAV), tracking the movements of birds, small animals, and even insects, fingertip accelerometer virtual keyboards, monitoring environmental conditions affecting crops and livestock, inventory control, and smart office spaces.

1. "And why beholdest thou the **mote** that is in thy brother's eye, but considerest not the beam that is in thine own eye?" *Matthew 7:3 (KJV)*

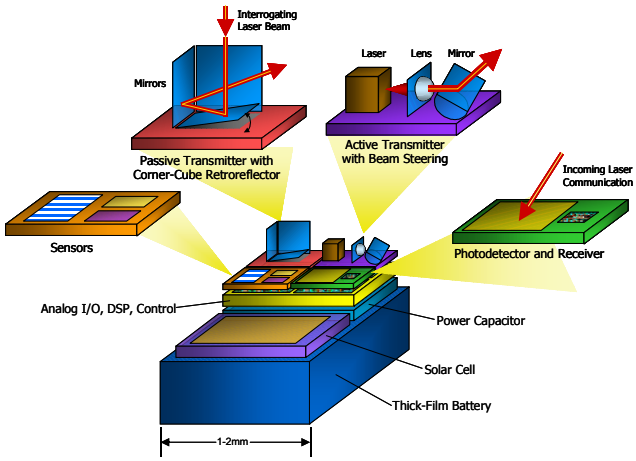


***Figure 1.*** *Smart Dust conceptual diagram.*

Other academic efforts at building small wireless sensor nodes include the multisensor microcluster [2] at the University of Michigan, Wireless Integrated Network Sensors [3] at UCLA and the Rockwell Science Center, and PicoRadio [4] at UC Berkeley. However, these nodes are one or more orders of magnitude larger, use correspondingly more power, and utilize RF communication.

The development of Smart Dust will require evolutionary and revolutionary advances in miniaturization, integration, and energy management. These advances will be facilitated by progress in Microelectromechanical Systems (MEMS), which allows us to build small sensors, optical communication components, and power supplies; and microelectronics, which provides increasing amounts of functionality in smaller areas and with decreasing energy consumption. Figure 1 shows the conceptual diagram of a Smart Dust mote. The power system may consist of a battery and/or an energy harvesting device such as a solar cell with a charge integrating capacitor for periods of darkness. A variety of sensors, including light, temperature, vibration, magnetic field, acoustic, and wind shear, can be integrated on the mote depending upon the application. An integrated circuit will provide sensor signal processing, communication, control, data storage, and energy management. A photodiode will

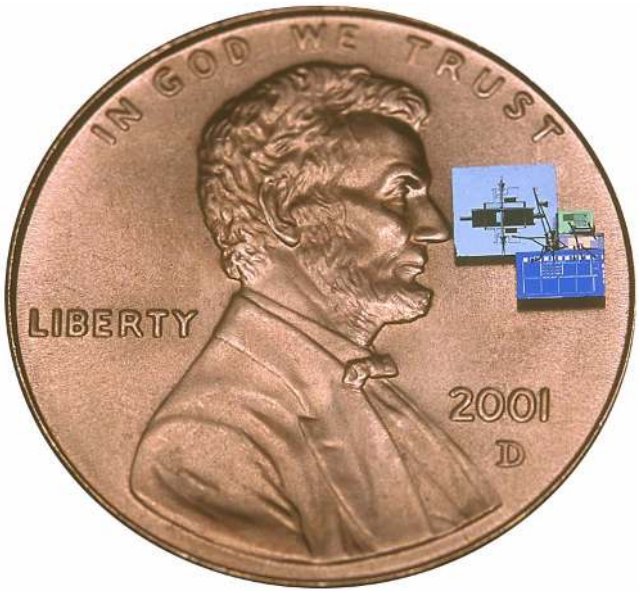


***Figure 2.*** *Mock-up of the 16mm$^3$ autonomous solar-powered mote with bi-directional communications and sensing, composed of a 0.25µm CMOS ASIC, solar power array, accelerometer (not yet demonstrated in the system) and CCR, each on a separate die. See Figure 9 for annotations.*

allow optical data reception, while two transmission schemes are being explored: passive transmission using a corner-cube retroreflector (CCR) [5] and active transmission using a laser diode and steerable mirrors [6].

The diminutive size of the mote makes energy management a primary design constraint. Current micromachined battery technology provides 5.6 J/mm$^3$ [7] while capacitors store up to 10 mJ/mm$^3$. Energy harvesting techniques are attractive for sensor nodes to allow indefinite lifetimes in the field, particularly given the small size and abundance of the motes, but system power consumption must still be minimized to maintain the tiny size of energy havesting devices.

Free-space optical communication provides several advantages over RF communication for small, energy-constrained wireless nodes. First, optical radiators can be made more efficient as well as with much higher antenna gain (> $10^6$) at the millimeter scale. Furthermore, optical transmitters are more power efficient at low power because of reduced overhead and since received power only drops as $1/d^2$, compared with $1/d^4$ for RF transmissions subject to multi-path fading.

Preliminary motes [8] have previously demonstrated various concepts of Smart Dust. The current work describes the first fully autonomous mote (Figure 2) utilizing all custom components to yield the smallest device yet. The mote consists of three die—a CMOS ASIC, an SOI solar cell array, and CCR, with a circumscribed volume less than 16 mm$^3$. This device incorporates a photosensor, an analog to digital converter (ADC), an optical receiver, a four-quadrant CCR for optical transmission, solar cells for power, and a simple

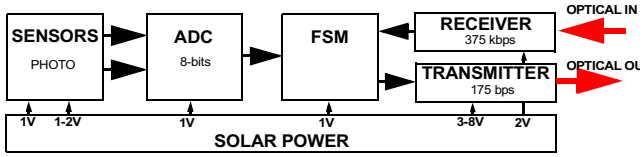


***Figure 3.*** *High-level functional diagram of the demonstrated mote. The optical downlink and uplink beams are shown separately for clarity, but in practice may be the same beam. (Since the downlink beam is modulated at frequencies well above the uplink signal band, downlink and uplink can share the same channel.)*

finite state machine (FSM) controller (Figure 3). An accelerometer has also been fabricated but not yet been demonstrated in the system. This type of mote would be used in an application that allows line-of-sight communication between one or more base station interrogators and a large number of sensor nodes, such as environmental, atmospheric, space, or military monitoring.

## COMPONENTS

### Sensors

Two sensors were designed for this mote to demonstrate integration of multiple physical sensors into a cubic millimeter node. Both sensors are wired through an analog multiplexer to the ADC and selected by the FSM.

The first sensor is an ambient light sensor integrated entirely on the CMOS ASIC. This sensor consists of an N-well/substrate photodiode in series with a polysilicon resistor to the analog voltage supply. The photodiode has an area of 200 µm × 200 µm and a responsivity of approximately 0.1 - 0.3 A/W from visible through near IR illumination. The resistance is approximately 1 MΩ, resulting in an overall sensitivity of 4 - 12 mV/(W/m$^2$).

The second sensor is a simple capacitive accelerometer (Figure 4) fabricated in an SOI process with electrical

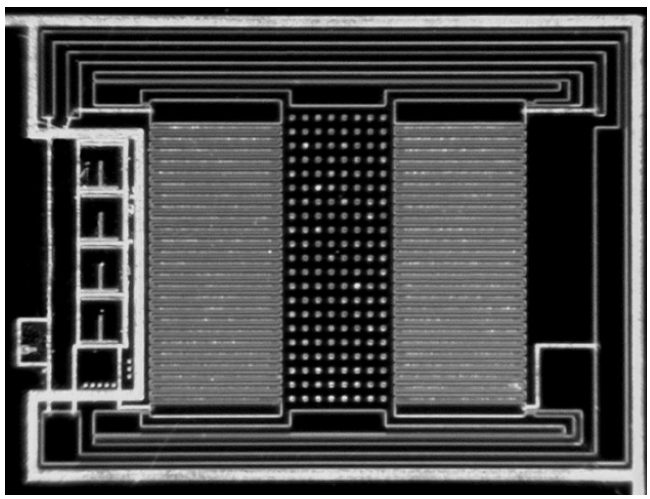

***Figure 4.*** *Photomicrograph of the gap-closing capacitive accelerometer with excitation solar cells (four squares on the left) fabricated in an SOI process. It is 0.9 x 1.3 mm.*

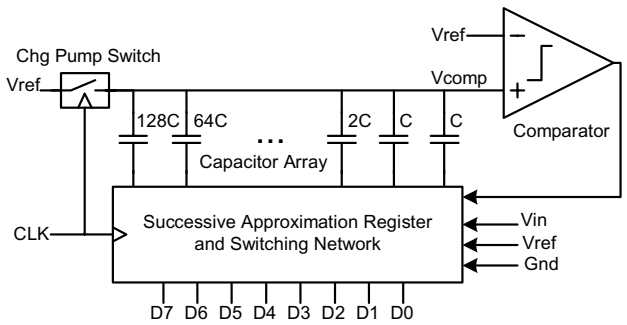


***Figure 5.*** *Successive approximation ADC architecture with a charge redistribution DAC (shown for an 8-bit converter).*

trench isolation. Small on-chip solar cells are used to provide the excitation voltage for the sensor. The accelerometer was designed so that an acceleration of 1 *g* would produce a large enough signal to be readily detected by the ADC – several 10s of mV.

To maximize sensitivity, albeit at the expense of bandwidth and linearity, gap closing capacitive sensing is used to detect the proof mass position rather than the more common lateral comb sensing. The proof mass and spring constant were designed to be $2.5\times10^{-5}$ g and 1 N/m, respectively, yielding a resonant frequency of 1 kHz and a deflection of 0.25 μm at 1 g with a layout area of 0.9 x 1.3 mm. However, mechanical testing of the accelerometer showed an overdamped response that limited the bandwidth to a few tens of Hz. The high sensitivity of this accelerometer leads to a low pull-in voltage of approximately 2 V. To achieve maximum sensitivity, the solar cell excitation network is laser trimmed so that the optimum excitation voltage can be applied without pull-in.

Although the accelerometer was tested as a stand alone device, problems with the final processing steps prevented its integration into the mote.

### Analog to Digital Converter

The successive approximation ADC architecture [9] with charge redistribution digital to analog converter (DAC) is an ideal fit for low energy applications such as Smart Dust. As shown in Figure 5, it uses only one comparator independent of the converter resolution, along with a fairly simple switching and logic network to implement the search algorithm. Assuming that the digital logic contributes very little power to the total dissipation (a good assumption since the logic is simple and has no static current drain), then energy consumption is dominated by two processes: (1) charging the binary weighted capacitors to reference voltages and (2) the *N* comparison operations (where *N* is the number of bits of resolution desired in the resulting conversion).

The successive approximation register (SAR) presents an *N*-bit digital code to the switching network that is converted to a voltage at $V_{comp}$ by the capacitor array. The comparator then compares $V_{comp}$ to $V_{ref}$. The SAR uses the result to compute its next "guess" for the digital code. A binary search algorithm leads to an *N*-bit serial conversion cycle, with the final digital output code available after the *N*th comparison. It should be noted that any search algorithm, including reduced output resolution, could be implemented in the successive approximation architecture with the appropriate digital logic. This makes the architecture flexible for sensor network applications, as the search algorithm can be modified to take advantage of sample statistics, or dynamically reduce the conversion resolution to save energy.

In the actual implementation of the mote, the comparator circuit (based on [10]) and its associated bias circuitry dominate the power consumption of the ADC, consuming 1.8 μW. The SAR [11] and switching network are simple and contribute very little to the overall power consumption of the ADC.

The core circuitry for the ADC measures approximately 0.053 $mm^2$. The maximum clock frequency of the ADC is approximately 100 kS/s, yielding 31 pJ/S with a 1 V supply. However, in this system the ADC has an enable period of 200 μs, resulting in an energy per sample of approximately 360 pJ/s. The standby power consumption is 41 pW at 1V.

The ADC achieves a signal-to-noise-and-distortion ratio of 7.9 effective bits for low input frequencies. The input signal bandwidth is fairly dependent upon supply voltage due to the basic CMOS passgates used in the sample-and-hold. This bandwidth is approximately 2.5 kHz for a 1 V supply, much faster than the sampling rate in this system.

### Optical Receiver

An optical receiver is used for downlink communication to the mote. The receiver is completely integrated into the CMOS ASIC and consists of a photodetector, analog signal processing circuits, digital timing recovery, and logic to decode incoming packets. For simplicity, the same laser beam used to interrogate the CCR is used as the downlink channel. This requires that the downlink signal spectrum be above the frequency band of the CCR uplink. In addition, to make it easy to distinguish from ambient illumination, the downlink signal should not contain any low frequency components, a constraint that occurs regardless of whether a single beam is shared for uplink and downlink. To meet this constraint, the downlink signal is Manchester encoded at 375 kbps to ensure that there is very little low frequency signal content.

Figure 6 shows a block diagram of the photodetector and analog processing in the optical receiver. Due to the small size of the mote, the optical receiver intrinsically has a small aperture. This results in low optical power collection, making the receiver sensitivity a key specification. Accordingly, a 200 μm × 200 μm N-well/substrate diode is employed as the photodetector because it has the highest responsivity of the available diodes in this process—approximately 0.25 A/W at 660 nm. Furthermore, it has the lowest capacitance,

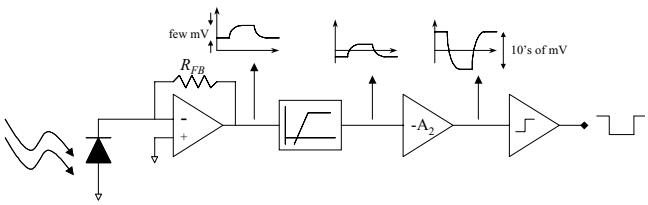


***Figure 6.*** *Optical receiver analog architecture showing the photodiode, transimpedance amplifier, high pass filter, gain cell, and comparator.*

which allows the use of higher sense impedance for a given bandwidth, yielding lower noise. A transimpedance amplifier is chosen over a simple resistor for the front-end detector because of its superior noise performance for a given input impedance [12]. An optical filter in front of the photodiode blocks most of the ambient light, including solar illumination. The remaining ambient light is not strong enough to saturate the front-end amplifier in this design, but is rejected by a high pass filter to allow the received signal to be further amplified and accurately compared, yielding a digital data stream. The receiver has been demonstrated to correctly detect optical signals as low as 50 $nW_{p\text{-}p}$ (-43 dBm, 135 fJ/bit), corresponding to an optical intensity of 1.25 $\mu W/mm^2$.

Timing recovery is performed entirely in the digital domain. One advantage of Manchester encoding is that a very robust and rapid adaptation timing recovery circuit can be implemented in an extremely compact and low power sequential logic circuit [13]. Recovered timing pulses are used to shift the serial data stream into a parallel-out shift register. When the 4-bit start flag delimiter is detected at the end of the shift register, the 8-bit data portion of the packet is latched into a data register for later access by the FSM, even after the receiver analog core has been powered off.

Power consumption during reception is approximately 26 µW at 2.1 V or 69 pJ/bit at 375 kbps.

### Corner Cube Retroreflector

Optical transmission uses a passive reflector consisting of three mutually orthogonal mirrors that form the corner of a cube (Figure 1), hence the name corner cube retroreflector (CCR) [5]. Light entering the CCR bounces off each of the mirrors and is reflected back parallel to the incident beam. By electrostatically actuating the bottom mirror, the orthogonality is broken, causing less light to return to the sender. The CCR thus communicates with an interrogator by modulating the reflected light. Energy is only consumed to charge the actuator capacitance. This technique consumes much less power on the mote than use of an active radiator, such as lasers or RF, but it does not facilitate peer-to-peer communication.

The CCR was fabricated on an SOI wafer with a 50 µm device layer to obtain flat, smooth mirror surfaces and thus approach the diffraction limit for the device size. The device and substrate layers of the wafer form the opposing electrodes of a gap-closing actuator. A sacrificial oxide etch of the 2 µm buried oxide layer yields a gap between the Si layers that provides enough angular deflection for long distance communication while enabling a high actuation force with a low drive voltage. The actuated device plate is suspended by two torsional springs. An extended device layer beam and an electrically isolated substrate island act as the mechanical stop to prevent shorting between the plates after pull-in. The two vertical cross mirrors are fabricated elsewhere on the wafer, then mounted on top of the substrate using a pair of fine tweezers. Small feet on the mirrors slide into spring-loaded slots in the substrate for anchoring, while springs on each of the mirrors lock them together, maintaining accurate alignment. In this way, four CCRs that share a common actuated bottom mirror are simultaneously fabricated (Figure 9). As silicon only reflects around 30% of visible light, 50 nm of gold is evaporated after assembly to improve the optical performance of the CCR.

DC pull-in voltages of 3.5 V have been measured. Laser doppler vibrometer measurements of the frequency response show a resonant frequency for the device at 1.3 kHz with the 3-dB cut-off frequency around 2.1 kHz. As a result the CCR can transmit data in excess of 4 kbps with a demonstrated range of 180 m.

For a 3.5 V actuation and a capacitance of up to 3 pF after pull-in, the average energy consumption is 16 pJ/bit. This compares quite favorably to other (RF) approaches such as Bluetooth, which has a fundamental transmission cost of 1 nJ/bit over a few 10s of meters.

### Solar Cells

As solar radiation is one of the most abundant sources of energy available for scavenging and is particularly amenable to a system that already needs line-of-sight for optical communication, solar cells were a natural choice for power. Furthermore, they are fairly compact, capable of efficiently generating multiple potentials, compatible with our other processes, and a well-developed technology compared to other energy harvesting techniques.

The solar cell array was fabricated on a 50µm device layer SOI wafer with a process that features back-filled electrical isolation trenches, front contacts for both n and p regions, a highly doped back-surface-field and an antireflective oxide coating. The SOI wafers were fabricated by bonding two wafers together then grinding and polishing the device layer back to the desired thickness. Before bonding, a highly doped p-type region was implanted into the p-type device wafer to create the back-surface-field, which improves the efficiency of the cells. Three implants form the solar cells: n- to create the large area p-n junction and n+ and p+ to allow a good ohmic contact to the aluminum collector lines. The isolation trenches are etched in an STS deep reactive ion etcher (DRIE), then lined with 5000Å of silicon nitride

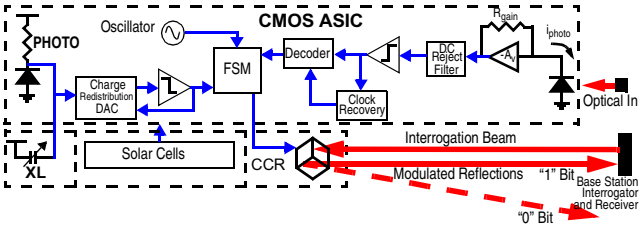


***Figure 7.*** *Detailed block diagram of the mote. The on-chip oscillator clocks the FSM, which directs the system through a demonstration of all mote functions, including sampling the photosensor and accelerometer, and transmitting both the sensor data and downloaded packets through the CCR. The accelerometer is functional but hasn't been incorporated into the mote yet.*

and filled with undoped LPCVD polysilicon. The isolation trenches allow a virtually unlimited number of cells to be connected in series—arrays of 200 cells with open circuit voltages of approximately 88 V have been demostrated.

The mote is powered by a 2.6 $mm^2$ solar cell array with multiple cell potentials: 1 V for the digital circuits, 1 V for the ADC (clean analog reference supply), 2 V for the receiver analog circuits, and 3-8 V (selectable) for the CCR. The cells in each bank were sized to meet their individual power requirements. For example, the cells for the CCR are 100 x 100 µm while the receiver analog supply cells are 500 x 500 µm. Solar illumination yields around 1 $mW/mm^2$ (1 $J/day/mm^2$) in full sunlight or 1 $\mu W/mm^2$ under bright indoor illumination. The solar cells are about 10-12% efficient, which allows the mote to function at light levels of approximately one sun.

### Controller (FSM)

The operation (Figure 7) of the mote is controlled by a 13-state finite state machine. It begins by toggling the sensor mux to select the next sensor to sample from and initiates the A/D conversion. Once the conversion is complete, the byte is sent serially to the CCR for transmission. Next, the most recent byte detected by the optical receiver is sent to the CCR; this echo allows us to verify the functionality of the receiver. Upon the completion of the transmission, the cycle repeats.

Transmissions can either occur asynchronously, wherein they are driven by a slow internal clock, or synchronously, in which each bit transmitted is triggered by the reception of a start flag delimiter from the interrogator. Synchronous transmission is advantageous when a base station is communicating with a large number of motes simultaneously as they will then all use the same time base. Both modes have been shown, but only the asynchronous mode has been demonstrated under solar power.

The ASIC is clocked by an integrated oscillator formed from a ring oscillator driven from a $V_{th}$-referenced weak inversion current source. The oscillator consumes 1.5 µW at

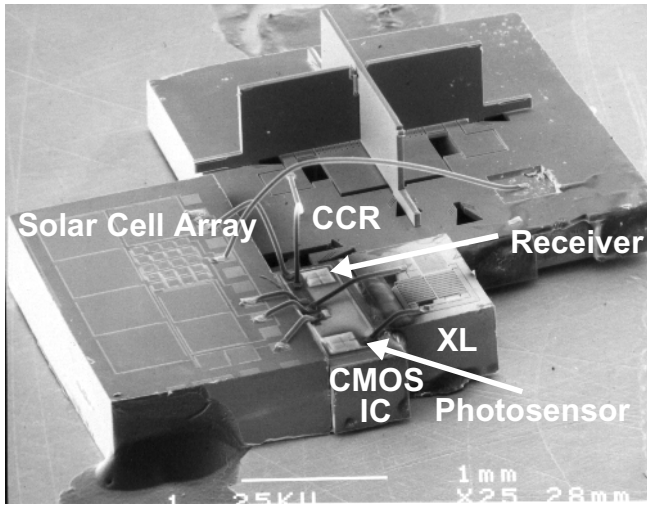


***Figure 9.*** *Scanning electron micrograph (SEM) of the 16 $mm^3$ mock-up shown in Figure 2. The solar cell sizes are adjusted to meet the power requirements of each of the four different sources. The accelerometer is an early version of that described in the text and shown in Figure 4.*

1V and 3.9 MHz and has a measured frequency variation of +0.8%/-1.8% with a ±10% variation in the 1V supply; however, it has significant variation with process spread.

## THE SYSTEM

All of the previously described components compose the sensor node system diagrammed in Figure 7 along with the interrogator. As shown by the dashed lines, the system is comprised of several die—accelerometer, solar cell array, CCR and 0.25µm CMOS ASIC (Figure 8). Currently, the system is hand assembled with conductive epoxy and wire bonds into an autonomous unit less than 16 $mm^3$ as shown in Figure 9. Such a device (sans accelerometer) has successfully sampled photosensor data and transmitted it over an optical link with the CCR using about one sun of illumination (Figure 10). The digital circuit consumed 28 µA at 0.76 V; the nominally 1 V solar supply drooped due to the load.

The mote is powered with 810 nm laser illumination, and a 660 nm laser is utilized for communication. A 750 nm

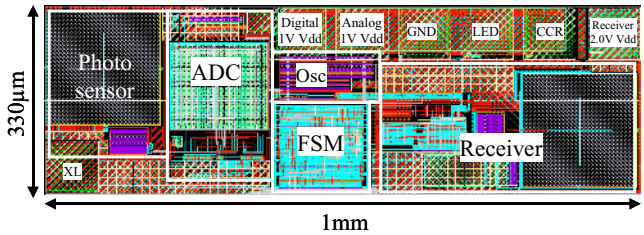


***Figure 8.*** *Annotated layout of the CMOS ASIC incorporating the oscillator, FSM, receiver, ADC, and photosensor. The pad on the bottom left is the input for the accelerometer or other off-chip sensor. External input voltages applied to this pad have successfully been digitized, but not from the accelerometer.*

short-pass filter (ground and diced to approximately 0.25 x 0.25 x 1 mm) was assembled over the receiver photodiode to pass the optical communication while blocking the illumination used for power. With this filter in place, successful optical reception in the presence of high intensity light has been demonstrated. Wire-bonding problems prevented the CCR from being integrated with this mote, however the CCR has been demonstrated in similar motes without the optical filter. For future devices laser lift-off [14] will be attempted to remove the thin-film filter from the thick fused silica substrate.

A new DRIE SOI/CMOS process is in development that will integrate the solar cells, CCR, capacitive accelerometer and high voltage FETs for driving electrostatic actuators on a single chip. Individual functionality of the solar cells, CCR, and accelerometer has been demonstrated to various degrees, but more process development is necessary. When successful, this new process will yield a 6.6 $mm^3$ mote using only two die.

## CONCLUSION

Pushing forward the frontiers of system integration, miniaturization, and energy consumption, an autonomous solar-powered sensor node with optical communication has been demonstrated in less than 16 $mm^3$. The mote digitizes signals from a photosensor, transmits the data over a long distance optical link, and echoes received data packets in a one-to-many network configuration. Future motes will be smaller through higher levels of integration, have more functionality by means of fully programmable controllers, and incorporate more types of sensors.

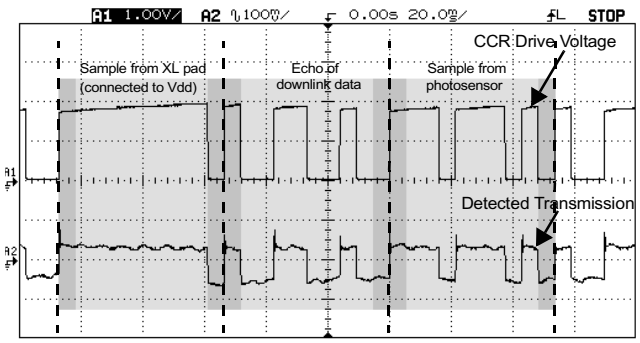


***Figure 10.*** *End-to-end communication and sensing. Shown above are three data packets transmitted from the mote and received via a photodiode detector 1.5 meters away. Start ("1") and stop ("0") bits from each packet are highlighted. The mote is powered from the solar cell array under illumination of roughly one sun. The first packet is an ADC sample of the accelerometer input pad, which was connected to Vdd. The second packet is an echo of a byte from the receiver. The final packet is a sample from the on-chip photosensor. The asynchronous transmit data rate is approximately 183 bps.*


## ACKNOWLEDGEMENTS

The authors would like to thank Al Molnar for adding hooks facilitating the asynchronous communications mode and Seth Hollar for developing the new process. This work was funded by DARPA/MTO with support from the Howard Hughes Doctoral Fellowship program and the Fannie and John Hertz Foundation.


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