An Efficient BICS Design for SEUs Detection and Correction in Semiconductor Memories

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Abstract

In this paper we propose a new Built in Current Sensor (BICS) to detect single event upsets in SRAM. The BICS is designed and validated for 100nm process technology. The BICS reliability analysis for process, voltage, temperature, and power supply noise are provided. This BICS detect various shapes of current pulses generated due to particle strike. The BICS power consumption and area overhead are also provided. This BICS found to be very reliable for process, voltage and temperature variation and under stringent noise conditions.

1. Introduction

Memories occupy the largest block of area in modern ICs. In addition, memories are more sensitive to failures than logic, and this includes both hard and soft (transient) failures. Thus memories involve the largest amount of failures in modern ICs, becoming the major cause for reliability problems. One of the main causes of reliability reduction comes from particle strikes that create *soft errors*, also referred as SEUs (single event upsets) [7, 11, 5]. With past technologies, this problem was limited to radiation hostile environments like in space. However, with very-deep-submicron technologies (VDSM), aggressive device size and power supply reductions have impacted severely circuit sensitivity, as they reduced aggressively the critical charge of memory cells. Thus, low energy particles can flip memory cells, making memories sensitive to atmospheric neutrons as well as to alpha particles created by unstable isotopes that can be found in the materials of a chip. Thus, soft errors are today a concern even at ground level, at least for those applications where reliability is an important attribute. To maintain acceptable reliability levels in memories, Error Correcting Codes (ECC) are often used to detect and correct SEUs. But ECCs may cause significant area, performance and power dissipation penalties. Also, ECC only detects and corrects the error at the time the faulty word is being read, and not when it occurs. In large memory systems, there can be a long latency between the occurrence of the SEU and the error correction, which can cause accumulation of SEUs, can invalidate the error detection and correction capabilities of ECC.

To cope with these drawbacks, an approach using asynchronous Built in Current Sensor (BICS) on the vertical power lines of a memory and parity bit per memory word was used in [3]. The BICS is asynchronous, since the occurrence of particle strikes is random in time. This makes the BICS design more difficult than synchronous BICSs proposed for detecting permanent faults. During a particle hit that flips a memory cell, the BICS placed on the power lines feeding the cell detect the abnormal current dissipation, and locates the faulty column. The parity bit allows locating the faulty word and correcting the error. Because SEUs are detected as soon as they occur, error detection latency is eliminated. At the same time, the area overhead is reduced drastically with respect to ECC (since we use a single parity bit per memory word, and a single BICS for every two memory columns. Further, speed penalty is eliminated, since we do not need to check the read data at each read cycle. The work in [3], uses a BICS that induces a 300mV voltage drop on the Vdd and 400mV on the Gnd lines. This sensor was designed with an old technology and its operation was not validated for voltage, temperature and process variations and for different shape of current pulses.

The aim of this work is to propose a new BICS which is designed for current CMOS process (100nm), operates reliably under wide voltage, temperature, and process variations, as well as stringent noise conditions. At the same time, the new BICS is also smaller than the previous one, and dissipates less power. Another important characteristic is that the voltage drop induced by the new BICS on the Vdd and Gnd lines is only 7.5mV and 8.5mV, respectively. Thus, the new BICS will not affect the noise margins of the memory, which is not the case for the old one. Note also

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that these characteristics make our BICS approach practical, while this is not a case in earlier BICS approaches monitoring logic parts [13]. The reason is that in logic parts a large number of gates switch concurrently, creating a huge transient current. This results in a high voltage drop and noise in the power supply making the BICS impractical. Solutions using a BICS per a small number of gates are also impractical, due to the high area cost. In contrast, in our approach, only one memory cell can be active per memory column, resulting on a small transient current and a small voltage drop.

This paper is divided into following sections. Section 2 discusses about the SEUs in SRAM cell. Section 3 discusses proposed new BICS to detect SEUs in SRAM in contrast with BICS of [3]. Section 4 discusses the simulations mechanism and SPICE simulation results when different shapes of current pulses are injected at the sensitive node of the memory cell. Section 5 describes BICS reliability for process, voltage and temperature variations and power supply noise. This section also discusses about the power dissipation of BICS. Section 6 presents comparisons between new BICS and BICS of [3]; we conclude in section 7.

2. Single Event Upsets in SRAM

A Single Event Upset (SEU) in the SRAM cell occurs when a charged particle strikes at the sensitive node and flips the state of the SRAM cell. These charged particles are present in the space environment as cosmic rays and also within the chip as α-particles. With advanced silicon technologies, SEUs can also be created at ground level by secondary particles created during the interaction of atmospheric neutrons with die materials. The α-particles are emitted due to the radioactive decay of uranium and thorium impurities present in the chip materials and interconnects. SEUs in the memory cause logic error as they change the logic value stored in the cell by flipping it from 1 to 0 or 0 to 1. The is temporary i.e. the cell is not permanently damaged and it can be rewritten in the next memory write cycle.

Every memory cell has two sensitive nodes, the drain of the OFF-NMOS transistor and drain of the of the OFF-PMOS transistor. The drain and substrate of the OFF-transistor create a reverse-biased junction. The reverse-biased junctions of the cell are most sensitive nodes to the particle strike. Immediately followed by the particle strike, charges generation and collection occur. Electrons and holes are generated when the particle passes through the depletion region formed between the drain and substrate of the OFF-transistor. The generated charges are collected at the opposite voltage terminals of the reverse-biased junction i.e. electrons move towards positive voltage and holes move towards negative voltage. The movements of charges cause a current pulse at the struck node. The memory cell flips when the collected charge, Q, is more than the charge stored at the struck node. The minimum charge required to flip the cell is called Q_{crit}. The Q_{crit} not only depends on the collected charge but also on the shape of the current pulse. The current pulse is represented by an equivalent current source between the drain and the substrate of the transistor [10, 8, 2, 9, 14, 6].

A 1 to 0 flip is defined as when a particle strike discharges the charge stored at the drain of the OFF-NMOS transistor, and similarly 0 to 1 flip is defined as when a particle strikes at the drain of the OFF-PMOS transistor. As technology scales down, the charge stored at the sensitive nodes of the memory cell is reduced because $Q_{node} = C \times Vdd$ making SRAM more prone to soft errors.

3. New Built in Current Sensor

Figure 1 shows the BICS used in [3]. This BICS is a high-speed current-mode comparator which detects transient current pulses and provides logic level output to set the asynchronous latch. This BICS is composed of two current comparators and an asynchronous latch. The comparator I_{UH} is symmetrical counterpart of the comparator I_{UL}. The fundamental operation of the BICS is based on the current controlled current switches. The transistor T_{L1} in I_{UL} comparator is turned off when upset current I_{UL} flows into the source of this transistor. Similarly, the upset current I_{UH} causes to turn off transistor T_{H1}. Turning off these transistors under the upset current flow is very sensitive to process, voltage and temperature variations making the BICS very sensitive to these variations. This BICS also reduces the noise margins of the memory cell as it causes voltage drop around 300mV on Vdd and 400mV on Gnd lines.

To overcome these limitations, we have designed a new BICS which uses current mirror and current source load inverter to amplify the upset current pulse and convert it into logic level voltage pulse. Figure 2 depicts the new BICS, $Svdd$ in this figure is a 1 to 0 flip detector which detects and amplifies a transient current pulse generated due to 1 to 0 flip and provides logic level voltage pulse. For 0 to 1 flip detection, $Sgnd$ is used which is a symmetrical counterpart of $Svdd$. The logical pulses provided by $Svdd$ and $Sgnd$ are used to set an asynchronous latch. The BICS provides Vdd' and Gnd' for the whole column of the memory cell.

$Svdd$ is formed using transistors M_{V1} - M_{V8}. Transistors M_{V1} and M_{V2} forms a n-channel current mirror and M_{V7} with M_{V8} makes current source load inverter. Transistors M_{V5} and M_{V6} are the source resistors for the current mirror. The source current for the current mirror and current source load inverter is provided by transistors M_{V3}, M_{V4} and M_{V8}. The biasing voltage for transistors M_{V3},

M_{V4} and M_{V8} is provided by the reference voltage generator which is common for 8 or 16 BICS. The reference voltage generator is a simple CMOS voltage divider which provides two levels of biasing voltage, B_V and B_G for $Svdd$ and $Sgnd$ respectively. This reference voltage generator is used for ensuring correct BICS operation under power supply variations. It decreases or increases the output biasing voltage when Vdd decreases or increases.

When a particle strikes at the drain of OFF NMOS-transistor of the SRAM cell it causes a transient current pulse at the struck node. The current flows from the Vdd to the struck node through the complementary ON PMOS-transistor which is shown as I_V. As I_V flows from Vdd to the struck node, the current through transistor M_{V1} decreases. It results to a decrease of the current flowing through M_{V2}, and thus to the increase of the voltage drop between drain and source of M_{V2}. The drain of M_{V2} is connected to the gate of M_{V7}, so the difference between gate to source voltage of M_{V7} increases, which results in a voltage pulse at the drain of M_{V7}. This voltage pulse is again amplified to the full logic level at node E_V by the inverter formed by transistors M_{V9} and M_{V10}. Similarly $Sgnd$ provides a voltage pulse at node E_G when particle strikes at the drain of OFF PMOS-transistor. The signals $Bypass_{vdd}$ and $Bypass_{gnd}$ are used to disable the BICS operation during memory write and read operations.

The outputs E_V and E_G of $Svdd$ and $Sgnd$ respectively are connected to the asynchronous latch. If any of the two outputs goes high, the latch is triggered and it activates the Err_i signal. A reset signal is used to reset the asynchronous latch after the upset is detected and information is read from the latch for correction.

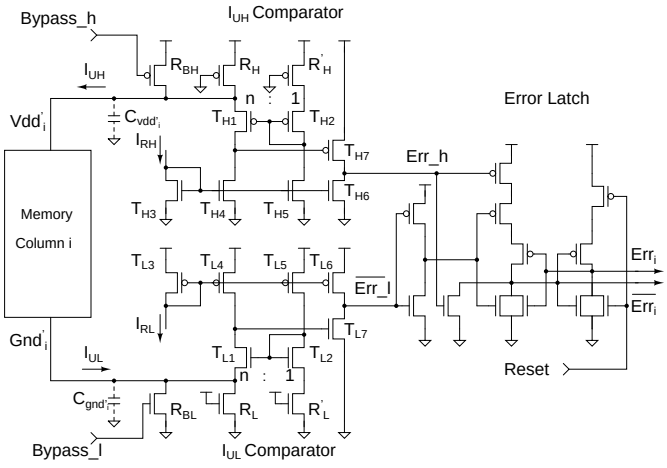

Figure 1. BICS proposed in [3]

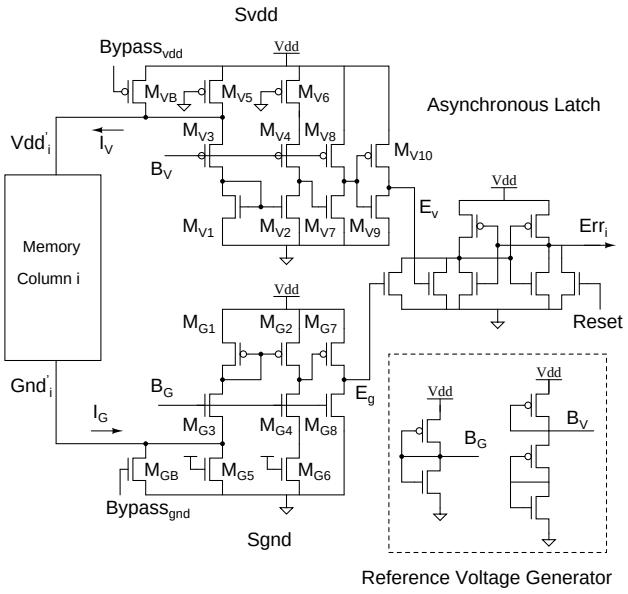

Figure 2. New BICS

4. Simulation Mechanism and Results

The BICS and memory cell was designed in 100nm process technology. The power supply voltage for this technology was used as 1.2v and the SPICE parameters were obtained from [1, 4]. The layout design rules were scaled to this technology according to MOSIS layout rules for $0.18\mu m$ technology.

In CMOS circuits SEUs are modeled by injecting a current pulse at the sensitive node. This pulse has rapid rise time and gradual fall time. The shape of the pulse can be approximated by the following equation proposed in [12].

$$I_\alpha(t) = \frac{Q}{t_f - t_r} \times (e^{\frac{-t}{t_f}} - e^{\frac{-t}{t_r}}) \quad (1)$$

Where Q is the charge collected due to the particle strike and t_r is the time constant for initially establishing the ion track, usually assumed few pico seconds (<10ps) [9], t_f is the decay time of the current pulse. In SPICE simulations, we vary both Q and t_f and observe additional delay due to the α-particles strike at the output of the circuits. we are assuming t_r = 5ps. Figure 3 shows the shape of the injected current pulse for different values of Q and t_f with $t_r = 5ps$ For SPICE simulations, a BICS is placed at the end of the memory column. The BICS feeds power to the whole column of 128 memory cells. For 1 to 0 flip simulations, a current source is used between the drain of the OFF-NMOS transistor and the ground which applies current pulse of equation 1. Similarly for 0 to 1 flip simulations, the current source is used between Vdd and drain of OFF-PMOS transistor.

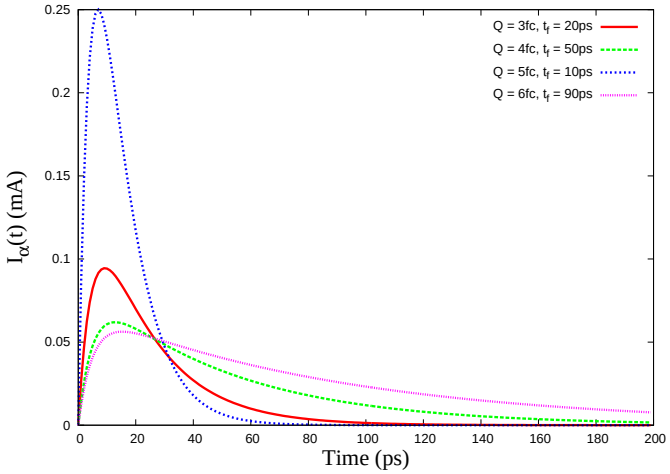

Figure 3. The shape of the current pulse for different values of Q and t_f

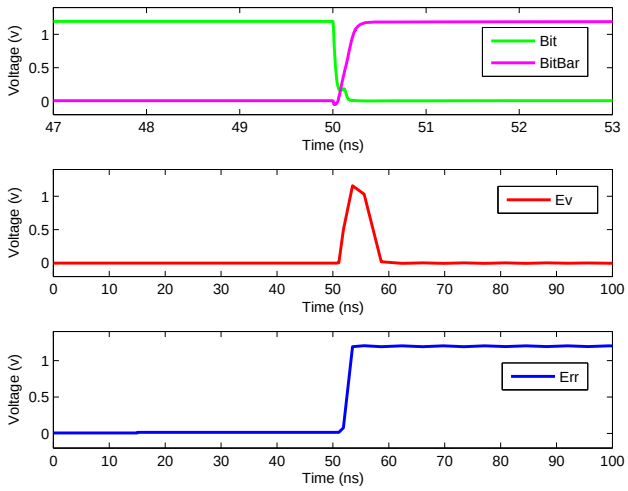

Figure 4. SPICE simulation results for 1 to 0 flip for Q = 3fC and t_f = 30ps

4.1. Simulation Results

Figure 4 shows the SPICE simulation results for 1 to 0 flip which occurred at 50ns. The top chart shows that the memory cell flips when a current pulse is injected at the drain of OFF-NMOS transistor. This current pulse was generated using equation 1 for Q = 3fc and t_f = 30ps. In this case, the particle strike flips the memory cell and the flip is detected by $Svdd$ part of the BICS. The middle chart shows logic level output (E_V) of $Svdd$. The voltage pulse produced at the output of $Svdd$ is latched in the asynchronous latch as shown in the bottom chart. Similar results were obtained for 0 to 1 flips, these results are tabulated in tables 1 and 2 for various shapes of injected current pulses. The simulation results for 1 to 0 pulses, are shown in table 1. The first column shows the amount of collected charge, Q. For every value of Q, decay time t_f is varied between 10ps and 100ps using a step of 10ps. As said earlier t_r is selected to be 5ps, we could vary this time from 2ps to 6ps to be sure that we cover all practical situations, but the variation of t_r in such a narrow range does not affect the results. The diamonds in table 1 show the case when a particle hits a cell but the cell does not flip and the particle hit is not detected. The Stars show the case when a particle hits a cell but the cell does not flip and particle hit is detected. The triangles show the case when a particle strike flips the cell and is detected by the $Svdd$ part of the BICS. The simulation results for 0 to 1 flip, i.e. when the particle hit at the drain of the OFF-PMOS transistor, are shown in Table 2.

We have not found current pulses that can flip the cell but the current sensors do not detect the event. Thus, the BICS scheme is very efficient for SEU detection, as we do not observe escapes. However, we observe that in some situations we have false alarms, as the BICS detects the particle hit, but the hit does not flip the cell. These false alarms could create a problem if we mis-correct a correct cell, thus creating an error. However, this situation cannot happen because no parity bit will detect an error, thus no mis-corrections will be performed.

Q (fC)	Decay time, t_f, (ps)									
	10	20	30	40	50	60	70	80	90	100
2	★	♦	♦	♦	★	★	★	★	★	★
3	▲	▲	▲	▲	▲	★	★	★	★	★
4	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
5	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲

▲ -Flip and detected
★ -No flip but detected
♦ -No flip and no detection

Table 1. Simulation results for 1 to 0 flip

5. BICS Reliability Analysis

5.1. Process, Voltage and Temperature (PVT) Analysis

To emulate the effect of the process variation the SPICE simulations were run for Vtn $\pm 10\%$, and Vtp $\pm 10\%$, where Vtn and Vtp are the threshold voltages of NMOS

Q (fC)	Decay time, t_f, (ps)									
	10	20	30	40	50	60	70	80	90	100
3	♦	♦	♦	♦	♦	★	★	★	★	★
4	▲	★	★	★	★	★	★	★	★	★
5	▲	▲	★	★	★	★	★	★	★	★
6	▲	▲	▲	★	★	★	★	★	★	★
7	▲	▲	▲	▲	★	★	★	★	★	★
8	▲	▲	▲	▲	▲	★	★	★	★	★
9	▲	▲	▲	▲	▲	▲	★	★	★	★
10	▲	▲	▲	▲	▲	▲	▲	★	★	★
11	▲	▲	▲	▲	▲	▲	▲	▲	★	★
12	▲	▲	▲	▲	▲	▲	▲	▲	▲	★
13	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
14	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲

▲ -Flip and detected
★ -No flip but detected
♦ -No flip and no detection

Table 2. Simulation results for 0 to 1 flip

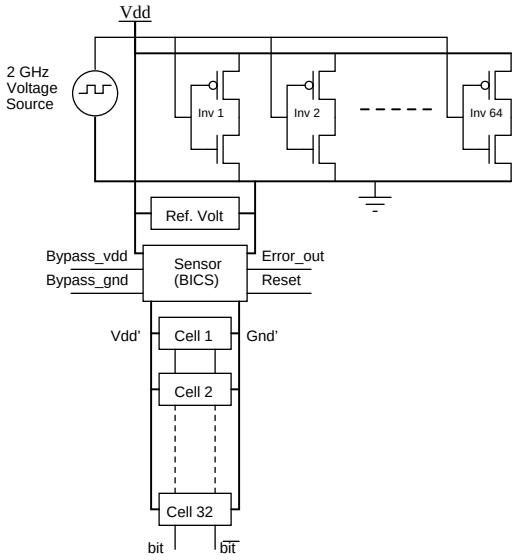

Figure 5. Simulation setup for the noise analysis of the BICS

and PMOS transistors, respectively. The Vdd was also varied from 1.08 to 1.32 volt where nominal Vdd was 1.2 volt. The temperature range was -25 to 85 C. The BICS was found to work perfectly for all these variations.

5.2. Power Supply Noise analysis

To emulate the noise in the power supply, 64 inverters (very large in size) were switched simultaneously by a voltage source of 2GHz frequency. Figure 5 shows the simulation setup for the noise analysis. A common Vdd and Gnd were used for the inverters, the reference voltage generator and the BICS which assures that the noise generated by the inverters propagates to the reference voltage generator and BICS. 64 inverters were chosen as they produced good amplitude of noise current in the Vdd. The absolute value of this noise current was around 600mA. The SPICE simulations showed that BICS works perfectly under this noisy environment.

5.3. Power Dissipation Analysis

The power dissipation of BICS under nominal voltage and temperature is 11.32μW for the typical process parameters. Table 3 shows the power dissipation of the sensor at room temperature (T = 27C) for various process and Vdd variations. The first column shows Vdd variations in the range of $\pm 10\%$. The subsequent columns show 5 process variations combining typical, slow and fast transistor characteristics.

Vdd(v)	Power dissipation (μW)				
	TT	SS	FF	SF	FS
1.08	6.15	4.43	8.48	6.77	5.65
1.2	11.32	8.41	15.08	12.45	10.34
1.32	19.27	14.67	24.95	21.16	17.58

TT - Typical NMOS, Typical PMOS
SS - Slow NMOS, Slow PMOS
FF - Fast NMOS, Fast PMOS
SF - Slow NMOS, Fast PMOS
FS - Fast NMOS, Slow PMOS

Table 3. Power dissipation for voltage and process variations

From this table and given that the BICS was designed to monitor 256 memory cells in a column and one BICS is used for two columns, we can find that the extra power dissipation due to BICS for the memory. For example, for 1 Mbit SRAM architecture with 256 rows and 4096 columns, 2048 BICSs will be required so the power penalty for typical process will be 23.18 mW.

6. Comparisons

Table 4 shows the comparisons between our proposed BICS and one given in [3]. Our proposed BICS causes to reduce the noise margins in Vdd and Gnd lines only 8.5mV and 7.5mV respectively which is $<$1% of 1.2v Vdd where as BICS in [3] reduces noise margins around 6 % and 8% respectively for 300mV and 400mV for 5v Vdd. It is to be noted that in table 4, some entries are marked as no-data. In that case the authors in [3] have not provided data. The biasing for the new BICS is based on voltage biasing where as for BICS in [3] is based on current biasing. The current based biasing needs a constant current source on the chip which is additional overhead and also cause power dissipation. The voltage based biasing in new BICS, makes it more reliable as it is easy to create biasing voltage and if the Vdd varies, the biasing voltage varies so the BICS still keeps working. The number of transistors in new BICS are 27 where as for BICS in [3] are 34, so the area overhead of new BICS is smaller than the BICS in [3] The BICS in [3] wasn't validated for PVT, noise and current shape analysis. We have also shown power consumption by BICS for various supply voltages and process variations.

Type	new BICS	BICS in [3]
Noise Margins	8.5mv, 7.5mV	300mV, 400mV
Biasing	Voltage	Current
Number of Transistors	27	34
PVT analysis	Yes	No-data
Power supply noise analysis	Yes	No-data
Validated for different shape of current pulses	Yes	No-data
Power consumption analysis	Yes	No-data

Table 4. Comparisons between new BICS and BICS of [3]

7. Conclusion

We have proposed a new Built in Current Sensor (BICS) to detect single event upsets in SRAM. The BICS was design and validated for 100nm process technology. The PVT and power supply noise analysis shows that BICS is reliable in harsh environment. We have provided data for power consumption by BICS and detection of different shape current pulses. The proposed BICS shows many advantages over BICS proposed in [3].

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