An Efficient Signal Processing Scheme Using Signal Compression for Software GPS Receivers

Deuk Jae Cho, Deok Won Lim, Chansik Park, and Sang Jeong Lee*

Abstract: The software GPS receivers based on the SDR technology provide the ability to easily adapt the other signal processing algorithms without changing or modifying the hardware of the GPS receiver. However, it is difficult to implement the software GPS receivers using a commercial processor because of the heavy computational burden for processing the GPS signals in real-time. This paper proposes an efficient GPS signal processing scheme to reduce the computational burden for processing the GPS signals in the software GPS receiver, which uses a fundamental notion compressing the replica signals and the encoded look-up table method to generate correlation values between GPS signals and replica signals. In this paper, it is explained that the computational burden of the proposed scheme is much smaller than that of the typical GPS signal processing scheme. Finally, the processing time of the proposed scheme is compared with that of the typical scheme, and the improvement in the aspect of the computational burden is also shown.

Keywords: Compression, correlation, GPS, look-up table, processing time, SDR.

1. INTRODUCTION

Recently, the GPS (Global Positioning System) receiver design using SDR (Software Defined Radio) technology has been performed by many researchers. The SDR technology permits the communication schemes to be modified easily because the digital processing part is implemented by the software. Therefore, a great deal of work has been reported to design systems using SDR technology in the field of communication systems as well as GPS [1-3]. The software GPS receiver has no need to change the hardware in the case of adapting the advanced algorithms or processing schemes to another communication system. It has the benefits of flexibility and reconstruction, which are weak points of the previous GPS receiver implemented by hardware. However, the software GPS receiver is currently hard to implement in real-time because the commercial processor needs to handle a large amount of data to implement the multiple correlators for GPS signals [3,4]. In the software GPS receiver to be implemented currently, the RF/IF (Radio Frequency /Intermediate Frequency) part still converts the GPS signals into the quantized IF signals by the hardware. But the subsequent signal processing is performed by the software.

This paper proposes an efficient signal processing scheme to reduce computational burden in the software GPS receiver. The signal processing scheme can compute the correlation value of 4-samples of IF signal at once through the compressed replica signals and the encoded look-up table method.

Section 2 explains the problems of the typical GPS receivers in a point of the software GPS receiver. Section 3 describes the proposed signal processing scheme to reduce computational load efficiently. Section 4 presents some performance results regarding the processing time. Finally, summary and concluding remarks will be given.

2. TYPICAL SIGNAL PROCESSING SCHEME OF THE GPS RECEIVER

The typical GPS receiver consists of antenna, RF/IF part, digital signal processor and micro-processor as shown in Fig. 1. Among these, the role of the RF/IF part is to convert the GPS signals into the quantized

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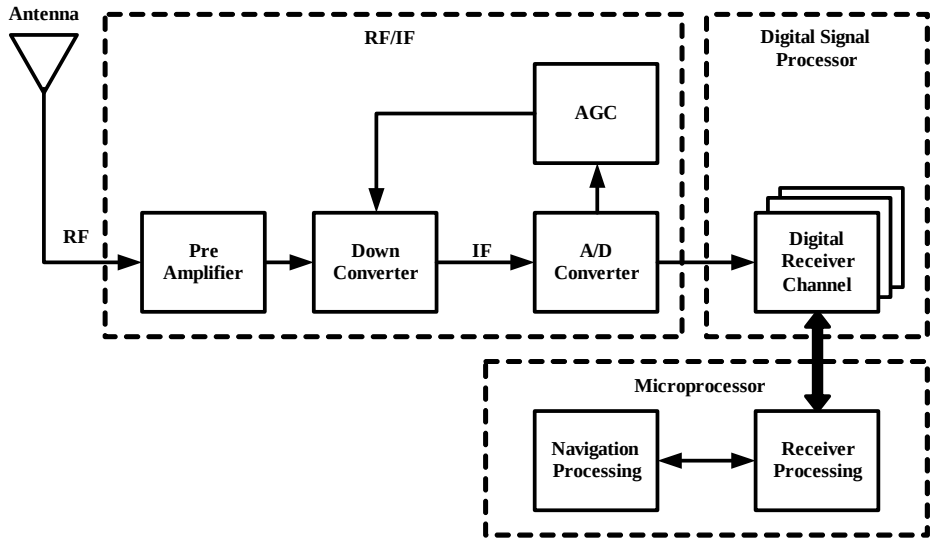


Fig. 1. Typical GPS receivers.

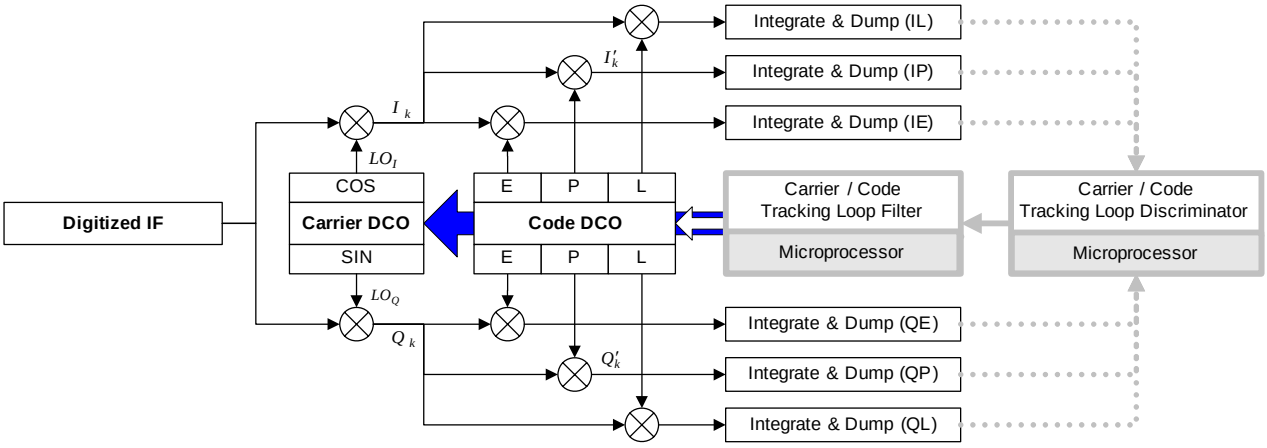


Fig. 2. Structure of the typical digital signal processor.

IF signals. These signals are transferred to the digital signal processor. The main function of the digital signal processor is to wipe off the carrier and code from the IF signals, and gives the error signals to tracking loops for synchronization [5,6]. These error signals are different according to the type of discriminator.

Generally, a digital signal processor gives in-phase correlation values and quadrature-phase correlation values to the carrier tracking loop, as well as early code correlation values and late code correlation values. Furthermore, it gives a code phase to measure pseudorange from the GPS satellite to the GPS receiver. To perform these functions, a structure of the typical digital signal processor is shown in Fig. 2.

The in-phase carrier replica, LO_I in Fig. 2 is given by

$$LO_I = \cos[2\pi f_r t_k + \phi_{rk}]. \tag{1}$$

And the in-phase carrier mixer output, I_k is given by

$$I_k = \frac{1}{2} A_k C_k D_k \cos[2\pi(f_{IF} - f_r)t_k + \phi_k - \phi_{rk}] + \frac{1}{2} A_k C_k D_k \cos[2\pi(f_{IF} + f_r)t_k + \phi_k + \phi_{rk}], \tag{2}$$

where f_r and ϕ_{rk} are the frequency and the phase of the in-phase carrier replica, respectively.

The in-phase code mixer output, I'_k is determined by multiplication of the in-phase carrier replica, LO_I is given by (1) and the in-phase carrier mixer output, I_k is given by (2), such that

$$I'_k = \frac{1}{2} A_k C_k C_{rk} D_k \cos[2\pi(f_{IF} - f_r)t_k + \phi_k - \phi_{rk}] + \frac{1}{2} A_k C_k C_{rk} D_k \cos[2\pi(f_{IF} + f_r)t_k + \phi_k + \phi_{rk}], \tag{3}$$

where C_{rk} is the C/A (Coarse/Acquisition) code.

The accumulator, I_Σ accumulates the code mixer

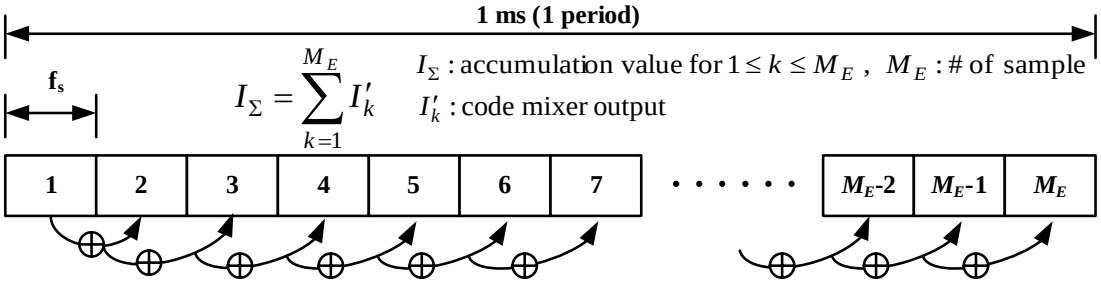


Fig. 3. Concept of the typical signal processing scheme.

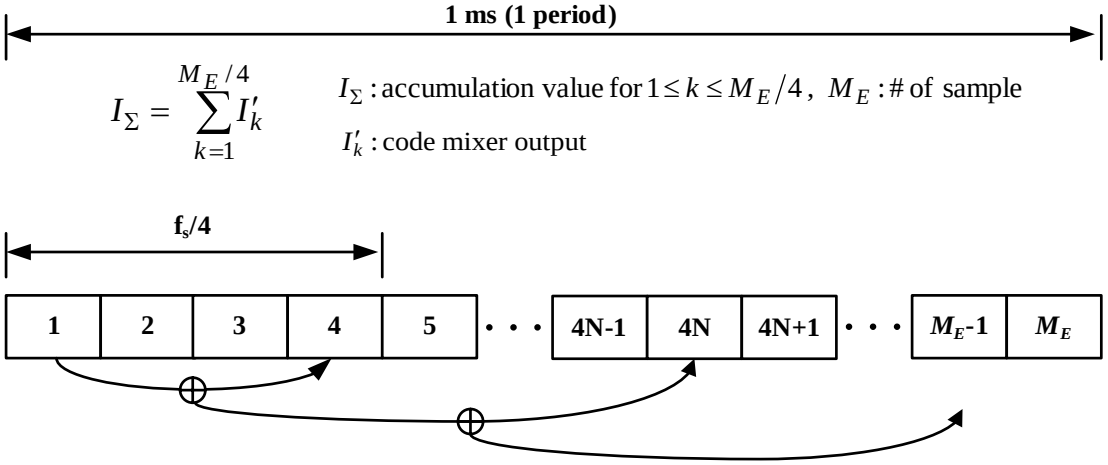


Fig. 4. Concept of the proposed signal processing scheme.

output during the period of the C/A code, and is given by

$$\begin{aligned} I_\Sigma &= \sum_{k=1}^{M_E} I'_k \\ &= \frac{A}{2} M_E \frac{\sin(\pi \Delta f_\Sigma T)}{\pi \Delta f_\Sigma T} R(\tau_\Sigma) D_\Sigma \cos(\Delta \phi_\Sigma), \end{aligned} \tag{4}$$

where T is the period of the C/A code, M_E is the number of samples for T, f_Σ is the frequency error, τ_Σ is the time difference between the input C/A code and the replica C/A code, and $R(\tau_\Sigma)$ is the auto-correlation function of the C/A code, and is given by

$$R(\tau) = \begin{cases} 1 - |\tau|, & |\tau| \le 1 \\ 0, & |\tau| > 1. \end{cases} \tag{5}$$

The typical digital signal processor mixes the IF signal with the replica signal and accumulates the mixed signals during the period of the C/A code [5]. If the 5.714MHz (f_s) sampling frequency is used, the accumulator (I&D, Integrate & Dump) should sum up the 5,714 values (M_E) for 1-milisecond as shown in Fig. 3. In other words, the digital signal processor should handle one sample every 175-nanoseconds.

As a result, the software implemented GPS receiver executes 548,544 multiplications and 411,408 summations in 1-milisecond to operate the 12-channel correlators as given by

- Multiplications for 1ms: 5,714 (samples) × 8 (multi-plication/channel) × 12 (channels)= 548,544
- Summations for 1ms: 5,714 (samples) × 6 (I&D/ channel) × 12 (channels)= 411,408.

3. PROPOSED SIGNAL PROCESSING SCHEME

The proposed digital signal processor collects four IF sample signals and accumulates them with replica signals at once. Namely, the proposed digital signal processor uses a look-up table method with multi-bit processing scheme to generate correlation values between several GPS signals and replica signals at once. Hence, the computational burden is reduced effectively as much as the typical digital signal processor by processing the 4-samples at once. The proposed signal processing scheme is presented in Fig. 4.

Fig. 5 shows the major difference of the proposed digital signal processing scheme in software and the typical digital signal processing scheme in hardware.

As mentioned above, the structure of the proposed

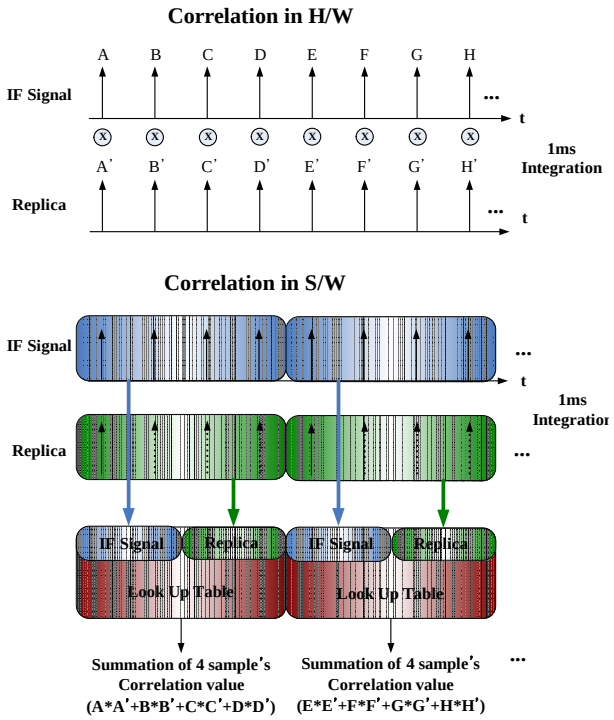


Fig. 5. Mechanism comparison of the digital signal processor.

digital signal processor is shown in Fig. 6. The proposed digital signal processor collects input IF sample signals by the Serial-to-Parallel Control block, and concatenates them along with replica signals as a type of multi-bit. Lastly, the proposed digital signal processor determines correlation values by using the encoded look-up table from the multi-bit. Namely, the software GPS receiver proposed in this paper executes 102,852 summations only without any multiplications in 1-milisecond to operate the 12-channel correlators.

The carrier replica and the code replica proposed in this paper are generated by adopting a fundamental notion of the DCT (Discrete Cosine Transform) used primarily in image compression. That is, the basic concept of the carrier and the code replica generation

Table 1. I/Q phase according to the carrier DCO phase.

DCO Phase	In-Phase	Quadrature-Phase
000	1	2
001	2	1
010	2	-1
011	1	-2
100	-1	-2
101	-2	-1
110	-2	1
111	-1	2

is that changes between the neighboring IF samples are small; the replica patterns are concentrated on the low frequency. More accurately, the replica signals designed in this paper are patterns generated frequently every sampling frequency.

The digital signal processor generates four types of the in-phase carrier replica and the quadrature-phase carrier replica, ± 1 and ± 2. The number of carrier patterns for processing 4-samples at once using four types of the carrier replica is all 256 types.

Generally, the carrier output for the N-digital IF sample is given by

$$LO_{I_N} = \sum_{n=1}^{N} \cos[2\pi f_r t_k + \phi_{rk+\mathrm{mod}([n-1]\times 2,8)}], \qquad (6)$$

where $\mathrm{mod}([n-1]\times 2, 8)$ means the residual of $[n-1]\times 2$ divided by eight.

In case of N=1, (6) identifies (1).

In (6), the phase, $\phi_{rk+\mathrm{mod}([n-1]\times 2,8)}$ is determined by the carrier DCO (Discrete Controlled Oscillator) phase. That is, the in-phase and the quadrature-phase are given according to the carrier DCO phase as indicated in Table 1.

In case of N=4, from (6) and Table 1, if the carrier DCO phase is '001', then it can be estimated that the current value of the In-Phase is to be '2' and the next three values are to be '1, -2, -1' with a 92% probability.

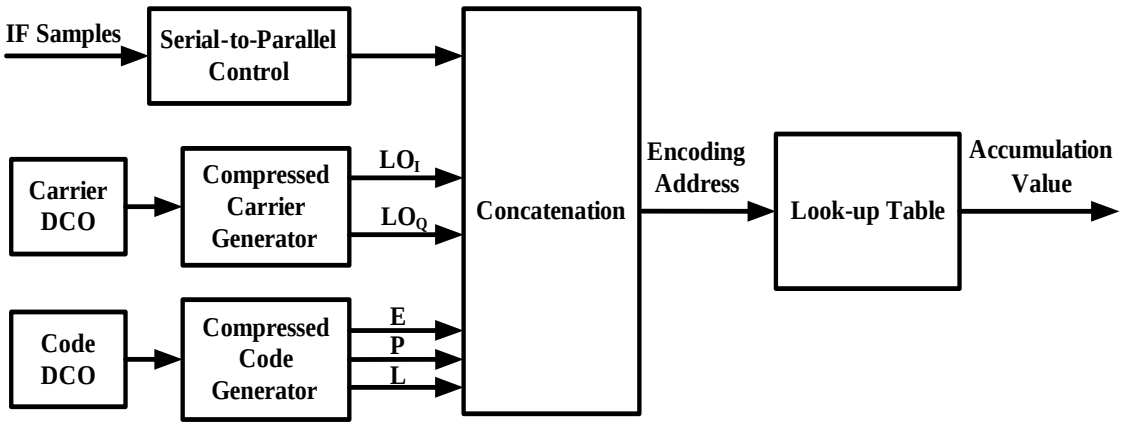


Fig. 6. Structure of the proposed digital signal processor.

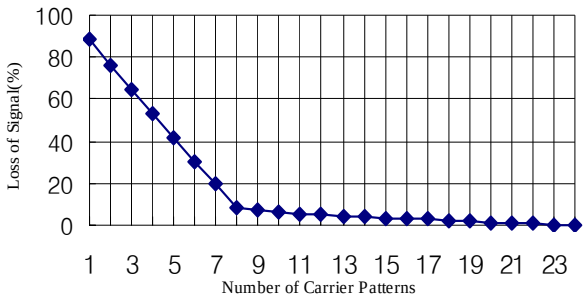


Fig. 7. Probability of the signal loss due to the number of carrier patterns.

Table 2. Carrier patterns and the encoding values.

Carrier Pattern				3-bits encoding value		
-2	-1	2	1	0	0	0
-2	1	2	-1	0	0	1
-1	-2	1	2	0	1	0
-1	2	1	-2	0	1	1
1	-2	-1	2	1	0	0
1	2	-1	-2	1	0	1
2	-1	-2	1	1	1	0
2	1	-2	-1	1	1	1

For the above reason, it is able to make the patterns of the carrier replica, and the optimum number of patterns is set to be eight (see Fig. 7). The 3-bits encoding values according to the carrier pattern are shown in Table 2.

In case of the code replica generation, the relation between the code phase and the sampling frequency is important. That is, the code pattern is determined by the number of the C/A code to be sampled by the sampling frequency according to the code phase. The digital signal processor generates two types of the code replica, ± 1. The number of code patterns for processing 4-samples at once using two types of the code replica is all 8 types, since the patterns like '1 -1 1 -1' cannot occur absolutely. The code patterns are presented in Table 3.

Table 3. Code patterns and the encoding values.

Code Pattern				3bits encoding value		
-1	-1	-1	-1	0	0	0
-1	-1	-1	1	0	0	1
-1	-1	1	1	0	1	0
-1	1	1	1	0	1	1
1	1	1	1	1	0	0
1	1	1	-1	1	0	1
1	1	-1	-1	1	1	0
1	-1	-1	-1	1	1	1

Table 4. IF signal patterns and the encoding value.

IF Signal Pattern				8bit encoding value			
-1	-1	-1	-1	00	00	00	00
-1	-1	-1	-3	00	00	00	01
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
3	3	3	1	11	11	11	10
3	3	3	3	11	11	11	11

Table 5. An example of the proposed signal processing scheme.

Encoding Bit (14Bit)	11111110		010		010
IF bit (8Bit)	11111110	3	3	3	1
Carrier Bit (3Bit)	010	-1	-2	1	2
Code Bit (3Bit)	010	-1	-1	1	1
Accumulation Value	3 + 6 + 3 + 2 = 14				

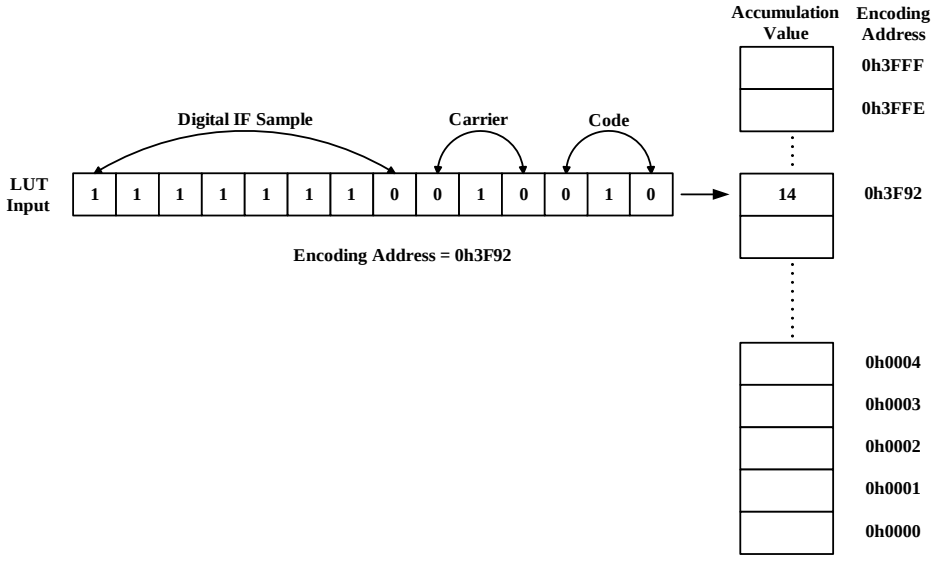


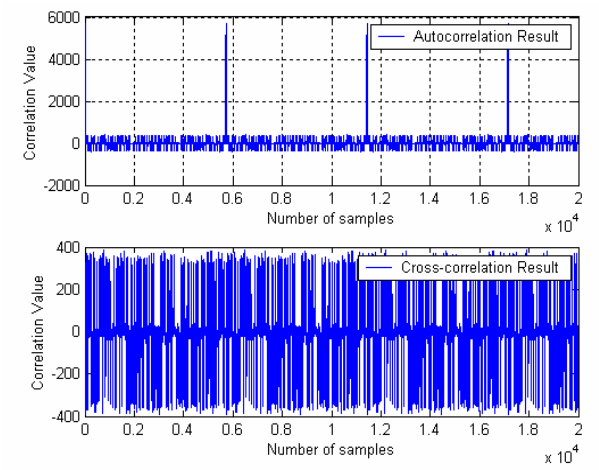
Fig. 8. An example of the proposed signal processing scheme.

The patterns of the IF signal and those encoding values are shown in Table 4. It adapts the encoding method composed of the sign-bit and magnitude-bit, and it is just extended to 8-bits.

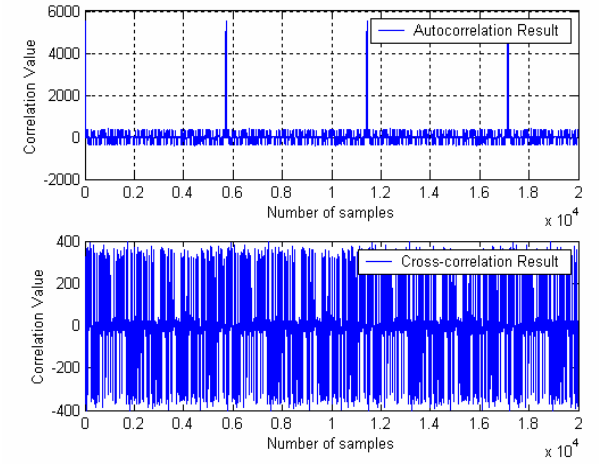
An example of the proposed signal processing scheme is shown in Fig. 8 and Table 5. If the 14-bits encoding value (0h3F92) is made by the encoding values of the digital IF signal, carrier and code replica, then the accumulation value (14) is obtained by the look-up table without any multiplications.

4. PERFORMANCE EVALUATION

Prior to evaluating the performance regarding processing time, the comparison of the correlation characteristic has been done. The doppler effect is not considered herein.



(a)



(b)

Fig. 9. Correlation result of (a) the typical and (b) the proposed signal processing scheme.

Table 6. Comparison of the correlation property.

	Period	Auto Corr.	Cross Corr.	Ratio [dB]
Typical Scheme	1msec	5,714	363	23.94
Proposed Scheme	1msec	5,552	362	23.72

As shown in Table 6, the proposed scheme has a 0.22dB correlation loss compared with the typical scheme.

This paper evaluated the performance of the proposed signal processing scheme using a sampled IF data with a 60 second length acquired from the digitized signal acquisition equipment as shown in Fig. 10.

Table 7 and Fig. 11 present the results of the comparison between the typical signal processing scheme and the proposed signal processing scheme in real-time through the software GPS receiver based on the 2.4GHz PC (Personal Computer).

The processing time of software GPS receiver with the proposed signal processing scheme is reduced to 15% as much as one with the typical signal processing

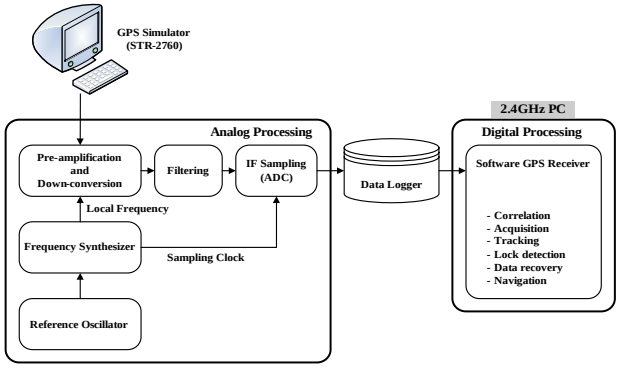


Fig. 10. Test setup.

Table 7. Comparison of processing time.

# of channel	Processing Time		SNR Loss [dB]
	Typical Scheme	Proposed Scheme	
1	3 min. 16 sec.	45 sec.	0.2
2	5 min. 29 sec.	46 sec.	0.2
3	6 min. 14 sec.	77 sec.	0.2
4	7 min. 55 sec.	82 sec.	0.3
8	13 min. 49 sec.	138 sec.	0.3
12	20 min. 37 sec.	179 sec.	0.3

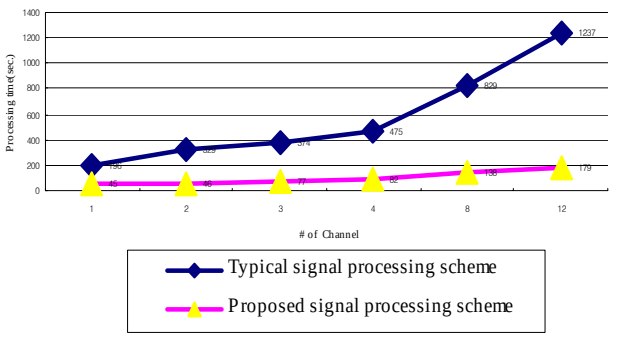


Fig. 11. Comparison of the processing time.

scheme even though 0.3dB-SNR (Signal to Noise Ratio) loss.

As a result, the software GPS receiver with the proposed signal processing scheme can operate to 2-channels in real-time.

5. SUMMARY AND CONCLUSION

An efficient signal processing scheme that runs on a commercial off-the-shelf PC have been proposed and implemented. The proposed signal processing scheme is utilizing the concept of signal compression, and only the frequently used replica signals are generated, so that 4-sample IF signals are processed at once. The effectiveness of the proposed scheme is evaluated using the real GPS signal. The total signal processing time is reduced to 15% of the typical signal processing scheme despite 0.3dB SNR loss.

It is expected that a real-time software GPS receiver can be possible using the proposed scheme. Furthermore, greater computational burden reduction can be possible with the extended version of the proposed scheme to 8 or 16 samples through partial correlation. In this case, additional researches on the implementation schemes and the loss analysis are required.

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