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An Electrothermal Model for AlGaN/GaN Power HEMTs Including Trapping Effects to Improve Large-Signal Simulation Results on High VSWR

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***Abstract*—A large-signal electrothermal model for AlGAN/GaN HEMTs including gate and drain related trapping effects is proposed here. This nonlinear model is well formulated to preserve convergence capabilities and simulation times. Extensive measurements have demonstrated the impact of trapping effects on the shapes of *I(V)* characteristics, as well as load cycles. It is shown that accurate modeling of gate- and drain-lag effects dramatically improves the large-signal simulation results. This is particularly true when the output loads deviate from the optimum matching conditions corresponding to real-world simulations. This new model and its modeling approach are presented here. Large-signal simulation results are then reported and compared to load–pull and large-signal network analyzer measurements for several load impedances at high voltage standing wave ratio and at two frequencies.**

***Index Terms*—AlGaN/GaN HEMTs modeling, drain lag, gate lag, large-signal network analyzer, trapping effects.**

I. Introduction

THANKS TO their very high breakdown voltages and their high sheet carrier densities, AlGaN/GaN HEMTs are a very promising solution for high-power and high-frequency applications. The progress made on their technology over the last few years now make them usable in systems, and hence, there is a need for electrical models. Many topologies and solutions to extract models are reported in the literature [1]–[4]. Here we propose a complete nonlinear model, including the thermal effects and taking into account the electrical anomalies due to the trapping effects. Indeed, the latter have a strong impact on the electrical performances of these components, and it is hard today to imagine that they will be completely removed soon, even if solutions exist to reduce them.

We will show that modeling the trapping effects dramatically improves the large-signal simulation results, and that this is particularly true when the output loads deviate from the optimum matching conditions.

Thus, such designed models can prove interesting for wideband application designs in which devices cannot be optimally loaded on the whole bandwidth, or also to have an idea of the shapes of the load cycles when the devices are submitted to electrical perturbations (in order, for example, to check if destructive operating modes are reached or not). Considering this last point, this model was also designed to be able to reach high compression levels, i.e., the equations used are well formulated to preserve good convergence capabilities.

This paper is organized as follows. In Section II, the nonlinear model used is described with particular emphasis on the way trapping effects are taken into account. In Section III, the extraction procedure based on pulsed *I(V)* and pulsed S-parameters is described [5]. It is shown how the time constants of the traps are evaluated, and the results are evaluated for a variety of dc and pulsed *I(V)* characteristics. In Section IV, classical load–pull measurements, as well as time-domain large-signal measurements, are extensively used to validate the proposed model. Those measurements were performed at two different frequencies, namely, 5 and 10 GHz, and for several load impedances at high voltage standing-wave ratio (VSWR).

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II. Description of the Nonlinear Model

Fig. 1 shows the topology of the complete equivalent circuit we use to model the devices. All the parts of this schematic are described in the following.

A. Current Source

The main current source of the model is described by modified Tajima's equations [3], [4]. Both diodes D_{GD} and D_{GS} have classical forms.

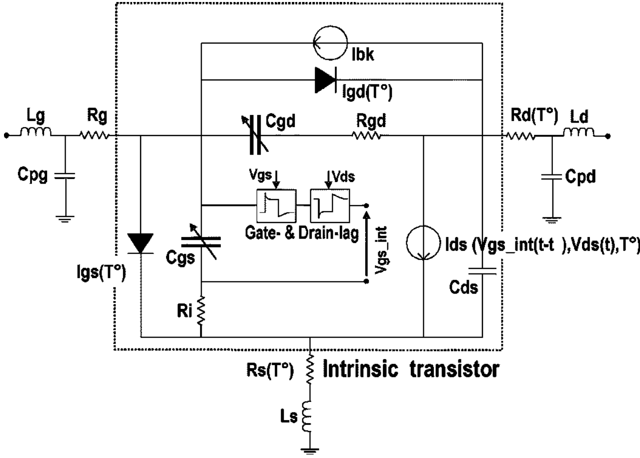

Fig. 1. Structure of the nonlinear model used. $I\text{ds}$ equation is given in [5] and charge equations are given in [6]. The extrinsic parameters are assumed constant. $I\text{ds}$, $I\text{gs}$, $I\text{gd}$, Rs, and Rd depend on the temperature.

The equations of the main current source are

$$\begin{aligned}
Id &= Id_t \cdot \gamma_{md} \\
\gamma_{md} &= 1 + \beta gm \cdot (V\text{ds} + Vdm) \\
&\quad \cdot (1 + \tanh(\alpha gm \times (V\text{gs_int} - Vgm))) \\
Id_t &= \frac{I_{\text{DSS}}}{1 - \frac{1}{m}(1 - e^{-m})} \left[V_{\text{GSN}} - \frac{1}{m}(1 - e^{-mV_{\text{GSN}}}) \right] \\
&\quad \cdot \left[1 - e^{-V_{\text{DSN}}\left(1 - aV_{\text{DSN}} - bV_{\text{DSN}}^2\right)} \right] \\
V_{\text{GSN}} &= 1 + \frac{V\text{gs_int}(t - \tau) - V\phi}{V_P} \\
V_{\text{DSN}} &= \frac{V_{\text{DS}}}{V_{\text{DSP}}\left(1 + w\frac{V\text{gs_int}(t-\tau)}{V_P}\right)}
\end{aligned}$$

and $V_P = V_{P0} + pV_{\text{DSP}} + V\phi$.

The equations of the diodes are

$$ID_{\text{gd}} = I s\text{gd} \cdot e^{\frac{q \cdot V\text{gd}}{k \cdot T s\text{gd} \cdot N\text{gd}}} \quad ID_{\text{gs}} = I s\text{gs} \cdot e^{\frac{q \cdot V\text{gs}}{k \cdot T s\text{gs} \cdot N\text{gs}}}.$$

B. Trapping Effects

The circuits used here to model the gate- and drain-lag effects and the methods to extract their associated parameters have been described in [7]. Such circuits modeling trapping effects are necessary in advanced modeling of HEMTs, and different solutions have been studied, particularly in [8]–[10].

Here, the effect of the traps is presented as a contribution to the command voltage $V\text{gs}$. Indeed, the trapping effects induce that $I\text{ds} = f(V\text{gs}, V\text{ds}, V\text{bias}, \text{time})$, whereas $I\text{ds} = f(V\text{gs}, V\text{ds})$ in the ideal case. In the model presented, $I\text{ds}$ is unchanged, but the command voltage is modified to take into account the trapping effects. We then have here $I\text{ds} = f(V\text{gs}, V\text{ds})$ and $V\text{gs} = f(V\text{bias}, \text{time})$.

Thus, these subcircuits, mounted in series between the gate resistance and the current source (cf. Fig. 1), modify the command voltage of the current source (called $V\text{gs_int}$) by adding

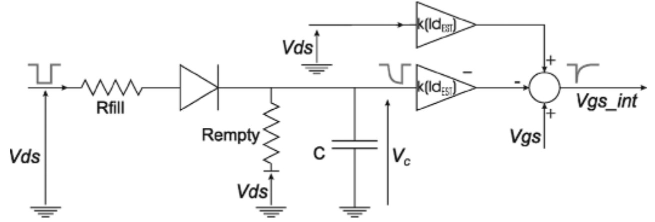

Fig. 2. Schematic of the drain-lag model.

transients to $V\text{gs}$. These transients are related to the capture or the emission of charges by the traps.

The drain-lag subcircuit topology, considering only one trap level, is shown at Fig. 2. The gate-lag subcircuit is based on the same architecture, but the input voltage is $V\text{gs}$, and the diode direction and the sign of k are changed.

The capture time constant is given by

$$\tau_{\text{fill}} \approx R_{\text{fill}} \cdot C \ (\text{as } R_{\text{empty}} \gg R_{\text{fill}}).$$

The emission time constant is given by

$$\tau_{\text{empty}} = R_{\text{empty}} \cdot C.$$

In a mathematical form, the circuit gives

$$V\text{gs_int} = k(I\text{ds}_{\text{EST}}) \cdot [V\text{ds} - V_C] + V\text{gs}$$

with

$$k(I\text{ds}_{\text{EST}}) = k_{\text{rel}} \cdot I\text{ds}_{\text{EST}}(V\text{gs}) \cdot A_{DL}$$

where A_{DL} is a fitting factor in Amp^{-1}.

The amplification factor k is linked to the amplitude of the trap and we assume that it is linearly dependent on the output current. This current, noted $I\text{ds}_{\text{EST}}$, is an estimate of the total drain current, which is calculated in a very simple fashion, depending only on $V\text{gs}$ (linearly or with a tanh-based law), to preserve the convergence properties of the model. It is then provided by a different source from the one describing the full nonlinear channel current. We will show that this simple description gives, however, accurate results.

Thus, four parameters have to be extracted, i.e., C, $R\text{empty}$, $R\text{fill}$, and k. It should be noted that, by examining the circuit of Fig. 2 and taking into account the dissymmetry between the two time constants, the level of the control voltage $V\text{gs_int}$ is mainly determined by the high level of the drain voltage in pulsed conditions.

C. Nonlinear Capacitances

Both capacitances $C\text{gs}$ and $C\text{gd}$ are 1-D [6]. In order to keep them depending on their own terminal voltages (i.e., $V\text{gs}$ for $C\text{gs}$ and $V\text{gd}$ for $C\text{gd}$), they are extracted along an estimated load line corresponding approximately to the optimum load cycle locus. Modeling them that way is very practical in terms of simplicity of modeling. The impact of such simplification will be quantified in Section III-C.

D. Breakdown Model

The breakdown is simply described by exponential increases of the gate and drain currents when the breakdown voltage $\mathrm{BV_{GD}}$ is reached. A soft quasi-exponential function is used to keep an expression well suited for convergence [5] as follows:

$$I_{bk} = I_{bkDG} \cdot \exp_\mathrm{soft}(\alpha_{DG} \cdot V_{\mathrm{DS}})$$

with

$$\begin{aligned} \exp_\mathrm{soft} &= \text{if } (x < \max_\mathrm{arg}) \text{ then } \exp(x), \\ &\quad \text{else } \max_\exp \cdot (x + 1 - \max_\mathrm{arg}) \\ \max_\mathrm{arg} &= \ln(\max_\exp) \quad \max_\exp = 10^{99}. \end{aligned}$$

E. Thermal Dependence

The self-heating effects have an exponential behavior versus time when the power changes abruptly and, hence, can be reproduced by *RC* cells in an electrical simulator. The input of the circuit is the dissipated power calculated in the following way:

$$P_{\mathrm{DISS}} = I_G \cdot V_{\mathrm{GS}} + I_D \cdot V_{\mathrm{DS}}.$$

The output of the thermal circuit is a voltage corresponding to the temperature elevation. By adding the room temperature to this voltage, we obtain the device temperature.

The measurements show that the calculated temperature has an impact on the current source parameters $I\mathrm{dss}$ and P [5], the values of the access resistances Rs and Rd, the ideality factors (N_{GD} and N_{GS}) of the diodes D_{GD} and D_{GS} linearly, and on the saturation currents ($I s\mathrm{gs}$ and $I s\mathrm{gd}$) of the diodes exponentially.

Thus, we have

$$X = X_0 + X_T \cdot T$$

where X represents $I\mathrm{dss}$, P, Rs, Rd, $N\mathrm{gs}$, or $N\mathrm{gd}$

$$Y = Y_0 + Y_T \cdot e^{(T/Ta)}$$

where Y represents $I s\mathrm{gs}$ or $I s\mathrm{gd}$.

III. Pulsed I–V and Pulsed S-Parameters Characterizations: Extraction of the Parameters

The measurements were performed on a 600-μm ($8 \times 75 \times 0.25$ μm) $\mathrm{Al_{0.27}Ga_{0.73}N/GaN}$ HEMT from Thalès–Tiger grown by MOCVD on an SiC substrate.

A. Trapping Circuits Parameters

The parameter extraction is obtained by measuring the current transients during voltage pulses for which traps emit their charges. The form of these transients can be fitted by a few exponential terms. In the current case, two terms (i.e., two trapping levels) were chosen for both gate- and drain-lag circuits. This choice represents a tradeoff between the accuracy of the fit and the complexity of the circuit. However, it is not worth obtaining an excellent fit, as the trapping time constants strongly depend on the temperature, which is not taken into account in the model. On the other hand, it is important to avoid "parasitic" exponential terms due to self-heating during the measurements. That means that the thermal state of the device needs to remain: 1) the same before and during the pulse and 2) close to the one of the bias point of the spotted application because of the thermal dependence of the emission time constants.

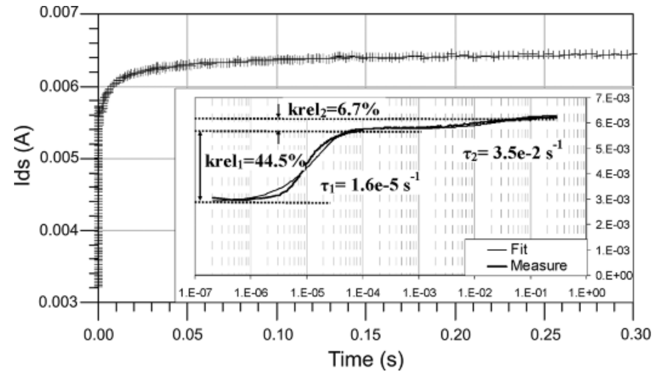

Fig. 3. Measurement of a drain-lag related current transient. $V\mathrm{gs}$ is kept at a fixed value equal to −6 V, whereas $V\mathrm{ds}$ is pulsed from 30 to 20 V. Self-heating effects are negligible in this case. The fit of the transient and the parameters extracted are also displayed.

In order to obtain the drain-lag related emission time constants, $V\mathrm{ds}$ was pulsed from 30 to 20 V and $V\mathrm{gs}$ fixed close to pinchoff in order to obtain a very low drain current to avoid thermal effects (the dissipated power variation is less than 0.05 W), and the temperature of the chuck was set to 110 °C in order to make the device work approximately in the same thermal state as for the foreseen application in class AB. The current transient, and also the curve modeling it by a sum of two exponential terms, are shown at Fig. 3. The main extracted parameters are also displayed on this figure.

Gate-lag related emission time constants are less precisely obtained, thermal transients being harder to avoid during measurements. We pulse the gate–source voltage in a short range near of $V\mathrm{gs_bias}$ with $V\mathrm{ds}$ equal to $V\mathrm{ds_bias}$. This implies that the temperature is close to that of the application.

The capture time constants are not extracted from measurements, as they are too fast to be measured in this case, and generally in most devices. However, it is worth noting that the key point to obtain good results in continuous wave (CW) large-signal applications is the asymmetry between short capture time constants and large emission time constants. Thus, the values are fixed to a few nanoseconds.

B. Pulsed I–V Measurements and Current Sources Parameters Extraction

In order to obtain the static characteristics of the device and to extract the current source parameters, pulsed *I–V* measurements are performed at the room temperature. The current source parameters are extracted from pulsed *I–V* measurements at a quiescent bias point of $V\mathrm{gs0} = 0$ V and $V\mathrm{ds0} = 0$ V (case 1). This quiescent bias point is chosen in order to: 1) obtain a quasi-isothermal measurement as pulses are very short (400 ns) and 2) to avoid trapping effects. Indeed, for this quiescent bias point configuration, the classical *I–V* curves measurement implies that $V\mathrm{gs}$ is pulsed down and $V\mathrm{ds}$ is pulsed up. Hence, the

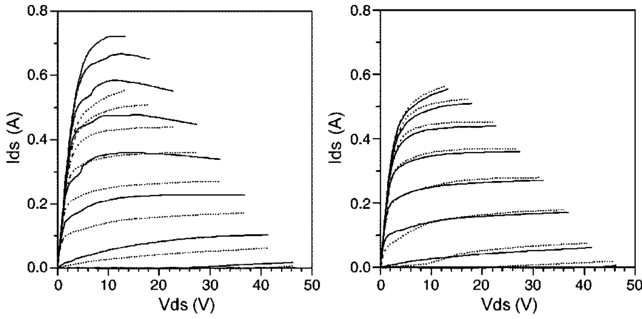

Fig. 4. 400-ns pulsed-*IV* measurements (with $V\mathrm{gs}$ from -8 to 1 V) on the 8×75 μm transistor at three different quiescent bias points. (*left*) $V\mathrm{gs0} = 0$ V and $V\mathrm{ds0} = 0$ V (case 1): continuous lines; $V\mathrm{gs0} = -8$ V and $V\mathrm{ds0} = 0$ V (case 2): dashed lines. (*right*) $V\mathrm{gs0} = -8$ V and $V\mathrm{ds0} = 0$ V (case 2): continuous lines; $V\mathrm{gs0} = -8$ V and $V\mathrm{ds0} = 20$ V (case 3): dashed lines. The differences on the left are attributed to gate-lag effects, whereas they are attributed to drain-lag effects on the right.

gate- and drain-lag related traps are filling. Considering that this filling phenomenon is very fast compared to pulse duration, the traps state is given by the voltage levels during the pulses.

The parameters of the diodes and the breakdown generator are also extracted from this measurement configuration.

Other quiescent bias point choices allow us to observe the trapping effects and even to separate gate- and drain-lag effects. Such types of measurements will also be useful to validate the trapping circuit parameters extraction. We can focus on the two following configurations [11].

1) If the quiescent bias point is, for example, $V\mathrm{gs0} = -8$ V (when the device is pinched off) and $V\mathrm{ds0} = 0$ V (case 2), the gate– and drain–source voltages are pulsed up during the measurement. Hence, the traps commanded by drain–source voltage are filling (fast), and the traps commanded by gate–source voltage are emptying (slowly). We can conclude that inside the pulse, the traps commanded by gate–source voltage remain in the state they had at quiescent bias point, and the state of the traps commanded by the drain–source voltage has changed and is now given by the drain–source voltage level inside the pulse.
2) If the quiescent bias point is, for example, $V\mathrm{gs0} = -8$ V (pinched off) and $V\mathrm{ds0} = 20$ V (case 3), the drain–source voltage is pulsed down for the measurement points where $V\mathrm{ds} < 20$ V and pulsed up for $V\mathrm{ds} > 20$ V.

Considering that the traps' discharge is very slow compared to the duration of the pulses, the state of the traps inside a pulse is that of the quiescent bias point for $V\mathrm{ds} < 20$ V, and that of the drain–source voltage for $V\mathrm{ds} > 20$ V.

Superimposed on Fig. 4 are three pulsed *I(V)* networks corresponding to the three cases of quiescent biases described earlier. The current is approximately 1.25 A/mm. We note that the current dispersion, for this device, is mainly due to the gate-lag effects. The drain-lag effects induce an increase of the knee voltage, especially manifest at low current.

This device presents an unusual behavior of the drain lag, as the saturation current is higher when $V\mathrm{ds_bias} = 20$ V than when $V\mathrm{ds_bias} = 0$ V. However, the difference is weak and was not observed on the other measured devices.

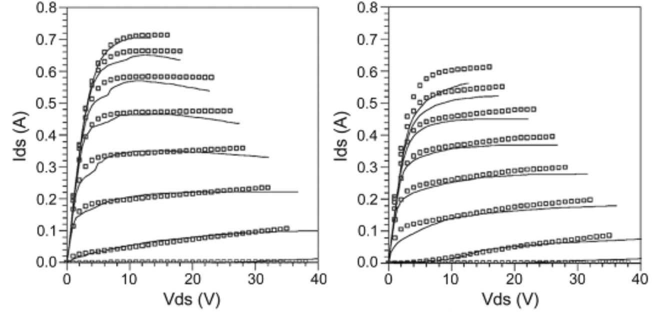

Fig. 5. Measured and simulated pulsed *I–V* networks at $V\mathrm{gs0} = 0, V\mathrm{ds0} = 0$ and at $V\mathrm{gs0} = -8$ V, $V\mathrm{ds0} = 20$ V on the 8×75 μm transistor for $V\mathrm{gs}$ from -8 to $+1$ V (continuous lines: measurements, squares: simulations).

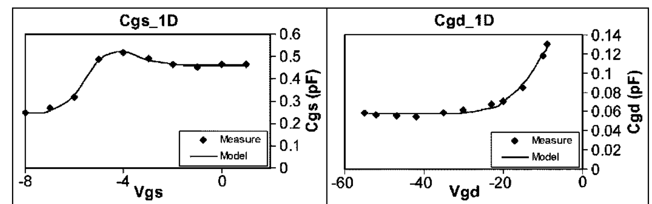

Fig. 6. 1-D nonlinear forms of $C\mathrm{gs}$ and $C\mathrm{gd}$ with equations based on hyperbolic tangents. The points correspond to values extracted along the estimated load cycle, the lines correspond to the model.

It has to be noted that we took care to maintain the output current equal to 0 A at the quiescent bias points and that we chose the length of the pulses as short as possible to avoid thermal effects and their influence on output current.

The simulated pulsed *I–V* characteristics are shown and compared to measurements at Fig. 5. We note that the proposed model can take into account the value of the quiescent bias, thus dramatically increasing the range of validity of the model. However, small discrepancies remain at high $V\mathrm{gs}$ voltages (around $V\mathrm{gs} = 1$ V). This can be due to: 1) the relative simplicity of the trapping circuits and/or 2) to a slight difference between several measured devices.

C. Pulsed S-Parameters Measurements and Frequency-Dependent Parameters Extraction

The pulsed S-parameters are measured for each point of the *I(V)* networks [5]. The extrinsic parameters are extracted from these S-parameters and then the intrinsic elements are calculated for each measured point. This multibias S-parameters extraction gives, in particular, the values of $C\mathrm{gs}$ and $C\mathrm{gd}$ for the points measured along the estimated load line. Very precise fits are obtained along the latter with tanh-based equations [6], as is shown at Fig. 6.

The errors made by using such 1-D forms are shown on Fig. 7 on a whole *I–V* network. These errors remain weak on a large area for $C\mathrm{gs}$, while they rapidly increase for low values of $V\mathrm{ds}$ for $C\mathrm{gd}$. However, those capacitance models ensure a very robust behavior of the model even at high compression levels.

Other intrinsic parameters, i.e., $R\mathrm{gd}$, Ri, $C\mathrm{ds}$, and τ, are kept constant (18.5 Ω, 0.65 Ω, 139 fF, and 1.88 ps^{-1}, respectively).

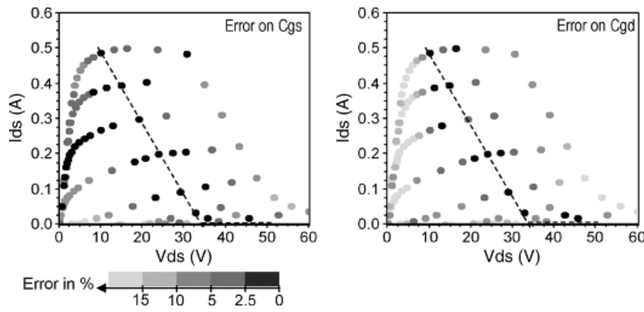

Fig. 7. Error made on capacitance values by using 1-D equations. (*left*) $C\mathrm{gs}$. (*right*) $C\mathrm{gd}$. From black to light gray points, error is respectively inferior to 2.5%, between 2.5%–5%, between 5%–10%, between 10%–15%, and superior to 15%. The dashed lines represent the estimated load lines.

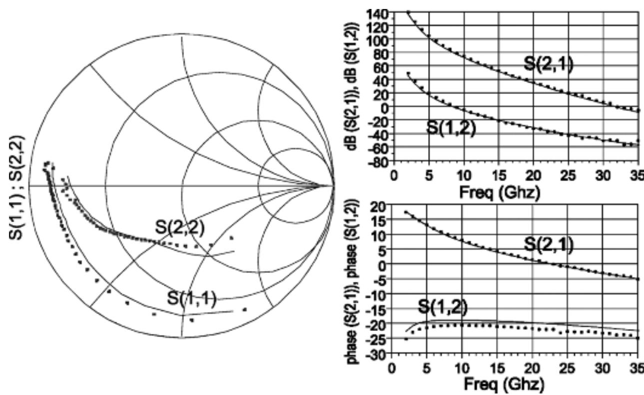

Fig. 8. Measured and modeled pulsed S-parameters at a quiescent bias point of $V\mathrm{gs}0 = -4$ V, $V\mathrm{ds}0 = 25$ V and a pulse level at $V\mathrm{gs}0 = -4$ V, $V\mathrm{ds}0 = 24$ V on the 8 × 75 μm transistor (measurements: points, model: continuous lines).

Fig. 8 shows a comparison between measured and modeled S-parameters at the bias point for a characterization at a quiescent bias point equal to the bias point of the spotted application.

D. Thermal Circuit Parameters and Thermal Dependence

The thermal circuit is obtained by fitting the hot spot temperature transient obtained by 3-D finite-element simulations. Fig. 9 shows the self-heating obtained by applying a dissipated power of 7 W/mm, and also the fit obtained by modeling it with five *RC* cells.

Measurements have been performed on these devices to confirm the values obtained from the 3-D simulation and a relatively good agreement has been found for the thermal resistance. However, time constants of trapping and thermal effects mix together and are very difficult to separate. Thus, we relied on the 3-D simulation (validated in [12]) to derive the dynamical thermal subcircuit, as shown at Fig. 9.

Note: Fig. 9 shows that the self-heating is not negligible after 400 ns, which corresponds to the typical pulse duration during pulsed *I(V)* measurements. However, it is difficult to obtain shorter pulses considering the voltage and current ranges applied. Moreover, the temperature modeled is that of the point located at the center of the channel, having the fastest heating.

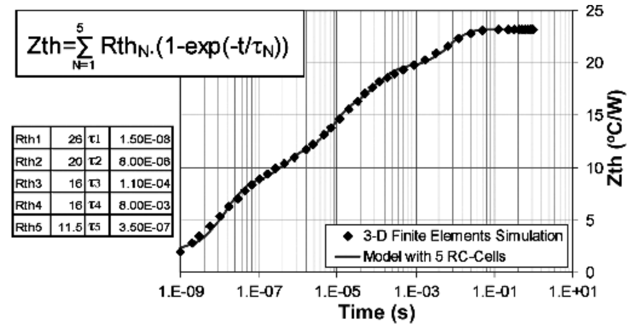

Fig. 9. Extraction of the thermal impedance versus time of the modeled device. Simulations are performed with a 3-D model of the transistor in the software ANSYS. The points correspond to the simulated self-heating for a dissipated power of 7 W/mm, the continuous lines corresponds to the values given by the electrical model with five *RC* cells.

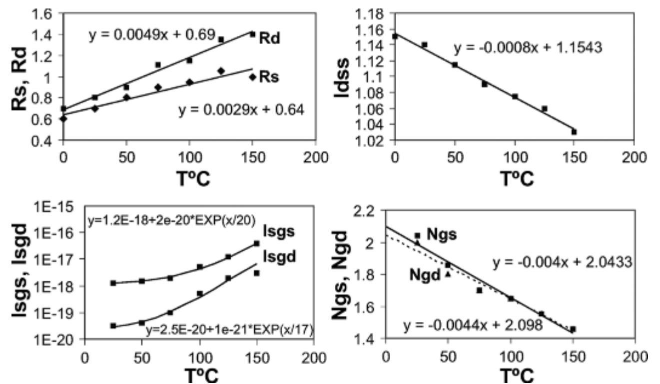

Fig. 10. Thermal dependence of parameters of the model: the access resistances Rs and Rd, the parameter of the Tajima's current source $I\mathrm{dss}$, and the ideality factors of the diodes $N\mathrm{gs}$ and $N\mathrm{gd}$, linearly dependent on the temperature; the saturation currents of the diodes, exponentially dependent on the temperature (points: extracted values, continuous lines: model, excepted for $N\mathrm{gd}$ (dashed line).

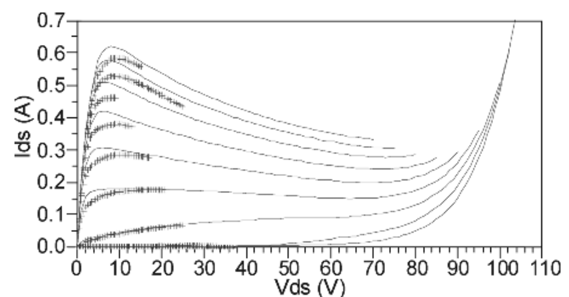

Fig. 11. Measured and modeled dc *I(V)* curves for $V\mathrm{gs}$ from -8 to $+1$ V. The modeled breakdown locus is also showed (measurements: crosses, model: continuous lines).

The thermal dependence of the current source parameters is obtained by fitting quasi-isothermal pulsed *I(V)* networks measured at several chuck temperatures (typically from -60 °C to 200 °C): the values of most parameters remain the same, but they have to be changed for some of them (*cf* Section II-E). The variations obtained in this case are shown at Fig. 10.

A comparison between dc *I(V)* measurements and simulations is given at Fig. 11 (the modeled breakdown locus is also

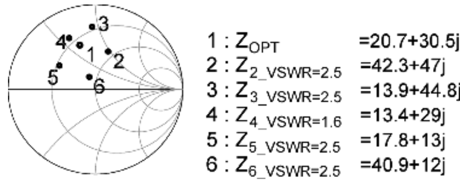

Fig. 12. Measured and modeled load impedances at 10 GHz on the $8 \times 75\ \mu$m transistor. The VSWR values are calculated with respect to Zopt.

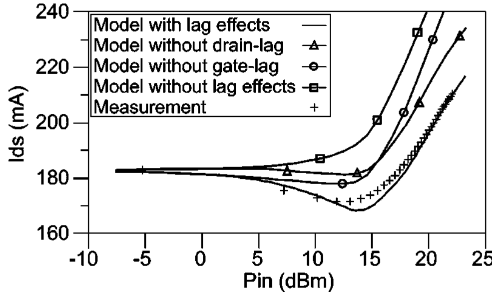

Fig. 13. Measured (crosses) and modeled average output current in different conditions: by taking into account any trapping effect, by modeling only gate lag, by modeling only drain lag, and by modeling gate and drain lag, at the optimum load impedance.

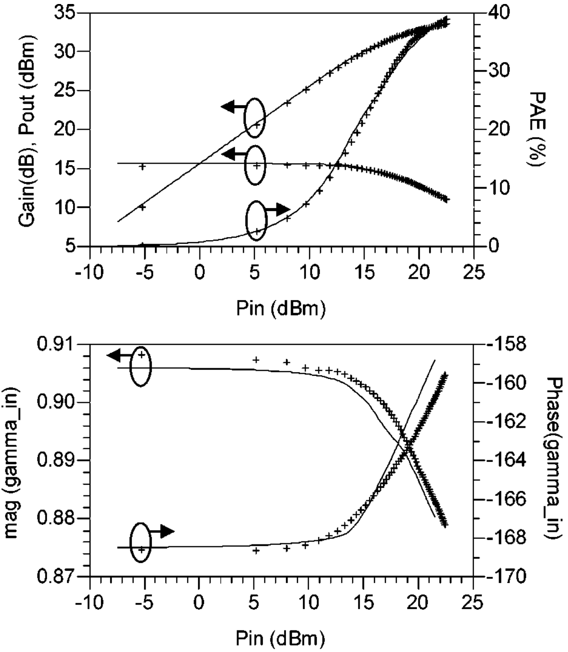

Fig. 14. Measured and modeled power characteristics (gain, output power, PAE, magnitude and phase of the input reflection coefficient, versus input power (measurements: points, simulations: continuous lines) at the optimum load impedance at 10 GHz.

shown). The quite good correlation validates the method of thermal modeling, despite the approximations made: the "hot spot" temperature is not fully representative of the temperature of the transistor, but extracting it from the simulator in order to model the self-heating is the most practical way in terms of easiness and time. Moreover, and for example, we remarked that it is not worth modeling the thermal impedance of several representative points in the device structure [13] (in the access areas for Rs and Rd, in the active area for the other parameters), as the gain in precision on the electrical simulations is negligible, even if it allows knowing more precisely the temperature at each of these points.

IV. Validation of the Model Against Large-Signal Measurements: Simulations on Several Load Impedances

Load–pull measurements were performed at a drain bias of 25 V (dc) in class AB and at 10 GHz (CW) for several load impedances, shown at Fig. 12. These load impedances correspond to a VSWR of 2.5, except for a point at a VSWR of 1.6 (load 4).

A. Load–Pull Measurements/Simulations on the Optimum Load Impedance

First, large-signal simulations were performed on the optimum load impedance (load 1 in Fig. 12). A maximum power of 2.5 W (4 W/mm) was measured with a small-signal gain of 15.5 dB and a maximum power-added efficiency (PAE) of 39%. The comparison between measurements and simulations is given at Figs. 13 and 14, and demonstrates the improvement brought by the new model. The impact of trapping effects on the average current is particularly obvious, and both effects have an influence on it. The current decrease with increasing power is a significant consequence of the asymmetric nature of the traps capture and emission processes and cannot be attributed to the thermal effects, which are also modeled. Indeed, the traps state is determined by the peak values of Vgs and Vds, which increase when the input power increases.

B. Load–Pull Measurements/Simulations on Output Impedance Mismatches

The large-signal simulation results on other load impedances are shown in Fig. 15 in the numbering order given in Fig. 12.

These results of simulations with trapping effects included are better for all the impedances contouring the optimum load, and especially the mean output current and PAE. They validate the fact that the model is able to reproduce the large-signal characteristics on a wider range of load impedances when the trapping effects are taken into account.

We can note that the influence of the trapping effects on the output current depends on the load impedance and, therefore, on the forms of the load cycles and voltages excursions. On Z_2, Z_3, and Z_4, the trapping effects are significant, leading to bad behavior of the model without trapping subcircuits. On Z_5 and particularly on Z_6, the trapping effects have less influence (the current do not decrease strongly before the compression), and the characteristics could be fairly well reproduced without modeling the trapping effects. However, these cases are isolated, and the characteristics are all better reproduced when the trapping effects are taken into account, even if they are quite simply modeled.

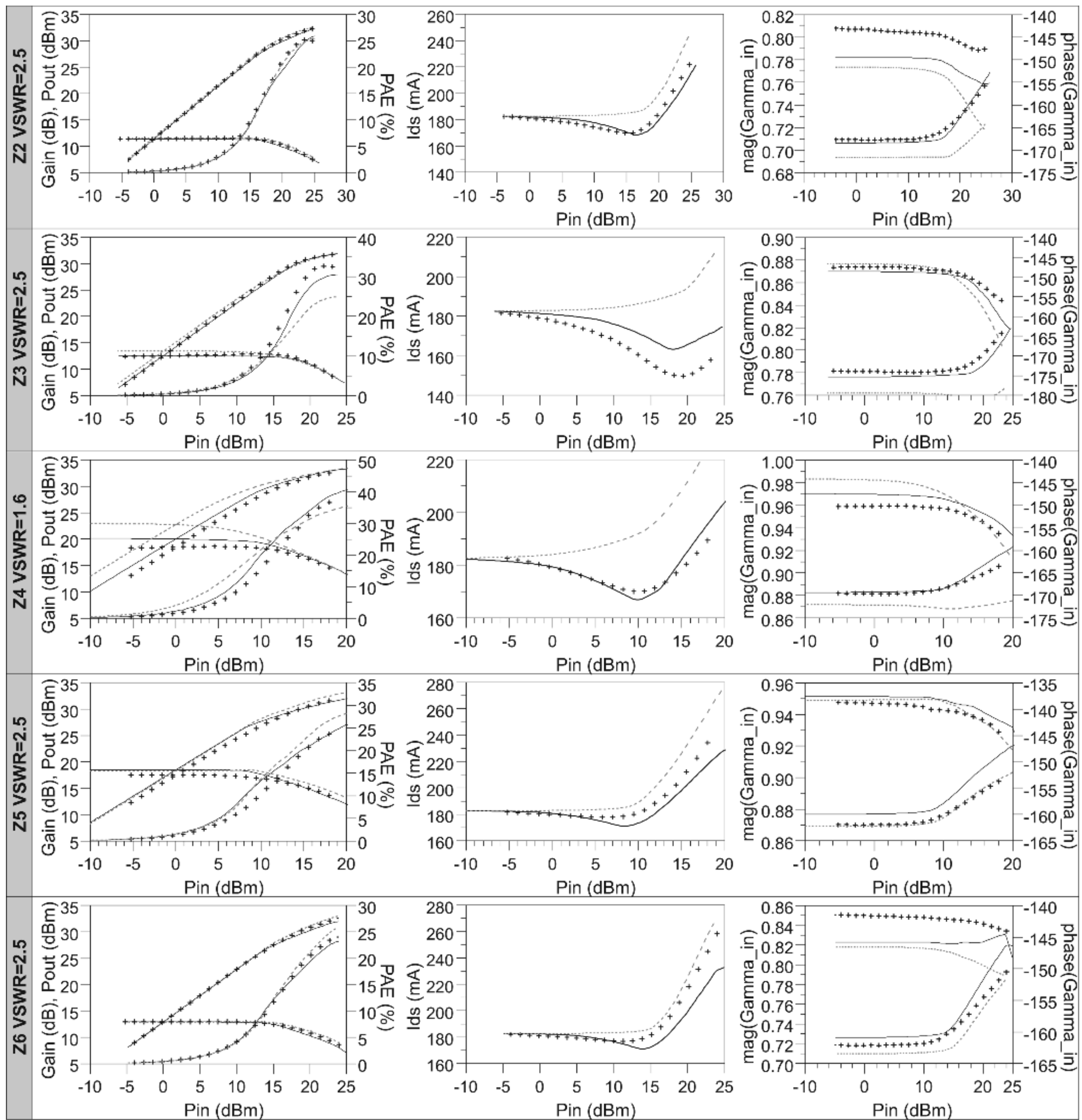

Fig. 15. Comparison between measurements and simulations for the load impedances 2–6 with the model including trapping effects and the model not including them (crosses: measurements, continuous lines: model with trapping effects, dashed gray lines: model without trapping effects).

It has to be noted that the input reflection coefficient ($\gamma_{\rm in}$) is also better modeled when the trapping effects are taken into account. This is important to predict instabilities or to adapt the devices inputs.

This proves that modeling the traps is very important for these types of devices, as the models which do not include the trapping effects show their limitations when the load impedance is modified. This is all the more true as the transistors mounted in amplifiers cannot be loaded on the optimum impedance in many cases. An example is the case of wideband amplifiers, for which the matching is often chosen for the most critical frequency in terms of power, and represents a compromise in order to meet the specifications on the entire bandwidth. Another example is the case of systems terminated by antennas, which can receive RF power and then transmit it to the outputs of the transistors, thus modifying their load impedances. Such behavior deserves a

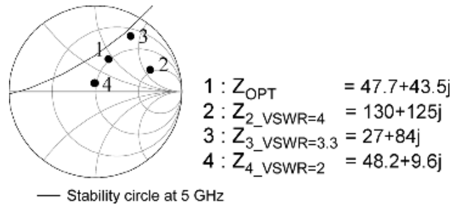

Fig. 16. Measured and modeled load impedances at 5 GHz on the $8 \times 75\ \mu$m transistor. The line delimits the stability area at 5 GHz.

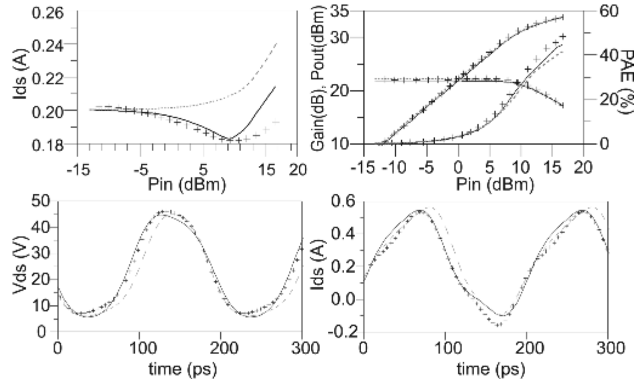

Fig. 17. Comparison between measurements and simulations (with and without trapping effects included) at the optimum load impedance $(Z = 47.7 + j.43.5)$. Waveforms are shown at 5-dB compression (crosses: measurements, continuous lines: simulations with trapping effects, dashed lines: simulations without trapping effects).

more detailed analysis, which can be performed through simulations and time domain load–pull measurements, as presented in Section V.

V. Large-Signal Network Analyzer (LSNA) Measurements and Simulations on Several Load Impedances

Load–pull measurements with an LSNA [14], [15] were performed at 5 GHz on a transistor of the same process and the same development, but fabricated on another wafer. The model was, however, unchanged and simulations were performed in the same conditions as for measurements. Our LSNA load–pull setup allows reconstructing the time-domain waveforms with a cutoff frequency of 20 GHz. Thus, we are able to measure the four first harmonics at 5 GHz, which allows a good precision on the waveforms even at high compression levels. Measurements have been performed on several load impedances, located on a Smith chart in Fig. 16 and numbered from 1 to 4. Optimum load could not be encircled, as the device became unstable (the simulated stability circle at 5 GHz is also shown). From Figs. 17–19, results of simulations are compared to these measurements and will be commented upon.

On the optimum load impedance (Fig. 17), we note that both models (with and without trapping effects) give good power results, except for the dc output current form, where the model with traps gives better results. However, the waveforms (here at 5-dB compression) are better described when trapping effects are activated.

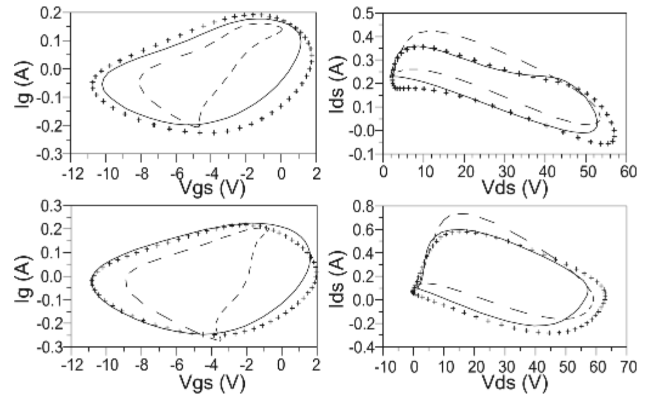

Fig. 18. Comparison between measurements and simulations (with and without trapping effects included) of the extrinsic input and output load cycles at load impedance 2 $(Z = 130 + j.125)$ at 4.6-dB compression for the top graphs, and at load impedance 3 $(Z = 27 + j84)$ at 7-dB compression for the bottom graphs (crosses: measurements, continuous lines: simulations with trapping effects, dashed lines: simulations without trapping effects).

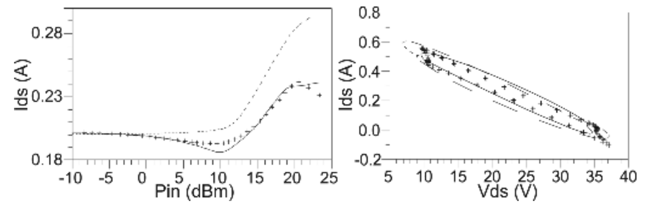

Fig. 19. Comparison between measurements and simulations (with and without trapping effects included) of the dc output current and the extrinsic output load cycle at load impedance 4 $(Z = 48.1 + j.9.6)$ at 8-dB compression (crosses: measurements, continuous lines: simulations with trapping effects, dashed lines: simulations without trapping effects).

In Fig. 18, the measured and simulated input and output extrinsic load cycles are shown for load impedances 2 and 3 (at 4.6- and 7-dB compression, respectively). We remark that the input load cycles are better described when trapping effects are activated. It shows particularly well the importance of the capacitances Cgs and Cgs on the extrinsic waveforms at the input: these are swept differently, as the output current is better modeled when trapping circuits are activated. The output load cycles are also better described, but we can note that the maximum value of $V\mathrm{ds}$ is never reached by the models, which may be due to the relative imprecision of the current source at low current, and the strong impact of the trap levels on the buffer conduction at pinchoff.

In Fig. 19, the measured and simulated (with and without trapping effects) dc output current and output load cycle for load impedance 4 are shown. Measurements were driven at a very high level of compression (8 dB). It is interesting to note that the model with activated trapping effects is able to simulate quite well the output load cycle (and particularly the increase of the knee voltage due to the trapping effects), and the abrupt collapse of the dc current when the input power reaches 20 dBm.

VI. Conclusion

A nonlinear model for AlGaN/GaN HEMTs was proposed especially for high power amplifier design, and then the most im-

portant nonlinearities, i.e., the nonlinear capacitances Cgs and Cgd, thermal effects, and trapping effects were taken into account. They have been described in a simple fashion in order to keep a good tradeoff between the accuracy of the simulation results and the convergence, simulation times, and extraction procedure duration.

We have demonstrated here that including trapping effects in a nonlinear model has a significant impact on large-signal results, especially the output loads that deviate from the optimum matching conditions.

The design of the lag subcircuits has two main advantages: only one parameter has to be changed to reproduce the variations of the lag amplitudes, as it is often the case among several transistors of a wafer, and adding them do not require modifying the topology of the main current source. Hence, they can be separately implemented in other nonlinear models.

Many simplifications were done in the description of the trapping effects, and the most interesting way of improvement seems to take into account the thermal dependence of the trapping time constants, and to describe the amplitude of the traps as not only depending on the current. However, these improvements should be reserved for specific studies, as they will undoubtedly have a strong impact on the convergence of the model.

The simulations performed with this model are fast, and we did not notice convergence problems. Activating/deactivating the lag subcircuits multiplies the simulation times in harmonic balance by an approximate factor of 1.5.

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