An Element-Matched Electromechanical ΔΣ ADC for Ultrasound Imaging

D'Urbino, Michele; Chen, Chao; Chen, Zhao; Chang, Zu-Yao; Ponte, Jacco; Lippe, Boris; Pertijs, Michiel

DOI
10.1109/JSSC.2018.2859961

Publication date
2018

Document Version
Accepted author manuscript

Published in
IEEE Journal of Solid-State Circuits

An Element-Matched Electro-Mechanical $\Delta\Sigma$ ADC for Ultrasound Imaging

Michele D'Urbino, *Member, IEEE*, Chao Chen, *Member, IEEE*, Zhao Chen, *Student Member, IEEE*, Zu-Yao Chang, Jacco Ponte, Boris Lippe, and Michiel Pertijs, *Senior Member, IEEE*

***Abstract*—This work presents a power- and area-efficient approach to digitizing the echo signals received by piezoelectric transducer elements, commonly used for ultrasound imaging. This technique utilizes such elements not only as sensors, but also as the loop filter of an element-level $\Delta\Sigma$ ADC. The receive chain is thus greatly simplified, yielding savings in area and power. Every ADC becomes small enough to fit underneath a 150 μm $\times$ 150 μm transducer element, enabling simultaneous acquisition and digitization from all the elements in a 2D array. This is especially valuable for miniature 3D probes. Experimental results are reported for a prototype receiver chip with an array of 5 $\times$ 4 element-matched ADCs and a transducer array fabricated on top of the chip. Each ADC consumes 800 μW from a 1.8 V supply and achieves a SNR of 47dB in a 75% bandwidth around a center frequency of 5MHz.**

***Index Terms*—Band-Pass ADC, $\Delta\Sigma$ ADC, Electro-Mechanical Filter, Piezoelectric Transducer, Ultrasound Imaging.**

I. Introduction

ULTRASOUND imaging is a safe and affordable medical imaging technique, widely used in the diagnosis and treatment of a variety of health conditions, such as cardiovascular diseases. Conventional ultrasound probes employ a linear array of ultrasound transducer elements to transmit acoustic pulses into the body and to receive the resulting echo signals. These elements are individually connected using cables to an imaging system, where beamforming is used to form a cross-sectional two-dimensional (2D) image.

Since the structures to be visualized are inherently three dimensional (3D), ultrasound probes that can produce real-time 3D images have important advantages. Instead of a linear array of transducer elements, this requires a 2D array to enable beamforming in the 3D volume of interest. The resulting number of elements readily exceeds 1000, making it difficult to interface them individually to an imaging system. In-probe application-specific integrated circuits (ASICs) have been used to locally drive the transducer elements and pre-process the received signals. These ASICs employ multiplexing switches, pulsers or sub-array beamforming circuits to allow the probe to be connected to an imaging system using a manageable number of cables [1] [2] [3] [4] [5]. These ASICs are subject to stringent size constraints, to provide direct connections between the elements and the associated on-chip circuitry, and stringent power constraints, to avoid overheating the patient's tissue.

Most prior ultrasound ASICs employ an analog interface to the imaging system. In-probe digitization of the received echo signals, in contrast, has important advantages: digital signal processing can be leveraged to locally process the received data [6], and high-speed digital data-links can be exploited to communicate the data in a robust manner to an imaging system using fewer cables than using analog signaling [7]. Ultimately, the RF data from all the individual transducer elements can be sent fully to an imaging system to enable new imaging schemes that rely on the availability of the (non-beamformed) data, such as synthetic aperture [8] and plane-wave imaging [9], which can provide better resolution or high frame rates than conventional imaging schemes.

A few ASICs that provide in-probe digitization have been reported. [10] and [7] employ SAR ADCs at the output of a sub-array beamformer, and therefore do not provide access to the signals of the individual transducer elements. [11] employs element-level ADCs, but with a die size per element that far exceeds the area of an individual transducer element in a 2D array. [12] employs a SAR ADC shared by an array of elements via a multiplexer, and hence all element-level signals can only be collected from repeated pulse-echo cycles (synthetic receive aperture), at the cost of a reduction of frame rate. [6], in contrast, integrates a $\Delta\Sigma$ ADC for each element, thus digitizing all element-level signals in parallel. However, to realize this within an area of 250 μm $\times$ 250 μm, an advanced 28 nm FD-SOI CMOS technology is required. In spite of this, the 250 μm pitch is larger than the ideal half-wavelength pitch for the 5MHz transducers used, which is 150 μm.

This work presents an element-level ADC realized in a mature 0.18 μm CMOS technology that fits underneath a 150 μm $\times$ 150 μm 5-MHz transducer element [13]. This work targets in particular the receive part of miniature endoscopic probes for 3D cardiac imaging (so-called trans-esophageal echocardiography, TEE), in which the self-heating constraints are demanding, requiring the power consumption per element for a 1000-element array to be kept below 1 mW [14]. The presented approach, however, is also applicable to other probes.

The main novelty that this work introduces is the idea of exploiting the filtering properties of the ultrasound transducer

Michele D'Urbino was with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands, and is now with SiTime, Delft, The Netherlands.

Chao Chen was with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands, and is now with Butterfly Network, New York, NY, USA.

Zhao Chen, Zu-Yao Chang and Michiel Pertijs are with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands.

Jacco Ponte and Boris Lippe are with Oldelft Ultrasound, Delft, The Netherlands.

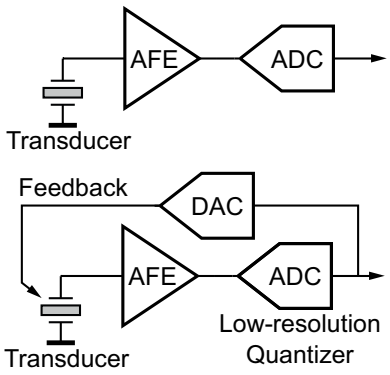


Fig. 1. Comparison of traditional ultrasound front-ends (top) with the proposed solution (bottom).

element to reduce the hardware needed for the A/D conversion of the acoustic input, thus making it possible to fit an entire oversampled ADC underneath a transducer element with a size of 150 μm × 150 μm (see Fig. 1). In particular, the band-pass characteristic of the transducer will be used as the only noise shaping element of a Continuous-Time Band-Pass ΔΣ Modulator (CTBPSDM) specifically built around the transducer.

This approach enables the use of a low-resolution quantizer rather than a full-sized ADC at the output of the analog front end (AFE), because the quantization noise is reduced in the bandwidth of interest thanks to the ΔΣ loop. The idea of exploiting a sensing element's frequency-domain characteristics in a ΔΣ loop has been proposed in a few areas, like accelerometers [15], where a mechanical force-feedback loop is implemented, electrochemical sensors [16], and wind sensors [17]. The goal of this work is to extend this concept to the ultrasound imaging field.

This paper is organized as follows. Two possible ways of exploiting the transducer are proposed in Section II. The ADC's implementation details are discussed in Section III. The design, layout and fabrication a prototype chip are shown in Section IV. Section V describes the obtained experimental results. Section VI concludes the paper.

II. Operating Principle

A. Transducer Modeling

In order to exploit the properties of a transducer in a new way, it is fundamental to find a good model for it which captures all its relevant features, but is simple enough for an intuitive circuit-level analysis. There exist several commonly-used ultrasound transducers: bulk piezoelectric transducers, capacitive micro-machined ultrasonic transducers (CMUT) and piezoelectric micro-machined ultrasonic transducers (PMUT) [18]. The transducers used in this work are bulk piezoelectric transducers made of PZT, but the concept can be easily extended to all transducer types, as they share similar impedance characteristics. They show a mainly capacitive behavior across the spectrum, due to the electrical capacitance between the transducer's electrodes, and a resonance at the target transmit frequency, caused by the main mechanical vibration mode.

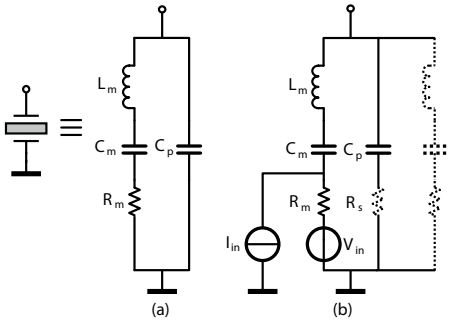


Fig. 2. Butterworth-van Dyke model (a) with a single resonance mode, (b) with multiple resonance modes and a signal source.

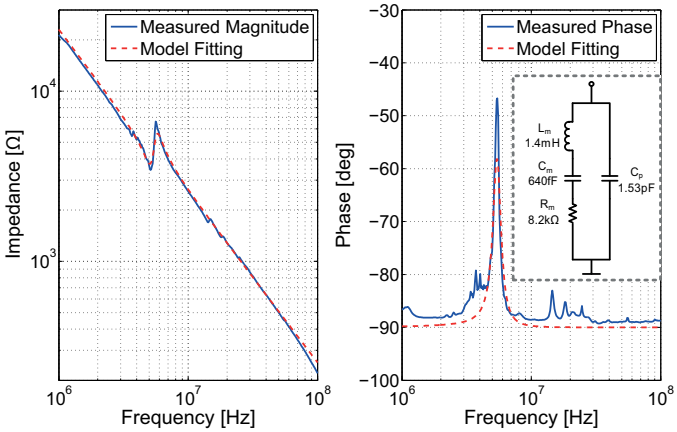


Fig. 3. Impedance (magnitude and phase) of the employed PZT element, along with the Butterworth-Van Dyke model. The measurement was performed using an impedance analyzer on a transducer element integrated on top of the implemented ASIC, which in turn was mounted on a PCB (see Section V), after applying acoustic gel on the transducer array.

The simple Butterworth-Van Dyke (BvD) model, shown in Fig. 2a, captures both of these aspects. While this model is inadequate for the representation of the transduction between the mechanical and electrical domains, being only a 1-port model, it has been used successfully to model the electrical impedance of a variety of ultrasound transducers [19]. The BvD model is accurate only around the resonance frequency and it fails to account for secondary resonances and the transducer's behavior at very high frequencies. If required, the model can be modified to include parasitic resonances (multiple RLC branches in parallel) and resistive behavior at high frequencies (resistor R_s in series with C_p), as shown in Fig. 2b. To represent the acoustic input, the model can be extended with a voltage source V_{in} *or* a current source I_{in}, also shown in Fig. 2b.

A curve fitting on the measured frequency response can provide us with the values of the lumped electrical components in the BvD model. The model fits reasonably well with the impedance of the fabricated transducer elements used in this work, as can be seen in Fig. 3. The motional resistance R_m determines the intrinsic thermal noise added by the transducer and the quality factor of the resonance. The first directly yields the required thermal noise performance for the whole ADC, as the target is to have the ADC contribute a noise level

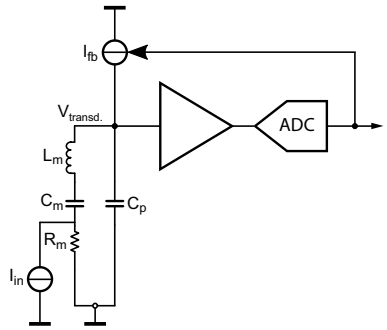


Fig. 4. Current-feedback block-level circuit diagram.

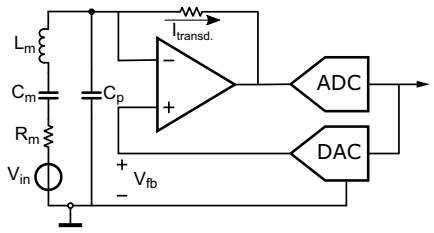


Fig. 5. Voltage-feedback block-level circuit diagram.

comparable to that of the transducer. The second, defined as $Q = \frac{2\pi f_0 L_m}{R_m} = \frac{2\pi f_0}{Bandwidth}$, determines the intrinsic bandwidth of the transducer, where f_0 is the resonance frequency. The quality factor corresponding to the measured impedance characteristic of Fig. 3 is approximately 5, which translates into a 20% 3dB bandwidth around the center frequency.

When exploiting the transducer in the loop filter of a $\Delta\Sigma$ modulator ($\Delta\Sigma$M), it is important to determine whether the motional RLC branch dominates the impedance at resonance, or if the capacitive component still has a low enough impedance to outweigh the RLC branch. In other words, one can distinguish two cases:

1) $R_m > \frac{1}{2\pi f_o C_p} = \frac{\sqrt{L_m C_m}}{C_p}$
2) $R_m < \frac{1}{2\pi f_o C_p} = \frac{\sqrt{L_m C_m}}{C_p}$

Based on this, one can decide to build a low-pass $\Delta\Sigma$M with current-mode feedback, if C_p dominates the impedance at resonance, or a band-pass $\Delta\Sigma$M with a voltage-mode feedback, if R_m has a lower impedance than C_p. These two cases will be analyzed in Sec. II-B and Sec. II-C.

B. Current-Feedback Mode

In certain types of ultrasound transducers, such as PMUTs [18] and some CMUTs, the transducer impedance at resonance is mainly dominated by C_p [20]. In such case, in order to suppress the noise near that frequency, one can exploit this large capacitance as an integration element to form a low-pass $\Delta\Sigma$ modulator (LPDSM). In this scenario, it is convenient to consider the current source I_{in} in Fig. 2 as the signal source. At resonance, the impedances of L_m and C_m cancel each other. Thus the current source sees a divider between R_m and C_p, where most of the current will flow into C_p. In this case, the feedback must also be provided in the current domain (I_{fb}), by means of a current DAC, so that C_p can be exploited as an integration element:

$$V_{transd.}(s) = I_{fb}\frac{1}{sC_p}\frac{(I_{in}-I_{fb})R_m C_m s + I_{in}(L_m C_m s^2+1)}{L_m C_m s^2 + R_m C_m s + 1 + \frac{C_m}{C_p}} \quad (1)$$

One can read out the resulting $V_{transd.}$ across C_p with a voltage amplifier, which offers a high impedance to the transducer, and digitize its output. The resulting system is shown in Fig. 4. Further integration stages can be added, if needed to achieve the SQNR specifications. However, (1) clearly shows the contributions of the RLC branch in the form of a resonance (numerator) and anti-resonance (denominator). This contribution should be mitigated in order to get a pure integration, else the obtained SQNR will be lowered. A compensation can be achieved by adding specific filters in the signal path before the quantizer, at the cost of increased system complexity. Alternatively, if C_p is sufficiently big, the SQNR degradation can be tolerated.

C. Voltage-Feedback Mode

In bulk piezoelectric transducers, instead, R_m generally has a lower impedance than C_p at resonance. This is the case for the transducer element that was used for our prototype chip, which shows an R_m of $\approx 8.2k\Omega$ and a C_p of $\approx 1.5pF$, corresponding to an impedance of $21.2k\Omega$ at resonance. Therefore, the chosen system architecture uses a voltage-feedback topology, in which the RLC branch is used to provide the noise shaping for a band-pass $\Delta\Sigma$ modulator (BPDSM). A band-pass ADC is desirable for the target application, as it is able to focus its performance on a specific band of interest (in this case, around the resonance frequency). Nyquist-rate ADCs and LPDSMs, in contrast, usually have a bandwidth that extends from DC to the upper edge of the band of interest, effectively wasting power over a bandwidth that does not contain any desirable information.

The signal source can be modeled as the voltage source V_{in} in Fig. 5. This time, because the resonance should be exploited, one must convey feedback in the voltage domain, by means of a DAC that provides a voltage V_{fb}, and read out the resulting current $I_{transd.}$, collected by the low-impedance input node of a transimpedance amplifier (TIA):

$$I_{transd.}(s) = \frac{(V_{in}-V_{fb})sC_m}{L_m C_m s^2 + R_m C_m s + 1} - V_{fb} s C_p \quad (2)$$

The first part of this equation shows the desired noise shaping, while the second part contains an undesired high-pass component, which needs to be compensated for. This issue will be addressed in Sec. III. The TIA's output voltage can be directly digitized by a quantizer, which in turn drives a DAC, connected to the TIA's non-inverting input. The negative feedback in the TIA ensures that also its inverting input and hence the transducer are driven by the DAC voltage V_{fb}. Exploiting the RLC branch as a noise shaping element is advantageous also because it guarantees that the low quantization noise zone is always matched with the transducer element resonance frequency, thus eliminating the need for calibration.

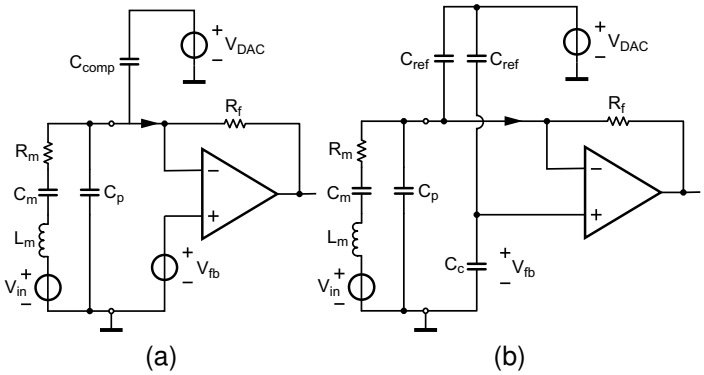


Fig. 6. Circuit diagram of the ADC's front-end with (a) a compensation capacitor and (b) a capacitive bridge configuration to compensate for the effect of C_p.

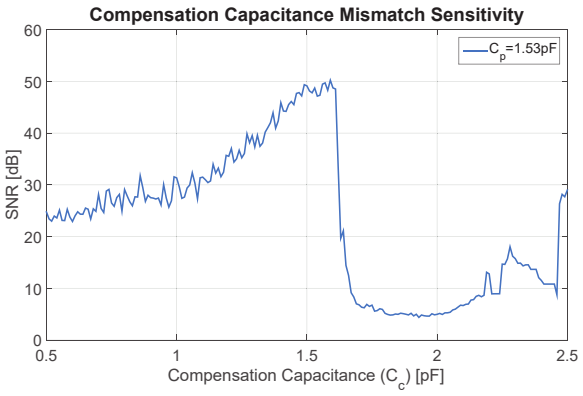


Fig. 7. System-level simulation of the effect of variations in C_c on the ADC's SNR, with a nominal C_p of 1.53pF.

III. Element-Level Design

The specifications for our prototype ADC were derived from our earlier work on 3D TEE probes [14]:

- The area should be 150µm × 150µm.
- The power consumption should be <1mW, allowing a high number of elements per chip (>1000) without prohibitive power consumption.
- The system bandwidth around the center frequency of 5MHz should be sufficient to capture the full bandwidth of the transducer. We design for a bandwidth of 75% to reflect a typical transducer bandwidth used for imaging, even if the bandwidth of our prototype transducers, as mentioned in Sec. II-A, is less.
- The target SNR is 50dB. Note that the SNR of the final image will be higher than that, as the correlated outputs of multiple elements are combined, while the noise is uncorrelated [21].

System-level behavioral simulations suggested that the noise shaping introduced by the transducer is sufficient to reach the target SNR, provided that a 3-bit quantizer and a sampling frequency of 200MHz are used. In the following sub-sections, the concepts needed to compose the final architecture will be discussed.

A. Capacitance Compensation

The effect of the parasitic capacitance C_p can be compensated for by adding another explicit capacitance (C_{comp} in Fig. 6a), driven by a second DAC, the output of which is a scaled version of the main one. A similar anti-resonance cancellation technique was employed in [22]. C_{comp} provides the current needed for C_p to be charged to the DAC's new level. In this solution, this current does not come from the TIA, therefore it does not cause a voltage drop across the feedback resistance.

In Fig. 6b, an improved version of the same solution is proposed: in this case, the two DACs are combined into a single DAC, which takes care of providing the feedback to the modulator, as well as performing the capacitance compensation as explained above.

The modulator feedback is obtained by a simple capacitive divider between C_{ref} and C_p, while a copy of C_{ref}, connected to the inverting input of the amplifier, provides the compensation current. This configuration is similar to the well-known Wheatstone bridge. The capacitance C_c should be tuned so that its value is the same as C_p. Thus, only the unbalance in the bridge, i.e. the current associated with the RLC branch, contributes to the output.

Unfortunately, this compensation scheme does introduce some vulnerabilities: if the current in C_c is larger in absolute value than the one which it should cancel, the feedback becomes positive and the modulator will quickly become unstable. The tuning range (50fF to 3.15pF) and LSB capacitance (50fF) of C_c should be sized to provides enough flexibility to face the variability of the transducer characteristics (the measured 1σ variation of C_p is 12%) and avoid positive feedback. The simulated sensitivity to the value of C_c is illustrated in Fig. 7. This figure also shows how the chosen LSB capacitance guarantees that the ADC operates in the narrow and flat high-SNR region. A non-negligible variability of C_p is expected not only between transducer elements belonging to different arrays, but even within the same acoustic stack. Therefore, each ADC has a dedicated trimming code for C_c, stored in a shift register when the chip is configured. Behavioural simulations show that the modulator is relatively robust to variability of R_m and the transducer's resonance frequency. Variations up to $\pm 20\%$ can be tolerated without trimming.

B. Time-Gain Compensation

In ultrasound systems, acoustic echoes originating from nearby tissues will reach the transducers earlier and will face low attenuation, while the waves scattered back by the farthest tissues will arrive later and be subject to more propagation attenuation. Therefore the ADC needs to handle large inputs at the beginning of the receive phase and small ones at its end. To compensate for this, the gain of the analog front-end can be increased dynamically as time progresses. This operation is referred to as Time-Gain Compensation (TGC), and it allows the system to feature an input dynamic range (i.e. the ratio between the highest and lowest signal that can be processed

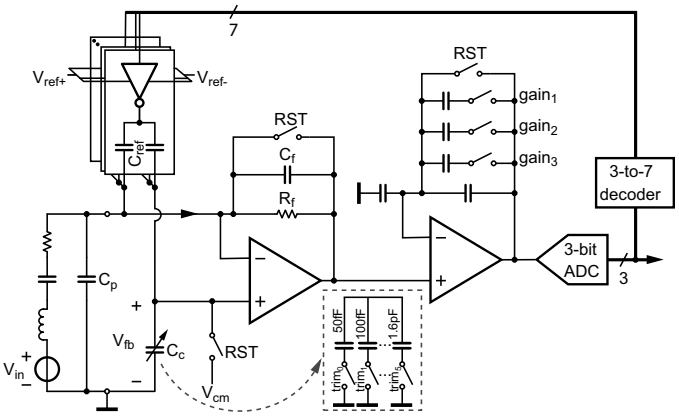


Fig. 8. Implemented ADC architecture.

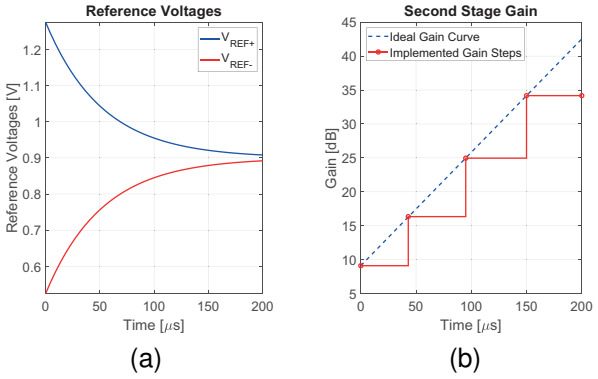


Fig. 9. (a) Time-varying reference voltages to implement TGC; (b) time-varying gain of the second-stage to maintain approximately constant loop gain during TGC.

by the ADC) significantly higher than its instantaneous output SNR [23].

In this system, the TGC is implemented by varying the DAC reference voltages V_{ref+} and V_{ref-} as a function of time, as shown in Fig. 9a. This has been realized by means of two off-chip 12-bit DACs, which could be integrated on-chip in a re-design. These DACs are updated 125 times during a 200μs receive phase, providing a resolution of 0.192dB/step. Thus, the full-scale of the ADC is adjusted dynamically as a function of time, as shown in Fig. 9a tracking the decreasing amplitude of the echo signals. To ensure that the loop gain in the $\Delta\Sigma$ loop and the voltage swing at the quantizer's input remain approximately constant as the reference voltages change, a second stage is added after the TIA to provide programmable gain. The gain is programmed by two control bits (decoded into four states) that change dynamically during the receive phase, as shown in Fig. 9b. The second stage gains are 9dB, 16dB, 24dB and 33dB.

C. Noise Filtering

The capacitance C_p in the transducer model introduces another issue to be solved: it high-pass filters the input-referred noise of the TIA. In order to mitigate this effect, a capacitor was placed in parallel with the TIA's feedback resistor. This adds a dominant pole and ensures that the noise gain at high frequencies flattens instead of continuing to ramp up. Additionally, the previously described second stage filters the high-frequency noise further. This stage has been implemented as a non-inverting amplifier, in order to keep its input capacitance as low as possible and thus avoid loading the first stage. The cut-off frequencies of the first and second stages (10MHz and 16MHz) are much lower than $\frac{f_s}{2}$ (100MHz), therefore limiting the achievable SQNR. However, because of the noise filtering, the resulting SNR is better than if a high-bandwidth stage would have been used. This can be seen as a trade-off between thermal noise filtering and quantization noise shaping.

Fig. 8 shows the final implemented block-level architecture. Reset switches (RST) provide the modulator with a known starting point, which force the non-inverting input of the TIA

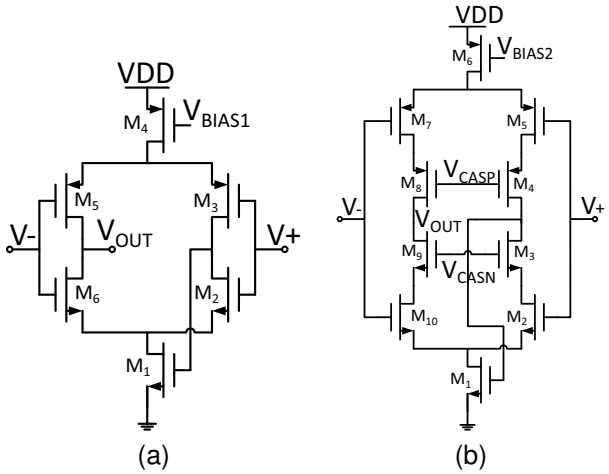


Fig. 10. Transistor-level schematic of the first (a) and second (b) stage OTAs.

to a known voltage and place the two stages in unity gain configuration. Further, the DAC is now shown in more detail: it is composed of 7 inverters, each driving two capacitors and supplied by two reference voltages V_{ref+} and V_{ref-}. These inverters are driven by the 7-bit thermometer code, decoded from the 3-bit quantizer output.

D. Implementation of the OTAs

The Operational Transimpedance Amplifier (OTA) employed for the TIA uses a current-reuse topology [24], as shown in Fig. 10a. This implementation was chosen for its current efficiency (NMOS and PMOS share the same current). This block consumes by far the highest amount of current from the analog supply (∼173μA), as its noise ultimately determines the ADC's SNR (see Fig. 15). The chosen topology relies on a local feedback which biases the bottom current source (M_1), so that no extra components are needed for a more complex common-mode feedback loop. The PMOS current source (M_4) is biased by a dedicated biasing circuit, implemented once per ADC, in order to improve the system's PSRR. The achieved g_m for each input transistor is 1.53mS, while the DC gain is 36dB. The first open-loop pole occurs at 36MHz. The closed-

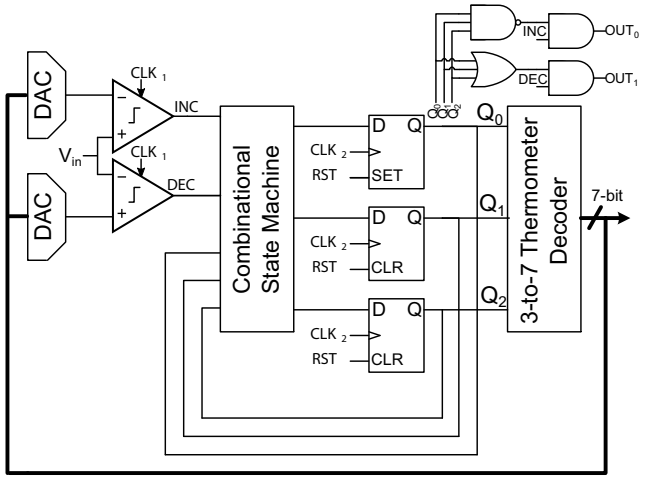


Fig. 11. Block-level schematic of the implemented tracking quantizer.

loop pole is determined by R_f and $C_f + C_{gd,5} + C_{gd,6}$ and is fixed at 10MHz. R_f has a value of $100k\Omega$: a lower value would introduce excessive thermal noise (see Fig. 15), while a higher value would yield a high input impedance, as the open-loop gain is only 36dB, leading to signal attenuation.

The second-stage OTA employs a similar current-reuse topology as the one discussed above. As the closed-loop gain of this stage, for the highest gain setting, is 33dB, the OTA's open loop gain should be more than 20dB more. Therefore, the input transistors were cascoded to achieve a better gain accuracy. This stage consumes 44μA from the analog supply and introduces a closed-loop pole at 16MHz, due to the intrinsic bandwidth limitation of the OTA.

E. Quantizer Architecture

Implementing a 3-bit flash quantizer would require the use of 7 comparators, all clocked at f_s=200MHz, yielding a prohibitive power consumption. A SAR quantizer, on the other hand, would require a single comparator to be clocked at 600MHz, a quite impractical frequency for a 0.18μm technology.

The implemented 3-bit quantizer uses a tracking architecture instead [25]. In the specific implementation that was adopted in this design, shown in Fig. 11, only two comparators are employed: the purpose they serve is to keep the input signal between an upper and a lower reference voltage, provided by two DACs. At every clock cycle, after the comparators' decision, a purely combinational state machine computes the new 3-bit value based on the comparators' decision and the quantizer's output from the previous cycle. Three D-flip-flops are then clocked by a delayed version of the comparators' clock (CLK_2), and save the new digital output. The three flip-flops are followed by a binary-to-thermometer decoder, which drives the two quantizer DACs and the overall $\Delta\Sigma$ feedback. The comparator outputs contain all the necessary information to reconstruct the internal 3-bit word. An overload protection circuit gates the comparator outputs so that if the input signal goes beyond the quantizer full scale, the outputs will not be updated any more.

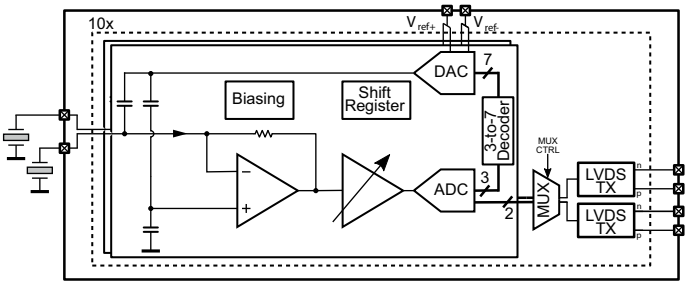


Fig. 12. Block diagram of the prototype chip.

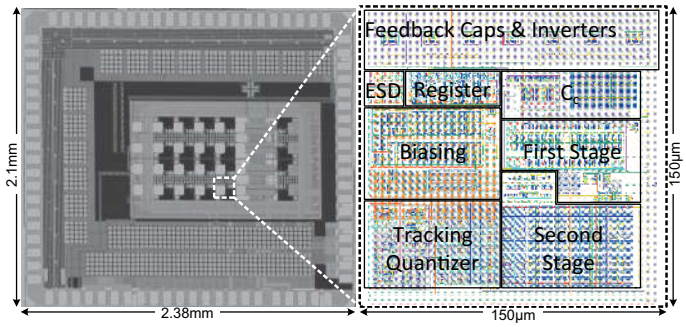


Fig. 13. Chip micrograph and element layout.

A downside of this particular topology is that the output cannot change by more than one LSB per cycle, therefore fast signals cannot be tracked properly and slope-overload distortion is introduced [26]. In order for the quantizer to work properly, the maximum slope of the input signal should be lower than the LSB divided by the sampling period.

Fortunately, as discussed in Sec. III-C, the bandwidths of the two stages do not reach the Nyquist frequency (f_N). For this reason, the modulator follows the ideal noise shaping behavior only up to ∼20MHz. Because of this relatively low bandwidth in comparison to the high sampling frequency (needed to reach the target SQNR), the system is not as chaotic as one would expect from a second-order BPDSM. Indeed, it was found from system-level simulations that the probability for the ADC output to change by more than 1 LSB per cycle is only 0.005%. This justifies the use of a tracking quantizer and explains why slope overload distortion does not limit the performance in this system.

The implemented $\Delta\Sigma$ ADC is very robust to jitter, as the target SNR is relatively low and a multi-bit quantizer was employed [27]. System-level simulations suggest that the system can tolerate a jitter of $\sigma_j = 411$ps without a noticeable SNR drop. For similar reasons, the system is very robust to excess loop delay (ELD), as system-level simulations suggest that it can withstand a delay in the feedback branch as high as $\frac{1.8}{f_s}$.

IV. Chip-Level Design

In order to prove the proposed architecture, a prototype chip was fabricated in TSMC 0.18μm technology. A block diagram of the chip is show in Fig. 12. It hosts a 5 × 4 array of the previously described ADCs. Each modulator produces two 200MHz bitstreams, taken at the quantizer comparators' outputs, giving a total of 40 digital bitstreams. In order to

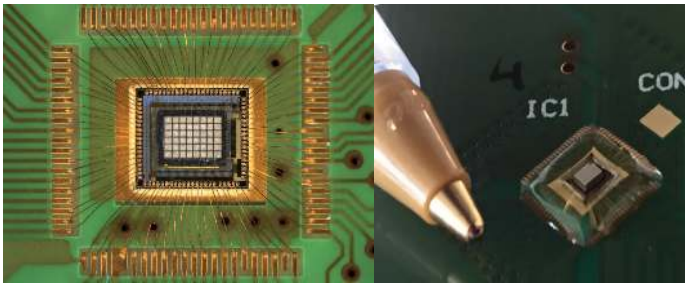


Fig. 14. Photo of the prototype array built on top of the ASIC (before applying the ground foil, which forms the common counter-electrode of the transducer elements).

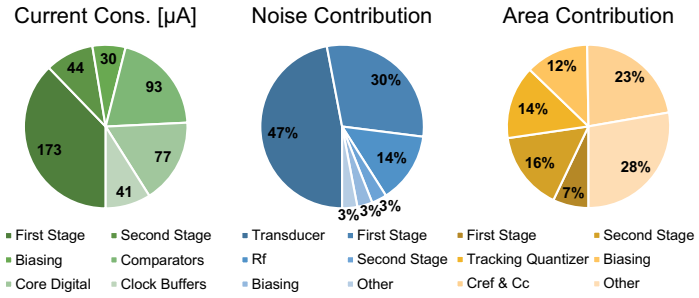


Fig. 15. Pie charts showing the current consumption (a), noise (b) and area (c) contributions for the element-level ADC.

achieve maximum flexibility and reduce the design time, on-chip decimation has not been implemented. Instead, 20 LVDS transmitters were included on chip. A 2:1 multiplexing scheme, implemented in order to reduce the amount of I/Os required, allows to read out either the top or the bottom half of the array. An FPGA samples the high-speed bitstream coming from the chip and sends it to a computer for further processing.

Fig. 13 shows a chip micrograph along with the element-matched layout of the ADC. The chips to be tested had PZT transducers built on top of them, so that their acoustic performance could be fully evaluated (see Fig. 14). The transducer integration process is described in [14]. Four transducer elements were wired directly to the pad-ring, allowing them to be driven by an off-chip pulser, thus enabling pulse-echo measurements.

In a future re-design, it is desirable to also integrate TX/RX switches and transmit circuitry. This causes additional constraints for the ADC in terms of area, that could be addressed by choosing a smaller feature size or reducing the area of the second stage feedback and the biasing circuit. Another option would be to include TX-only elements in a specific geometry, as has been demonstrated in [4], [7] and [14] without compromising the RX-element area, noise or power.

V. Measurement Results

The chip described above was tested to verify its functionality, both with an electrical and an acoustic input signal. In order to do that, the chip, with the transducer array on top, was bonded on a daughter-board, which in turn can be plugged on a bigger motherboard, hosting all the necessary components for

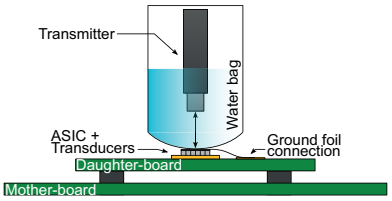


Fig. 16. Artist impression of the employed acoustic measurement setup. The medium is water and the distance between the acoustic stack and the transmitter is approximately 2-3 cm.

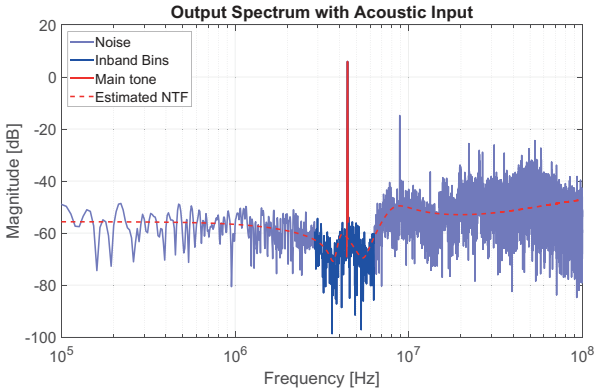


Fig. 17. FFT of the ADC's measured bitstream compared to the estimated NTF based on a Butterworth-Van Dyke model of the measured impedance of the transducer. The center frequency is slightly shifted because of the uncertainties linked to transducer fabrication.

testing. For acoustic measurements, a plastic bag with water was placed in contact with the transducer array, while a 5MHz unfocused ultrasound transmitter was placed into the water, generating an acoustic wave traveling towards the transducer array, as can be seen in Fig. 16. The water inside the plastic bag mimics the acoustic impedance that a probe would be subject to while operating inside the human body.

Fig. 17 shows the FFT of the modulator output bitstream. The bandpass characteristic is evident, as the quantization noise is low in the bandwidth of interest (around 5MHz) and higher everywhere else. In particular, two dips are recognizable next to the main tone at 3.75MHz and 5.65MHz. Although the system was designed accounting for a single resonance around 5MHz, it proves to be robust enough to provide the desired noise shaping. The modulator's noise transfer function (NTF) was estimated using a linear model and the measured values of the lumped components in the Butterworth-Van Dyke model (using two RLC branches). As shown in Fig. 17, this estimation is in good agreement with the noise shaping observed in the measured FFT.

Compared to the measured impedance characteristic shown in Fig. 3, an additional resonance at 3.75MHz is observed, which is likely due to the acoustic interface between the transducer and the plastic water bag, and shifts the main resonance to a slightly higher frequency of 5.65 MHz. As mentioned in Sec. III-C, the noise shaping is only visible until around 20MHz because of the bandwidth limitations of the two stages. The second-order distortion peak is at -20dBFS, which is in line with simulations. The distortion is not a problem for

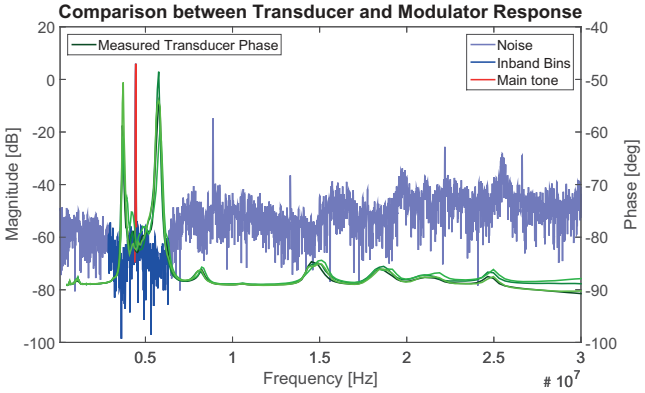


Fig. 18. Details of the measured noise shaping, correlated with the transducer impedance measurement.

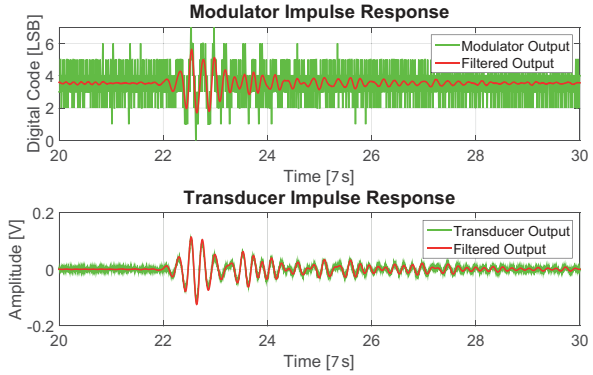


Fig. 19. Time-domain response of the ADC to an acoustic pulse compared with that of the transducer. Measured in water at a distance of 2-3 cm.

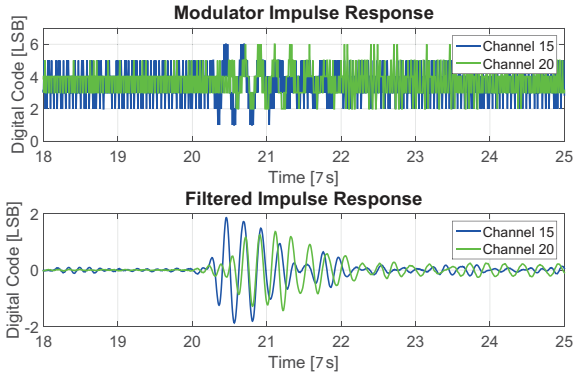


Fig. 20. Measured response from two elements, with an angled acoustic wave incoming. The two reported channels are located on opposite sides of the array. The x-axis refers to the start time of the TX pulse.

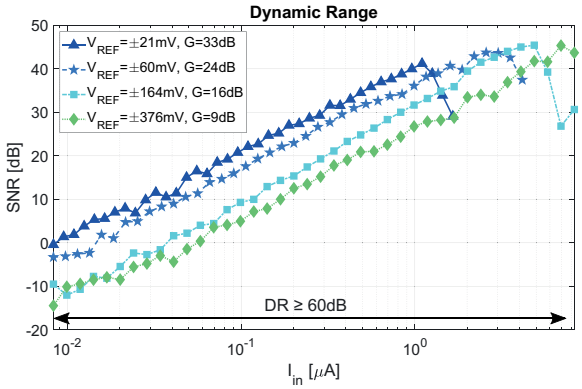


Fig. 21. Measured dynamic range for all TGC steps. V_{REF} is the distance of V_{REF+} and V_{REF-} from the common mode level (0.9V), while G is the second stage gain.

fundamental imaging, and is suppressed by the decimation filter, which is implemented in software for this prototype. The measured SNR is 45dB, 47dB, 45dB and 41dB for the four TGC steps (i.e. gain settings of the second stage). The lower SNR in the last TGC step is likely due to noise coming from the off-chip reference voltages V_{ref+} and V_{ref-}, generated by monolithic DACs on the test PCB.

In Fig. 18 the modulator output's FFT is shown together with the measured phase of the transducer impedance. The correlation between the two plots is evident. In particular, the two peaks in the bandwidth of interest occur at the same frequency. Moreover, the transducer's high frequency peaks are also visible in the modulator output. From this, one can conclude that the PZT element is really acting as a noise shaping element for the implemented $\Delta\Sigma$ ADC.

Shifting the focus to the time-domain (see Fig. 19), one can compare the ADC's response to an acoustic pulse with the same element's TIA analog output, with the ADC feedback disabled. In the latter case, the TIA provides an amplified version of the transducer's output voltage. The two responses show a clear correlation, although they are not perfectly identical. A possible explanation for this effect is that when the modulator's feedback is applied, the termination condition for the transducer is different. The correlation is clearer comparing the two filtered outputs. Here, a software high-order FIR filter is applied to both signals.

In an additional experiment, the ultrasound transmitter was placed in a tilted position with respect to the transducer array, so that the acoustic wave would reach different elements at different times. In this experiment, the responses of two elements at the opposite sides of the array are compared, as shown in Fig. 20. The delay between the two responses is evident and in agreement with expectations. Cross-talk between elements has not been evaluated for this design, but is expected to be dominated by acoustic crosstalk rather than electrical cross-talk between element-level ADCs.

Given that the elements act as loop filters in this design, some additional cross-talk may occur due to coupling of quantization noise between different modulators in the array. However, the amplitude of the parasitic transmission caused by the feedback DAC forcing a voltage on the transducer is orders of magnitude lower than the voltage levels used in traditional TX pulsers. The complete evaluation of this phenomenon is a topic for future investigation.

Fig. 21 shows the measured dynamic range (DR) for four different values of the DAC reference voltages, corresponding to four points in the TGC range. The quantity on the x axis is the TIA's input current, which was injected by a function generator through an on-chip capacitor. Because of the limited

TABLE I
COMPARISON OF THIS WORK WITH SIMILAR PUBLICATIONS.

	This Work	[6]	[11]	[28]	[29]	[30]	[31]
Transducer Type	PZT	CMUT	N/A	N/A	N/A	N/A	CMUT
Architecture	CTBPDSM[1]	DTLPDSM[2]	SAR[3]	CTBPDSM[1]	CTLPDSM[4]	CTLPDSM[4]	CTLPDSM[4]
Technology [nm]	180	28	130	65	65	130	180
No. of Channels	20	16	64	8	1	128	1
Element Matched [μm]	Yes (150)	Yes (250)	No	No	No	No	No
Center Freq. [MHz]	5	5	5	260	4	2.5	2
Bandwidth [MHz]	3.125-6.875	10	8	20	15	10	8
Area/Channel [mm2]	0.025	0.0625	0.1	0.03	0.4	-	0.177
Power/Channel [mW]	0.8	17.5	6.32	13.1	6.96	30.1	3.01
SNR/Channel [dB]	47	60	48.5	54	74.6	65	71
FOM_W [pJ/conv.]	0.58	1.1	1.8	0.8	0.053	1	0.065

[1]Continuous-Time Band-Pass $\Delta\Sigma$ Modulator
[2]Discrete-Time Low-Pass $\Delta\Sigma$ Modulator
[3]Successive Approximation Register
[4]Continuous-Time Low-Pass $\Delta\Sigma$ Modulator

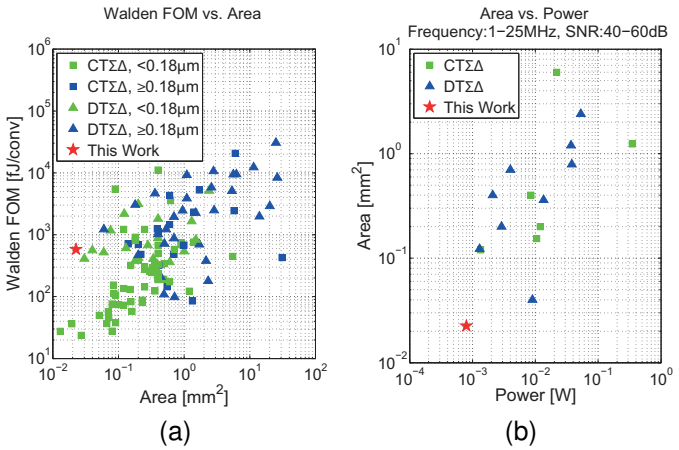


Fig. 22. Comparison of this work's FOM and Power vs. active area with designs published at ISSCC and VLSI [32].

range of the function generator, the point where the DR plot flattens cannot be measured for the high gain configuration. However, one can conclude that the dynamic range, accounting for the time-gain compensation, exceeds three decades (60dB).

Table I compares this work with recently published ultrasound ADCs. As this design uses the ultrasound transducer as the loop filter for a BPDSM, the area typically reserved for the reactive components in standard loop filters is saved. This allows the designed converter to be very competitive in terms of area. The chip consumes 0.8 mW per channel from a 1.8 V supply. This is an order of magnitude lower than the state of the art, even if it achieves a worse SNR. The achieved Walden Figure of Merit (FOM_W), defined as:

$$FOM_W = \frac{Power}{\frac{f_s}{OSR} 2^{\frac{SNR-1.76}{6.02}}} \tag{3}$$

is in line with the state of the art.

Fig. 22a shows a performance comparison between this work and other $\Delta\Sigma$ modulators published in two of the most important circuit conferences. The green markers show designs that use a feature size smaller than 0.18µm, while the blue ones represent modulators employing a 0.18µm technology or an older one. The x-axis represents the area, while on the y-axis, the Walden figure of merit is shown.

A general trend can be identified, which associates a lower active area with a smaller FOM. This work achieves by far the lowest area compared to designs using a similar technology. Furthermore, only two of the converters employing a smaller feature size achieve a lower area. The Walden FOM, while being more than one decade above the state of the art, can still be considered as a competitive result. This is because the implemented $\Delta\Sigma$ADC also incorporates the functionality usually provided by the analog front-end (AFE) placed before the ADC, i.e. low-noise amplification and TGC.

Furthermore, in the current implementation, 50% of the power goes to the digital core and the comparators, which would benefit greatly from a smaller feature-size technology (see Fig. 15). Finally, Fig. 22b shows a direct comparison between area and power consumption, for modulators with similar SNR and bandwidth, using any technology node. This work features the lowest area, as well as the smallest power consumption among all the designs.

VI. CONCLUSION

This work has introduced a way to digitize the signal received by an ultrasound transducer element in a power- and area-efficient manner. In particular, this concept has been demonstrated using a 150 µm-pitch 2D array of 5MHz PZT transducer elements, paving the way towards full in-probe digitization in endoscopic and catheter-based ultrasound probes. Combined with a high-speed data-link, the described method could lead to a significant cable-count reduction in such probes, and thus a narrower, less invasive shaft without impairing the image quality.

The employed approach consists in using a piezo-electric transducer element not only as a signal source, but also as the electro-mechanical loop filter of a bandpass $\Delta\Sigma$ modulator, thus reducing to a minimum the amount of circuitry needed for the signal digitization. As a matter of fact, most of the analog blocks in the previously described system are common to most of the ultrasound front-ends found in literature (e.g. the TIA and the PGA), while the feedback DAC and compensation

capacitance, which were added for this design, do not significantly contribute to the power and area budgets. The same technique could be similarly applied to ultrasound systems employing different transducer types (e.g. CMUT, PMUT), as well as to other application domains where the sensor shows a similar frequency response.

REFERENCES

[1] I. O. Wygant, X. Zhuang, D. T. Yeh, Ö. Oralkan, A. S. Ergun, M. Karaman, and B. T. Khuri-Yakub, "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 55, no. 2, pp. 327–341, 2008.

[2] Q. Liu, C. Chen, Z. Y. Chang, C. Prins, and M. A. P. Pertijs, "A mixed-signal multiplexing system for cable-count reduction in ultrasound probes," *IEEE International Ultrasonics Symposium,*, pp. 1–4, 2015.

[3] T. M. Carpenter, M. W. Rashid, M. Ghovanloo, D. M. Cowell, S. Freear, and F. L. Degertekin, "Direct digital demultiplexing of analog TDM signals for cable reduction in ultrasound imaging catheters," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 8, pp. 1078–1085, 2016.

[4] C. Chen, Z. Chen, D. Bera, S. B. Raghunathan, M. Shabanimotlagh, E. Noothout, Z. Y. Chang, J. Ponte, C. Prins, H. J. Vos, J. G. Bosch, M. D. Verweij, N. De Jong, and M. A. Pertijs, "A Front-End ASIC with Receive Sub-array Beamforming Integrated with a 32 x 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 994–1006, 2017.

[5] Y. Katsube, S. Kajiyama, T. Nishimoto, T. Nakagawa, Y. Okuma, Y. Nakamura, T. Terada, Y. Igarashi, T. Yamawaki, T. Yazaki, Y. Hayashi, K. Amino, T. Kaneko, and H. Tanaka, "Single-chip 3072ch 2D array IC with RX analog and all-digital TX beamformer for 3D ultrasound imaging," *IEEE International Solid-State Circuits Conference*, vol. 60, pp. 458–459, 2017.

[6] M.-C. Chen, S.-R. Kothapalli, P. Cathelin, A. Cathelin, S. S. Gambhir, and B. Murmann, "A Pixel-Pitch-Matched Ultrasound Receiver for 3D Photoacoustic Imaging with Integrated Delta-Sigma Beamformer in 28nm UTBB FDSOI," *IEEE International Solid-State Circuits Conference*, pp. 456–458, 2017.

[7] C. Chen, Z. Chen, D. Bera, E. Noothout, Z. Y. Chang, H. Vos, J. Bosch, M. Verweij, N. De Jong, and M. Pertijs, "A 0.91mW/Element Pitch-Matched Front-End ASIC with Integrated Subarray Beamforming ADC for Miniature 3D Ultrasound Probes," *IEEE International Solid-State Circuits Conference*, 2018.

[8] J. A. Jensen, S. I. Nikolov, K. L. Gammelmark, and M. H. Pedersen, "Synthetic aperture ultrasound imaging," *Ultrasonics*, vol. 44, pp. e5–e15, 2006.

[9] G. Montaldo, M. Tanter, J. Bercoff, N. Benech, and M. Fink, "Coherent plane-wave compounding for very high frame rate ultrasonography and transient elastography," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 56, no. 3, pp. 489–506, 2009.

[10] J. Y. Um, E. W. Song, Y. J. Kim, S. E. Cho, M. K. Chae, J. Song, B. Kim, S. Lee, J. Bang, Y. Kim, K. Cho, B. Kim, J. Y. Sim, and H. J. Park, "An analog-digital-hybrid single-chip RX beamformer with non-uniform sampling for 2D-CMUT ultrasound imaging to achieve wide dynamic range of delay and small chip area," *IEEE International Solid-State Circuits Conference*, vol. 57, pp. 426–427, 2014.

[11] Y.-J. Kim, S.-E. Cho, J.-Y. Um, M.-K. Chae, J. Bang, J. Song, T. Jeon, B. Kim, J.-Y. Sim, and H.-J. Park, "A Single-Chip 64-Channel Ultrasound RX-Beamformer Including Analog Front-End and an LUT for Non-Uniform ADC-sample-clock Generation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 1, pp. 87–97, 2017.

[12] M. Tan, C. Chen, Z. Chen, J. Janjic, V. Daeichin, Z. Y. Chang, E. Noothout, G. Van Soest, M. Verweij, N. De Jong, and M. Pertijs, "A front-end ASIC with high-voltage transmit switching and receive digitization for forward-looking intravascular ultrasound," *Proceedings of the Custom Integrated Circuits Conference*, pp. 1–4, 2017.

[13] M. D'Urbino, C. Chen, Z. Chen, Z.-y. Chang, J. Ponte, B. Lippe, and M. Pertijs, "An Element-Matched Band-Pass Delta-Sigma ADC for Ultrasound Imaging," *IEEE Asian Solid-State Cirtuits Conference*, vol. 2, pp. 137–140, 2017.

[14] C. Chen, S. B. Raghunathan, Z. Yu, M. Shabanimotlagh, Z. Chen, Z.-y. Chang, S. Blaak, C. Prins, J. Ponte, E. Noothout, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, "A Prototype PZT Matrix Transducer With Low-Power Integrated Receive ASIC for 3-D Transesophageal Echocardiography," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 1, pp. 47–59, 2016.

[15] A. Spineanu, P. Bénabès, and R. Kielbasa, "A digital piezoelectric accelerometer with sigma-delta servo technique," *Sensors Actuators A Phys.*, vol. 60, pp. 127–133, 1997.

[16] S. Sutula, J. Pallares Cuxart, J. Gonzalo-Ruiz, F. X. Munoz-Pascual, L. Teres, and F. Serra-Graells, "A 25- μW All-MOS potentiostatic delta-sigma ADC for smart electrochemical sensors," *IEEE Transactions on Circuits and Systems*, vol. 61, no. 3, pp. 671–679, 2014.

[17] K. A. A. Makinwa and J. H. Huijsing, "A Smart Wind Sensor using Time-Multiplexed Thermal $\Sigma\Delta$ Modulators Thermal $\Sigma\Delta$ modulation," *European Solid-State Circuits Conference*, pp. 452–455, 2001.

[18] Y. Qiu, J. V. Gigliotti, M. Wallace, F. Griggio, C. E. Demore, S. Cochran, and S. Trolier-McKinstry, "Piezoelectric micromachined ultrasound transducer (PMUT) arrays for integrated sensing, actuation and imaging," *Sensors (Switzerland)*, vol. 15, no. 4, pp. 8020–8041, 2015.

[19] H. Jin, S. Dong, J. Luo, and W. Milne, "Generalised Butterworth-Van Dyke equivalent circuit for thin-film bulk acoustic resonator," *Electronics Letters*, vol. 47, no. 7, p. 424, 2011.

[20] I. Wygant, "A comparison of CMUTs and piezoelectric transducer elements for 2D medical imaging based on conventional simulation models," *IEEE International Ultrasonics Symposium*, pp. 100–103, 2011.

[21] P. L. Muntal, K. Faerch, I. H. Jorgensen, and E. Bruun, "System level design of a continuous-time $\Delta\Sigma$ modulator for portable ultrasound scanners," *Nordic Circuits and Systems Conference & International Symposium on System-on-Chip*, pp. 1–4, 2015.

[22] R. Yu and Y. P. Xu, "A 47.3-MHz SAW resonator based CMOS second-order bandpass sigma-delta modulator with 54-dB peak SNDR," *Proceedings of the Custom Integrated Circuits Conference*, no. 1, pp. 204–207, 2005.

[23] J. Yao, Z. Yu, M. Pertijs, G. Meijer, C. Lancée, J. Bosch, and N. De Jong, "Design of a low power time-gain-compensation amplifier for a 2D piezoelectric ultrasound transducer," *IEEE International Ultrasonics Symposium*, pp. 841–844, 2010.

[24] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, 1991.

[25] L. Dörrer, F. Kuttner, P. Greco, P. Torta, and T. Hartig, "A 3-mW 74-dB SNR 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2416–2426, 2005.

[26] M. Trakimas and S. Sonkusale, "An Adaptive Resolution Asynchronous ADC Architecture for Data Compression in Energy Constrained Sensing Applications," *IEEE Transactions on Circuits and Systems*, vol. 60, no. 4, pp. 1097–1099, 2011.

[27] M. Ortmanns and F. Gerfers, "Continuous-Time Sigma-Delta A/D Conversion," 2005.

[28] J. Jeong, N. Collins, and M. P. Flynn, "A 260 MHz IF Sampling Bit-Stream Processing Digital Beamformer With an Integrated Array of Continuous-Time Band-Pass Delta-Sigma Modulators," *IEEE Journal of Solid-State Circuits*, pp. 1–9, 2016.

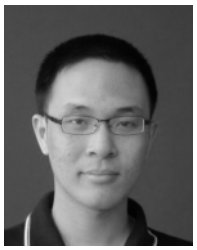
[29] Y. Zhang, C.-H. Chen, T. He, and G. C. Temes, "A Continuous-Time Delta-Sigma Modulator for Biomedical Ultrasound Beamformer Using Digital ELD Compensation and FIR Feedback," *IEEE Transactions on Circuits and Systems*, vol. 62, no. 7, pp. 1689–1698, 2015.

[30] M. K. Chirala, P. Huynh, J. Ryu, and Y. H. Kim, "A 128-ch Delta-Sigma ADC based mixed signal IC for full digital beamforming Wireless handheld Ultrasound imaging system," *IEEE Engineering in Medicine and Biology Society*, pp. 1339–1342, 2015.

[31] T.-C. Cheng and T.-H. Tsai, "CMOS Ultrasonic Receiver with On-Chip Analog-to-Digital Front End for High-Resolution Ultrasound Imaging Systems," *IEEE Sensors Journal*, vol. 16, no. 20, pp. 7454–7463, 2016.

[32] B. Murmann, "ADC Performance Survey 1997-2016," 2016. [Online]. Available: http://web.stanford.edu/ murmann/adcsurvey.html

Michele D'Urbino received his B.Sc. degree in biomedical engineering from Politecnico di Milano, Milan, Italy, in 2014 (*cum laude*) and his M.Sc. in microelectronics from the Electronic Instrumentation Laboratory, TU Delft, Delft, the Netherlands, in 2017. He was a Design Engineer at Caeleste, Mechelen, Belgium, where he worked on high-speed imaging sensors. Since December 2017 he is employed at the Delft-based branch of SiTime Corporation as an Analog/Mixed-Signal Design Engineer, working on nano-power analog building blocks for MEMS-based timing integrated solutions. His main research interests are low-area and -power data converters, high-speed Delta-Sigma modulation and novel sensor analog front-ends. He was the recipient of the A-SSCC 2017 best student paper award.



Chao Chen (S'12M'17) received the B.Sc. degree in microelectronics from Tsinghua University, Beijing, China, in 2010, and the M.Sc. (*cum laude*) and Ph.D. degrees in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2012 and 2018, respectively. His Ph.D. research topic was front-end application-specified integrated circuit (ASIC) design for 3D medical ultrasound imaging. Since November 2017, he has been a Senior Analog IC Designer with Butterfly Network Inc., Guilford, CT, USA, where he continues his research in the design of ASICs for next-generation medical ultrasound systems. His current research interests include integrated circuits for medical ultrasound imaging, low-power sensor interfaces, and data converters. Dr. Chen was a recipient of the Huygens Scholarship in 2011, the ISSCC 2013 STGA Award, and the winner of the IEEE IUS 2017 Student Paper Competition Award. He was a co-recipient of the A-SSCC 2017 Best Student Paper Award.

Zhao Chen received the B.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2011, and the M.Sc. degree in electrical and electronic engineering from Imperial College, London, U.K., in 2012. He is currently pursuing the Ph.D. degree in electrical engineering at the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands. His Ph.D. research is focused on ASIC design for 3-D medical ultrasound imaging. His current research interests include analog and mixed-signal electronics, especially for biomedical application.

Zu-Yao Chang received the M.Sc. degree in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2003. Since 2003, he has been a Staff Member with the Electronic Instrumentation Laboratory, Delft University of Technology, working on impedance measurement systems and smart sensor systems.

Jacco Ponte was born in Dordrecht, the Netherlands, in 1971. After a technical education in precision Mechanics and Material Science (and later Mechatronics), he worked as a Technician with the Dutch Cancer Institute, Amsterdam, the Netherlands. Then, he worked as a Service Engineer on ophthalmic instruments for examination and treatment of the human eye. Since 2002, he works as a Mechanical Engineer with Oldelft Ultrasound, Delft, the Netherlands, where he is working on the mechanical part of transducer building and design.

Boris Lippe was born in Berlin (Germany) in 1981. He received the B.E. and M.E. degrees from Technical University Berlin, 2003 and 2006. He joined Oldelft Ultrasound, Delft, The Netherlands, in 2014, and is working as an mixed signal ASIC developer. His main areas of expertise and research interest are digitally controlled analog circuits (mixed-signal processing) in the field of integrated circuits for medical and industrial ultrasound applications.

Michiel A. P. Pertijs (S'99-M'06-SM'10) received the M.Sc. and Ph.D. degrees in electrical engineering (both *cum laude*) from Delft University of Technology, Delft, The Netherlands, in 2000 and 2005, respectively. From 2005 to 2008, he was with National Semiconductor, Delft, where he designed precision operational amplifiers and instrumentation amplifiers. From 2008 to 2009, he was a Senior Researcher with imec / Holst Centre, Eindhoven, The Netherlands. In 2009, he joined the Electronic Instrumentation Laboratory of Delft University of Technology, where he is now an Associate Professor. He heads a research group focusing on integrated circuits for medical ultrasound and energy-efficient smart sensors. He has authored or co-authored two books, three book chapters, 12 patents, and over 80 technical papers. Dr. Pertijs served as an Associate Editor of the IEEE Journal of Solid-State Circuits (JSSC). He is a member of the technical program committee the European Solid-State Circuits Conference (ESSCIRC), and also served on the program committees of the International Solid-State Circuits Conference (ISSCC) and the IEEE Sensors Conference. He received the ISSCC 2005 Jack Kilby Award for Outstanding Student Paper and the JSSC 2005 Best Paper Award. For his Ph.D. research on high-accuracy CMOS smart temperature sensors, he received the 2006 Simon Stevin Gezel Award from the Dutch Technology Foundation STW. In 2014, he was elected Best Teacher of the EE program at Delft University of Technology.