Open access • Journal Article • DOI:10.1109/66.843637

An empirical three-dimensional crossover capacitance model for multilevel interconnect VLSI circuits — Source link

Shyh-Chyi Wong, Trent Gwo Yann Lee, Dye-Junn Ma, Chuan-Jane Chao

Institutions: National Chiao Tung University, National Chung Hsing University

Published on: 01 May 2000 - IEEE Transactions on Semiconductor Manufacturing (IEEE)

Topics: Capacitance and Crossover

An Empirical Three-Dimensional Crossover Capacitance Model for Multilevel Interconnect VLSI Circuits

Shyh-Chyi Wong, Trent Gwo-Yann Lee, Dye-Jyun Ma, and Chuan-Jane Chao

***Abstract*—We develop an empirical model for the crossover capacitance induced by the wire crossings in VLSI with multilevel metal interconnects. The crossover capacitance, which is formed in any three adjacent layers and of a three-dimensional (3-D) nature, is derived in closed form as a function of the wire geometry parameters. The total capacitance on a wire passing many crossings can then be easily determined by combining the crossover capacitance with the two-dimensional (2-D) intralayer coupling capacitance defined on a same layer. The model agrees well with the numerical field solver (with a 6.7% root-mean-square error) and measurement data (with a maximum error of 4.17%) for wire width and spacing down to 0.16 μm and wire thickness down to 0.15 μm. The model is useful for VLSI design and process optimization.**

***Index Terms*—Closed-form models, crossover capacitance, multilevel interconnects, VLSI circuits.**

I. Introduction

DEEP submicrometer integrated circuit performance is influenced by interconnect RC delay [1]–[3]. Although the device delay decreases as the technology scales down, the interconnect-induced delay, however, increases, because both line resistance and intralayer capacitance increase [1], [2], [4]. In VLSI circuits with multilevel interconnects, lines in adjacent metal layers are placed orthogonally to each other to minimize overlapped capacitances and enhance routing flexibility. This procedure forms many wire crossings, inducing crossover capacitance, which becomes the major factor in affecting the circuit speed [2], [5]. An accurate model for the crossover capacitance is essential for estimating the interconnect circuit performance.

Many previous works on interconnects exist in the literature. The works of [3], and [5]–[7] either considered two-dimensional (2-D) structures or approximated the three–dimensional (3-D) wirings by 2-D cross sections; both approaches cannot model 3-D fringe field. The models of [5]–[7] were based on numerical solutions, thus not allowing for closed-form estimation. The work of Chern [2] gave a crossover model for triple-level metal layers but with same thickness in all layers. The work of Pan *et al.* [8] derived an analytical expression for crossover capacitance specifically for packaging geometries. The work of Kuhn *et al.* [9] gave an optimization study for delay time and power dissipation using combined device and interconnect capacitances; it, however, ignored both intralayer coupling and crossover capacitances that are important in deep submicron VLSI. The work of Vladimir and Mittra [10] gave improved boundary conditions for numerical solution of interconnect and packaging capacitances. Some other works focused on novel measurement methods for extracting interconnect capacitance on various layout structures. For instance, the work of Wee *et al.* [11] developed a complete set of structures for characterizing multilevel metal capacitances for both stack and crossing configurations; the impact of metal-edge slope and void was also extracted. The work of Nouet and Toulouse [12] characterized interlayer and intralayer capacitance novel test patterns, and compared on-chip and off-chip measurement. In [12], it was identified that the 3-D crossings (crossover) is a critical component in the total wiring capacitance, and a linear model with different components was then proposed with linear dependence on area, periphery length, and spacing. The work of Aoyama *et al.* [13] characterized coupling and ground capacitance using test patterns and numerical solutions, and it provided an optimization study by wire pitch to dielectric thickness ratio. The work of Chao *et al.* [14] presented a novel extraction methodology and test pattern, with verifications on SOG and CMP processes. The work of Chen *et al.* [15] gave a novel on-chip measurement method for small wire capacitance. In [16], we developed models for 2-D wiring capacitance, wire delay, and interwire cross-talk noise. The capacitance model of [16] gives accurate intralayer and line-to-ground capacitance estimation for both parallel lines on a plane and lines between two planes, with agreement with measurement data.

In this paper, we continue our previous effort of [16] by focusing on the modeling of crossover capacitance for VLSI's with multilevel metal interconnect of arbitrary dielectric and wire thickness, width, and spacing in all layers. The crossover capacitance is formed in any three adjacent layers of the multilevel metal interconnects and is of a 3-D nature. We derive closed-form formula for the crossover capacitance as a function of the wire geometry parameters of three adjacent layers, including the wire width, spacing, thickness, and dielectric thickness of a line and of lines in the upper and lower layers. The total net capacitance on a wire passing many crossings can then be easily obtained by combining the crossover capacitance with the 2-D intralayer coupling capacitance defined on a same layer

Manuscript received May 8, 1999; revised November 15, 1999.

S.-C. Wong is with the Research Development, Taiwan Semiconductor Manufacturing Corporation, Hsinchu, Taiwan, ROC.

T. G.-Y. Lee is with the Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, ROC.

D.-J. Ma is with the Department of Electrical Engineering, National Chung-Hsing University, Taichung, Taiwan, ROC.

C.-J. Chao is with the Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, ROC.

Publisher Item Identifier S 0894-6507(00)03546-6.

obtained in [16]. The result of our model shows agreement with the numerical field solver [17] and measurement data. This work extends the work of [16] to provide a complete solution for the modeling of interconnect capacitance for arbitrary multilevel interconnects. The complete model can be used in the delay and capacitance estimation in circuit design and process optimization.

II. Capacitance Model

The crossover capacitance is formed in any three adjacent layers of the multilevel metal interconnect. Consider any triple-level wire crossings, as shown in Fig. 1, where the second-level metal lines (M_2) cross the first-level (M_1, the lower level) and third-level (M_3, the upper level) metal lines. The line width, spacing, and thickness are denoted by W_i, S_i, and T_i for the ith-level metal layer, $i = 1, 2, 3$. The dielectric layer thickness is denoted by H_1, H_2, and H_3 for the dielectric between M_1 and the substrate (or the next lower layer, say, M_0), M_2 and M_1, and M_3 and M_2, respectively. For each M_2 line crossing M_1 line, a crossover capacitance C_{cr} exists. Note that M_1 and M_3 lines are not necessarily aligned to each other. This capacitance C_{cr} is restricted within a neighborhood of the lines intersection. Outside the intersection neighborhood, M_2 line capacitance can be estimated by existing 2-D intralayer coupling capacitance models [16].

To derive the crossover model for C_{cr}, we adopt an empirical approach here, because the usual power series or numerical solutions for Poisson's equation are not appropriate for VLSI simulation [17], [18]. In deriving these expressions, a rational function is first constructed to model each type of electrical flux variations with geometry variation. The rational functions are then multiplied to each other to form one flux component. Finally, all flux components are added, giving the lumped crossover capacitance C_{cr}. Here, three flux components, C_1, C_2, and C_3, are involved. That is

$$C_{cr} = C_1 + C_2 + C_3. \tag{1}$$

Capacitance C_1 represents the area component from M_1 top surface to M_2 bottom surface. Capacitance C_2 represents the component from M_1 side wall to M_2 bottom surface. Capacitance C_3 represents the component from the M_2 side wall to M_1 top surface.

To derive C_1, note that C_1 is simply the plate-to-plate capacitance, and hence

$$\frac{C_1}{\epsilon_{ox}} = \frac{W_1 W_2}{H_2}. \tag{2}$$

The flux component C_2 is modeled as the product of rational functions in the following general form:

$$\frac{C_2}{\epsilon_{ox}} = c_1 W_2^{\alpha_1} (S_1 \times S_2)^{\alpha_2} \left(\frac{T_1}{T_1 + c_2 H_2}\right)^{\alpha_3} \left(\frac{T_1}{T_1 + c_3 S_1}\right)^{\alpha_4} \times \left(\frac{H_1}{H_1 + c_4 S_1}\right)^{\alpha_5} \exp\left(\frac{-H_2}{c_5 (S_1 + c_6 H_2)}\right) \tag{3}$$

where the c_i's are constants and the α_i's are the power coefficients, both to be determined later.

We now explain the physical rationale behind each term adopted on the right-hand side of (3) for C_2: 1) the W_2 term follows from a power-law dependence of the capacitance on the line width [2], [3], [18]; 2) the S_1 and S_2 terms are to catch the intrawire spacing dependence: Because the M_1 side wall to M_2 wire flux is reduced by intra-M_1 flux as shown in the cross-section A of Fig. 1, C_2 decreases with reduced intra-M_1 spacing S_1; similar impact can be induced by intra-M_2 spacing S_2. Here, the same power coefficient α_2 is used to reflect their same influence; 3) the term $(T_1/(T_1 + c_2 H_2))^{\alpha_3}$ is adopted to model the fact that the flux originated from side wall heavily relies on the wire side wall thickness with a power-law dependence [3]. The power-law dependence has been proved in [18] as a good approximation to the field strength between adjacent nonoverlapping perpendicular surfaces. Note that this dependence will be weakened for large thickness (because such flux only exists at the side wall corner adjacent to the dielectric layer); the constant c_2 reflects this dependence weakening; 4) the terms $(T_1/(T_1 + c_3 S_1))^{\alpha_4}$ and $(H_1/(H_1 + c_4 S_1))^{\alpha_5}$ are used to model the fact that C_2 decreases with reduced T_1/S_1 as well as with reduced H_1/S_1 because of enhanced flux from M_1 to ground plane, as shown in the cross-section A of Fig. 1; and 5) the exponential term modifies the $1/H_2$ dependence constructed in (2), giving weakened H_2 impact with increased H_2/S_1, because intra-M_1 flux prevents field lines from being pulled up to M_2, electrode, as shown in the cross-section A of Fig. 1.

To derive C_3, we observe that C_3 is approximately a 180° turnover of C_2. Therefore, similar mathematical patterns will be adopted to emulate the similar electrical flux distributions. Differences in C_2 and C_3 exist, however: C_2 has a larger plate next to (or under) the side wall flux, whereas C_3 has many narrower wirings (M_3 wires) next to (or above) the side wall component. The consequence is that the side wall flux reduction induced by larger adjacent plane in C_2 and by adjacent wirings in C_3 will be different. C_3 is modeled in the following general form:

$$\frac{C_3}{\epsilon_{ox}} = d_1 W_1^{\beta_1} S_1^{\beta_2} S_2^{\beta_3} \left(\frac{T_2}{T_2 + d_2 H_2}\right)^{\beta_4} \exp\left(\frac{-H_2}{d_3 (S_2 + d_4 H_2)}\right) \times \left(\frac{H_3}{H_3 + d_5 S_2}\right)^{\beta_5} \tag{4}$$

where the d_i's are constants and the β_i's are the power coefficients, both again to be determined later.

Now, similar physical explanation, as is the case with C_2, can be made for each term on the right-hand side of (4) for C_3: 1) the W_1 term shows the power-law dependence as before; 2) the power terms of S_1 and S_2 again catch the intrawire spacing dependence, but here we use different power coefficients for them because their influence will be different. In fact, the influence of S_2 term in C_3 is weaker than in C_2, for the impact in C_3 is weakened by the M_3-to-M_2 flux; 3) the term $(T_2/(T_2 + d_2 H_2))^{\beta_4}$ models the fact that C_3 increases with increased T_2/H_2; 4) the exponential term further modifies the $1/H_2$ dependence constructed in (2), giving weakened H_2 impact with increased H_2/S_2, because intralayer flux prevents field lines from being pulled down to M_1 electrode; and 5) the last term $(H_3/(H_3 + d_5 S_2))^{\beta_5}$ models the impact of M_3 layer

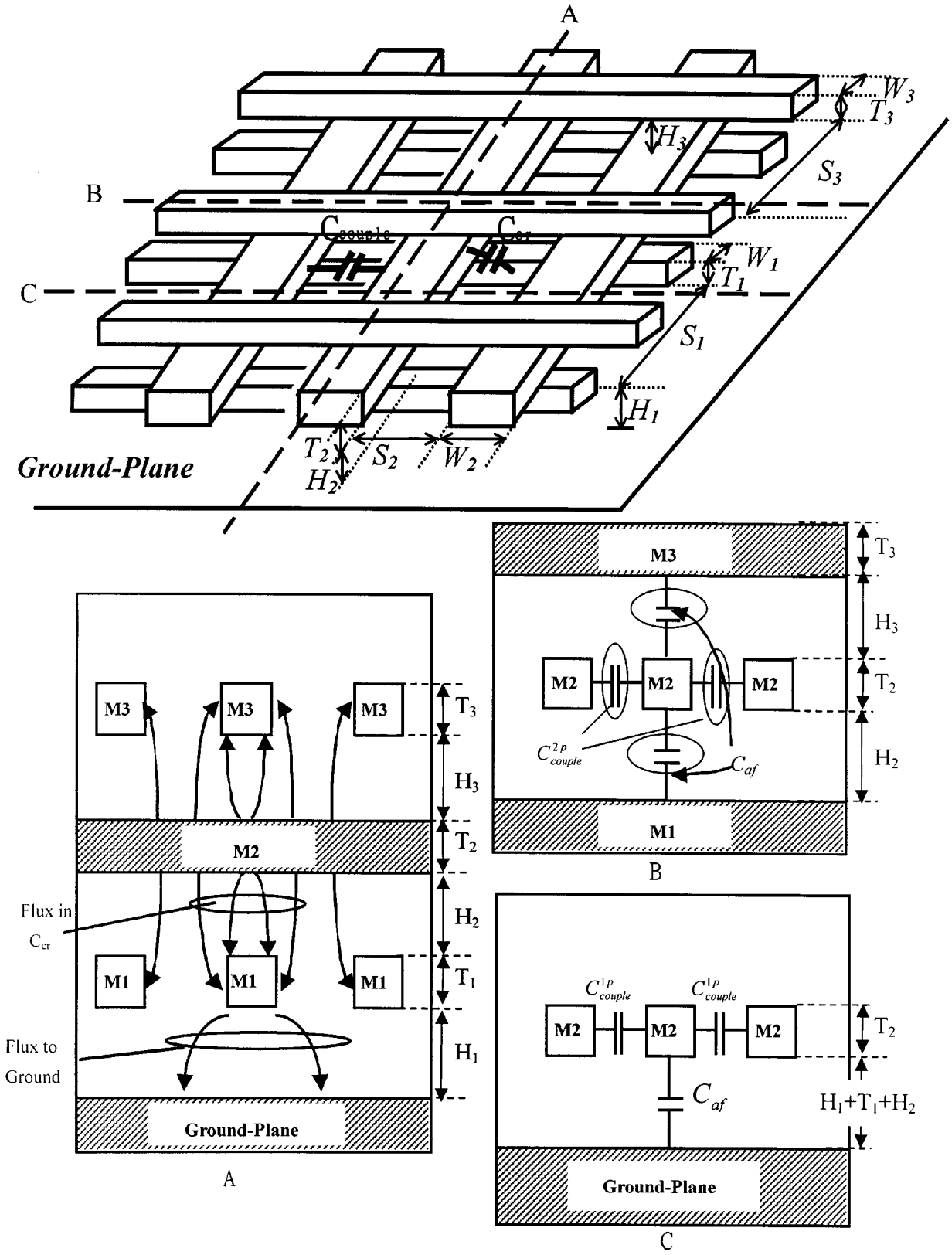


Fig. 1. Metal wiring crossover structure and cross sections along cut lines A, B, and C. H_1, H_2, and H_3 are dielectric thickness, T_1, T_2, and T_3 are metal wire thickness, W_1, W_2, and W_3 are wire width, and S_1, S_2, and S_3 are interwire spacing.

on C_3, which gives reduced C_3 with reduced H_3/S_2, because the intralayer coupling flux between M_2 lines forms a shield that isolates the C_3 flux from the influence of the M_3-to-M_2 flux. This shielding effect is very strong when S_2 is small, as shown in the cross-section B of Fig. 1. This shielding effect is reduced with large S_2, and hence, C_3 can be significantly reduced with

reduced H_3. Note that this effect is opposed to the phenomenon that C_3 increases with increased S_2, as predicted by the power terms of $(S_1)^{\beta_2}$ and $(S_2)^{\beta_3}$. This term and the power-law term provide contradictory influences by S_2 spacing, and our model can well describe these two opposing phenomena, which will later be demonstrated in Fig. 3.

To determine all constants and power coefficients in (3) and (4) for C_2 and C_3, we use the approach of least-mean-squares-errors fitting, and we obtain

$$\frac{C_2}{\epsilon_{ox}} = 3.73 W_2^{0.6} (S_1 \times S_2)^{0.2} \times \left(\frac{T_1}{T_1 + 0.035 H_2}\right)^{0.64} \times \left(\frac{T_1}{T_1 + 0.851 S_1}\right)^{0.12} \times \left(\frac{H_1}{H_1 + 0.051 S_1}\right)^{1.0} \times \exp\left(\frac{-H_2}{0.7(S_1 + 0.4 H_2)}\right) \tag{5}$$

and

$$\frac{C_3}{\epsilon_{ox}} = 3.73 W_1^{0.6} S_1^{0.2} S_2^{0.1} \left(\frac{T_2}{T_2 + 0.035 H_2}\right)^{0.64} \times \exp\left(\frac{-H_2}{0.7(S_2 + 0.4 H_2)}\right) \times \left(\frac{H_3}{H_3 + 0.015 S_2}\right)^{3}. \tag{6}$$

The root-mean-square error between the model and the numerical solutions is 6.71%, based on a total of 272 data points using the least-squares-error fitting approach. The 272 total data points were basically selected randomly, but with more dense data points chosen toward smaller dimension range (as the capacitance effect is more pronounced at smaller dimension range). A list of error distribution is shown is Table I, which only displays a partial set of our data used for parameter fitting.

The segments of M_2 outside the intersection neighborhood can be modeled by the 2-D capacitance formulas derived previously by the authors [16]. The capacitance components here include 1) intralayer coupling capacitance C^{1p}_{couple}, which is the intra-M_2 flux in the wire region without M_3 wirings crossing above, as shown in the cut-line C and cross section C of Fig. 1, 2) C^{2p}_{couple}, which is the intra-M_2 flux in the M_2 region with M_3 wirings crossing above, as shown in the cut-line B and cross-section B of Fig. 1, and 3) line-to-ground capacitance C_{af} in the region without M_3 wirings crossing above, as shown in the cross section C of Fig. 1. These capacitances were obtained in [16] as

$$\frac{C_{af}}{\epsilon_{ox}} = \frac{W_2}{H} + 2.217 \left(\frac{S_2}{S_2 + 0.702 H}\right)^{3.913} + 1.171 \left(\frac{S_2}{S_2 + 1.51 H}\right)^{0.764} \times \left(\frac{T_2}{T_2 + 4.532 H}\right)^{0.12} \tag{7}$$

$$\frac{C^{1p}_{\text{couple}}}{\epsilon_{ox}} = 1.144 \frac{T_2}{S_2} \left(\frac{H}{H + 2.059 S_2}\right)^{0.0944} + 0.7428 \left(\frac{W_2}{W_2 + 1.592 S_2}\right)^{1.144} + 1.158 \left(\frac{W_2}{W_2 + 1.874 S_2}\right)^{0.1612} \times \left(\frac{H}{H + 0.9801 S_2}\right)^{1.179} \tag{8}$$

and

$$\frac{C^{2p}_{\text{couple}}}{\epsilon_{ox}} = 1.412 \frac{T_2}{S_2} \exp\left(-\frac{2S_2}{S_2 + 8.014 H_2} - \frac{2S_2}{S_2 + 8.014 H_3}\right) + 1.1852 \left(\frac{W_2}{W_2 + 0.3078 S_2}\right)^{0.25724} \times \left\{\left(\frac{H_2}{H_2 + 8.961 S_2}\right)^{0.7571} + \left(\frac{H_3}{H_3 + 8.961 S_2}\right)^{0.7571}\right\} \times \exp\left(-\frac{2S_2}{S_2 + 3(H_2 + H_3)}\right) \tag{9}$$

where $H = H_1 + H_2 + T_1$. In [16], the above 2-D capacitance model provides accurate capacitance prediction, with a root-mean-square error of 3.68, 4.45, and 16.13% for C_{af}, C^{1p}_{couple}, and C^{2p}_{couple}, respectively, compared with the numerical solutions.

TABLE I
ERROR TABLE OF THE MODEL COMPARED WITH NUMERICAL SOLUTIONS

Technology dimension (μm)						Wire dimension (μm)						Error(%)
H3	H2	H1	T3	T2	T1	W3	W2	W1	S3	S2	S1	
2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	-2.700
0.16	0.16	0.16	0.16	0.16	0.16	2.0	2.0	2.0	2.0	2.0	2.0	-3.900
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	1.0	0.16	-2.285
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	1.0	0.5	1.166
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	0.16	1.0	-3.982
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	0.16	1.0	1.0	-0.152
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	1.0	1.0	-0.223
3.0	0.9	0.16	0.6	0.6	0.6	0.3	0.3	0.3	0.3	0.3	0.3	2.953
3.0	0.9	3.0	0.6	0.6	0.6	0.3	0.3	0.3	0.3	0.3	0.3	-7.232
0.9	0.16	0.9	0.6	0.6	0.6	0.3	0.3	0.3	0.3	0.3	0.3	0.596
0.16	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	2.682
0.89	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	4.693
3.0	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	5.145
0.16	0.16	0.16	0.16	0.16	0.16	2.0	2.0	2.0	0.16	0.16	0.16	-5.500
0.3	0.3	0.3	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	8.905
0.5	0.5	0.4	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	5.470
0.5	0.5	0.9	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	-0.241
0.5	0.16	0.5	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	8.028
0.16	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	0.414
0.4	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	1.341
0.89	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	1.759
3.0	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	2.035
0.16	0.16	0.16	2.0	2.0	0.16	0.16	0.16	0.16	0.16	0.16	0.16	4.800
2.0	2.0	2.0	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	8.300
2.0	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	6.300
0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	6.400

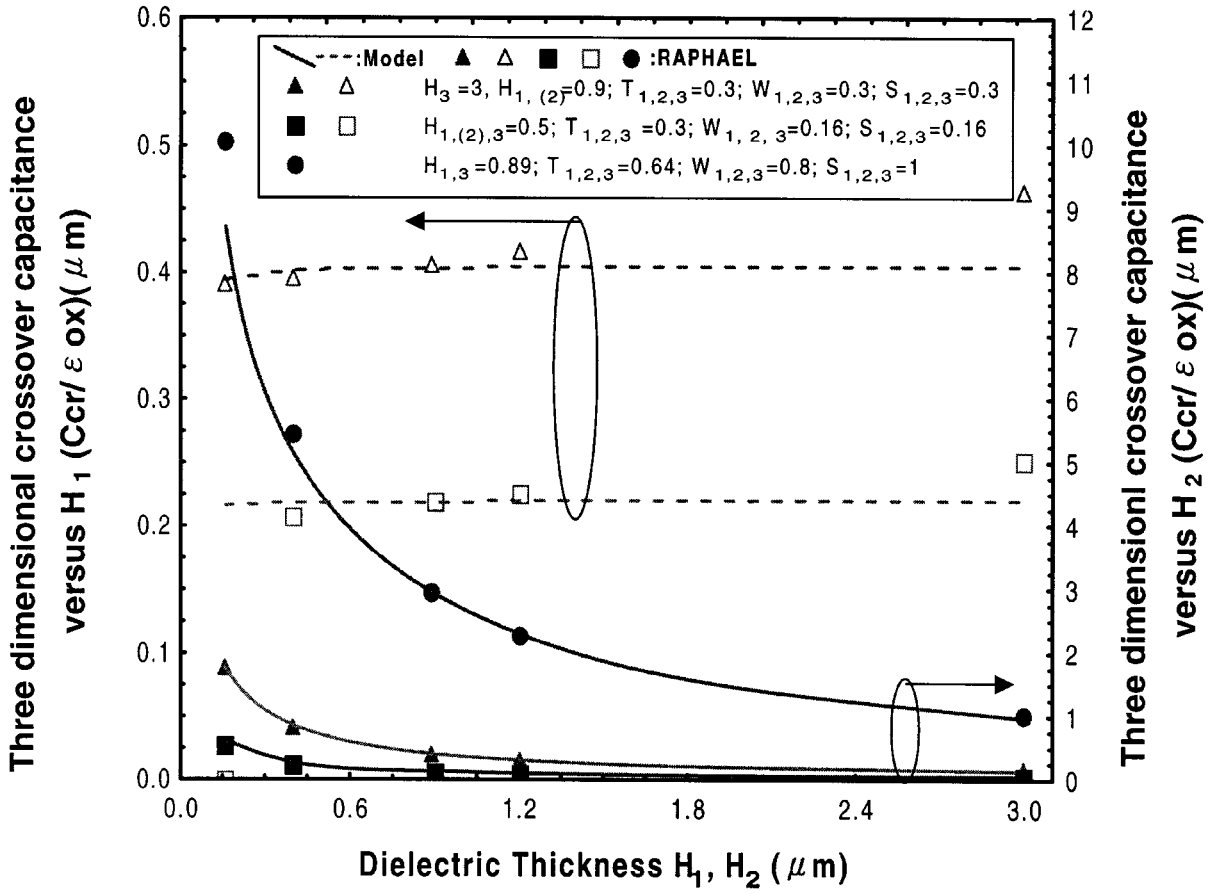


Fig. 2. Crossover capacitance variation versus dielectric thickness. Symbols denote Raphael simulation, and dashed and solid lines denote our model calculation.

The total capacitance on a M_2 line of length L with n M_1–M_2 crossings and another n M_2–M_3 crossings can be calculated by combining the total intralayer coupling capacitance and the total crossover capacitance. The total intralayer coupling capacitance is easily determined as

$$(L-nW_1)C^{1p}_{\text{couple}}+nW_1C^{2p}_{\text{couple}}+(L-nW_1)C_{af}.$$

The total crossover capacitance is calculated according to the following: 1) each crossing of M_1 and M_2 gives a crossover capacitance $C_{cr(M_1-M_2)}$ as exactly calculated by formulas (1), (2), (5), and (6); 2) each crossing of M_2 and M_3 also gives a crossover capacitance $C_{cr(M_2\text{-}M_3)}$. To compute $C_{cr(M_2\text{-}M_3)}$, we need to view the triple-layer upside down before applying the above-developed formulas. That is, M_3 is now treated as the lower layer and M_1 the upper layer, which means that H_3 should be used as H_2 and H_2 should be used as H_3 in the formulas. H_1 to be used in the formulas should be the spacing between M_3 and the next adjacent higher layer (say, M_4 if exists). If M_3 is the actual top layer, we have $H_1=\infty$. Here, in such a case, we use the value $H_1=5\,\mu$m as infinity.

Combining the crossover and intralayer coupling capacitances, we have

$$\begin{aligned}C_{\text{total}}=&n[C_{cr(M_1-M_2)}+C_{cr(M_2-M_3)}]+(L-nW_1)C^{1p}_{\text{couple}}\\&+nW_1C^{2p}_{\text{couple}}+(L-nW_1)C_{af}.\end{aligned}\tag{10}$$

Our model, which is derived based on three-metal layers, can be applied to a process with any number of metal layers. The crossover capacitance of a metal wire with the layer underneath it can be accurately predicted by our model, with or without above-passing wires. In the general multilayer case, any layer above the first layer or under the third layer is shielded from the second layer and, hence, does not affect the crossover capacitance.

III. Results and Discussions

The agreement between our model and the numerical field solver [17] is shown in Table I. In Table I, the error is defined as Error $=$ (model-Raphael/Raphael) $\times$ 100%. The final model has been tested based on 272 data points with a root-mean-square error of 6.71%. The valid ranges of the model are the following: $0.16\,\mu\text{m}\le S_1, S_2, S_3\le 5\,\mu\text{m}$, $0.16\,\mu\text{m}\le W_1, W_2, W_3\le 2\,\mu\text{m}$, $0.15\,\mu\text{m}\le T_1, T_2, T_3\le 1.2\,\mu\text{m}$, and $0.16\,\mu\text{m}\le H_1, H_2, H_3\le 3\,\mu\text{m}$. The valid ranges for our model were determined based on practical applications in integrated circuit (IC) technology. The upper bound for parameter S set at $5\,\mu$m is to take care of both dense and sparse lines. The upper bounds for H and T were set to match the practical dieletric and metallization thicknesses.

The comparison between the model and the numerical simulations [17] for various H_1 and H_2 is shown in Fig. 2. The strong

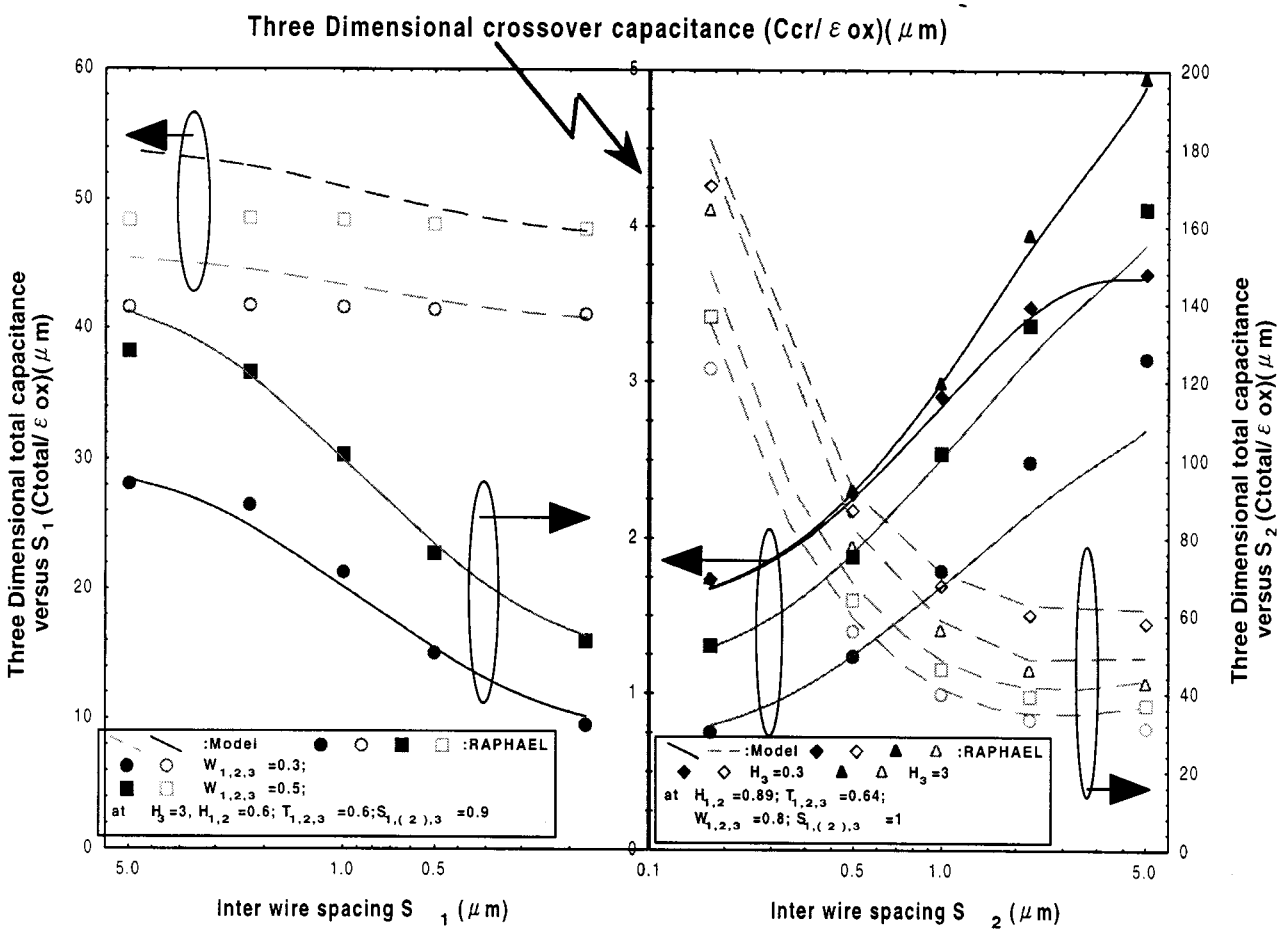


Fig. 3. Crossover capacitance and total capacitance variation versus intralayer wire spacing. Symbols denote Raphael simulation, and lines denote our model calculation. The left graph and right graph are correlated to each other by sharing the common axis of C_{cr} for comparing the different C_{cr} variation versus S_1 and S_2.

H_2 dependence can be accurately predicted by our model. On the other hand, H_1 only influences C_{cr} minorly, simply because the flux of C_{cr} is shielded from the line-to-ground flux by the intra-M_1 flux, as shown in the cross-section A in Fig. 1. The intra-M_1 flux plays the role of electrical buffer between C_{cr} and line-to-ground flux, and this buffer is weakened for small H_1 (here, $H_1 \leq 0.5\,\mu$m), as shown in Fig. 2. Our model is useful here for predicting strong H_2 dependence, weak H_1 dependence induced by intra-M_1 flux shielding effect, and the onset of weakened shielding effect when C_{cr} reduces with reduced H_1.

The comparisons of the crossover capacitance C_{cr} and total M_2 wiring capacitance C_{total} between our model and the numerical solutions for various intralayer spacing are shown in Fig. 3. Note that C_{cr} decreases with reduced S_1 and S_2 because of enhanced intra-M_1 and intra-M_2 coupling effects, respectively. At small S_1 (or S_2), the C_{cr} variation versus S_1 is symmetrical to that of versus S_2. At large S_1 or S_2, it should be noted that C_{cr} variations with S_1 and S_2 are different, and this difference depends on the magnitude of H_3. To investigate this in more detail, note that for the curves with $H_3 = 3\,\mu$m, C_{cr} increases strongly with increased S_2 than with increased S_1, which can be explained as follows: because large H_3 (at $3\,\mu$m) is adopted in these data, increased S_2 eliminates the intra-M_2 flux and enhances the C_{cr} flux. On the other hand, with increased S_1, considerable line-to-ground flux (as shown in the cross-section A of Fig. 1), becomes influential because H_1 is only $0.6\,\mu$m, and will retard the C_{cr} flux. As a result, C_{cr} increases with increased S_2 much stronger than with increased S_1.

Another point worth studying is the following question. When can the impact of top-level metal in any three-level metal combination be ignored for C_{cr} between the first and second level metals? Being able to identify a no-influence region here would allow for an easy C_{cr} estimation without considering parameters of the top-level wire, which will greatly simplify RC extraction [5] and process design [1], [4]. To investigate this process, first it can be observed that the impact of H_3 is negligible for small S_2, because $H_3 = 0.3\,\mu$m, and $H_3 = 3\,\mu$m gives the same C_{cr} for $S_2 \leq 0.5\mu$m, because the strong intra-M_2 flux completely shields the M_3-to-M_2 flux from influencing C_{cr}. The impact of H_3 is much more pronounced when S_2 is larger than $0.8\,\mu$m, because C_{cr} can be significantly retarded by the M_3-to-M_2 flux, as shown in the cross-section B of Fig. 1, especially when the intra-M_2 coupling disappears. Hence, C_{cr} at $H_3 = 3\,\mu$m is much larger than at $H_3 = 0.3\,\mu$m. Furthermore, as mentioned before, for $H_3 = 0.3\,\mu$m, C_{cr}

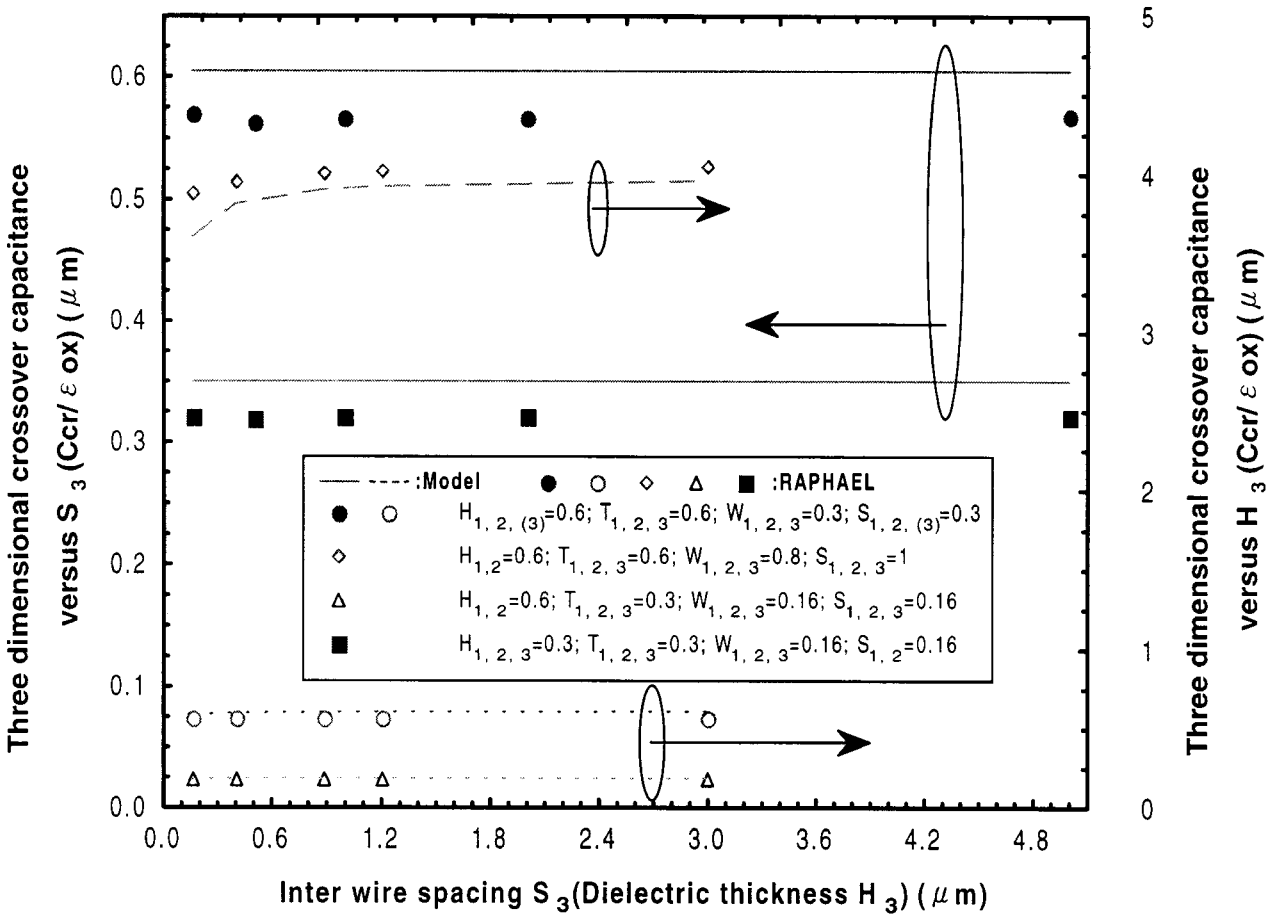


Fig. 4. Crossover capacitance variation versus top-level wire dielectric thickness and intralayer wire spacing. Symbols are Raphael simulation, and lines denote model calculation.

saturates with reduced H_3/S_2 (or increased S_2) for $S_2 \geq 4\,\mu$m, as predicted by the term $(H_3/(H_3 + d_5 S_2))^{\beta_5}$ in (4). These observations on C_{cr} give us a region where C_{cr} is influenced by the third-level metal, and this region is defined by $S_2 \geq 0.3\,\mu$m and $H_3 \leq 0.3\,\mu$m. Outside this region, C_{cr} immunizes from the impact of M_3, and thus C_{cr} estimation can be performed with the top-level wiring effect ignored.

The calculated C_{total} is the total M_2 capacitance in a cell with ten lines for M_1, M_2, and M_3 each. It is shown that C_{total} slightly increases with increased S_1, because of increased C_{cr}. On the other hand, C_{total} significantly decreases with increased S_2, because of decreased C^{2p}_{couple} between M_2 lines. The larger error of C_{total} for $S_1 \geq 0.5\,\mu$m is induced by the approximation of the last term in (10), i.e., $(L - nW_1)C_{af}$. The calculation of the 2-D capacitance using this term in the region outside the crossing neighborhood may overestimate the line-to-ground capacitance, because many metal-2 field lines near the crossing neighborhood will be attracted to the crossing metal-1 instead of being terminated to ground, as shown in cross-section A of Fig. 1. This process implies that the approximated length for C_{af} of $L - nW_1$ may cause slight overestimation. Note that because our model mainly tends to be used in deep submicron VLSI, the error for S_1 larger than $0.5\,\mu$m may not affect the calculation accuracy for densely packed VLSI.

The impact of the top layer wiring is shown in Fig. 4, where C_{cr} varies with S_3 and H_3. C_{cr} is noticeably reduced with reduced H_3 when intrawire spacing is $1\,\mu$m, agreeing with our observation from Fig. 3 made in the previous paragraph, as some M_2 flux is attracted to the M_3 electrode. The disagreement between the model and numerical solution at small H_3 is caused by the large variation generated by the last term in (6) as a result of its rational function form. The form is chosen for tradeoff at large H_3.

The comparison between our model and measurement data is performed based on test structures fabricated in a 0.35-μm twin-well logic CMOS process. The interconnection in this process is composed of AlCuSi metal lines, an oxide dielectric layer, and chemical–mechanical polished dielectric layers. Three test structures are included in this study, with each test structure composed of three layers of intracoupled wires. Each test structure has 726 crossovers. The C_{cr} between M_2-to-M_3 or between M_2-to-M_1 is then measured by grounding all additional wires to eliminate all intralayer and line-to-ground flux. Measurement has been performed on ten dies a wafer for four wafers, with the mean and standard deviation shown in Table II. Agreement is shown between our model and measurement with a maximum error of 4.17%.

TABLE II
COMPARISON BETWEEN MEASUREMENT DATA AND THE MODEL

Capacitance/ Parameters(μm)	Model (aF/crossover)	Measurement (aF/crossover) Mean, standard deviation
M_2-M_3 C_{cr} W_1=W_2=S_1=S_2=0.4, T_1=T_2=0.6, H_1=2.602, H_2=0.848, H_3=0.979	26.06	24.85, 1.64%
M_2-M_3 C_{cr} W_1=W_2=0.8, S_1=S_2=0.4, T_1=T_2=0.6, H_1=2.602, H_2=0.848, H_3=0.979	55.69	56.49, 1.67%
M_1-M_2 C_{cr} W_1=W_2=0.4, S_1=S_2=0.4, T_1=T_2=0.6, H_1=0.966, H_2=0.848, H_3=0.979	25.95	24.91, 2.42%

It should be noted that our model has been derived based on normalized dielectric constant, and is, hence, independent of the oxide dielectric constant. In comparing our model with measurement data, however, dielectric constant must be determined. The dielectric constant is determined by measuring large-plate capacitors using HP4284 impedance meter at 100 kHz, with an exciting signal of 100 mV. Based on the measured unit-area capacitance C_{ox}, ϵ_{ox} is obtained by $\epsilon_{ox} = t_{ox}C_{ox}$. In this work, we have obtained nearly the same $\epsilon_{ox} = 3.79$ for all dielectric layers. For cases with various dielectric layers having different values of dielectric constant, it is also possible to apply our model by taking their dielectric constant average as a common ϵ_{ox} and used in the model equations, but this has not been tested yet.

From our analysis, it is easily seen that the crossover capacitance, because of its 3-D feature, can be influenced by numerous parameters, and the impacts of these parameters are strongly coupled with each other. Our model here can be very helpful in predicting the capacitance variation versus various electrical flux fluctuations, and in optimizing the total capacitance via appropriately adjusting physical dimensions.

IV. CONCLUSION

A complete closed-form model for the crossover capacitance in multilevel, densely packed interconnections has been developed for arbitrary wiring dimensions. The combined use of the developed crossover capacitance model and existing intralayer coupling and lines-to-ground capacitance model can determine the total capacitance on a wire passing many crossings. The model has been validated by the numerical solutions and measurement data, and it can be used for VLSI design and process optimization.

REFERENCES

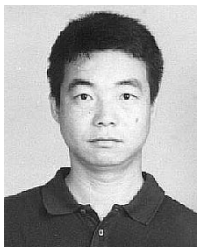
[1] M. T. Bohr, "Interconnect scaling—The real limiter to high performance ULSI," in *Proc. IEDM*, 1995, pp. 241–244.
[2] J.-H. Chern, J. Huang, L. Arledge, P.-C. Li, and P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," *IEEE Electron Device Lett.*, vol. 13, pp. 32–34, 1992.
[3] T. Sakurai, "Closed-form formulas for interconnection delay, coupling and crosstalk in VLSI's," *IEEE Trans. Electron Device.*, vol. 40, pp. 118–124, 1993.
[4] K. Rahmat, O. S. Nakagawa, S.-Y. Oh, J. Moll, and W. T. Lynch, "A scaling scheme for interconnect in deep-submicron process," in *Proc. IEDM*, 1995, pp. 245–248.
[5] N. D. Arora, K. V. Roal, R. Schumann, and L. M. Richardson, "Modeling and extraction of interconnect capacitances for multilayer VLSI circuits," *IEEE Trans. Circuits Syst.*, vol. 15, pp. 58–67, 1996.
[6] K. J. Chang *et al.*, "Parameterized SPICE subcircuits for multilevel interconnect modeling and simulation," *IEEE Trans. Circuits Syst.II*, vol. 39, pp. 779–789, 1992.
[7] D. H. Cho, Y. S. Eo, M. H. Seung, N. H. Kim, J. K. Wee, O. K. Kwon, and H. S. Park, "Interconnect capacitance, crosstalk and signal delay for 0.35 μm CMOS technology," in *Proc. IEDM*, 1996.
[8] G.-W. Pan, M. Toupikov, and B. K. Gilbert, "A combined finite difference and analytic expression approach to crossover capacitance in a multilayer dielectric environment," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 19, pp. 615–620, 1996.
[9] S. A. Kuhn, M. B. Kleiner, P. Ramm, and W. Weber, "Performance modeling of the interconnect structure of a three-dimensional integrated RISC processor/cache system," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 19, pp. 719–727, 1996.
[10] V. Vladimir and R. Mittra, "A technique for fast calculation of capacitance matrices of interconnect structures," in *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 21, 1998, pp. 241–249.
[11] J.-K. Wee, Y.-J. Park, H.-S. Min, D.-H. Cho, M.-H. Seung, and H.-S. Park, "Measurement and characterization of multilayered interconnect capacitance for deep-submicron VLSI technology," *IEEE Trans. Semiconduct. Manufact.*, vol. 11, pp. 636–644, 1998.
[12] P. Nouet and A. Toulouse, "Use of test structures for characterization and modeling of inter-layer capacitances in a CMOS process," *IEEE Trans. Semiconduct. Manufact.*, vol. 10, pp. 233–241, 1997.
[13] K. Aoyama, K. Ise, H. Sato, K. Tsuneno, and H. Mauda, "A new characterization of sub-μm parallel multilevel interconnect and experimental verification," *IEEE Trans. Semiconduct. Manufact.*, vol. 9, pp. 20–26, 1996.
[14] C.-J. Chao, S.-C. Wong, M.-J. Chen, and B. K. Liew, "An extraction method to determine interconnect parasitic parameters," *IEEE Trans. Semiconduct. Manufact.*, vol. 11, pp. 615–623, 1998.
[15] J. C. Chen, D. Sylvster, and C. Hu, "An on-chip interconnect capacitance characterization method with sub-femto-farad resolution," *IEEE Trans. Semiconduct. Manufact.*, vol. 11, pp. 204–210, 1998.
[16] S.-C. Wong, G.-Y. Lee, and D.-J. Ma, "Modeling of interconnect capacitance, delay and cross-talk in VLSI," *IEEE Trans. Semiconduct. Manufact.*, to be published.
[17] *RAPHAEL Users' Manual*, Technology Modeling Associate, 1995.
[18] J. D. Kraus and K. R. Carver, *Electromagnetics*, 2nd ed. New York: McGraw-Hill, 1973, pp. 290–304.

Shyh-Chyi Wong received the B.S. degree in electronics engineering from the National Chiao-Tung University, Taiwan, R.O.C., in 1983 and the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1985 and 1989, respectively.

From 1989 to 1993, she was with Analog Devices Inc., MA, where she worked on SPICE modeling and characterization of various MOS devices, circuits, and processes. From 1993 to 1995, she was with Taiwan Semiconductor Manufacturing Corp. as the Manager of the Device Department. From 1995 to 1998, she was with the Department of Electronics Engineering, Feng-Chia University, Taiwan, as an Associate Professor. From 1998 to 1999, she was with the Winbond Electronics Corp., Taiwan, as the Director of Device and Reliability Division. Since 1999, she has been with Taiwan Semiconductor Manufacturing Corp. as the Program Manager for mixed signal and RF processes. Her research interests include device modeling and simulation, interconnect modeling and layout extraction, statistical modeling, device reliability, and analog circuit design.

Trent Gwo-Yann Lee was born in Taiwan in 1974. He received the B.S. and M.S. degrees in electrical engineering from Feng-Chia University in 1996 and 1998, respectively. He is currently pursuing a Ph.D. degree from National Chiao-Tung University.

His research interests include interconnection and device modeling and computer simulation method.



Dye-Jyun Ma received the B.S. degree in electronics engineering from National Chiao-Tung University, Taiwan, R.O.C., in 1979 and the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1984 and 1988, respectively.

From May 1988 to June 1993, he was with Digital Equipment Corp., MA, as a Principal Engineer. Since August 1993, he has been with the Department of Electrical Engineering, National Chung-Hsing University, where he is presently a Professor. His research interests include control and optimization and interconnect and statistical modeling.

Chuan-Jane Chao received the B.S. and M.S. degrees from National Chiao-Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 1990 and 1992, respectively, all in electronics engineering. She is currently pursuing the Ph.D. degree in electronics engineering at NCTU.

From 1992 to 1998, she was with Taiwan Semiconductor Manufacturing Corp., Hsinchu, Taiwan, R.O.C., as a Principle Device Engineer in device engineering, responsible for SPICE modeling and device characterization. Since October 1998, she has been with Winbond Electronics Corp., Hsinchu, where she works on SPICE modeling and characterization of various MOS devices, circuits, and processes. Her research interests are in the area of device and interconnect modeling and characterization.