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An Energy-Efficient, Resistor-Based Smart Temperature Sensor

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Contents

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Kianoush,

Delft,

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1 Introduction

1.1 Introduction

Temperature is a critical operating parameter of most electrical, mechanical, magnetic, chemical, radiant, and biological systems [1]. This is because such systems often exhibit some sort of temperature dependency, which in turn necessitates temperature measurement and control in many systems [2-8].

Smart temperature sensors output a digital code representing ambient temperature. As shown in Fig. 1.1, the first step involves using a sensor to convert temperature into an electrical signal. This signal is then processed by an analog front-end and digitized by an on-chip analog-to-digital converter [9, 10]. The sensor's digital output then can be readily transmitted to other digital building blocks of a system [11], in a robust manner.

The goal of this project is to design an energy-efficient, high-resolution (sub-mK) and highly accurate temperature sensor (<0.1°C) for the compensation of frequency references based on micro electro-mechanical systems (MEMS). In the following, a brief introduction to MEMS frequency references will be given and the requirements for this application will be further discussed. Then, the energy-efficiency of existing CMOS temperature sensors is discussed, and a number of promising temperature sensing techniques are identified.

1.2 MEMS Frequency References

Frequency references are widely used in electronic systems, where they often set limits to the obtainable performance, functionality, power consumption, size and cost [13, 14]. MEMS-based oscillators are being actively developed as sources of highly stable reference frequencies [15], with the small form-factor needed in hand-held wireless devices, and comparable power consumption than the original quartz-crystal-based frequency references [16].

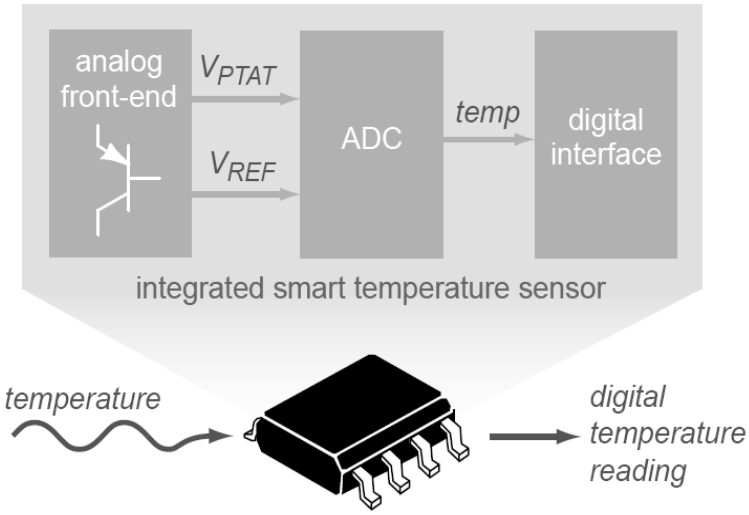

Figure 1.1. *Integrated smart sensor block diagram [9].*

Compared to quartz-crystal-based references, MEMS frequency references suffer from significantly inferior accuracy both in terms of temperature stability and manufacturing tolerance [15, 17]. As a result, an important research focus is on improving this [18, 19].

Process spread impacts the accuracy of MEMS resonators. This can be improved with more advanced lithography and multi-point (3-to-6 point) trimming. However, the large native temperature-coefficient of frequency (TCF) of MEMS resonators, typically ~30 ppm/°C, causes a drift of more than 5000 ppm across the military temperature range (-55°C to 125°C) [15]. Since many applications require variations of less than ±50ppm and even ±1ppm, temperature compensation becomes necessary for MEMS oscillators [20, 8]. Which in turn, in order to achieve a frequency-instability of a few ppms, the temperature sensor's inaccuracy should be less than 0.1°C [8].

In a recent publication [8], it has been shown that for high performance applications, the temperature sensor's noise should be less than 170µK (rms). Because of that the temperature sensor's noise will then determine the output jitter of the MEMS oscillator.

Lastly, to be able to track ambient temperature variations, the temperature sensor's conversion rate should be less than 100msec, while satisfying all the above mentioned requirements.

Since frequency references are widely used in portable, battery-powered devices, energy-efficiency is a key requirement. The relative energy-efficiency of smart temperature sensors can be assessed with the help of a resolution figure of merit (FOM) defined as the product of energy per conversion and square of resolution [22]:

$$Resolution\ FOM = Energy\ (per\ conversion) \times Resolution^2. \quad (1.1)$$

Table 1.1. *Target specifications of this work.*

Parameter	Value
Power consumption	<30uW
Analog core area	<0.1mm^2
Conversion time	100msec
Resolution (RMS)	<1mK
Inaccuracy (3σ)	<0.1°C
Calibration points #	3 to 6
Resolution FOM	<2pJ°K^2

State-of-the-art temperature sensors achieve a resolution FOM about 10pJ°K^2, however, only a few can also achieve mK-level resolution in a conversion time of 100msec [8, 9]. The aim of this work is to achieve a significant improvement in both energy efficiency and resolution. As discussed, multi-point trimming is required for MEMS frequency references, therefore, the integrated temperature sensor without any cost overhead. Table 1.1 summarizes the target specification of a temperature sensor for MEMS resonator compensation.

There are numerous temperature-sensing devices available in CMOS technology and consequently different manners of measuring temperature, each of which leads to a certain maximum energy-efficiency. To make the most energy-efficient temperature sensor, an appropriate choice should first be made as to the temperature-sensing device. In the next section, some existing temperature sensing methods are briefly investigated.

1.3 Temperature Sensors in CMOS Technology

In this section, four temperature sensing methods in CMOS are briefly discussed, and in the next section, their performance is compared.

1.3.1 BJT-Based Temperature Sensor

Figure 1.2 illustrates two bipolar transistors with emitter areas A_E and $r.A_E$, configured in a "*diode connected"* fashion, and biased by currents I_1 and pI_1, respectively [23, 24]. Two different temperature dependent signals with negative and positive temperature coefficients can then be generated. The base-emitter voltage V_{BE} has a complementary-to-absolute-temperature (CTAT) behavior with a temperature coefficient of ≈ -2mV/°C. The difference in base-emitter voltages ΔV_{BE}, on the other hand, has a proportional-to-absolute-temperature (PTAT) behaviour over temperature with a temperature coefficient of ≈100 µV/°C [12]. An appropriate linear combination of PTAT and CTAT voltages provides a temperature independent band-gap reference voltage [9]. The PTAT ratio μ in Eqn. 1.2, which represents the temperature, can then be readily determined by means of an analog-to-digital converter (ADC) [12].

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{BE}} \tag{1.2}$$

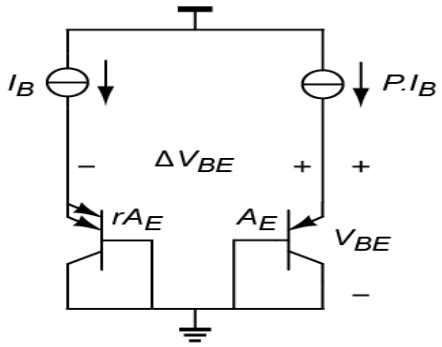

Figure 1.2. *The core of the BJT-based smart temperature sensor [12].*

A state-of-the-art BJT-based temperature sensor achieves an energy-efficiency of 11 pJ°K^2, and 5mK resolution in a 100msec conversion time. Moreover, this sensor obtains ±0.15°C inaccuracy over the military temperature range after a one point calibration and trim at room temperature [9].

1.3.2 ETF-Based (Electro-Thermal Filter) Temperature Sensor

Silicon's *Thermal Diffusivity* is defined as the rate at which heat diffuses through a silicon substrate. Recent research has shown that the thermal diffusivity D of silicon is a well-defined parameter, as the silicon wafer used for IC fabrication is a highly pure material [25]. The thermal diffusivity of bulk silicon is strongly temperature dependent: $D \approx 1/T^{1.8}$ [26]. Fig. 1.3 shows the structure of an electro-thermal filter (ETF), which uses a heater to generate heat pulses, and a thermopile (at a distance S from the heater), which converts the received temperature variations into a voltage signal. An ETF behaves like a low-pass filter in the thermal domain. Driving this filter at a certain frequency results in a temperature dependent phase shift which can then be digitized by an ADC. A state-of-the-art ETF-based temperature sensor achieves an energy-efficiency of 0.7µJ°K^2, and 20mK resolution in a 6.2sec conversion time. Also, after batch calibration, it achieves ±0.2°C inaccuracy over the military temperature range [27].

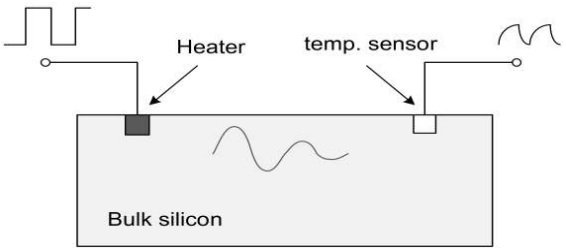

Figure 1.3. *Electro-Thermal Filter in CMOS technology [31].*

1.3.3 Temperature-Dependent-Delay-Line (TDDL-Based) Temperature Sensor

The time delay associated with an inverter is temperature dependent. It can then be measured and digitized by a time-to-digital converter (TDC) [28]. A temperature-dependent delay line consists of an even number of inverters (or equivalent delay buffers) as shown in Fig. 1.4. As the sensor's dynamic range is defined in the time-domain, the longer the inverter

chain is, the more resolution can be achieved. This temperature dependent delay is a function of channel's mobility, threshold voltage, and supply voltage, which results in poor supply dependency. A state-of-the-art TDDL-based temperature sensor achieves an energy-efficiency of 160nJ°K^2, and 91mK resolution in a 500msec conversion time. It also achieves ±0.6°C inaccuracy over a 0°C to 90°C temperature range after two point trimming [28].

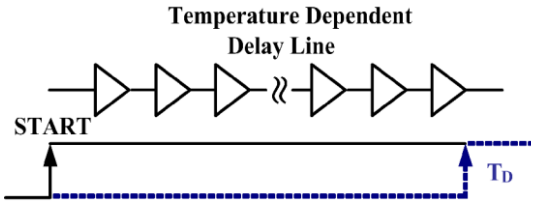

Figure 1.4. *Temperature dependent delay line implementation in CMOS.*

1.3.4 Resistor-Based Temperature Sensor

Resistors have been widely used as temperature sensors [8, 29, and 30]. In CMOS technology, their temperature-coefficient is a function of resistor type, with temperature coefficients ranging between 0.1%/°C and 0.4%/°C. There are different ways of reading out a resistor. One way is to make a half-Wheatstone bridge using resistors with different temperature coefficients [29]. The bridge is then balanced by a feedback loop based on a successive approximation algorithm. This work achieves an energy-efficiency of 19pJ°K^2, and 250mK resolution in a 12.5µsec conversion time. It also achieves ±0.5°C inaccuracy over a 0°C to 100°C temperature range after one point trimming [29]. Another way of reading out a resistor is by incorporating it in a voltage divider together with a switched-capacitor (SC) resistor. A feedback loop tries to balance the two impedances by regulating the SC resistor's effective impedance via its switching frequency. The required frequency then represents the temperature [8]. This work achieves an energy-efficiency of 13pJ°K^2, and 0.1mK resolution in a 100msec conversion time. It also achieves ±0.03°C inaccuracy over a -40°C to 85°C temperature range, but this is after 6 point trimming [8].

1.3.5 Comparison

Table 1.2 compares four temperature sensing topologies. It can be seen that the TDDL-based approach results in poor inaccuracy and exhibits a relatively high supply dependency. It also has poor energy-efficiency compared to resistor- and BJT-based sensors. In the case of ETF-based sensors, although good accuracy can be achieved, their inherently high power consumption prohibits their use in applications where energy-efficiency is vital. Resistor-based and BJT-based temperature sensors both have better energy-efficiency than the other two candidates.

Examination of Table 1.2 shows that resistor-based temperature sensors are less accurate than BJT-based ones. However, the multi-point trimming commonly used in MEMS resonator applications can also be re-used to improve their accuracy. In order to make a final choice between resistor and BJT-based temperature sensors, the fundamental limits on their energy-efficiency must be examined more carefully. This will be investigated in the following section.

Table 1.2. *State-of-the-art temperature sensors.*

Parameter	Resistor[29]	BJT[9]	ETF[27]	TDDL[28]
Technology	0.18µm	0.16µm	0.16µm	0.35µm
Supply voltage	1.2 to 2V	1.5V to 2V	5V	3.3V
Supply current	20µA	3.4µA	700µA	12µA
Supply sensitivity	0.625°C/V	0.5°C/V	----	33°C/V
Temperature range	0°C to 100°C	-55°C to 125°C	-70°C to 170°C	0°C to 90°C
Inaccuracy (Trim method)	±0.5°C (one point)	0.15°C(3σ) (voltage calibration)	±0.4°C(3σ) (batch calibration)	±0.6°C(3σ) (two point)
Resolution (conversion time)	0.25K (12.5µsec)	0.005K (100msec)	0.04K (6.25sec)	0.091K (500msec)
Resolution energy efficiency	19 pJ°K^2	11pJ°K^2	4.8µJ°K^2	160nJ°K^2

1.4 Energy-Efficiency Comparison

As concluded in the previous section, both resistor-based and BJT-based temperature sensors are suitable candidates for energy-efficient applications. To make the best choice, their energy-efficiency should be compared. This is the subject of the following sections.

1.4.1 Resistor-Based Sensing

A resistor-based temperature sensing technique is shown in Fig. 1.5 [8]. The temperature-sensitive-voltage signal is produced by making a voltage divider in which $R_{(T)}$ is a temperature dependent resistor and R_{ref} is a reference resistor assumed to be quite stable over temperature. The temperature sensitivity of the shown voltage divider then can be calculated as follows, while assuming $V_{DD} = 1.8V$, $R_{ref} = R_{(T)}$, and finally a typical temperature coefficient of 0.3%/K for available resistors in CMOS [8]:

$$\Delta V_{Sig} \approx \frac{1}{4}\left(\frac{\Delta R_{(T)}}{R_{(T)}}\right) V_{DD} = 1.44mV/°\mathrm{C}. \quad (1.3)$$

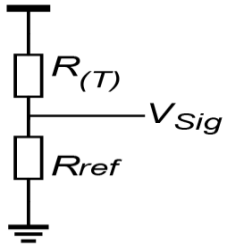

Figure 1.5. *Resistor-based temperature sensing [8].*

The noise associated with the voltage divider shown in Fig. 1.5, while drawing 1μA from a 1.8V supply (which means R = R_{Ref} = $R_{(T)}$ = 900kΩ) in a 5Hz bandwidth is equal to:

$$v_{n,Tot} = \sqrt{2 \times (4KT/R).(\frac{R}{2})^2.BW} = 189nV. \quad (1.4)$$

by combining this with the previously calculated sensitivity of the voltage divider together with its noise, then the temperature-sensing resolution can be calculated as follows:

$$\sigma_{T,Resistor} = \frac{v_{n,Tot}}{S_T^{\Delta V_{BE}}} = \frac{189nV}{1.44\ mV/\text{K}} = 131\mu\text{K}. \quad (1.5)$$

1.4.1 BJT-Based Sensing

The PTAT ratio μ in Eqn. 1.2, which represents the temperature, can be mapped into a reading in degrees Celcius by linear scaling:

$$D_{out} = A.\mu + B, \quad (1.6)$$

where A ≅ 600 and B= − 273. The temperature-sensing resolution of the BJT-based temperature sensor elaborated in [12] is as follows:

$$\sigma_{T,bip} = \frac{A}{V_{REF}}\alpha\sqrt{\frac{2kT(1-\mu)}{g_{m1}\cdot t_{conv}}}, \quad (1.7)$$

where g_{m1} is the transconductance of the transistor biased with the smaller bias current. Consequently, using A≅600, V_{REF}=1.2V and μ = 0.5 (which represents the bit density at room temperature), Eqn. 1.7 can be re-written as:

$$\sigma_{T,bip} \cong (5.1 \cdot 10^{-9}\ \text{KC}^{0.5}) \cdot \alpha\sqrt{\frac{1}{I\cdot t_{conv}}}, \quad (1.8)$$

where if t_{conv} = 100msec (5Hz bandwidth), α=20, and $I = 1\mu A$, the output-referred noise will be:

$$\sigma_{T,bip} \cong 320\mu\text{K}, \quad (1.9)$$

1.4.2 Conclusion

If the energy/conversion is assumed to be the same for both resistor and BJT-based approaches, then comparing Eqns. 1.5 and 1.9 and using Eqn. 1.1 reveals that the ultimate resolution FoM of resistor-based temperature sensors is about 6x better than the BJT-based FoM. This is because resistors can provide 2.5x more resolution.

1.5 Conclusion

It can be concluded that resistors are the best candidates for on-chip temperature sensing as far as energy-efficiency is concerned. However, designing an energy-efficient smart temperature sensor also requires energy-efficient readout circuitry. In order to prevent

excessive power from being wasted either in the sensor part or readout part, the readout circuitry noise-performance should be roughly the same as that of the sensor.

A literature study shows that in practice temperature sensor resolution is often limited by the noise of the readout circuitry. A resistor-based temperature sensor achieves 100µK in a 100msec conversion time, while its ultimate resolution should be 16µK under these conditions [8]. Also, a BJT based temperature sensor achieves 5mK with a 100msec conversion time, instead of the potentially achievable 0.2mK [9, 12]. This means that in these designs, the noise from the readout circuitry is still much higher than that of the sensor, thus there is still enough room to improve their energy-efficiency.

1.6 Thesis Organization

This thesis is organized as follows. A new resistor readout technique, called the "*Phase-Domain*" technique, is discussed in Chapter 2. Moreover, the sensor's design and implementation will be elaborated. In Chapter 3, the design of an energy-efficient temperature-sensing topology is presented. Furthermore, the circuit implementation and considerations of a first test chip are described. This chapter also includes the measurement results of the first test chip with a brief discussion on the weaknesses and potential points for improvement. In Chapter 4, the last chapter, the weaknesses of the first test chip will be addressed while a new ADC implementation based on the concept of a "*Hybrid Sigma-Delta Modulator*" is developed to address the previously mentioned requirements. This chapter ends with conclusion and a discussion of future work that can be done to further improve performance.

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2 *Temperature Sensing Principle*

2.1 Introduction

As previously discussed, than BJT-based temperature sensors, resistor-based temperature sensors are potentially more energy-efficient. In addition, an inaccuracy comparable with their BJT-based counterparts can be achieved by taking advantage of the multi-point trimming already used in the manufacture of MEMS frequency references [1-4].

As found in the literature and in a commercially available product, resistor-based temperature sensors have been used for MEMS resonator temperature compensation [1-7]. In this chapter some of the already existing readout principles, such as the use of RC oscillators [2] and an auto-balanced RC network [1], will be briefly described. Following that, a new approach based on measuring the temperature-dependent phase shift of an RC filter, called the phase-domain temperature sensing principle, will be presented [7]. This phase-shift can then be digitized by means of a phase-domain sigma-delta modulator (PDSDM) [8, 9]. This chapter continues with the requirements and design considerations related to the sensor's frontend. In the following chapter the requirements of the PDSDM for interfacing the RC filter will be discussed. Furthermore, the circuit implementation and considerations will be elaborated.

2.2 Existing Resistor-Based Temperature Sensors

The temperature information associated with a resistor's temperature-dependency can be extracted via different signals: voltage, current, phase, frequency, etc. As a result, widely different readout topologies can be used to extract this information. In the following some of the already existing temperature sensing methods used for MEMS resonator compensation is elaborated briefly.

2.2.1 Temperature-Dependent RC Oscillator

One way to read out a resistor is to bias it at a well-defined voltage and use the resulting temperature-dependent current to drive an oscillator [2]. Figure 2.1 shows a system-level implementation of this approach. This circuit consists of a temperature-dependent resistor R_{NW}, an operational transconductance amplifier (OTA), and an inverter-based ring-oscillator with an odd number of stages i and a total gate capacitance $C_G = \sum C_{G,i}$. The temperature dependent current flowing through the ring oscillator changes its output frequency. The dynamic equation which relates the current and frequency in the ring-oscillator can be expressed as follows [10]:

$$I = f.C_G.V, \tag{2.1}$$

Where I is the current flowing through the ring-oscillator, C_G is the gate capacitance, V is the supply voltage, and finally f is the logic's operational frequency. By using Ohm's law together with Eqn. 2.1, it can be shown that the oscillator's operational frequency will be proportional to $1/R_{NW}.C_G$, which in turn is a temperature dependent frequency [2].

It should be noted that the output frequency of a ring-oscillator is also supply-dependent [11]. This problem is mitigated by driving the inverters with a current source and also using a decoupling capacitor C_F to filter out high-frequency supply noise [2, 11-12]. In this design, the oscillator's phase-noise is dominated by the flicker-noise of the current sources and the opamp [11] which degrades the potentially high resolution achievable by using a resistor. This temperature sensor, after a one point trim, achieves ±3°C inaccuracy over a temperature range of 0°C to 100°C. It also achieves a resolution of 40mK in a 7.5msec conversion time while drawing 30µA from a 1V supply voltage, resulting a resolution-FoM of 36pJ°K^2 [2]. However, this performance is still two orders of magnitude worse than the resistor's ultimate energy-efficiency.

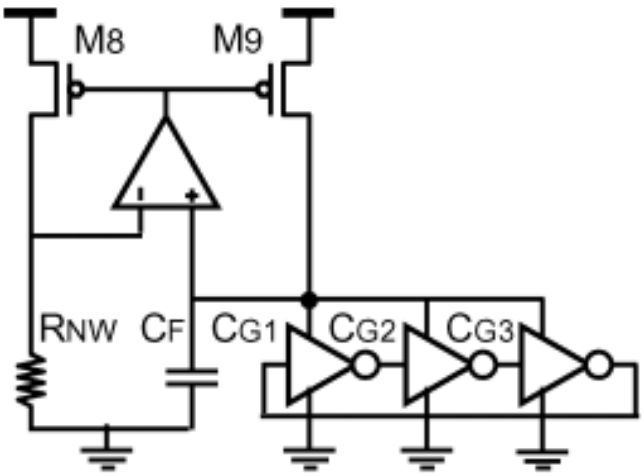

Figure 2.1. *Temperature sensing principle using the RC ring-oscillator [2].*

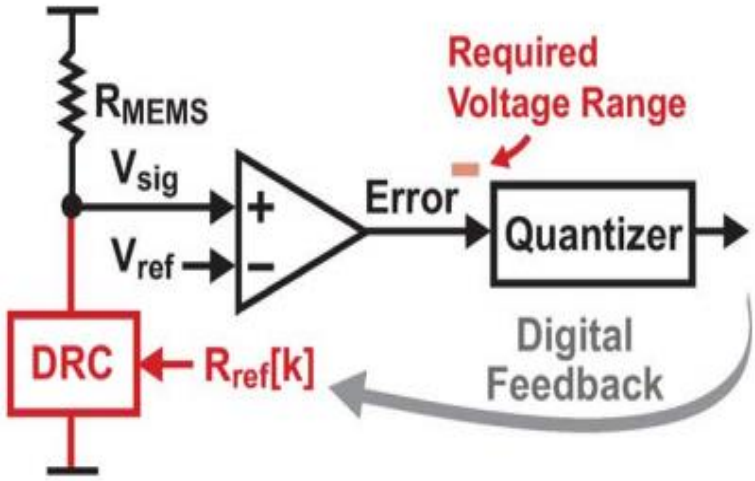

Figure 2.2. *Auto-balanced RC network readout principle [1].*

2.2.2 Auto-Balanced RC-Network

Another way of reading out a resistor is to embed the resistor in an auto-balancing voltage divider. Fig. 2.2 shows a system-level implementation of this approach [1]. It consists of a voltage divider, followed by an amplifier, and then a quantizer which digitally balances the reference impedance which is a part of the voltage divider. The voltage divider consists of a temperature dependent MEMS-resistor R_{MEMS} (0.3%/K) and a tuneable temperature independent reference impedance (implemented by stable capacitors over temperature). The voltage divider's output is then compared to a reference voltage by the following amplifier. The amplified error is then applied to a quantizer whose output will be fed back to tune the reference impedance. The task of the auto-balancing loop is to make the amplifier's output error zero. It is noticeable that the temperature-to-digital converter's (TDC) noise at low frequencies is dominated by the amplifier's flicker-noise, although windowed chopping technique is used. Whereas at high frequencies, the quantization noise associated with the quantizer is dominated. This readout technique achieves an energy-efficiency of 13 pJ°K^2, and 0.1mK resolution in a 100msec conversion time while the resolution of the sensing element is 16µK. Moreover, after 6 point trim, this approach achieves ±0.02°C inaccuracy over a -40°C to 85°C temperature range [1].

2.3 Phase-Domain Temperature-Sensing Principle

A digital temperature measurement requires a temperature-dependent signal and a temperature-independent signal as reference [13]. However, there is no accurate reference resistor in CMOS technology. Fortunately, in the context of MEMS frequency references a well-defined frequency is available [1-4]. So a well-defined SC resistor can be made, as discussed above. Alternatively, by translating the desired temperature-dependent signal into the time-domain, this frequency can be directly used as the desired reference signal [7].

One way of generating a temperature-dependent signal in time-domain is to exploit the fact that the phase-shift of an RC-filter is temperature dependent. So by driving an RC-filter at a fixed frequency the required temperature-dependent phase shift can be extracted. Since

metal-insulator-metal (MIM) capacitors and/or fringe capacitors are comparatively quite stable over temperature, the filter's phase shift will then be mainly a function of the resistor's temperature dependency. A point to be noted is that the RC-filter can be driven by a square-wave signal, which can be readily generated by digital circuits.

In the following sections, first, the way that an RC filter's phase-shift can be extracted will be elaborated. Then, since a high resolution temperature sensor is targeted, noise sources associated with the phase-domain temperature sensing principle are mentioned. The rest of this chapter is mainly devoted to the design and choice of the desired filter which converts the temperature information into the phase-domain.

2.3.1 Phase-Extraction Methodology

In order to extract the temperature-dependent phase shift associated with the RC-filter, phase demodulation can be employed [8-9]. This involves mixing the filter's output with a signal with the same frequency as the filter's driving signal but with a known phase. The mixer outputs an AC signal which is superimposed on a DC signal (see Eqn. 2.6). The mixer could be incorporated into a phase domain sigma-delta modulator (PDSDM) which then digitizes the phase-shift associated with the RC-filter [8, 9]. Figure 2.3 shows a system level implementation of a temperature sensor in the phase domain. A mathematical analysis of this system is described below.

Considering only the main tone of the filter's square-wave driving signal and assuming a phase shift of zero, the input to the RC filter can be expressed as:

$$\mathrm{Signal_{drive}} = \mathrm{A} \times \cos(2\pi \mathrm{f} + 0°). \tag{2.2}$$

The RC-filter's output then can be derived as:

$$\mathrm{Signal_{RC,Out}} = \mathrm{A} \times |\mathrm{TF_{RC}}| \cos(2\pi \mathrm{f} + \varphi_{\mathrm{RC}}). \tag{2.3}$$

The mixing signal can be modelled by a cosine function, whose phase shift is defined relative to the driving signal:

$$\mathrm{Signal_{Mixing}} = \mathrm{B} \times \cos(2\pi \mathrm{f} + \varphi_{\mathrm{Mix}}). \tag{2.4}$$

The mixed signal can then be calculated by using Eqn. 2.5:

$$\mathrm{Signal_{Mixer-out}} = \mathrm{Signal_{Mixing}} \times \mathrm{Signal_{RC-Out}}, \tag{2.5}$$

Substituting Eqns. 2.3 and 2.4 into Eqn. 2.5 results in:

$$\mathrm{Signal_{Mixer-out}} = \frac{\mathrm{AB}}{2} \times |\mathrm{TF_{RC}}| [\cos(\varphi_{\mathrm{RC}} - \varphi_{\mathrm{Mix}}) + \cos(4\pi \mathrm{f} + \varphi_{\mathrm{Mix}} + \varphi_{\mathrm{RC}})], \tag{2.6}$$

Where A is the amplitude of driving signal, B is the mixing signal's amplitude, $|TF_{RC}|$ is the magnitude of the filter's transfer-function, f is the filter's driving frequency, φ_{RC} is the phase shift associated with the filter, and finally, φ_{Mix} is the phase shift of the mixing signal.

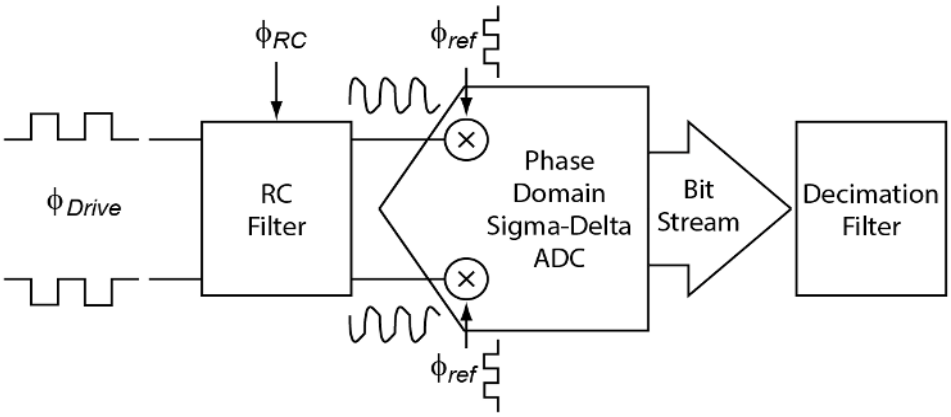

Figure 2.3. *System level implementation of a smart temperature-sensor in the phase-domain.*

2.3.1.2 Phase Extraction Linearity

In order to achieve the best accuracy, the temperature-to-phase mapping should be done in a linear manner, i.e. the mixer should be operated in its most linear region. From Eqn. 2.6, the DC signal bearing the temperature information is a cosine function, which can be linearized as follow if $(\varphi_{RC} - \varphi_{Mix})$ ~ 90 degrees:

$$\text{Signal}_{\text{Mixer,DC}} = \frac{AB}{2} \times |TF_{RC}| \times (\varphi_{RC} - \varphi_{Mix}). \quad (2.7)$$

2.3.2 Noise Sources Employing the Phase-Domain Principle

The noise sources associated with the phase-domain temperature sensing technique can be classified as follows, (also see Fig. 2.4):

1) Thermal noise of the filter
2) Readout circuitry noise (thermal & flicker noise)
3) Amplitude noise of the filter's driving signal
4) Phase noise of the filter's driving signal

The first two noise sources introduce only thermal noise, while the readout circuitry also causes flicker noise. It should be noted that lowering thermal noise usually requires more power. In order to be energy-efficient, while neglecting the flicker noise, the thermal noise contribution of the filter and the PDSDM should be the same at the filter's driving frequency Furthermore, the thermal noise should be much higher than the amplitude and phase noise introduced by the filter's driving signal. The effect of these noise sources are briefly elaborated below.

The noise of the filter's driving signal's amplitude could result in a noisy digital output, and depending on the ADC's operation principle and bandwidth, the output referred noise can then be calculated. The effect of this noise source will be discussed further in the next chapter.

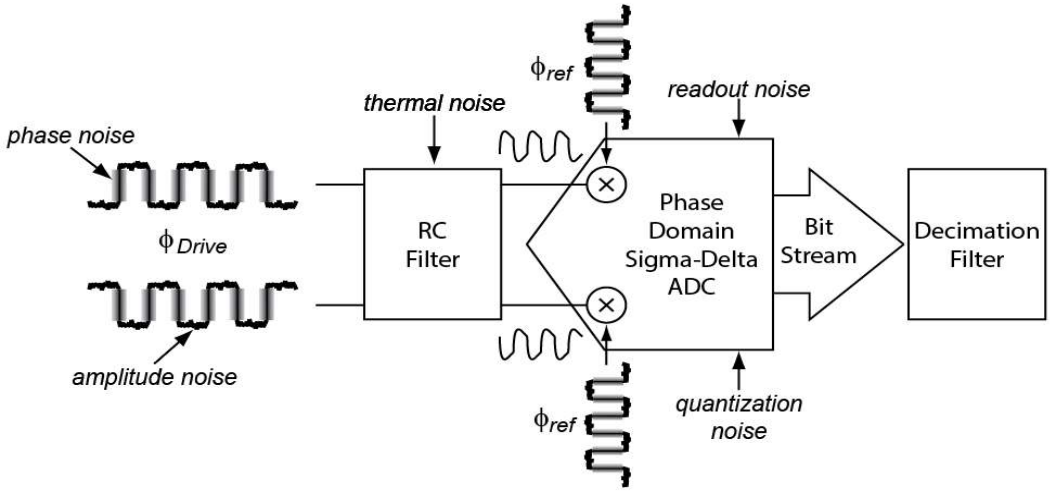

Figure 2.4. *Noise sources associated with the phase-domain approach.*

The phase noise of the MEMS frequency reference, ultimately limits the achievable resolution in the phase domain. The jitter performance of a state-of-the-art MEMS frequency reference is less than 1psec over a 20 kHz to 20MHz frequency range [1, 5]. This could be translated into a temperature-sensing resolution if the filter's phase-to-temperature sensitivity is known.

It should be mentioned that all the above discussions are based on the assumption that the quantization noise associated with the readout circuitry is much lower than the thermal noise of the whole system. This argument will be discussed in detail in the following chapter.

2.4 Considerations for the Filter's Implementation

While designing an RC-filter for temperature sensing application, several factors should be carefully considered, namely:

1) Phase-to-temperature sensitivity
2) Thermal noise of the filter
3) Amplitude of the driving signal
4) Phase-to-temperature linear-conversion
5) Filter's driving frequency

Below each of the aforementioned factors are introduced in detail:

With the purpose of making an energy efficient sensor, the most important factor to be considered is the sensor's phase-to-temperature sensitivity together with its noise; i.e. for a given noise floor, a higher temperature-sensitivity results in a higher signal-to-noise ratio (SNR). Phase-to-temperature sensitivity for three different types of filters, namely low-pass-filter (LPF), high-pass-filter (HPF), and band-pass-filter (BPF) will be discussed in this chapter.

While assuming the filter's thermal noise dominates all other noise-sources, the RC-filter phase-to-temperature sensitivity together with the filter's thermal-noise defines the sensor's

signal-to-noise ratio (SNR). To get the most resolution out of an RC-filter, while comparing sensitivity of different filters, the thermal-noise associated with each of them should also be considered. Moreover, the SNR associated with each of the aforementioned filters will be extracted.

From Eqn. 2.6, it can be concluded that the signal's change over temperature is proportional to the amplitude of the driving signal. Consequently, the higher the driving signal's amplitude, the better the achievable resolution will be. As a result, a rail-to-rail driving signal should be chosen.

Ideally, the temperature-to-phase mapping should be a linear function. However, the attenuation factor of an RC-filter causes high order systematic gain error. The effect of the non-linearity associated with the $|\mathrm{TF_{RC}(T)}|$ is shown in Eqn. 2.8:

$$\mathrm{Signal_{Mixer-out}} = \frac{\mathrm{AB}}{2} \times |\mathrm{TF_{RC}(T)}| \times (\varphi_{\mathrm{RC}} - \varphi_{\mathrm{Mix}}). \tag{2.8}$$

While investigating the filter's structure, this non-linear gain error should be taken into account. The residual gain error, after the intended multi-point trimming, should be much lower than the targeted inaccuracy, in order to prevent the need for more trimming points. In the following sections, phase-to-temperature mapping is discussed for the previously mentioned filters.

In order to choose the driving frequency of the RC-filter there are numerous considerations which should be taken into account. Since a high resolution temperature sensor is targeted, the first consideration is the flicker noise associated with the readout circuitry which dominates the noise performance in DC measurements. However, there are some other considerations such as parasitic effects and voltage dependency which restricts the choice of the filter's driving frequency. These factors should be taken into account while choosing the filter's driving frequency. Finally, a general remark to be noted is that implementing an RC filter regardless of its type in a differential topology gives 0.5bit more resolution compared to its single-ended counterpart. This is because, while signal power is 4x larger, noise power is only 2x greater. In addition, differential systems are more robust to external noise sources, since the noise appears as common-mode noise that can be mitigated by the differential system's common-mode rejection property.

2.4.1 Low Pass Filter (LPF)

The transfer function and phase of a 1st-order low-pass filter in the frequency-domain is expressed by Eqns. 2.9 and 2.10, respectively:

$$TF(T, j\omega) = \frac{1}{1+R_{(T)}Cj\omega} \tag{2.9}$$

$$\varphi_{\mathrm{RC-LP}}(\mathrm{T}, \mathrm{j}\omega) = -\tan^{-1}(\mathrm{R_{(T)}C}\omega), \tag{2.10}$$

where $\mathrm{R_{(T)}}$ is the temperature dependent resistor and C is the implemented capacitor value. Resistor temperature dependency changes the filter's time constant over the temperature. This variation can be modelled as a change in driving frequency while the time

constant is fixed. From Eqn. 2.10 it can be seen that the phase shift is also a function of frequency. Thus, the optimum driving frequency to achieve the maximum phase shift can be calculated. To do so, Eqn. 2.11 expresses the phase derivative as a function of angular frequency:

$$\frac{d(\varphi_{RC-LP}(T,\omega))}{d\omega} = -\frac{R_{(T)}C}{1+(R_{(T)}C\omega)^2} \tag{2.11}$$

Equation 2.11 reveals that for $\omega = \pm\infty$, the phase change due to the frequency change is zero. Since Eqn. 2.11 is a 2nd-order function, it will have a maximum at which the second derivative becomes equal to zero:

$$\frac{d^2(\frac{-R_{(T)}C}{1+(R_{(T)}C\omega)^2})}{d\omega} = 0 \rightarrow \left(3R_{(T)}^4C^4\omega^4 + 2R_{(T)}^2C^2\omega^2 - 1\right) = 0 \rightarrow \omega = 1/R_{(T)}C. \tag{2.12}$$

From Eqn. 2.12, it can be concluded that the second derivative becomes equal to zero at the filter's f_{-3dB} frequency which is equal to $1/(2\pi.R_{(T)}.C)$. Assuming a resistor with a temperature-coefficient of 0.3%/K, while driving the LPF at its f_{-3dB}, the filter's phase-shift will change by 15 degrees over the military temperature range. This is shown intuitively in Fig. 2.5.

2.4.1.1 1st-order LPF Noise

An LPF noise model is shown in Fig. 2.6 and its output-referred voltage noise power-spectral-density (PSD) is equal to:

$$S_{V_n,Out} = 4kTR \times |TF(T,j\omega)|^2, \tag{2.13}$$

where k is Boltzmann's constant, T is temperature, R is resistor value, and finally $|TF(T,j\omega)|$ is the magnitude of the filter's transfer function. Driving the filter at its f_{-3dB} frequency to get maximum phase shift, results in an attenuation of $|TF(T,f_{-3db})| \approx 0.7$. As a result, the filter's noise PSD at f_{-3dB} is:

$$S_{V_n,Out} = 4kTR \times \frac{1}{2}, \tag{2.14}$$

2.4.1.1 Temperature-to-Phase Conversion

The temperature-error associated with the temperature-to-phase conversion, after 3-point trim, should be much lower than the targeted inaccuracy. While using an ideal resistor with a constant linear temperature coefficient of 0.15%/K simulation result shows that, for an LPF a temperature inaccuracy of about 0.07°C could be achieved, after a 2nd-order polynomial fit (3-point trim) and over the industrial temperature range. Figure 2.7 shows the simulated temperature error of an LPF, which can be seen that an LPF could not satisfy the desired inaccuracy.

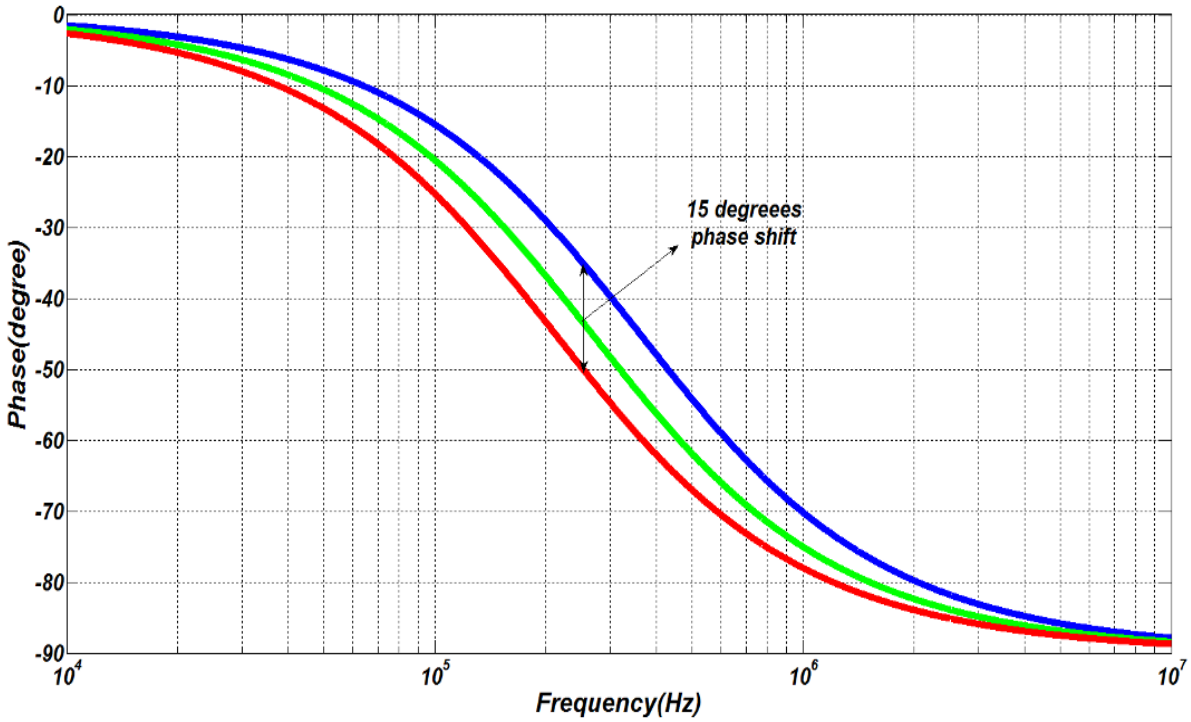

Figure 2.5. *LPF phase change over the military temperature range modelled in the frequency domain.*

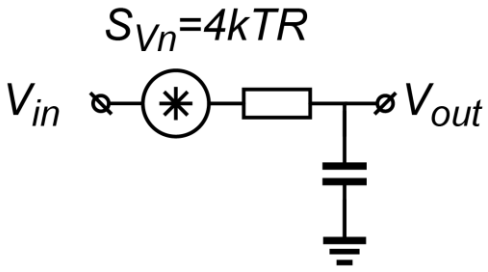

Figure 2.6. *LPF noise model.*

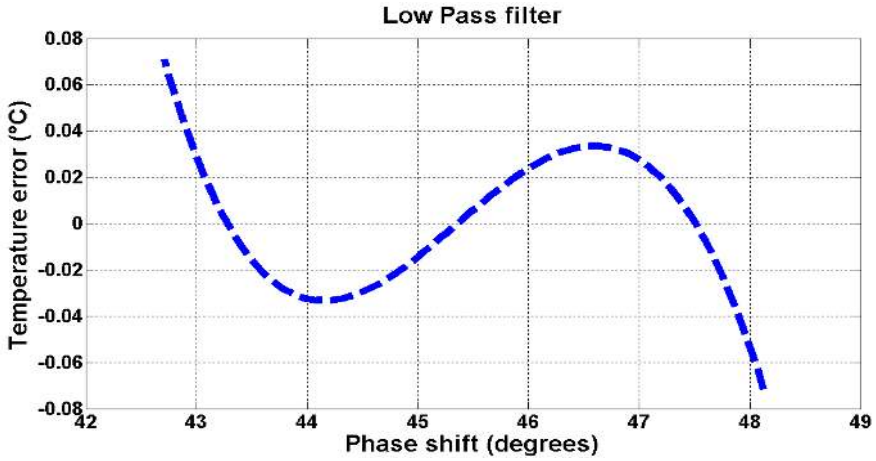

Figure 2.7. *Non-linearity associated with a 1st-order LPF after a 2nd-order fitting*

2.4.2 High Pass Filter (HPF)

Another possible filter implementation is a high-pass-filter. The transfer function and the phase response of a 1st-order HPF in the frequency domain is expressed by Eqns. 2.15 and 2.16, respectively:

$$TF(T, j\omega) = \frac{R_{(T)}Cj\omega}{1+R_{(T)}Cj\omega} \tag{2.15}$$

$$\varphi_{RC-LP}(T, j\omega) = \frac{\pi}{2} - \tan^{-1}(R_{(T)}C\omega), \tag{2.16}$$

where $R_{(T)}$ is the temperature-dependent resistor and C is the implemented capacitor. The phase-to-temperature sensitivity of an HPF will be exactly the same as an LPF under the previously determined condition for the LPF. As a result, assuming a resistor with a temperature-coefficient of 0.3%/°C, while driving the LPF at its f_{-3dB}, the filter's phase-shift will change by 15 degrees over the military temperature range. Moreover, for the same resistor value and filter's time constant, the noise PSD of an HPF at its f_{-3dB} will be the same as the LPF. Consequently, the only difference between the HPF and LPF could be their temperature-to-phase conversion which is elaborated below.

2.4.2.1 Temperature-to-Phase Conversion

The temperature-error associated with the temperature-to-phase conversion, after 3-point trimming, should be much lower than the targeted inaccuracy of less than 0.1°C. While using an ideal resistor with a constant linear temperature coefficient of 0.15%/K, simulation result for an HPF shows a temperature inaccuracy of about 0.07°C, after a 2nd-order polynomial fit (3-point trim) and over the industrial temperature range, which is exactly the same as LPF.

2.4.3 Band Pass Filter

In order to have a better understanding of how a BPF behaves in the time domain and frequency domain, Fig. 2.9 shows a BPF's square-wave response in the time domain, and Fig. 2.10 shows a 2nd-order BPF's Bode-plot, which consists of an LPF and an HPF. The BPF to be used for phase-domain approach should have the low pass filter's cut-off frequency to be the same as the HPF's stop band frequency. In this way the phase falls down over frequency with a constant slope of 90 degrees per decade, without any flat band in between. This could be done by choosing $R_{1(T)} = R_{2(T)}$ and $C_1 = C_2$.

2.4.3.1 Phase-to-Temperature Sensitivity

The same analysis done for the previous filter types could be repeated, in order to find the optimum filter's driving frequency to get the maximum phase change over temperature. To do so, first the filter's transfer function and phase response should be extracted. Equations 2.19 and 2.20 show the transfer function and phase response of the 2nd-order BPF sketched in Fig. 2.8:

$$TF(T, j\omega) = \frac{R_{(T)}Cj\omega}{\left(1-R_{(T)}^2C^2\omega^2\right)+3R_{(T)}Cj\omega} \tag{2.19}$$

$$\varphi_{RC-BPF}(T, j\omega) = -tan^{-1}\frac{(R_{(T)}^2 C^2\omega^2 - 1)}{3R_{(T)}C\omega}. \quad (2.20)$$

Assuming that resistors used in the 2nd-order BPF have the same temperature coefficient as the ones used in the LPF and HPF, then the resistor change results in a change of filter's time constant. Since phase shift is frequency dependent, there should be an optimum frequency which brings the most achievable phase shift. To calculate the optimum frequency, Eqn. 2.21 extracts the phase derivative over the frequency:

$$\frac{d(\varphi_{RC-BPF}(T,j\omega))}{d\omega} = -\frac{(3R_{(T)}C\omega)^2 \times (R_{(T)}^2 C^2\omega^2 + 1)}{\omega \times [(3R_{(T)}C\omega)^2 + \left(R_{(T)}^2 C^2\omega^2 - 1\right)^2]}. \quad (2.21)$$

Equation 2.21 reveals that for $\omega = \pm\infty$ the phase variation caused by the frequency change is zero. Since Eqn. 2.21 is a 4th-order function, it will have a maximum, at which the second derivative becomes zero. Equation 2.22 shows the 2nd derivative of the BPF phase response.

$$\frac{d^2\left(\frac{-R_{(T)}C}{1+(R_{(T)}C\omega)^2}\right)}{d\omega} = 0 \rightarrow \left(R_{(T)}^2 C^2\omega^2 - 1\right) = 0 \rightarrow \omega = 1/R_{(T)}C. \quad (2.22)$$

From Eqn. 2.22 it can be seen that the phase change is maximum at filter's center frequency. Assuming a resistor with temperature coefficient of 0.3%/K (the same as for the LPF and HPF), and driving the BPF at its center frequency, 20 degrees phase shift could be extracted over the military temperature range. This is shown intuitively in Fig. 2.10.

2.4.3.1 2nd-order BPF Noise

A noise model for a BPF is shown in Fig. 2.11. Then, the filter's output-referred voltage noise PSD is equal to:

$$S_{V_n,Out} = 4kT \times R_{Total,Out}(j\omega, T), \quad (2.23)$$

where $R_{Total,Out}$ is the filter's output resistance. The filter's output resistance is frequency dependent. While driving the filter at its center frequency, $R_{Total,Out}$ is equal to $\frac{2R}{3}$. It can be seen that the BPF noise PSD is 1.33x higher than that of the LPF or HPF (while resistor values are the same in both cases) while, the phase-to-temperature sensitivity of the BPF is about 1.33x greater. It can be concluded that the BPF's SNR is roughly the same as the LPF and HPF's SNR. Eqn. 2.24 mathematically proves that the SNR of a BPF in a certain bandwidth is about the same as that of its LPF (or HPF) counterpart.

$$\frac{SNR_{BPF}}{SNR_{HPF}} = \frac{10log\frac{(20\ \mathrm{deg})^2}{4kTR\times\frac{2}{3}\times BW}}{10log\frac{(15\ \mathrm{deg})^2}{4kTR\times\frac{1}{2}\times BW}} = 1.047, \quad (2.24)$$

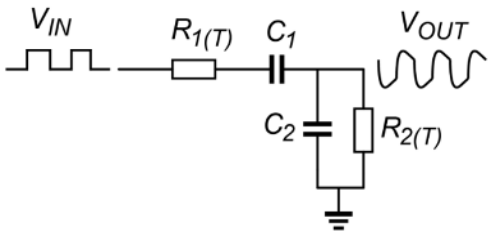

Figure 2.8. *BPF implementation and its square-wave response.*

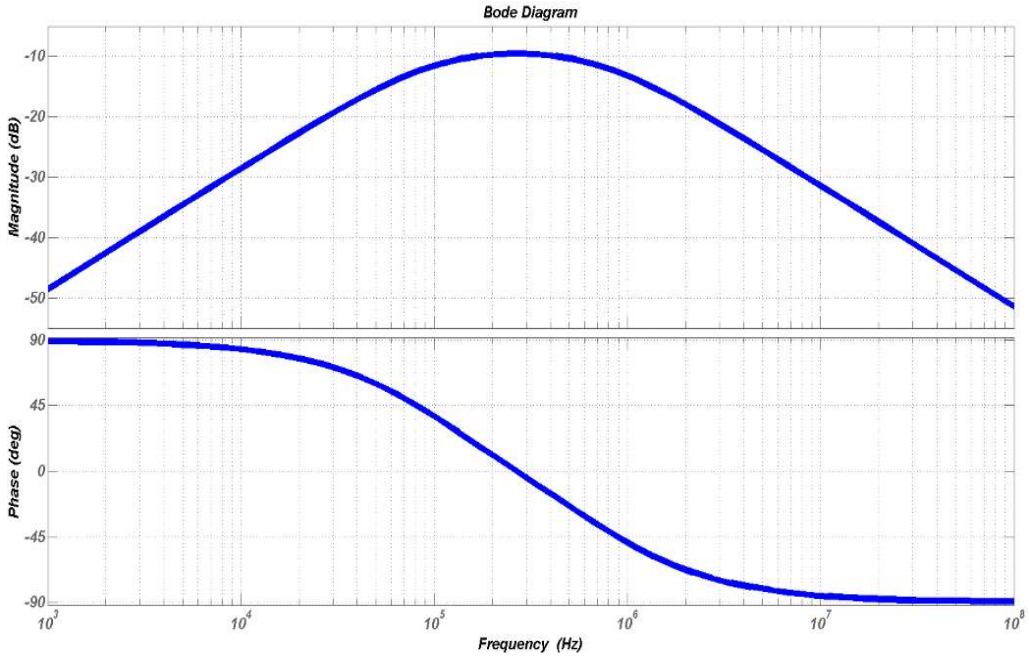

Figure 2.9. *BPF Bode-plot.*

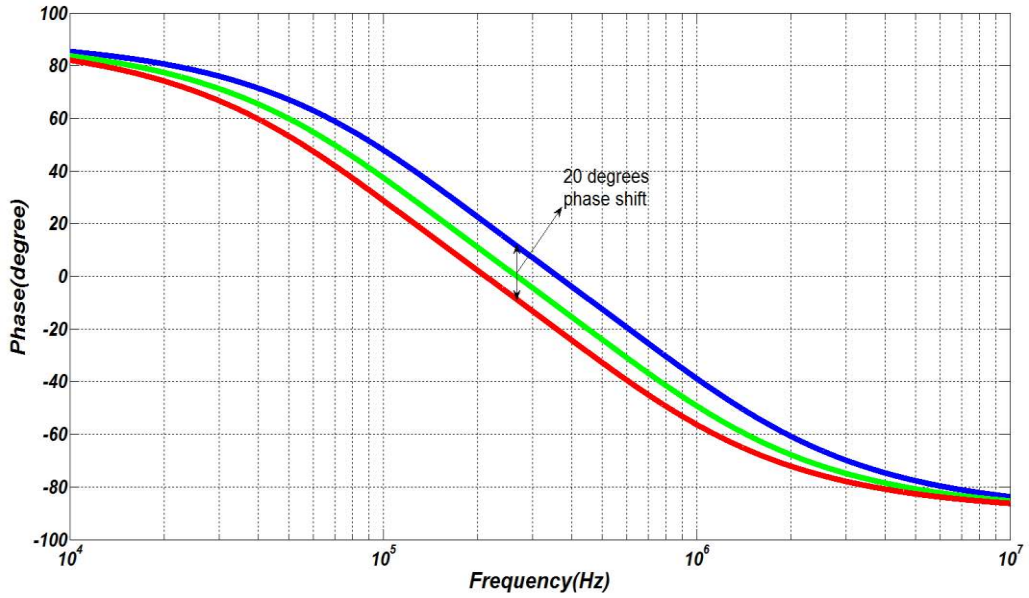

Figure 2.10. *BPF phase shift over the military temperature range*

2.4.3.2 Temperature-to-Phase Conversion

As discussed before, the temperature-error associated with the temperature-to-phase conversion should be much lower than the targeted inaccuracy of less than 0.1°C after a 3nd-order fitting. While using an ideal resistor with a constant linear temperature coefficient of 0.15%/K, simulation result for a BPF, show that the temperature inaccuracy after a 2nd-order polynomial fit (3-point trim) and over the industrial temperature range is about 0.03°C (see Fig 2.12) which is in line with the desired inaccuracy.

2.4.4 Conclusion

Looking at Table 2.1, it can be seen that neither the LPF nor the HPF could satisfy the targeted inaccuracy due to their systematic high-order non-linear temperature-dependence. However, that of a BPF is about 0.03°C which is in line with the targeted specification. This is due to the fact that the combination of an LPF with a HPF results in less non-linear temperature dependent gain error, while brings more phase change. On top of this, the BPF achieves a slightly higher SNR, which makes the BPF the best candidate of these three types of filters.

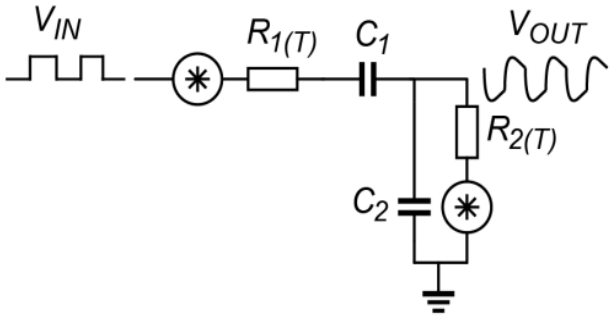

Figure 2.11. *BPF noise model*

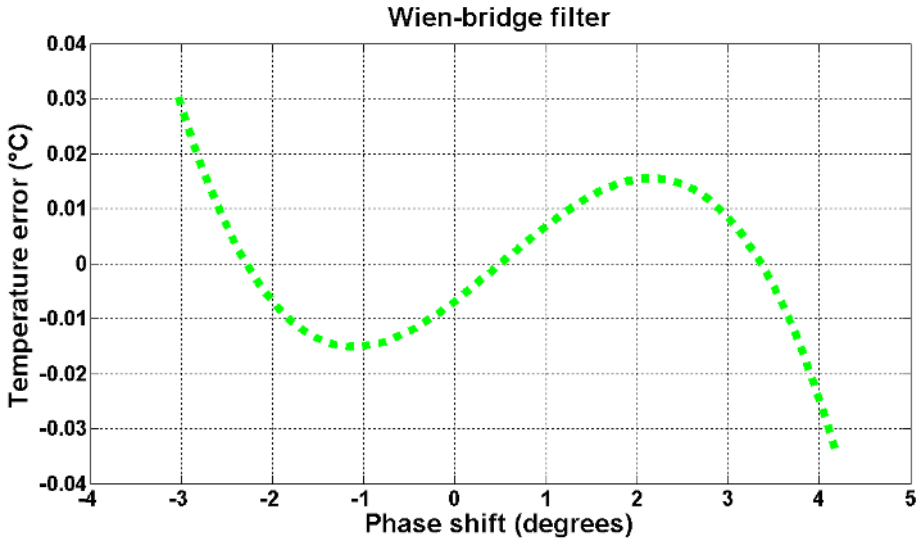

Figure 2.12. *Non-linearity of a 2nd-order Wien-bridge after a 2nd-order fitting.*

Table 2.1. *Characteristic of different type of filters*

Filter Type	Phase sensitivity (Degree/°C)	Normalized thermal noise	Systematic temperature error (3 point-trim)	SNR (normalized to *LPF*)
LPF	83m	$4kTR \times \frac{1}{2}$	0.07°C	1
BPF	110m	$4kTR \times \frac{2}{3}$	0.03°C	1.047
HPF	83m	$4kTR \times \frac{1}{2}$	0.07°C	1

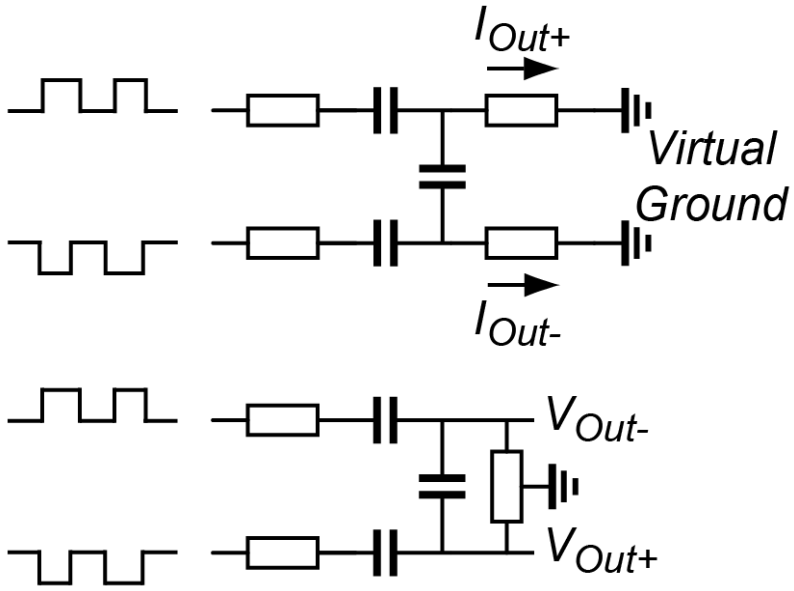

Figure 2.13. *BPF implementation: current output (top); voltage output (bottom).*

2.4.5 Implemented RC Filter

The BPF could be designed in such a way that its output can be in the voltage domain or in the current domain; both situations are shown in Fig. 2.13. The systematic temperature-error associated with them, are both equal to 0.01°C after a 3rd-order fitting. However, while considering the implemented readout circuit characteristics, one of them should be chosen. In the fabricated design, the band pass filter outputs a temperature dependent current which this filter is called Wien-bridge RC filter. The reason for this choice is motivated in Chapter 3 while discussing the readout implementation.

2.4.6 Conclusion

So far, it is shown that the Wien-bridge RC filter performs much better than the HPF and LPF, both in terms of systematic temperature-error and SNR. On top of this, an argument of how the SNR is related to the value of the implemented resistor was elaborated. However, in order to design the filter, characteristics of different type of resistors, available in the design kit, should be investigated, in order to satisfy the previously mentioned requirements. Next section discusses the characteristics of available resistors.

2.5 Available Resistors in CMOS

In order to make an energy efficient temperature sensor, the resistor's temperature coefficient must be as high as possible, so that a larger *SNR* could be extracted. In CMOS technology, there are different types of resistors available, each of which having different temperature coefficient. They also have different resistivities, parasitic capacitances, and voltage dependencies. Available resistors in CMOS could be mainly classified into 3 main branches:

1) Resistors with doped silicide
2) Resistors without doped silicide
3) N-well resistors

The resistors with doped silicide and the n-well resistors have the highest temperature coefficients. Although resistors with silicide have a high temperature coefficient, their unit sheet resistance is about two orders of magnitude lower than that of the other resistors. This characteristic makes the silicide resistors unsuitable, when large resistance is required.

Resistors without silicide have 2x lower temperature coefficient (except for the P^+ doped polysilicon resistor, which is 10x lower) than the other resistors, which results in 2x less resolution for the same resistor value. This drawback could be neglected by their relatively high resistivity when compared to silicide resistors. Thus, resistors without silicide (except P^+ poly-silicon) could be good candidates.

So far, the resistors without silicide (except P^+ Polysilicon) and n-well resistors look suitable for the targeted application. However, still some other considerations should be accounted for when using them as sensors. These considerations could be classified as: non-linear temperature dependence, voltage dependency, parasitic effects and area, which are all discussed in the following sections.

2.5.1 Non-Linear Temperature-Dependence

Since multi-point trim could be applied during trimming/calibration process, resistors' high-order non-linear behavior can be easily removed. However, in order to simulate and fairly judge the inaccuracy of different types of resistors and after a high-order fitting, resistors' high-order temperature coefficients are desired. Since these coefficients are not provided in the design kit, in the first design fabrication, four different RC filters using different types of resistors (N^+ diffusion, P^+ diffusion, n-poly and n-well under shallow trench isolation (STI)) are implemented.

2.5.2 Parasitic Effects

As previously discussed, the driving frequency of the filter should be higher than the flicker-noise corner frequency associated with the readout circuitry. This driving frequency could be translated into a certain time-constant for the implemented filter which is a function of the RC product. Parasitic effects should be considered since they could change the desired filter's transfer function. In the case of an N^+ diffusion resistor, the presence of the junction capacitance associated with the reverse-biased diode formed by the N^+ region and p-well

(shown in Fig. 2.14) results in a distributed RC network. To maintain the desired filter transfer function, the parasitic zeros and/or poles should preferably be separated by more than two orders of magnitude from the zeros and/or poles of desired filter. Consequently, the resistor and capacitor values should be chosen in such a way to satisfy this requirement.

2.5.3 Voltage Dependency

Resistors implemented in CMOS technology are voltage dependent. As a result the output of a resistor-based temperature sensor will also be voltage dependent. Moreover, the previously discussed junction parasitic capacitors are exponentially voltage-dependent. This problem can be tackled by biasing the resistors such that the junction diodes are deeply reverse-biasing, and thus have the minimum parasitic capacitance. In order to compete with other types of sensors, the targeted specification for the voltage dependency is less than 1°C/V.

2.5.4 Conclusion

As mentioned before, the promising resistors to be used as temperature sensing element, are N^+ diffusion, P^+ diffusion, n-poly and n-well. However, while implementing these resistors, the driving frequency of the filter should be chosen while considering temperature-sensing resolution and temperature-inaccuracy associated with the filter. As flicker noise dominates the noise performance in DC measurement, while assuming that chopping technique could be employed in order to mitigate it, a driving frequency higher than the flicker noise corner frequency is required. It should be mentioned that MOS devices in CMOS technology, typically have a flicker noise corner frequency about 100kHz. Moreover, the higher the driving frequency the faster the phase extraction loop converges. However, parasitic effects and voltage dependency associated with resistors, place an upper limit for the filter's driving frequency. Simulation results show that having a driving frequency higher than 250kHz, parasitic effects start to change the desired transfer function associated with the Wien-bridge filter.

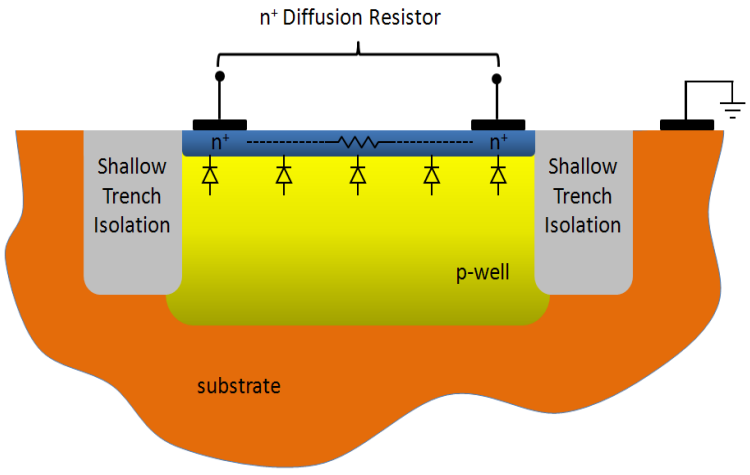

Figure 2.14. *N^+ diffusion resistor implemented in a p-well*

2.6 Temperature Sensing Resolution

As concluded above, a driving frequency of 250kHz is required for the Wien-bridge RC filter. The aforementioned driving frequency represents an RC time constant defining the centre frequency of the implemented Wien-bridge which is a function of RC product. However, in order to achieve a sub-mK resolution in a 5Hz bandwidth, resistor value should be chosen appropriately, while the temperature sensitivity of the implemented Wien-bridge is taken into account. A Wien-bridge exploiting the phase-domain temperature sensing approach is shown in Fig. 2.15.

2.6.1 Temperature Sensitivity

In order to calculate the desired resistor value, the temperature sensitivity of the Wien-bridge should be first extracted. From Eqn. 2.20, the phase shift of a Wien-bridge RC filter is a function of driving frequency together with the RC time constant. As the frequency is chosen to be 250kHz, the phase-to-temperature sensitivity is a function of the temperature dependency of the resistor, which can be calculated as follows:

$$\frac{d(\varphi_{RC-WB}(R_{(T)},\omega))}{d(R_{(T)})} \times \frac{d(R_{(T)})}{dT} = -\frac{(3R_{(T)}C\omega)^2 \times (R_{(T)}^2 C^2\omega^2+1)}{R_{(T)} \times [(3R_{(T)}C\omega)^2 + \left(R_{(T)}^2 C^2\omega^2 - 1\right)^2]} \times \frac{d(R_{(T)})}{dT}. \quad (2.25)$$

While substituting the temperature coefficient of the previously discussed resistors into Eqn. 2.25, phase-to-temperature sensitivity of the implemented Wien-bridge and for different resistors could be extracted. Table 2.2 shows the calculated phase-to-temperature sensitivity for different type of resistors. This phase-to-temperature sensitivity could be translated into a current-to-temperature sensitivity of the DC output current, by using Eqn. 2.26:

$$I_{\mathrm{DC,WB}} = \frac{\mathrm{V}}{2\mathrm{R}_{(\mathrm{T})}} \cdot |TF_{RC-WB}| \cdot \cos(90 - \varphi_{RC}) \quad (2.26)$$

Where V is the amplitude of the driving signal equal to 1.8V, $|TF_{RC-WB}|$ is the attenuation factor of the Wien-bridge at its center frequency which is equal to 1/3. Then, Eqn. 2.26 could be simplified as:

$$I_{\mathrm{DC,WB}} \cong \frac{300\mathrm{mV}}{\mathrm{R}_{(\mathrm{T})}} \cdot \varphi_{RC-WB}(\mathrm{T}) \quad (2.27)$$

Assuming a first-order temperature dependence for the resistors, $\mathrm{R}_{(\mathrm{T})} = \mathrm{R}_{(\mathrm{T}_0)}(1 + \alpha\Delta\mathrm{T})$, and using the previously calculated phase-to-temperature sensitivity, the current-to-temperature sensitivity could be calculated as follows:

$$S_T^{I_{DC,out}} = \frac{d(I_{\mathrm{DC,WB}})}{d(\mathrm{T})} = 300\mathrm{mV} \cdot \frac{\frac{d(\varphi_{RC-WB}(R_{(T)},\omega)}{d(\mathrm{T})} \cdot R_{(T)} - \frac{d(R_{(T)})}{d(\mathrm{T})} \cdot \varphi_{RC-WB}(R_{(T)},\omega)}{\left(\mathrm{R}_{(\mathrm{T})}\right)^2}. \quad (2.28)$$

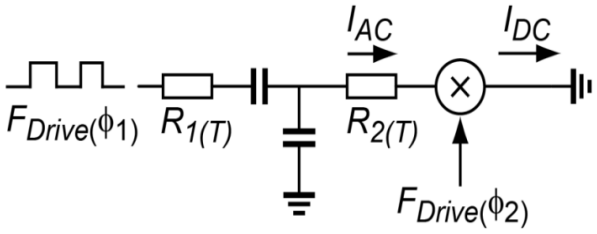

Figure 2.15. *single ended Wien-bridge RC-filter exploiting phase domain temperature sensing approach*

Table 2.2. *BPF DC current-change for the implemented resistors.*

Resistor type	DC current-change $(\frac{\text{mV/°C}}{R})$	Phase change (mradian/°C)
N-poly	0.57	55
P^+ diffusion	0.74	72
N^+ diffusion	0.74	72
N-well under STI	1.2	116
N-well under OD	1.42	138

Substituting the previously calculated phase-to-temperature sensitivity together with the temperature coefficient of the n-well resistor, the output current sensitivity could be calculated as follows:

$$S_T^{I_{DC,out}} = \frac{d(I_{\text{DC,WB}})}{d(\text{T})} = \frac{1.2\ \text{mV/°C}}{R}. \tag{2.28}$$

Then, the current-to-temperature sensitivity for different type of resistors is also shown in Table 2.2.

2.6.1 BPF Noise Analysis

In order to calculate the resolution, the output referred current noise PSD of the Wien-bridge at its centre frequency should be calculated, which determines noise floor at DC when mixing action takes place. Looking at Fig. 2.15, the noise of the resistor R_1 will be low-pass filtered, while the noise of the resistor R_2 will be high-pass filtered. Then, the filter's output-referred current noise PSD at its centre frequency and in a single-ended configuration could be calculated as follows:

$$\text{S}_{\text{I}_\text{n},\text{Out}} = \frac{1}{|TF_{WB,IN}|^2} \times \frac{4\text{kTR}_1}{\text{R}_2{}^2} + \frac{1}{|TF_{WB,Out}|^2} \times \frac{4\text{kTR}_2}{\text{R}_2{}^2} \xrightarrow{\text{R=R}_1\text{=R}_2} \approx \frac{4\text{kT}}{2\text{R}/3}. \tag{2.29}$$

Consequently, the integrated noise in a 5Hz bandwidth is as follows:

$$\sigma_{\text{I}_\text{n},\text{Out}} = \sqrt{\frac{6\text{kT}}{\text{R}} \times 5\text{Hz}}. \tag{2.30}$$

2.6.2 Temperature Sensing Resolution

The temperature sensing resolution, while the sensitivity of the n-well resistor is taken into account, could be calculated as follows:

$$\sigma_{T,WB} = \frac{\sigma_{I_n,Out}}{S_T^{I_{DC,out}}} = \frac{\sqrt{\frac{6kT}{R}\times 5Hz}}{\frac{1.2mV/°C}{R}} = \frac{\sqrt{6\cdot kT\cdot R\cdot 5Hz}}{1.2\ mV/°C}. \quad (2.30)$$

In order to achieve a resolution of better than 250μK in the 5Hz bandwidth and for the aforementioned n-well resistor, the resistor value should have a value lower than 150KΩ. Moreover, in order to satisfy the desired time constant, a capacitor value equal to 4pF is desired. This resolution represents an SNR of more than 120dB in the 5Hz bandwidth. In order to reach a signal-to-quantization-noise (SQNR) of higher than 120 dB, an appropriate PDSDM should be implemented, which is discussed in next chapters.

2.7 Conclusion

A band-pass-filter is selected in order to play the role of the temperature sensing element. The BPF brings a systematic non-linearity error of about 20mK after a 2nd-order fitting over the military temperature range which satisfies our targeted specification. A driving frequency of 250kHz has been chosen which defines the centre frequency of the Wien-bridge. In order to achieve sub-mk resolution while satisfying all the other considerations such as parasitic effects and voltage dependency, the Wien-bridge incorporates a 135kΩ resistor and a 4.4pF capacitor. The implemented Wien-bridge achieves a resolution of few hundreds μK in a bandwidth of a 5Hz, while using the aforementioned resistors available in CMOS technology. This signal can then be digitized by implementing a phase domain sigma-delta modulator. Next chapter, Chapter 3, first covers the system level design of the PDSDM. Afterwards, the circuit implementations and design considerations, in order to interface the Wien-bridge filter, will be further discussed.

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3 First Test Chip

3.1 Introduction

An energy-efficient, high-resolution phase domain analog-to-digital converter (ADC) is required for the targeted application. A sigma-delta ADC is the best choice for high-resolution applications since it only makes modest demands on the accuracy of its analog components [1, 2]. Oversampling is used to spread the quantization noise over a wider bandwidth and also it shapes quantization noise outside the signal band [5].

The aim of the first test chip is to determine the inaccuracy associated with each type of resistors, while exploiting a phase domain sigma-delta modulator (PDSDM). In order to be able to achieve an inaccuracy of less than 0.1°C, the resolution of the implemented PDSDM should be much lower than the targeted inaccuracy [5]. On top of this, the non-linear temperature dependence of the PDSDM should be much lower than what resistors have.

In this chapter, some of the prior PDSDM implementations are first briefly discussed. Then, the PDSDM implementation in order to satisfy the aforementioned requirements, together with the system level considerations is elaborated. In the following, the circuit level implementation of the first test chip will be presented. This chapter will be concluded with briefly discussing the weaknesses and possible improvement points, which will be then dealt with in more detail in next chapter.

3.2 Prior PDSDM Implementations

A 1^{st}-order continuous-time (CT) PDSDM incorporating a synchronous chopper demodulator which extracts the input phase signal is presented in [2]. The aim of this design was to extract the phase shift associated with an electro-thermal filter (ETF). The PDSDM incorporates a passive G_m-C integrator which constitutes an ADC (see Fig. 3.1) with a thermal noise floor of lower than -80dB while burning about130µA from a 5V supply.

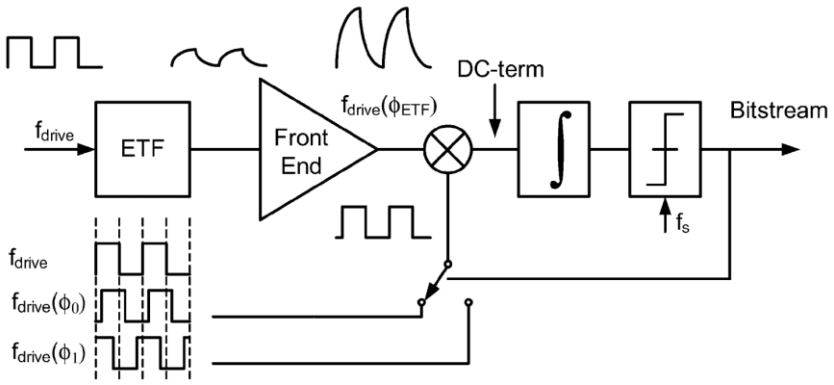

Figure 3.1. *1st-order CT PDSDM incorporating Gm-C integrator [2]*

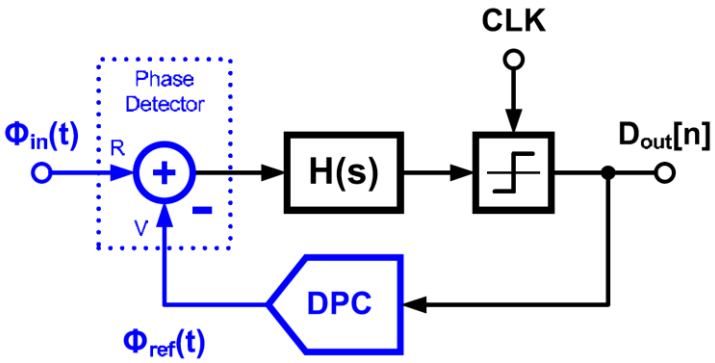

Figure 3.2. *Charge balancing scheme used in 2nd-order CT PDSDM [3]*

A 2nd-order CT PDSDM is presented in [3]. The utilized charge balancing scheme in the implemented PDSDM is exactly the same at the one used in (see Fig. 3.2) [2]. However, a 2nd-order loop-filter is employed to lower the desired conversion time together with the quantization noise floor. The loop filter incorporates CT active integrators which ensures a noise floor of lower than -80dB and over a 1MHz bandwidth. The whole ADC consumes 2.1mW from a 1.2V supply.

3.3 First Test Chip

The following section will discuss the system and circuit design of the first test chip which consists of four Wien-bridges (WB) followed by a 1st-order PDSDM. The target of this design is to extract the inaccuracy of four WBs, each of which uses one of the previously discussed resistors (n-poly, n-well under STI, P^+ diffusion and N^+ diffusion). Consequently, the 1st-order PDSDM should have a resolution much lower than the targeted inaccuracy of lower than 0.1°C.

3.3.1 PDSDM system level architecture

Figure 3.1 shows the simplified block-diagram of the proposed smart temperature sensor in the phase-domain, which mainly consists of 3 blocks as follows: Wien-brige RC-filter (WB), phase generator, and a 1st order PDSDM

The implemented Wien-bridge is the sensing element, which provides the desired temperature dependent phase shift signal. As previously discussed, the band-pass RC-filter is driven by a square-wave, at a constant frequency with a defined phase shift called φ_{drive}. The filter's phase shift can be extracted by mixing this signal with another signal, which has the same frequency but different phase shift. This mixer is incorporated in a PDSDM, which is controlled by the reference-phase signals. In next section, the system level design of a 1st-order PDSDM will be presented.

3.3.2 1st order PDSDM system-level design

The PDSDM operation is the same as the amplitude-domain counterparts. However, in phase domain the input is a phase signal, which requires the reference signals also to be in the phase-domain [1-4]. As shown in Fig. 3.3, the 1st-order PDSDM consists of a mixer, an integrator, a single-bit quantizer, and a one-bit phase-DAC. Depending on the output of the quantizer, the phase shifted output of the Wien-bridge RC filter will be mixed with one of the two reference-phase signals. The mixer acts as the $\Sigma\Delta$ modulator's summing node [5], which outputs a current whose DC component is proportional to the cosine of the phase difference between the output of the Wien-bridge, φ_{RC}, and that of the phase DAC, φ_{FB}. This current will be then accumulated by the following integrator whose output is fed to a quantizer. The quantizer outputs a bit-stream which is fed back to select the desired reference-phase signal. The average of the modulator's bit-stream is a weighted average of the two reference-phase signals φ_{ref1} and φ_{ref2}, which represents the phase-shift of the Wien-bridge, φ_{RC}.

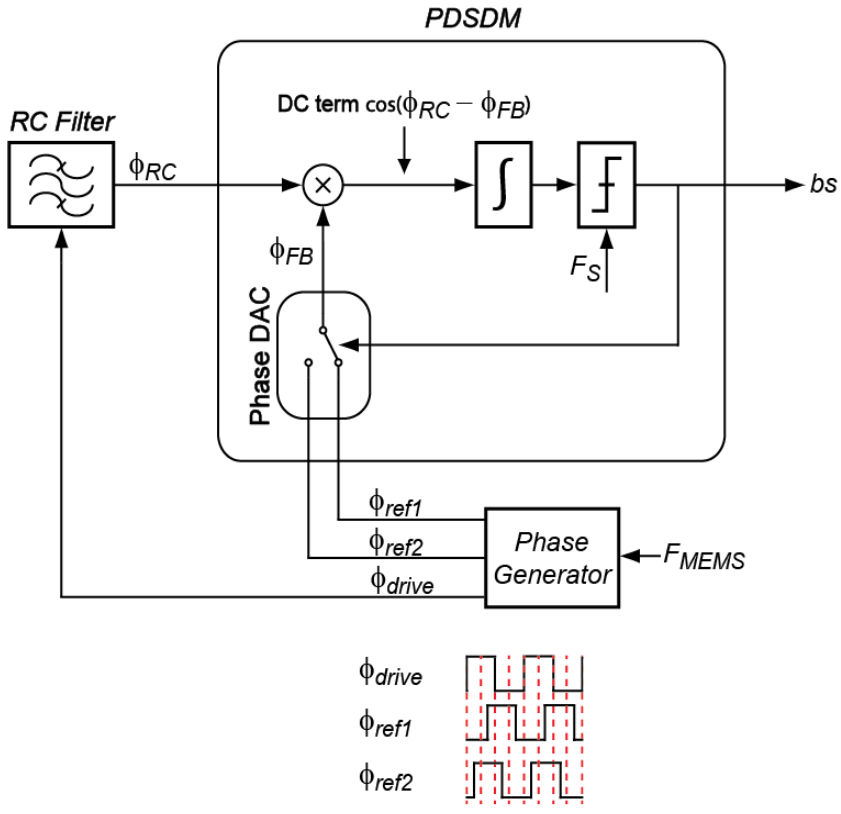

Figure 3.3. *phase-domain temperature sensing approach employing a PDSDM*

A complete block diagram of the first test chip is shown in Fig. 3.4. As discussed in Chapter two, the WB is driven at f_{drive}=250 kHz. Its micro-amp level AC output current which conveys the desired phase shift is then fed into the PDSDM. The modulator's mixer is implemented as a synchronous chopper demodulator, embedded in the current buffer and its integrator is implemented by capacitor C_{int}. As it is expected from the integrator's characteristics, the high-order harmonics of f_{drive}, present at the output of the synchronous demodulator due to mixing action, will be attenuated. The output of the integrator is then fed into the single-bit quantizer implemented in the PDSDM. The output of the quantizer will then select the desired reference-phase signal by controlling the implemented phase-DAC. This feedback loop balances the average charge accumulated by the integrator.

The phase generator block is implemented by an off-chip FGPA, which provides the desired reference-phase signals, driving signal and the quantizer's sampling frequency. As mentioned in chapter two, depending on the type of the resistor, the filter's phase shift varies between 10 to 20 degrees (radian) over the military temperature range. As a result, the ADC's full-scale, defined by the reference-phase signals, has to be larger than the phase-change over the temperature. Considering the resistor's spread, the full-scale phase is designed to be roughly 2x more than the maximum phase-change over the military temperature range.

3.3.2.2 Charge-balancing scheme in PDSDM

Discussed in Chapter two, the filter's phase-shifted signal after mixing with the reference-phase signal, results in a signal with a DC term together with a 2nd order harmonic of driving frequency. The mixer's output can be extracted from the Eqn. 2.6 as follows:

$$I_{\text{Mixed}} = \frac{\text{V}}{2\text{R}_{(\text{T})}} . |TF_{RC-WB}| \, [\, \cos(\varphi_{drive} + \varphi_{RC} - \varphi_{FB})$$

$$+\cos(4\pi f_{drive} + \varphi_{drive} + \varphi_{FB} + \varphi_{RC}) \,] \qquad (3.1)$$

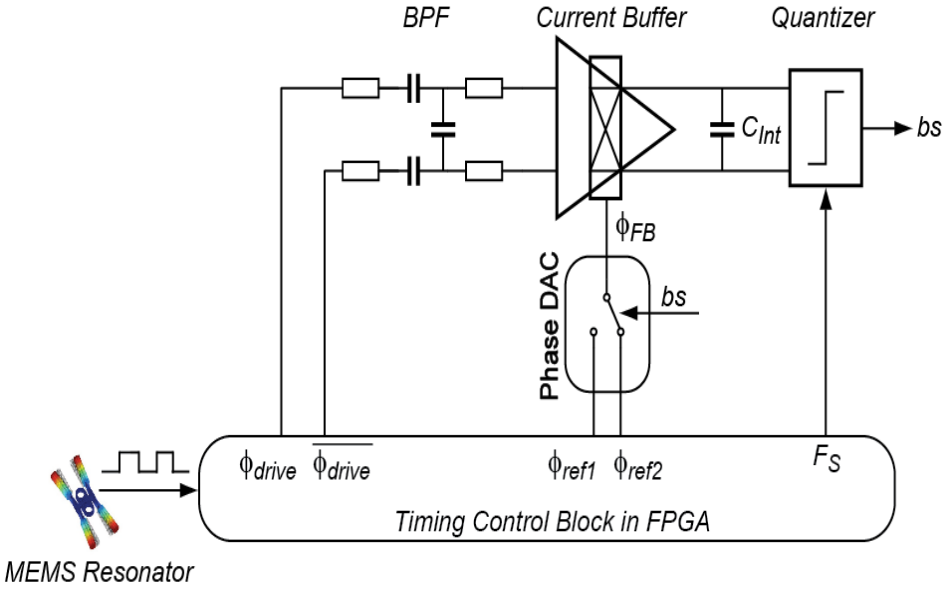

Figure 3.4. *Top-level implementation of Phase-domain temperature sensing approach*

Where V is the filter's driving signal voltage amplitude, R is the implemented resistor's value, $|TF_{RC-BPF}(T, j\omega)|$ is the magnitude of the Wien-bridge's transfer function, φ_{RC} is the phase shift associated with the WB, and φ_{FB}, toggles between the two reference phase signals depending on the polarity of the modulator's bit-stream.

The DC current which conveys the desired phase information will be accumulated by the C_{int}. This DC component contributes to the charge-balancing scheme of the PDSDM. Then, the 1st order sigma-delta feedback loop controls the reference signals and constructs the charge-balancing scheme associated with the sigma-delta structure. This balancing action could be mathematically shown as follows:

$$\mu.\frac{\mathrm{V}}{2\mathrm{R}_{(\mathrm{T})}} \times |TF_{RC-BPF}|[\cos(\varphi_{drive} + \varphi_{RC} - \varphi_{ref1}) +$$

$$(1-\mu)\frac{\mathrm{V}}{2\mathrm{R}_{(\mathrm{T})}} \times |TF_{RC-BPF}|[\cos(\varphi_{drive} + \varphi_{RC} - \varphi_{ref2}) \approx 0 \quad (3.2)$$

Where μ is a number between 0 and 1, which represents φ_{RC} as a weighted average of the two phase references, φ_{ref1}, and φ_{ref2}:

$$\mu \approx \frac{\cos(\varphi_{drive}+\varphi_{RC}-\varphi_{ref1})}{\cos(\varphi_{drive}+\varphi_{RC}-\varphi_{ref1})-\cos(\varphi_{drive}+\varphi_{RC}-\varphi_{ref2})}. \quad (3.3)$$

Described in Chapter two, the cosine function can be linearized while having a $\varphi_{drive} + \varphi_{RC} - \varphi_{ref}$ close to 90 degrees (radian). This condition could be satisfied by making a phase difference of 90 degrees between the driving signal and reference signal, which requires:

$$\varphi_{drive} + \varphi_{RC} = 90° + \varphi_{ref} \quad (3.4)$$

Then, the linearized relation between μ and phase signals could be shown as follows:

$$\mu \approx \frac{90-(\varphi_{drive}+\varphi_{RC}-\varphi_{ref1})}{\varphi_{ref2}-\varphi_{ref1}} \quad (3.5)$$

3.3.2.3 Considerations of Wien-bridge Interfacing

Figure 3.5 (a) shows how ideal readout circuitry should interface the Wien-bridge RC filter. Non-idealities such as the residual offset [Figure 3.5 (b)] added to the DC signal of Eqn. 3.2, or the electrical phase error [Figure 3.5 (c)] added by the current buffer to the AC signal (Eqn. 2.3 Wien-bridge's output) leads to errors in the digitized value of φ_{RC}. These errors will then lead to temperature reading error. In the case of a residual offset current, added to the demodulated DC signal, the modulator's feedback will still ensure that the average charge accumulated by the integrator is still approximately zero. Although, a different steady value μ' results:

$$\mu'.(V/2R) \times |TF_{RC-BPF}|[\cos(\varphi_{drive} + \varphi_{RC} - \varphi_{ref1}) +$$

$$(1-\mu')\cdot(V/2R) \times |TF_{RC-BPF}|[\cos(\varphi_{drive} + \varphi_{RC} - \varphi_{ref2}) + I_{OS} \approx 0 \quad (3.6)$$

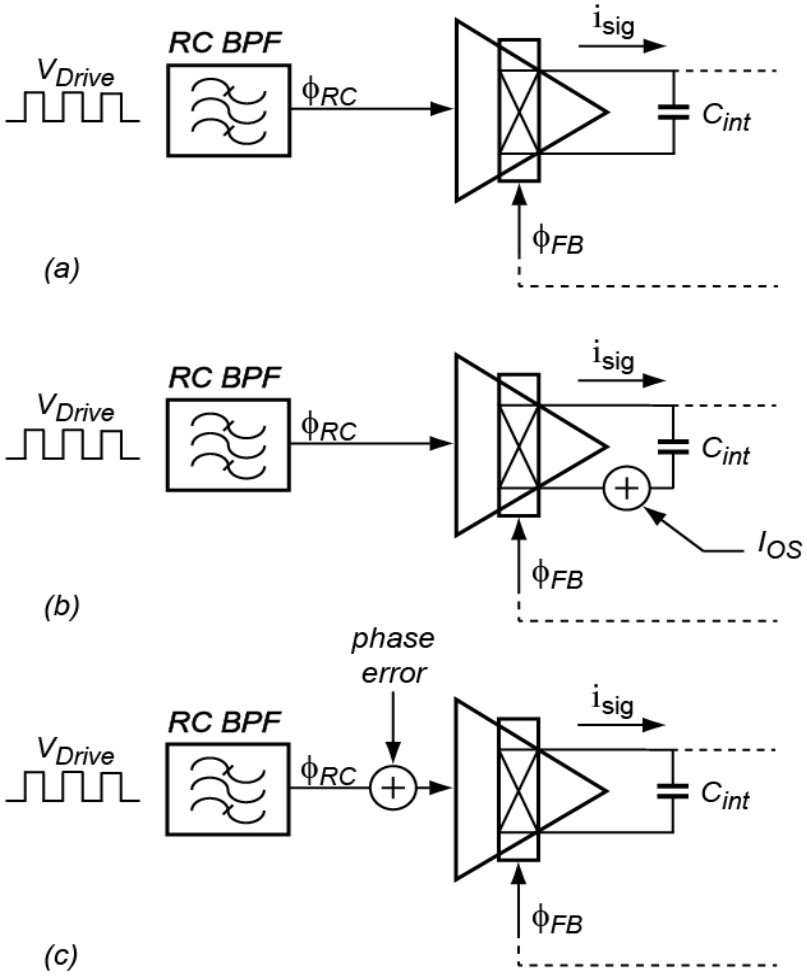

Figure 3.5. *Non-idealities associated with interfacing the WB*

As mentioned in the introduction of the thesis, a multi-point trim could be applied during the calibration process, which consequently removes the low-order temperature dependence of the offset. However, in order to satisfy the targeted inaccuracy, the offset associated with the readout circuitry should be mitigated. The other source of non-ideality is the electrical phase shift added to the WB's output current. The source of this phase shift is the non-zero input impedance of the current-buffer. This impedance is temperature dependent and also changes the desired phase response of the WB. This effect is discussed in detail later.

3.4 PDSDM Circuit Design

As shown in Fig. 3.3, the PDSDM requires an integrator. To minimize its power dissipation, this is implemented as a passive rather than an active integrator. On top of this, the filter outputs a phase shifted current rather than a voltage output. This is because, the filter is driven by a rail-to-rail square-wave (1.8V) and consequently its output amplitude is too large for linear handling by a traditional Gm-C integrator. The passive integrator is implemented by using a current-buffer together with an integrating capacitor C_{int}. Furthermore, the PDSDM requires a bias circuitry, a 1-bit quantizer and a 1bit phase-DAC. The design of these blocks will be described in the following sections.

3.4.1 Current-buffer Implementation

As discussed before, the phase readout accuracy ideally requires the input impedance of the current-buffer to be equal to zero. On top of this, the current-buffer input referred noise has to be roughly the same as the filter's output referred noise. Moreover, the residual offset current produced by the synchronous demodulator should be minimized. As mentioned before, the higher order (more than 2nd-order) temperature dependency of the residual offset is concerned, since a 2nd-order polynomial fitting could be applied. To satisfy the above mentioned requirements, the integrator is implemented as a gain-boosted, passive current-buffer together with an integrating capacitor, and an embedded chopper demodulator. The implementation of this integrator is shown in Fig. 3.6.

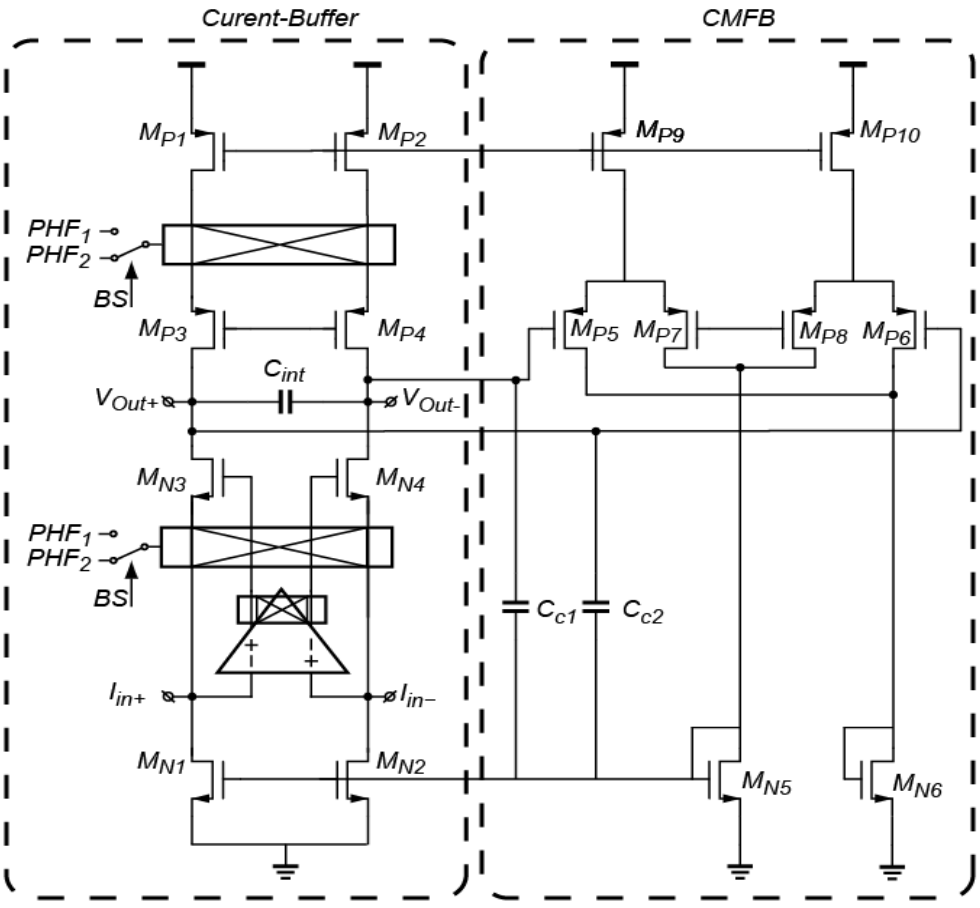

Figure 3.6. *Integrator implemented in the PDSDM*

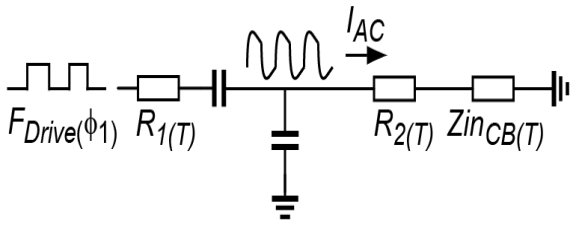

Figure 3.7. *Effect of the WB interfacing the current-buffer*

As shown in Fig. 3.6, the current buffer is formed by cascoded current sources. The current buffer is driven from the N-side folding node. The AC current conveying the phase information passes through the synchronous chopper demodulator which extracts the desired phase information. As shown, the synchronous chopper demodulators are placed on top of the current sources, both at the N-side and P-side folding nodes. The flicker noise and the offset of the current buffer are mostly dominated by the current sources implemented in the current-buffer. As a result, these low frequency sources of error will be up-modulated out of the desired DC signal bandwidth after passing through the synchronous demodulators. Looking at Fig. 3.6, the current buffer is gain-boosted at its input. Gain-boosting at the input reduces the input impedance of the current-buffer by the loop gain provided with the gain-booster which it helps to mitigate the extra inaccuracy added by the readout circuitry in two ways.

First, the phase response of the WB needs to remain unchanged, after being connected to the readout circuitry. This could be done by making the input impedance of the current buffer at least 100x lower than the filter's output impedance. To satisfy the aforementioned requirement, gain booster has to have a gain of more than 40 dB at the filter's driving frequency. Figure 3.7 shows the effect of having a non-zero input impedance of the current-buffer. On top of this, the non-zero input impedance of the current-buffer results in a voltage variation, caused by the rail-to-rail square-wave driving voltage, on top of the current sources (M_{N1}, M_{N2}). Figure 3.8 shows this situation caused by the non-zero input impedance of the current-buffer. Due to the channel-length-modulation, this voltage variation results an extra AC current fluctuations exactly at the same frequency as the driving frequency. Since the current-source's output impedance is a non-linear function of the temperature, it results in an extra temperature inaccuracy which is not favourable. Furthermore, this variation is a function of the filter's driving signal amplitude, which it will dominate the sensor's voltage dependency. Gain-boosting reduces the voltage variations on top of the current sources by the loop-gain provided by the gain booster.

The common-mode feedback (CMFB) of the current-buffer is formed by the two differential pairs made by $M_{P\,5,7}$ and $M_{P\,6,8}$ biased with current sources $M_{P\,9,10}$ together with the diode connected transistors $M_{N\,5,6}$ [7]. The gate of M_{P7} and M_{P8} are connected to the common-mode reference voltage, $V_{CM,ref}$, which sets the common-mode level of the output terminal. The gate terminals of M_{P5} and M_{P6} sense the negative and positive output terminals respectively. The sum of the output currents of M_{P7} and M_{P8} controls the common-mode level through the diode connected transistor M_{N5} and the bottom current sources $M_{N\,1,2}$. The transistors $M_{P\,5\text{-}8}$ make a translinear loop which Eqns. 3.7 and 3.8 express the relation between the gate-source voltages, V_{GS}, of these transistors:

$$V_{GS,P5} - V_{GS,P7} = V_{GS,P6} - V_{GS,P8} \tag{3.7}$$

$$\frac{V_{GS,P5}+V_{GS,P8}}{2} = \frac{V_{GS,P6}+V_{GS,P7}}{2} = V_{CM,ref} \tag{3.8}$$

The capacitors $C_{C1,2}$ each (150fF) provide frequency compensation for the CMFB loop in order to guarantee a minimum of 60° phase margin over the process, voltage and temperature variation.

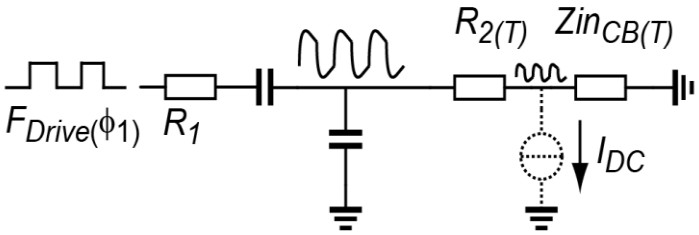

Figure 3.8. *Effect of the WB interfacing the current-buffer*

Another consideration, while designing the current-buffer, is its output impedance. In a sigma-delta modulator based on a passive integrator, the integrator leakage p, is determined by the DC output impedance of the current-buffer R_{out}, the integrating capacitor C_{int}, and the sampling frequency f_S:

$$p = e^{-1/f_s R_{out} C_{int}}. \tag{3.9}$$

The width of the widest dead band Δx in the modulator's DC characteristic normalized to its reference is given by [5, 8]:

$$\Delta x = \frac{1-p}{1+p}. \tag{3.10}$$

The current-buffer's DC output impedance is about 80MΩ, While the C_{int}=40pF, and a 250kHz sampling frequency, this means that the dead bands associated with integrator leakage will be no wider than 400 μdegrees (radian) in terms of φ_{ref}. This translates into a temperature measurement resolution of about 3mK, if the sensitivity associated with the n-well is taken into account.

Simulations show that the current buffer has an input-referred thermal noise floor of $1.35\text{pA}/\sqrt{Hz}$ at the driving frequency (the WB's output referred noise floor is $0.4\text{pA}/\sqrt{Hz}$) and a $1/f$ noise corner of 150kHz. Operating the chopper demodulator at 250kHz ensures that most of the $1/f$ noise is up-modulated out of the desired DC bandwidth. On top of this, the current buffer without the gain booster consumes 14μA, each branch 7μA, in order to make sure that the current buffer could handle the current fed by the WB (which is at most 5μA) over PVT variations. Moreover, the CMFB draws 100nA from a 1.8V voltage supply.

3.4.1.2 Gain booster

Previously discussed, gain- boosting [9] is required in order to reduce the inaccuracy added by the readout circuitry, and also to reduce the sensor's voltage dependency. The input impedance of the current-buffer before gain-boosting can be expressed as:

$$R_{on,chopper} + 1/gm_{cascode}. \tag{3.11}$$

Where the $R_{on,chopper}$ is the on resistance of the chopper's switches, and $gm_{cascode}$ is the transconductance of the cascode transistors $M_{N3,4}$ implemented in the current-buffer. This

input impedance is roughly few tens of kΩ, which is quite comparable with the WB's output resistance of $\frac{2}{3} \times 135\text{k}\Omega$. As shown in Fig. 3.6, a suitable location for the chopper is between the source terminals of the cascode transistors and the input terminals of the booster amplifier. In this way, the gain-booster will establish a virtual ground at the input of the current-buffer while reducing the input impedance of the current-buffer caused by the chopper and the cascode device. Moreover, in this way, the flicker noise associated with the gain-booster will be up-modulated out of the desired DC signal bandwidth. It should be noted that in order to maintain the correct feedback polarity the output of the boosters must then also be chopped.

Previously mentioned, the WB is driven by a 250kHz square-wave. As a result, the gain-booster should provide enough gain at this frequency. In order to keep the input impedance orders of magnitude lower than the filter's output impedance, a gain-booster with the DC gain of about 50dB, and a unity-gain bandwidth (UGBW) of 75MHz should be implemented. Figure 3.9 shows the implemented booster amplifier which is configured in a folded-cascode fashion. As shown, input common-mode regulation is used to set the common-mode level of the booster's input terminal [7]. The input pair $M_{P1,2}$ is provided with two extra transistors ($M_{P3,4}$) in a common-source configuration, whose gates are connected to the input common-mode reference $V_{CM\text{-}in}$. Due to the translinear loop formed by these input transistors, the DC voltage of the gate of the input transistors will be set as well. It should be noted that the nodes constituting the loop formed around the gain-booster (in the current-buffer) are all high impedance floating nodes. As a result, biasing the gate of the booster's input will bias all the other nodes in the loop, which this is done by the feedback loop. The gain booster consumes 5µA, while having a unity-gain bandwidth of 75MHz and a DC gain of 60dB, which represents a gain of about 50dB at the filter's driving frequency of 250kHz.

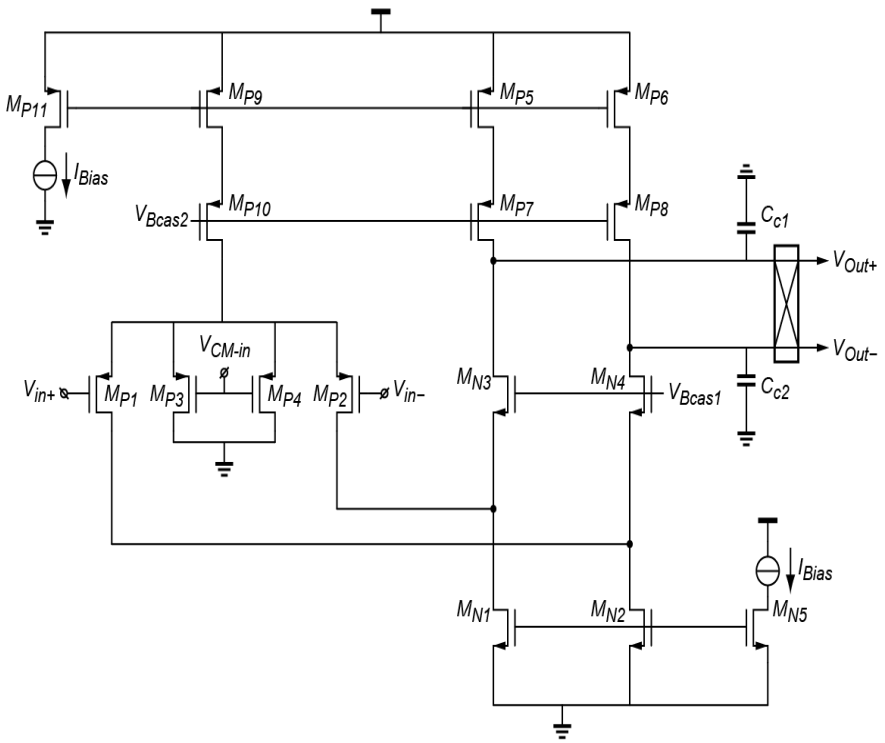

Figure 3.9. *Folded-cascode gain-booster*

3.4.1.3 Compensation

One should note that the gain-boosting loop around the cascode transistors includes chopper switches at the source of the cascodes as well as the output of the booster amplifier (see Fig. 3.5). The switching action taking place in the loop needs that the loop to guarantee the stability during this time [12, 9]. This could be grasped by looking at the simplified half-circuit shown in Fig. 3.10.

As shown in Fig. 3.11 the loop around the gain booster has two poles. The dashed line shows the open loop transfer function before compensation. In order to have a phase margin of 60 degrees (rad), the 2nd pole has to be placed about four times higher than the unity-gain bandwidth (UGBW) of the gain booster. To do so, a compensation capacitor C_{Cb} is added at the output of gain-booster which moves the dominant pole to the lower frequencies. As a result, the UGBW will also move to lower frequencies while the 2nd-pole remains at the same place as before. Figure 3.11 shows the 2nd pole, UGBW the dominant pole before and after compensation. To be concluded, in order to have a phase margin of at least 60 degrees, the stability condition could be summarized as follows:

$$\frac{g_{m2}}{C_{P,in}} > 4\left(\frac{g_{mb}}{C_{Cb}+C_{Pb}}\right). \tag{3.12}$$

Where g_{m2} is the transconductance of the cascode transistor, $C_{P,in}$ is the parasitic capasitance at the input of the current buffer, g_{mb} is the transconductance of the gain booster, and finally C_{Pb} is the parasitic capacitance at the output of the gain booster.

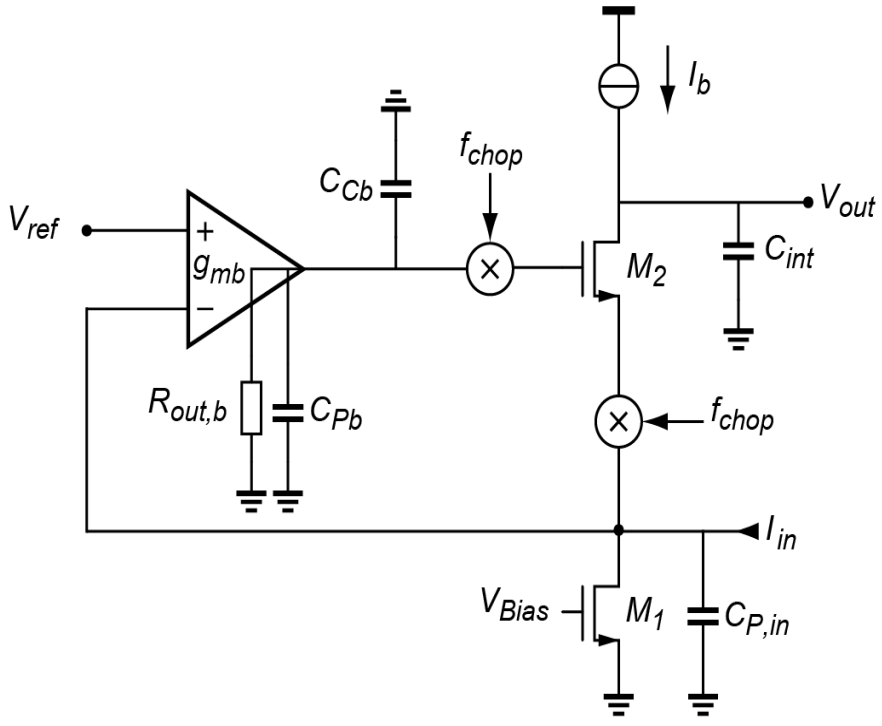

Figure 3.10. *Gain-boosting loop around a cascode transistor including choppers and parasitic capacitances (simplified single-ended half circuit)*

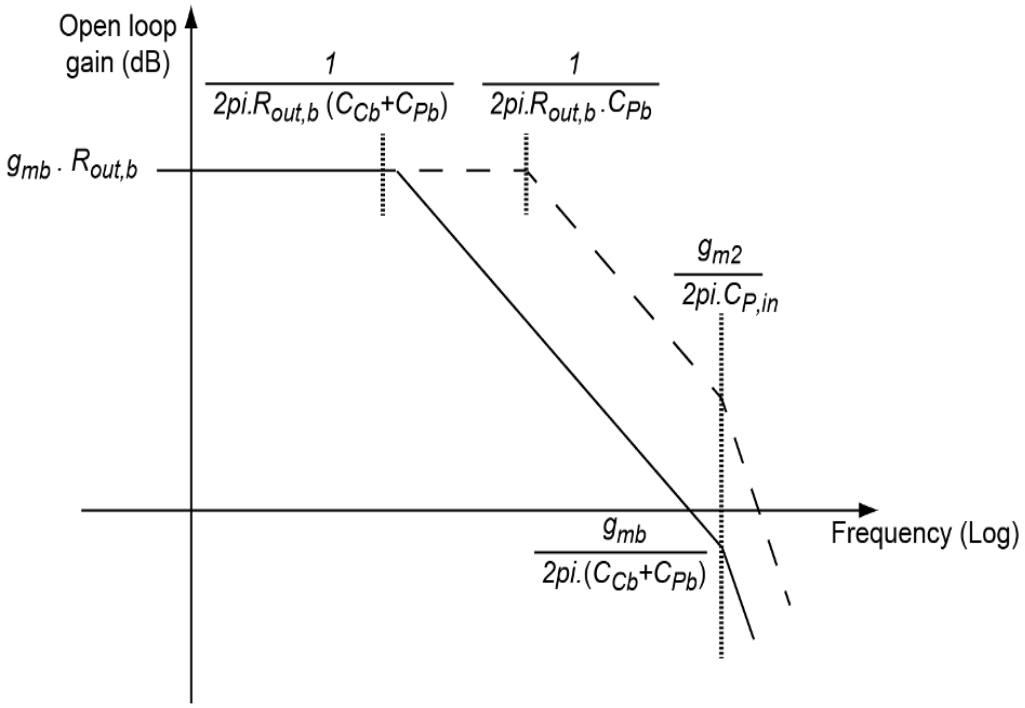

Figure 3.11. *Open-loop gain of the gain boosted cascode circuit in Fig. 3.9*

3.4.1.4 Mixer Implementation & Considerations

Depending on the signal DC level, chopper's switches can be made by using PMOS transistors, NMOS transistors or the combination of them as T-gate switches. The chopper demodulator implemented by NMOS switches is shown in Fig. 3.12. The whole idea behind the chopping is to extract the phase information, and on top of this, to up-modulate the flicker noise (and also the offset) out of the desired DC signal bandwidth. To do so, the chopper itself shouldn't contribute to any flicker noise, which requires the switches implemented in the chopper to operate deeply in the linear region. It should be noted that the charge injection and clock feed through associated with the switches in the chopper will result in some additional inaccuracy. However, due to the available multi-point trimming, this source of inaccuracy which mostly behaves like an offset will be trimmed out.

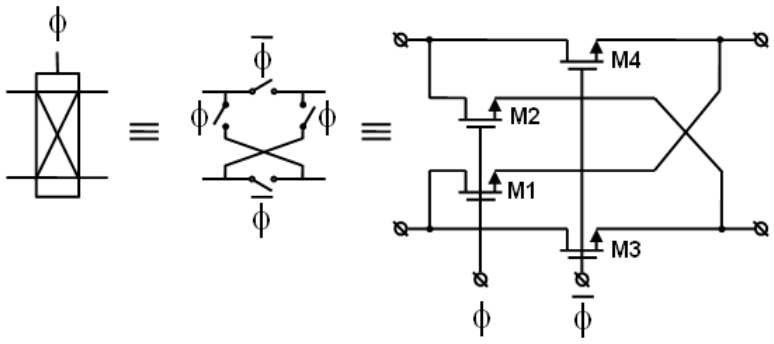

Figure 3.12. *Chopper implementation in CMOS using NMOS transistors*

3.4.1.5 Readout Noise

As shown in Fig. 3.13, the utilized chopping technique will up-modulate the flicker noise out of DC signal bandwidth. However, the noise PSD at DC and after chopping is the same as the noise PSD at the chopping frequency and before chopping. At the frequency of 250 kHz, all the noise sources have a thermally noise behaviour and the input referred current noise associated with the current-buffer can then be expressed as follows:

$$I_{N,in} \approx \sqrt{4kT\lambda\left(g_{m,M1} + g_{m,M4} + \frac{1}{g_{mb}\times {R_2}^2}\right)}\ {A}/{\sqrt{Hz}}. \tag{3.13}$$

Where λ is 2/3 for a strong-inversion region and 1/2 for a weak-inversion region, $g_{m,M1}$ is the transconductance of the N-side current source, and $g_{m,M4}$ is the transconductance of the P-side current source, and g_{mb} is the transconductance of the gain-booster's input device. It can be seen that for the noise of the gain-booster, only the noise associated with the input transistor is considered. It should be noticed that the gain-booster's input referred noise is in voltage domain. As a result, it will be translated into the input referred current noise of the current-buffer as it flows through the impedance seen at the input of the current-buffer.

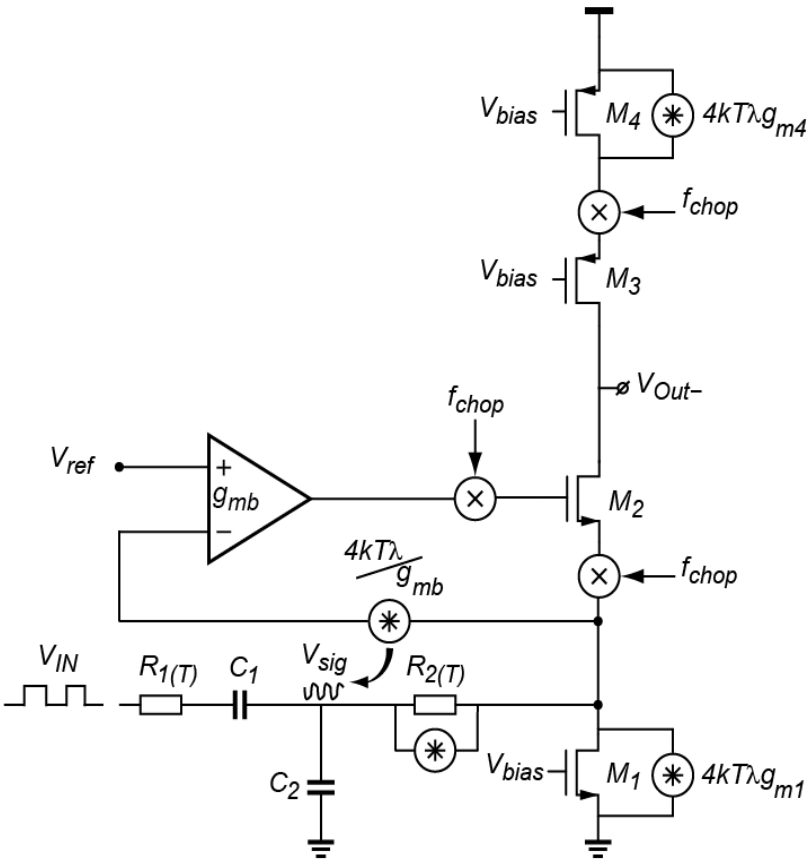

Figure 3.13. *Noise analysis of the implemented current-buffer (simplified half-circuit)*

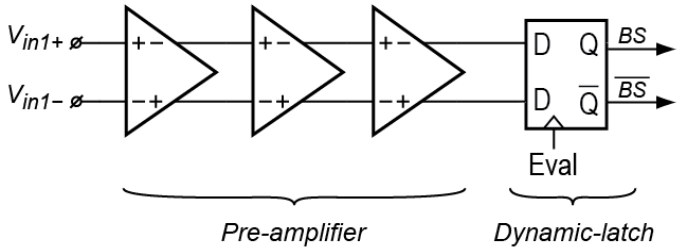

Figure 3.14. *Comparator system level implementation*

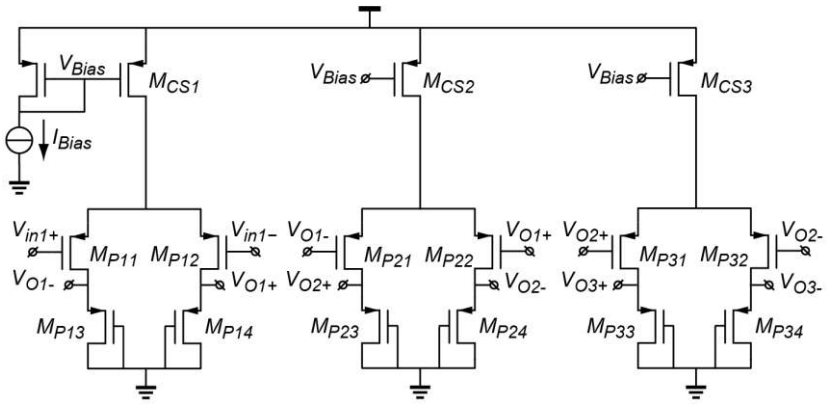

Figure 3.15. *Pre-amplifier implementation*

3.4.2 Comparator

The implemented comparator consists of three pre-amp stages followed by a dynamic latch [10]. The top-level implementation of the comparator is shown in Fig. 3.14. The pre-amps are added in order to mitigate the effect of the kick-back noise associated with the latch. The pre-amps are implemented by a simple differential amplifier which is shown in Fig. 3.15. Each differential pair consumes 50nA while providing a unity-gain bandwidth of about 1MHz and a DC gain of three. As shown in Fig. 3.15, a PMOS input pair has been used for the pre-amplifier. On top of this, a PMOS diode-connected load is implemented in the pre-amplifier. The gain associate with each pre-amplifier could be expressed as:

$$A_V = \frac{g_{m,MP11}}{g_{m,MP13}}. \tag{3.14}$$

The dynamic latch used in the comparator is shown in Fig. 3.16. Transistors M_{N1} and M_{N2} sense the pre-amp's output. By the time that the rising edge of the evaluation signal arises, this sensed signal will be passed to the latch to be held till the next cycle. Transistors M_{N5} and M_{N6} act as a switch between the input transistors and the output latch.

3.4.3 Phase Generator Block

As mentioned, the phase associated with the implemented band-pass-filters changes at most about 20 degrees over the military temperature range. While considering the chip-to-chip spread and overloading effect in the PDSDM, full-scale of the sigma-delta is designed to be 45 degrees (radian).

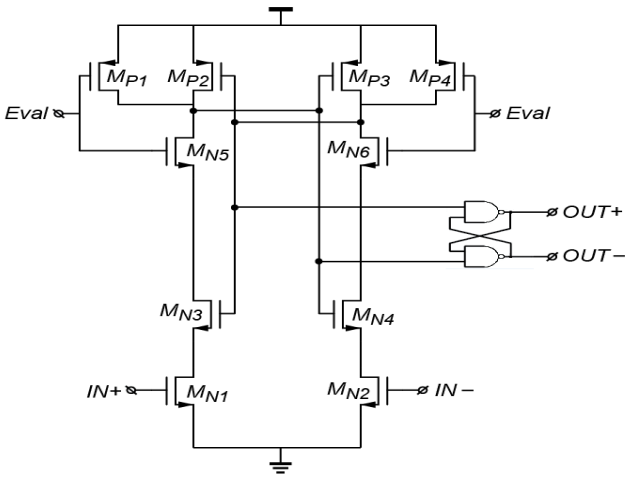

Figure 3.16. *Dynamic-latch transistor-level implementation*

On top of this, the WB driving signal should have a 90° phase-shift relatively to the phase reference signals. Consequently, the phase-reference signals have 90°+22.5° and 90° −22.5° degrees phase shift, respectively. The required phase-shift is generated by using toggle flip-flop (T-FF) which divides the MEMS frequency in order to get the desired frequency and phase-shift steps. The implemented T-FF is shown in Fig. 3.17. In order to have a frequency of 250 kHz with a phase steps of ±22.5°, a MEMS frequency of minimum 2MHz is required. The phase generator implementation is shown in Fig. 3.18 which provides with the filter's driving frequency and reference-phase signals. The F_{ref1} has 75° and Fr_{ef2} has 112.5° phase shift relatively to the filter's driving frequency.

3.4.4 Phase DAC

The implemented phase-DAC in the sigma-delta loop consists of two T-gate switches. The bit-stream will select one of the phase-reference reference signals which it will be then fed into the sigma-delta's summation node. The implementation of the phase-DAC is shown in Fig. 3.19.

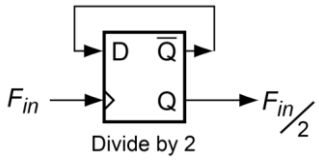

Figure 3.17. *Toggle flip-flop used for the frequency division by 2*

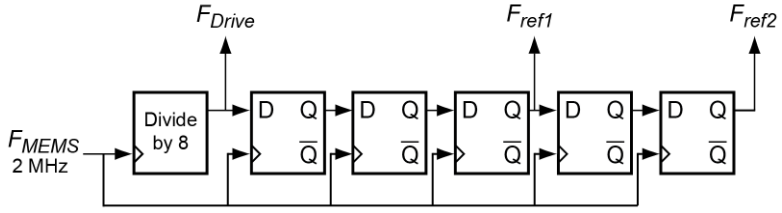

Figure 3.18. *Phase generator system level implementation*

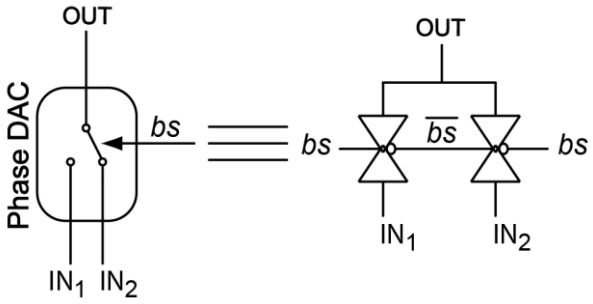

Figure 3.19. *Phase DAC implementation using T-gate switches*

3.4.5 Jitter and synchronization

Previously discussed, a sub-mK resolution is desired in this application, which it could be translated into a cycle-to-cycle jitter performance in order of few Pico seconds in time domain. Commercially available MEMS frequency references provide with a jitter performance in the same level as mentioned before. As noted before, the phase reference signals are generated by dividing a high frequency into a lower one and add a time-delay to each of them as required. However, the frequency division increases the jitter performance exponentially [11]. As a result, the phase reference signals becomes highly jittery which limits the achievable resolution. In order to tackle the this problem, a D-flip-flop synchronizes all the phase-domain signals with the frequency provided with the MEMS resonator's frequency [11]. In this way, the jitter performance of the phase reference signals will be limited by the MEMS frequency reference jitter performance which is good enough for the targeted resolution. The placement of the synchronization flip-flops and the synchronizer frequency is shown in Fig. 3.20.

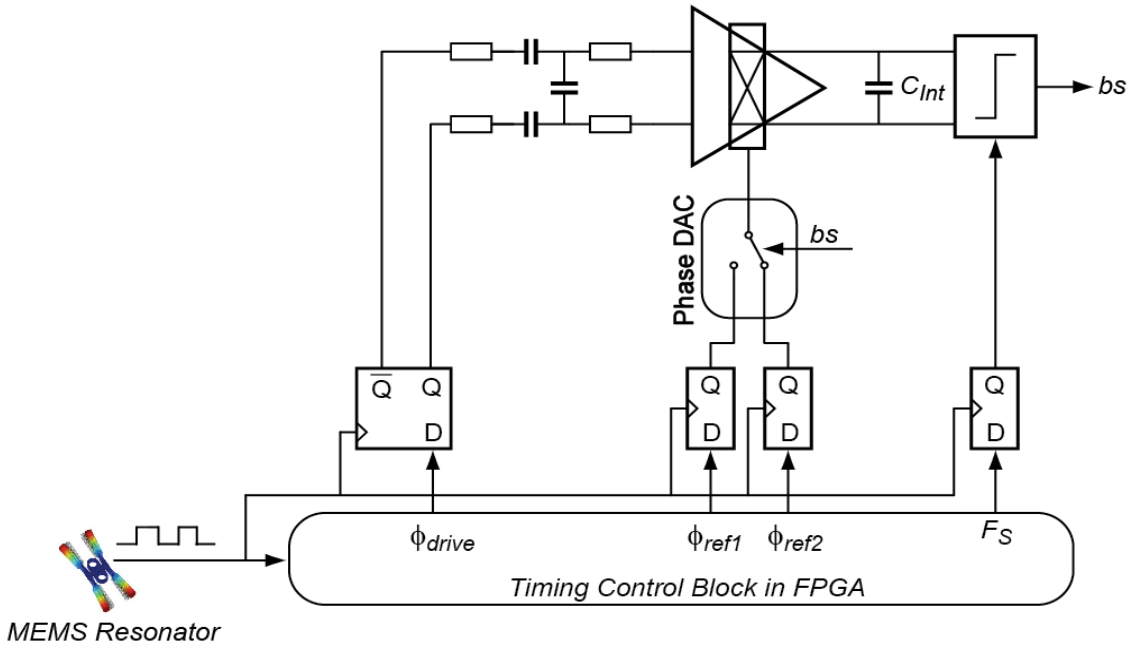

Figure 3.20. *Synchronization used for lowering the jitter in the proposed temperature sensing approach*

3.4.6 Constant-Gm Bias Circuit

The transconductance of MOSFETs plays a crucial role in analog circuits, i.e. the change of gain-booster's transconductance over the temperature could result in instability in the loop around the gain-booster. On top of this, the first test chip different resistor types are implemented in the WB each of which has different temperature dependency. As a result, in order to make sure that the current-buffer is able to handle the AC current fed by the WB over temperature a constant-Gm bias circuit should be used. The constant-Gm bias circuit is shown in Fig. 3.21. Using the constant-Gm bias circuit provides an output current which could be defined as [12]:

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)} \times \frac{1}{{R_S}^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2. \tag{3.15}$$

Thus, the transconductance of M_{P1} equals:

$$g_{m1} = \sqrt{2\mu_n C_{ox}(\frac{W}{L}) I_{D1}} = \frac{2}{R_S}(1 - \frac{1}{\sqrt{K}}), \tag{3.16}$$

a value which is independent of the supply voltage and MOS device parameters. However, the resistor implemented in the bias circuit is temperature dependent which this could be mitigated by combining resistors with different temperature coefficient to get a temperature independent current. Furthermore, it should be noted that still the resistor's spread could result in different biasing current from chip to chip. It should be noted that while assuming a 25% spread for the resistor (maximum spread from lot-to-lot reported by the fabrication) the whole circuit should operate as expected.

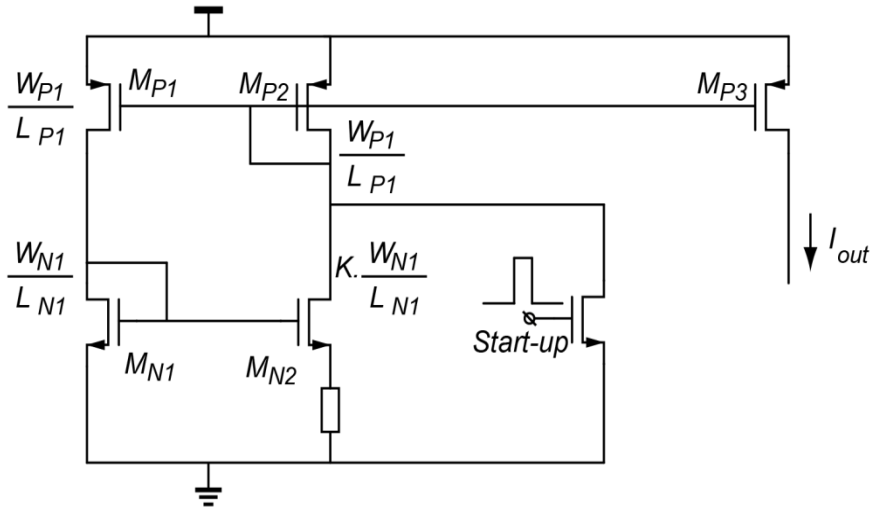

Figure 3.21. *Constant-Gm bias circuit implementation*

3.5 Expected Performance

So far, the circuit implementation is discussed. However, it is beneficial to investigate the performance of this design. This design consumes 36 µW from a 1.8 V supply. In order to extract the ultimate resolution achievable, while using the implemented first order PDSDM, dominant noise sources should be considered. The main noise sources are the readout thermal noise, the quantization noise. The effect of these noise sources will be investigated below, respectively.

3.5.1 Readout noise

As previously discussed, the noise associated with the readout circuitry could be extracted by using Eqn. 3.14. While in this design, the current sources have a g_m equal to 70 µS, and the transconductance of the gain-booster is equal to 100 µS, and the implemented resistor in the WB is 135 kΩ, the total noise could be calculated as:

$$\sigma_{curent,noise} \approx \sqrt{4kT \times \frac{2}{3}\left(70\ \mu S + 70\ \mu S + \frac{1}{100\ \mu S \times \left(\frac{135\ k\Omega}{4}\right)^2}\right)}\ {}^{A}/_{\sqrt{Hz}}. \quad (3.17)$$

where the total integrated noise in a 5Hz bandwidth could be calculated as follows:

$$\sigma_{curent,noise} \approx 3.1\ pA\ (\text{RMS}). \quad (3.18)$$

which is about 3.5x more than the noise associated with the WB in the same bandwidth. This noise represents a temperature-sensing resolution of 630 µK, while taking the sensitivity associated with the n-well resistor into account (see Chapter 2).

3.5.2 Quantization Noise

Another noise source is the quantization noise of the implemented PDSDM. As discussed the passive integrator results in a leaky behaviour. Consequently, the integrated charge will leak away in an exponential manner as shown in Eqn. 3.10. Matlab simulation (see Fig. 3. 22) shows that the normalized quantization noise PSD saturates at low frequencies due to the finite output resistance of the passive integrator (80MΩ), while C_{int}=40pF and the sampling frequency is equal to 250kHz. As can be seen the noise PSD at DC is about -110dB. While assuming a full scale of $\pm V_{REF}$ equal to 22.5° (radian), the noise representation in the phase domain and for a 5Hz bandwidth is as follows:

$$\sigma_{phase,noise} = \sqrt{45^2 \times 10^{-11} \times 5} \approx 400\ \mu\text{degrees(rad)rms}. \quad (3.19)$$

this noise represents a temperature-sensing resolution of 3 mK, while taking the sensitivity associated with the n-well resistor into account (see Chapter 2).

3.5.3 Total Noise

In order to calculate the total noise associated with the first test chip, the dominant noise sources should be taken into account. As calculated above, the quantization noise together

with the noise of the readout circuitry and sensor itself will determine the total noise. Consequently, the noise in thermal domain could be calculated as:

$$\sigma_{temp,noise} = \sqrt{(3\ \text{mK})^2 + (630\ \mu\text{K})^2 + (174\ \mu\text{K})^2} \approx 3\ \text{mK}. \quad (3.20)$$

This calculated value represents the temperature-sensing resolution while WB incorporates an n-well under STI resistor.

3.6 Measurement Results

As described in previous sections, besides the PDSDM, the first test chip included four WBs each of which incorporates n-poly, n-well, N^+ diffusion or P^+ diffusion. This chip is realized in a standard 0.18µm CMOS technology and has an area of 0.35mm^2 (see Fig. 3.23) and is packaged in a ceramic DIL package, and it consumes 36µW from a 1.8V supply. The required timing signals were generated in an FPGA and derived from a 8MHz Crystal oscillator. The sampling rate of the PDSDM was 250kHz and the output of the modulator was decimated with an off-chip sinc^2 decimation filter which limits the system bandwidth to about 5Hz after 100msec conversion time (50K sigma-delta cycles). The more complex sinc^2 filter was chosen over a sinc filter, because the former actually brings a bit more resolution. This is because the modulator's resolution in mainly limited by the quantization noise in a conversion time of 100msec. Figure 3.24 shows the output spectrum of the phase domain sigma-delta modulator at room temperature and before the decimation. The spurious noise shaping is due to the nature of the first order sigma-delta and also the leaky behaviour associated with the passive integrator. The variance of the measured noise in the decimated bit-stream was 0.5m degrees (rad) which is better than 16 bits. This noise corresponds to a temperature-sensing resolution of about 3mK, when the sensitivity of the n-well resistor is taken into account. Figure 3.25 shows the measured temperature sensitivity of the implemented WBs in terms of phase and over the military temperature range.

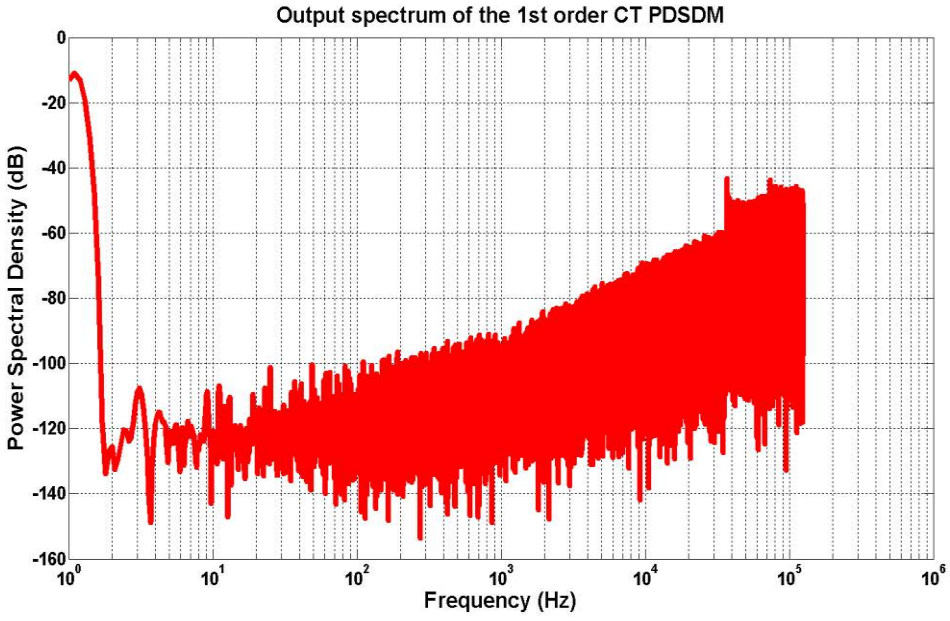

Figure 3.22. *Matlab simulation for the leakage effect in a 1st order PDSDM*

3.6.2 Resolution vs. Conversion Time

Figure 3.26 shows the obtained resolution as a function of the conversion time. The red curve shows the resolution extracted from one chip, while the blue curve shows the resolution associated with the difference of two chips running simultaneously. As can be seen the difference of the output of two chips provide with more resolution. This is due to the fact that the thermal noise associated with the environment acts as a common-mode, thus its effect will be cancelled out by the common-mode rejection property of the two chips. The environmental thermal noise could be mitigated further by placing two temperature sensors on each chip. It can be seen that the slope of the TDC's resolution-vs.-conversion time changes at 50msec conversion-time. This is due to the leakage associated with integrator which limits the quantization noise floor at about -110dB normalized to the full-scale of the modulator which is 45 degrees (rad).

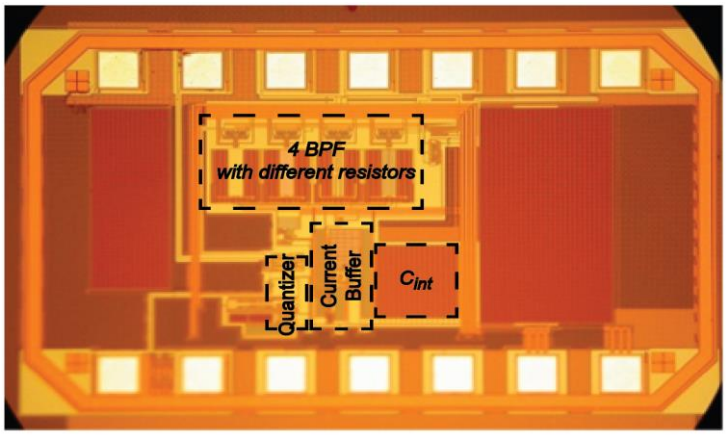

Figure 3.23. *Micrograph of the first test chip including 4 WBs and the PDSDM*

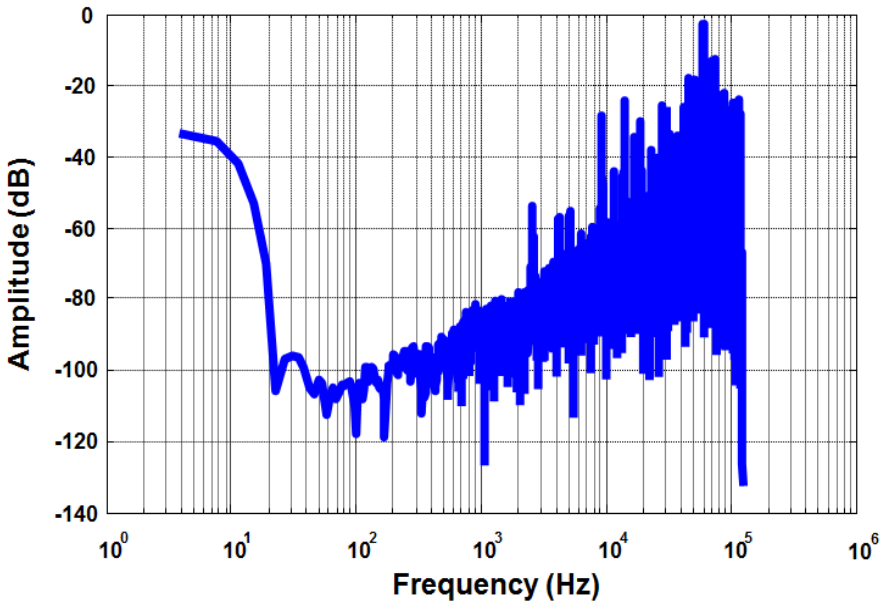

Figure 3.24. *Measured output spectrum of the temperature sensor at room temperature (65536-point FFT, Hanning window)*

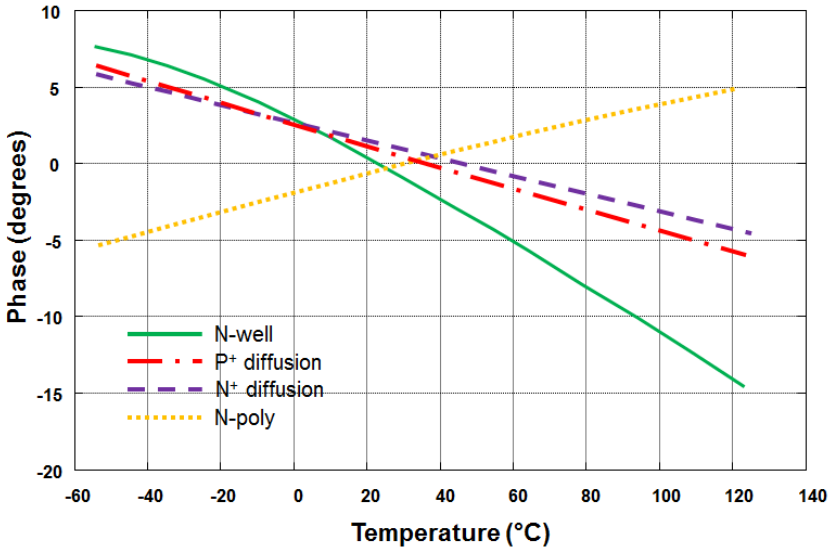

Figure 3.25. *Measured phase characteristics of temperature sensor incorporating different types of resistors*

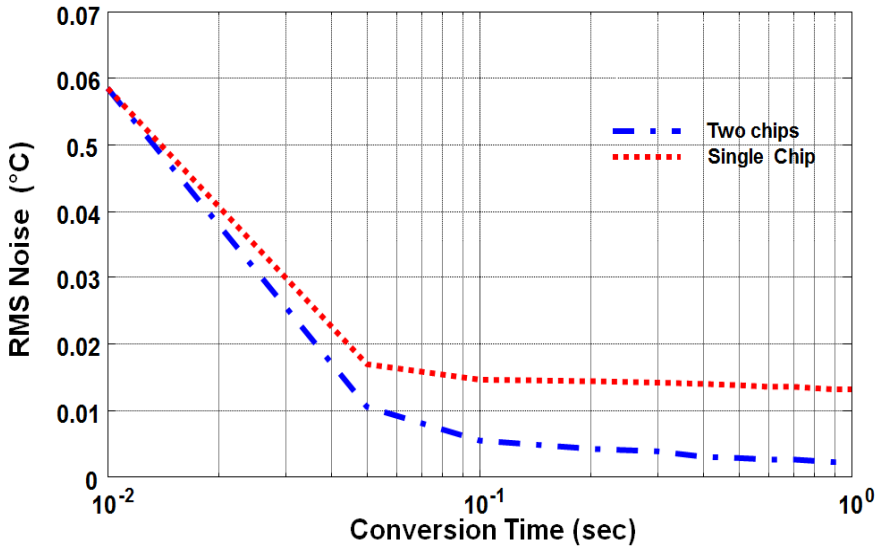

Figure 3.26. *Resolution vs. conversion time extracted from one and the difference of two chips*

3.6.3 Temperature Inaccuracy Associated with Resistor

In order to measure the inaccuracy of the devices, they were mounted in a good thermal contact with a large Aluminium block, and their temperature was then measured by a PT-100 temperature sensor. The 4 different WBs could be characterized by selecting them by means of an on-chip multiplexer. The averages of the measured phase-versus-temperature characteristics of 16 devices are shown in Fig. 3.25 each of which represents one type of resistors. These characteristics were obtained by converting the decimated value into its phase representation by using Eqn. 3.6 and then performing a high order polynomial fit on the measured data, i.e. the output of the PT-100 sensor and the decimated output of the chips.

Due to the different temperature sensitivity of the resistors, each type of resistor shows different phase-to-temperature sensitivity, which is at most 20 degrees (rad) over the military temperature range while for the other resistor types is about 10 degrees (rad) for the same temperature range. The average characteristics were then used to translate the decimated output of each chip into an absolute temperature value. Fig. 3.27 shows the 3-sigma temperature deviation from the average characteristic extracted from 16 measured devices and for different resistor types.

To measure the sensor's inaccuracy, 16 chips from one batch were characterized over the military temperature range. The phase-shift generated by different filters are shown in Fig. 3.25. In case of n-poly resistor, after a 2nd order polynomial fit (using three data points) the resulting 3σ inaccuracy was about ±0.1°C and over the industrial temperature range, but was dominated by a much larger systematic error. However, this error can be removed by a *fixed* 3rd-order polynomial (see Fig. 3.28). A similar approach was used to process the characteristics of the other filters and the results are summarized in Table 3.1. The N-poly resistor is the most accurate, while the N-well filter has about 2x more resolution, but at the expense of significantly more non-linearity, which required a fixed 4th order polynomial. Table 3.2 summarizes the performance of the N-poly filter and compares it with that of other resistor-based sensors.

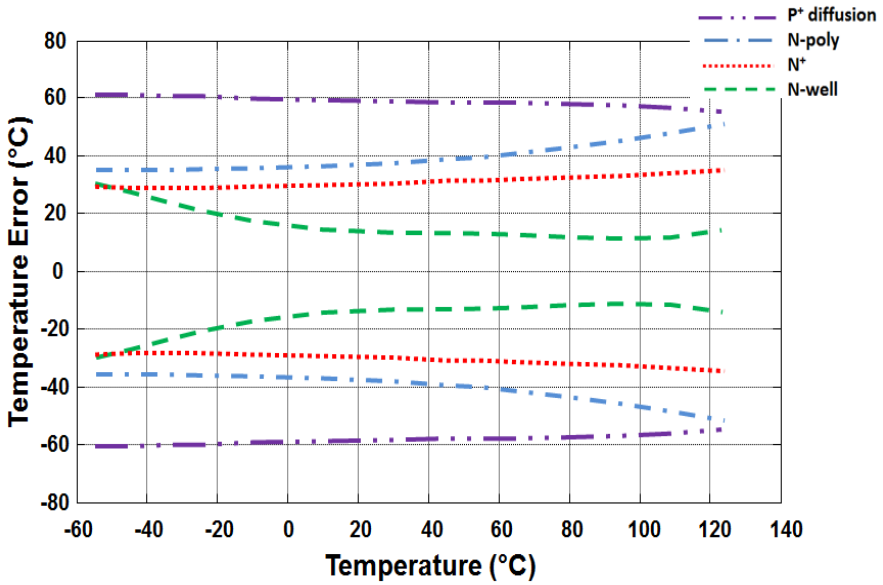

Figure 3.27. *Measured temperature-error of temperature sensor incorporating different type of resistors*

Table 3.1. *Performance of the different resistor types.*

Resistor Type	Temperature coefficient	Inaccuracy (after 2nd-order fit)	Order of correction polynomial	Total phase Shift
N+ diffusion	0.15%	±0.15°C	2	8 degrees
P+ diffusion	0.15%	±0.2°C	3	7.8 degrees
N-poly	-0.15%	±0.1°C	3	7.5 degrees
N-Well	0.3%	±0.2°C	4	15 degrees

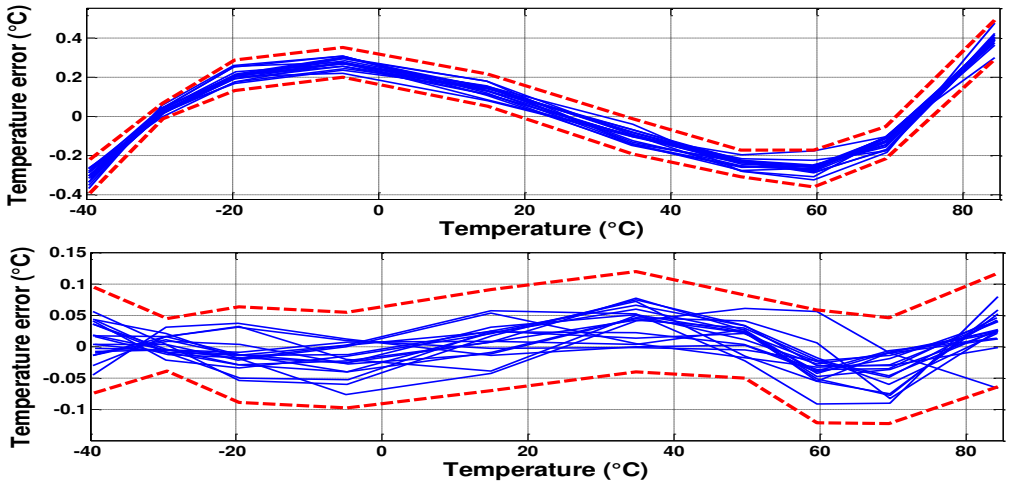

Figure 3.28. *Measured phase characteristics of temperature sensor incorporating N-poly resistor, top: 2nd-order fitting, bottom: after systematic error removal*

Table 3.2. *Chip performance and Comparison with prior-arts*

Parameter	This Work [4]	[14]	[13]
Technology	0.18µm	0.18µm	0.18µm
Chip area	0.35mm2	0.044 mm2	0.18 mm2
Power consumption	36µW	30 µW	13mW
Temperature range	-40°C - 85°C	0°C - 100°C	-40°C - 85°C
Inaccuracy (trim points)	±0.1°C † (3)	±0.33°C †† (3)	±0.015†† (6)
Resolution (Tconv)	0.006K (100msec)	0.04K (7.5msec)	100µK (100msec)
FOM(nJK2)	0.13	0.36	0.013

†: 3σ, † †:Min/Max

3.7 Conclusion

The temperature-dependent phase shift of a band-pass RC filter, incorporating n-poly resistors, is digitized by a phase-domain sigma delta modulator. It achieves 6mK resolution in a 100ms conversion time. After a 2nd order polynomial fit, and the removal of systematic non-linearity, the proposed sensor achieves ±0.1°C inaccuracy over the industrial temperature range: -40°C to 85°C. Moreover, the inaccuracy resulted from each type of resistors has been elaborated in the measurement result section. The noise performance of this design is mainly dominated by the quantization noise associated with the readout circuitry, which is about 10x more than the sensor's noise. In order to make an energy-efficient design, quantization noise should be suppressed to be lower than the thermal noise. However, more energy-efficiency could be obtained by improving the thermal noise while possibly lowering the power consumption. In next chapter, the weaknesses of this design will be first discussed. The second test chip, discussed in Chapter 4, will present a 2nd-order PDSDM based on the "*Hybrid sigma-delta*" approach.

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4 2^{nd} Test Chip

4.1 Introduction

As mentioned before, the first test chip was devoted to extract the inaccuracy associated with each type of resistors. Measurement result of the previous design showed that by using n-poly resistor the targeted inaccuracy of less than 0.1°C over the industrial temperature and after a 2^{nd} order fitting is achievable [1]. However, another possible candidate which is n-well under OD with higher sensitivity and a more linear temperature dependency (than the n-well under STI) will be implemented in the 2^{nd} test chip. The goal of the 2^{nd} test chip is to surpass the energy-efficiency of prior-art designs by at least 5x ($<2pJK^2$) [2]. To do so, the weaknesses associated with the first test chip should be tackled as far as energy-efficiency is concerned.

In order to achieve a better energy-efficiency, the noise performance of the temperature-to-digital converter (TDC) should be improved, while possibly lowering its power consumption and conversion time. As discussed in the previous chapter, the dominant noise source of the previous design was the quantization noise caused by the leaky behaviour of the passive integrator. Moreover, on the 2^{nd} place, the input referred noise of the readout circuitry was dominated by the thermal noise of the current-buffer, which is 3.5x more than the noise of the Wien-bridge (WB). While possibly lowering the thermal noise of the current-buffer, in order to push the quantization noise to be much lower than the thermal noise floor, a 2^{nd}-order phase-domain sigma-delta modulator is chosen which is also in line with the targeted conversion time of less than 100 msec.

In this chapter, first, the weaknesses of the first design will be elaborated in detail. Then, the modified first stage will be presented. In the following, the system-level implementation of the proposed energy-efficient "*2^{nd}-order Hybrid Sigma-Delta*" will be discussed. To be followed, the circuit implementation and considerations together with the simulation results

will be discussed. At the end, the expected performance and comparison with the state-of-the-art temperature sensors will be shown.

4.2 PDSDM requirements

In order to extract the ultimate resolution associated with the Wien-bridge filter, the PDSDM should achieve a SQNR of 120 dB in a 100msec conversion time. This can be translated into roughly 20-bit resolution.

Generally, in sigma-delta modulators, there are two noise sources: quantization noise, and thermal noise, which both are mitigated by increased conversion time. In the quantization-noise limited regime, resolution improves according to $\frac{1}{(T_{Conv})^L}$, where L is the order of the modulator. This argument is valid provided that the sampling frequency remains the same. After a sufficiently large number of cycles, the modulator enters the thermal noise limited regime and its resolution improves according to $1/\sqrt{T_{Conv}}$, since the ADC's bandwidth is inversely proportional to its conversion time. The resolution of 1st, 2nd and 3rd-order modulators as a function of conversion time is shown schematically in Fig 4.1. Energy-efficient design requires that the modulator's noise to be dominated by thermal noise rather than quantization noise, since reducing the former requires more power consumption than reducing the latter [8].

The sigma-delta order together with the sampling frequency defines the lowest conversion time at which the modulator becomes thermal noise limited [3]. In order to realize the most energy-efficient sigma-delta ADC, we should make sure that over the 100msec conversion time, the ADC is thermal noise limited at the minimum ADC's order and the oversampling ratio.

As previously discussed, the noise performance of the 2nd design is going to be improved by a factor of 20. Moreover, the dominant noise source in the previous design was the quantization noise of the TDC. As discussed in the introduction, a 2nd-order sigma-delta modulator could suppress the quantization noise to be lower than the thermal noise floor of the WB. The required number of cycles for a given resolution n_{bit} could be found as follows [4]:

$$\binom{N + L_a - 1}{L_a} = \frac{2^{n_{bit}}}{(l-1)u_{max}} \tag{4.1}$$

Where N is the number of cycles, u_{max} is the maximum normalized input signal, L_a is the order of the analog modulator, and l defines the level of the internal quantizer. As an example, for 20-bit resolution, with a second order architecture, assuming l=2 and $u_{max} = 0.7$, N=1730 is required. Therefore, assuming a sampling frequency of 250kHz, a conversion time of 7msec is desired in order to enter the thermal noise limited regime.

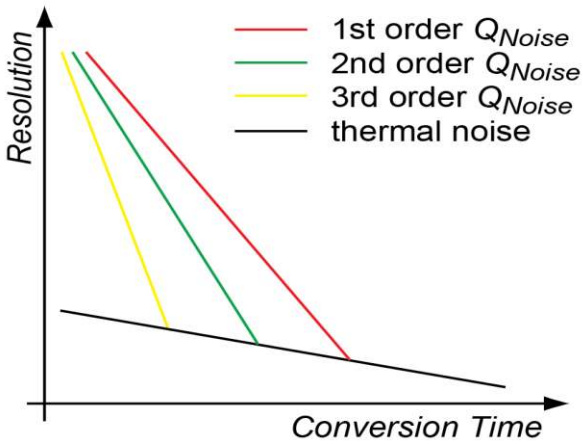

Figure 4.1. *Resolution vs. conversion time for different orders of sigma-delta modulators*

4.3 First design weaknesses

This section discusses some of the already mentioned weaknesses of the first design together with some other considerations such as voltage dependency, supply noise and moreover the power reduction techniques. Figure 4.2 shows the implemented current-buffer in the previous design.

4.3.1 Thermal Noise

While assuming that the quantization noise could be suppressed to be lower than the thermal noise, the 2nd dominant noise source is the thermal noise associated with the current-buffer. This noise source was about 3.5x more than the implemented WB and it was mainly dominated by the current sources implemented in the current buffer together with the noise of the gain-booster. The noise contribution of current sources was about 80% of the total input referred noise of the current buffer, while the rest was mainly dominated by the gain-booster. Referring to the Eqn. 3.13, the noise of the current buffer in a simplified single-ended configuration could be calculated as follows (also see Fig. 3.13):

$$\sigma_{I_n,in} \approx \sqrt{4kT\lambda\left(g_{m,M1} + g_{m,M4} + \frac{1}{g_{mb}\times {R_{WB}}^2}\right)}\ {A}/{\sqrt{Hz}}, \tag{4.2}$$

where $g_{m,M1}$ & $g_{m,M4}$ are the transconductance of the current sources, g_{mb} is the transconductance of the gain-booster, and R_{WB} is the resistor implemented in the WB filter. The noise of the current-source could be reduced by lowering its transconductance. However, lowering the transconductance requires more overdrive voltage and/or lower current flowing through the current source. Equation 4.3 shows the transconductance of the current source as a function of the previously discussed parameters.

$$g_m = \frac{2I_D}{V_{GS}-V_{TH}}, \tag{4.3}$$

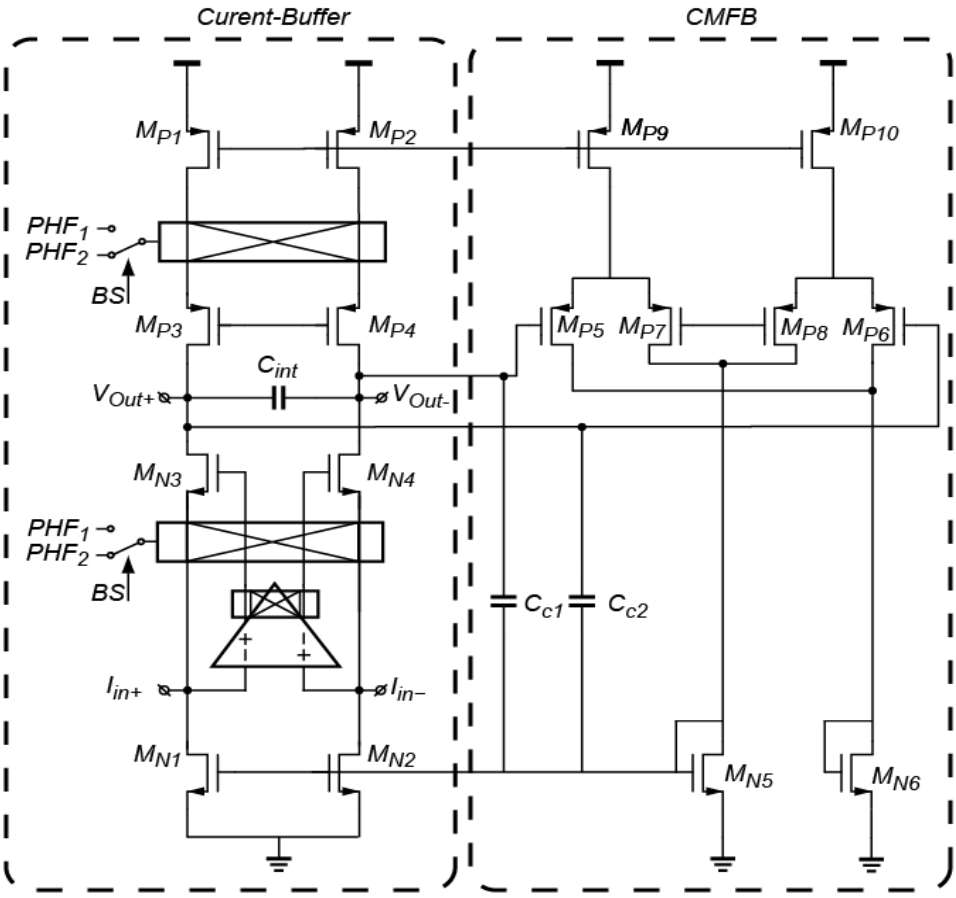

Figure 4.2. *Current-buffer implemented in previous design*

where I_D is the bias current, and $V_{GS} - V_{TH}$ represents the overdrive voltage of the current-source. It should be mentioned that in order to make the noise of the readout circuitry to be the same as the WB's noise, a transconductance equal to $\frac{1}{R_{WB}}$ is required, where R_{WB} is the value of resistor implemented in the WB equal to 135kΩ. Under the previous design's biasing condition, an overdrive voltage of 900mV (while V_{DD}=1.8 V) was required in order to get the desired transconductance.

4.3.1.2 Source Degeneration

In order to reduce the noise of the current sources, source-degeneration technique could be utilized. Figure 4.3 shows a source-degenerated current source. Adding the degeneration resistor results a series-series feedback loop around the current source. The loop gain provided with this feedback loop then could be expressed as follows [3]:

$$\text{Loop} - \text{gain} = g_m R_S. \tag{4.4}$$

As a result of the feedback loop, the noise of the current source including the flicker noise and thermal noise, will be reduced by the gain of $1 + g_m R_S$. However, the noise of the degeneration resistor will be buffered by the gain of the common-gate (CG) configuration which is equal to:

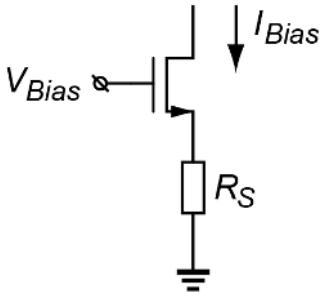

Figure 4.3. *Source-degenerated current-source*

$$A_{C,CG} = \frac{g_m R_S}{1+g_m R_S}. \tag{4.5}$$

Consequently, the current noise of the degenerated current-source could be expressed as follows:

$$S_{I_n} = 4\text{kT} \times \left[\frac{g_m}{(1+g_m R_S)^2} + \frac{1}{R}\left(\frac{g_m R_S}{1+g_m R_S}\right)^2\right]. \tag{4.6}$$

Source-degenerated current source requires less headroom to provide with a certain noise performance, than the normal current source. On top of this, source-degeneration also increases the output impedance by the loop-gain, which results in less leaky behaviour of the passive integrator.

4.3.2 Power Reduction

Better energy-efficiency can be achieved by lowering the power consumption, while improving the noise performance. As a result, possible power reduction techniques and modifications will be discussed. The bias current in the current-buffer branches are set such a way that to handle the AC current fed by the WB. This current was at most 6µA (peak-to-peak), for the n-well resistor caused by its high sensitivity. In order to keep the maximum AC current for all types of the resistors to be the same, the n-well resistor is scaled up by a factor of 2. Consequently, all WBs provide with an AC current of about 3µA (peak-to-peak) which then the current required for the current-buffer could be also reduced by a factor of 2. Another power reduction point is the implemented gain-booster. In previous design a fully-differential folded-cascode was implemented which took 5µA from the supply. However, in this design a fully-differential telescopic opamp is used which inherently requires less power in order to have the same DC gain and UGBW. The implemented gain-booster will be discussed in more detail in the coming sections.

4.3.3 Voltage Dependency

Discussed in Chapter 2, parasitic capacitance associated with the reverse-biased diodes to the substrate is voltage dependent. The reverse-biased diodes are shown in Fig. 4.4 for an n-well resistor. In order to deeply reverse bias these diodes and for an N-type resistor, a DC bias voltage close to the supply voltage is required. It should be noticed that this DC bias voltage could be set by the input common-mode level of the current buffer. Consequently, the

input of the current buffer should be placed at the P-side in order to satisfy the required high DC bias voltage.

4.3.4 Supply Noise

Amplitude noise of the filter's driving signal, results in a noisy output while employing a PDSDM. Figure 4.5 exaggerates the effect of this noise after mixing with the reference-phase signal. The synchronous demodulator should output a current which is only a function of the phase shift, however, this current is also a function of the amplitude noise of the filer's driving signal. This noise can be modelled as a noise in the reference-phase signal. The bandwidth in which the noise of each reference will be integrated is a function of the decimated value. However, this noise could be mitigated by regulating the supply voltage of the filter's driving buffer. Figure 4.6 shows the filter's driving buffer together with the implemented regulator. As shown, a control switch is also implemented which bypasses the regulator. In this way, the resolution performance could be measured with or without the regulator. The regulator consists of a sample & hold switch capacitor circuit together with a native NMOS transistor [5]. The supply voltage will be sampled and held during the sigma-delta's conversion time. As shown in Fig. 4.6, this voltage controls the gate of the native NMOS which is implemented in a source-follower configuration. As a result, the voltage fed to the filter's driving buffer is equal to $V_{DD} - V_{GS,native}$ while the perturbations associated with the supply will be suppressed by its intrinsic gain equal to $g_m R_{out}$.

It should be noticed that the sampled charge on the sampling capacitor will leak due to the sub-threshold leakage of the sampling switch and more importantly due to the gate oxide tunnelling current of the native NMOS [6]. Furthermore, the leakage current increases with temperature. The voltage drop across the sampling cap results in an additional source of inaccuracy. In order to keep the effect of this voltage drop much lower than the targeted inaccuracy, a sampling capacitor of 10 pF is chosen, which in worst case results in a voltage drop of 20mV.

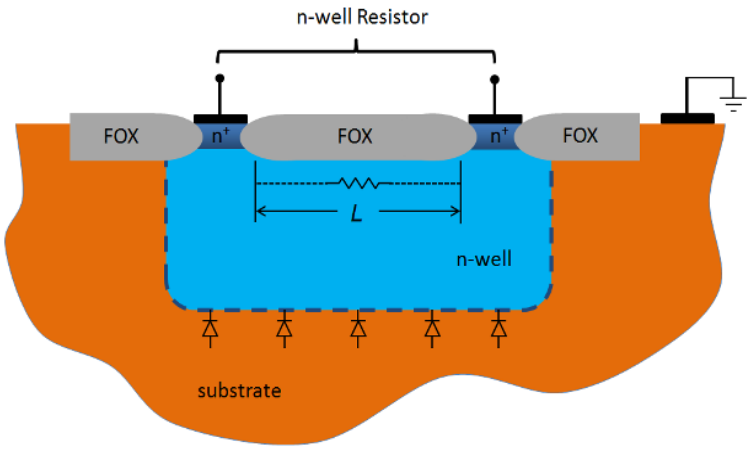

Figure 4.4. *N-well resistor implemented in standard CMOS technology*

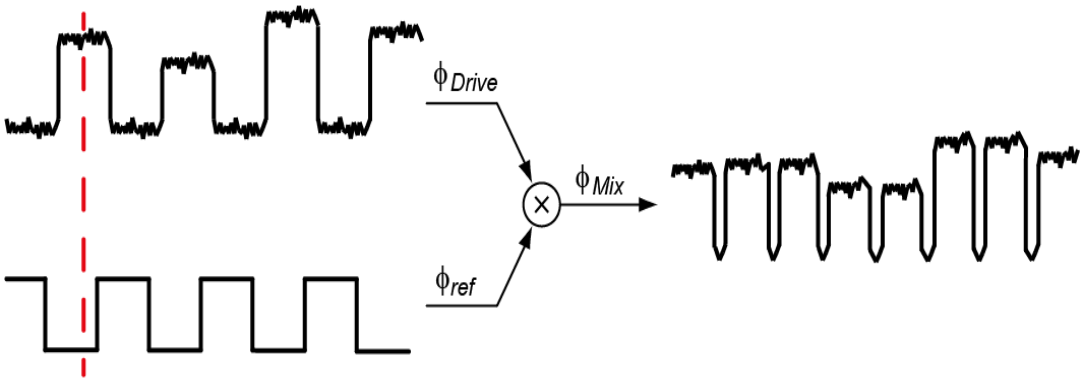

Figure 4.5. *Effect of supply noise after mixing with the reference signal*

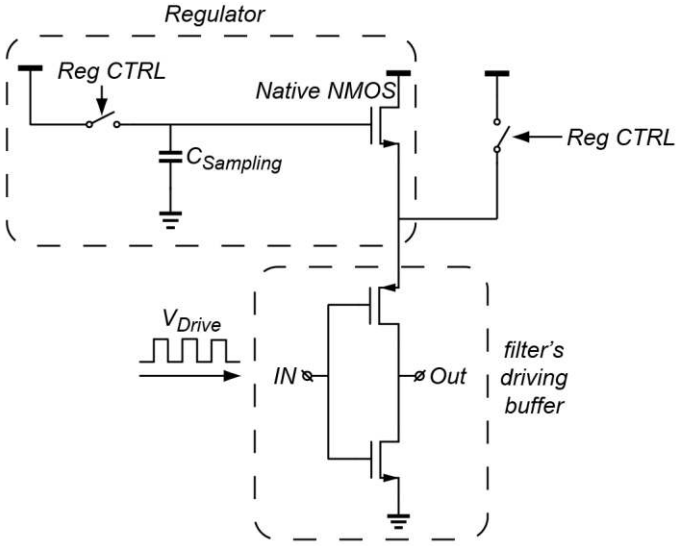

Figure 4.6. *Implemented regulator for reducing the noise of filter's driving signal [5]*

4.3.5 Conclusion

As can be seen, source degeneration is used for the current sources, and also the input of the current-buffer is placed at the P-side. The modified current-buffer lowers the input referred noise by more than 2x, while consuming about 2x less power. On top of this, supply noise is mitigated by employing a simple regulator. As discussed before, since the thermal noise floor is more than 120 dB, a 2nd order sigma-delta is required in order to have a thermal noise limited TDC in a conversion time of less than 100 msec. The 2nd-order loop is implemented based on the concept of "*Hybrid Sigma-Delta*" whose system-level implementation is discussed in next section.

4.4 2nd-order "Hybrid Sigma-Delta"

In this section the system design of a 2nd-order PDSDM is presented. While exploiting the "*Hybrid Sigma-Delta*" concept [7, 8], the 2nd-order loop filter incorporates a first stage continuous-time (CT) and a second stage discrete-time (DT).

4.4.1 System Implementation

Figure 4.7 shows the sigma-delta modulator which consists of a charge-balancing loop-filter and a clocked quantizer. At every clock cycle, the bit-stream polarity determines that whether the positive reference-phase signal or the negative one should be input to the loop-filter. As can be seen, the charge-balancing scheme is exactly the same as the previous design.

As previously discussed, the PDSDM employs a synchronous chopper demodulator which extracts the phase information associated with the WB. However, the mixer outputs a DC signal which conveys the temperature information together with an AC signal with a frequency of $2 \times f_{Drive}$ while the offset of the first integrator is also up-modulated to the frequency of equal to f_{Drive} (see Eqn. 2.6). Both of these non-idealities cause extra temperature inaccuracy. While choosing a sampling frequency of $2 \times f_{Drive}$ and synchronized with the WB's driving signal for the following DT integrator, these sources of inaccuracy could be filtered out in z-domain.

Figure 4.8 shows the implemented 2nd order loop filter. In order to stabilize the loop filer, the 2nd stage includes a feed-forward path which also reduces the required output-swing of the 1st integrator since the input signal component is high-pass filtered. While the achieved extra headroom, could be traded for a lower thermal noise floor, which is in line with the targeted energy-efficienct performance. Moreover, the coefficients of the loop-filter is chosen such a way that guaranties the stability of the loop-filter, which results an output swing of less than 200 mV for both integrators over PVT variations. To do so, while the modulator's sampling frequency is equal to $2 \times f_{Drive}$, the time-constant ω_0 of the CT should be normalized to the modulator's sampling frequency. As a result, the time constant of the first integrator could be calculated as follows:

$$\omega_0 = 0.06.2\pi.2f_{Drive} = 0.2\ Mrad/sec. \tag{4.7}$$

The transfer function of the first integrator could be then shown as follows:

$$H_{(S)} = \frac{1}{1+{}^{S}/_{0.2\text{M rad/sec}}}. \tag{4.8}$$

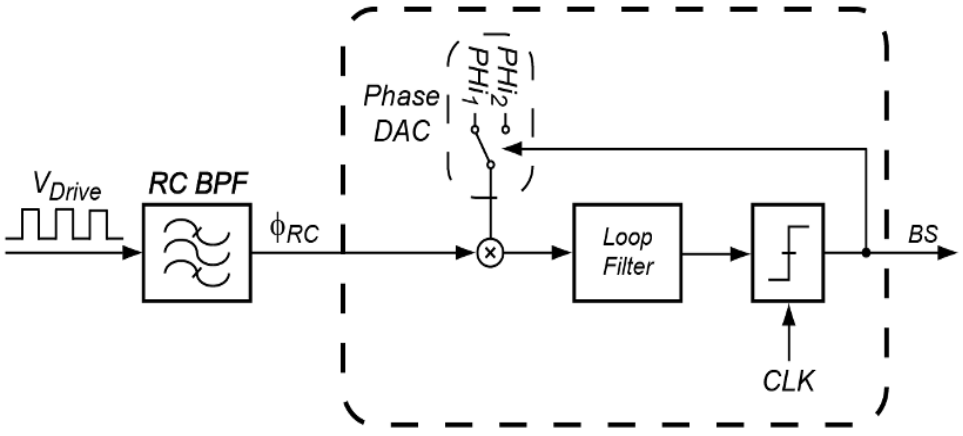

Figure 4.7. *Charge-balancing scheme in the implemented sigma-delta modulator*

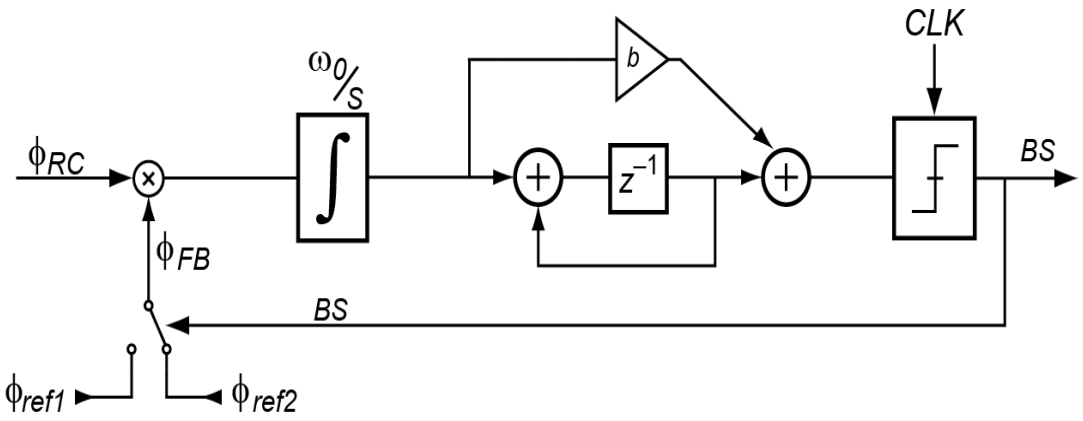

Figure 4.8. *The simplified block-diagram of the feed-forward second-order sigma-delta modulator*

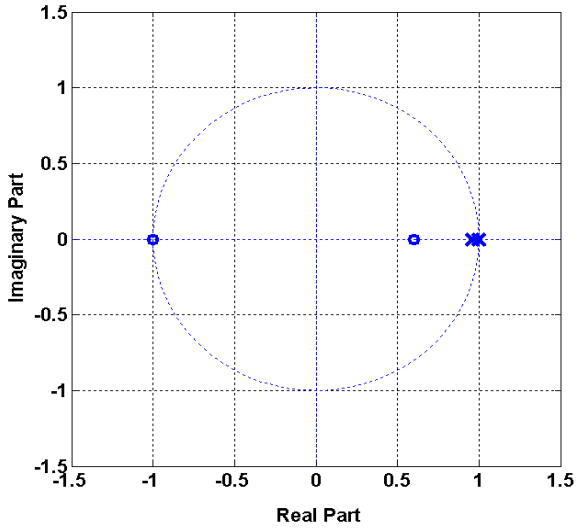

Figure 4.9. *The zero-pole distribution of the equivalent DT loop-filter in z-domain (F_S=500KHz)*

While having a sampling frequency of $2f_{Drive}$ and assuming a linear interpolation between the sampled data, the continuous-time integrator could be translated into a Z-domain (discrete-time) as follows:

$$H_{(Z)} = \frac{Z+1}{Z-0.96} \quad . \tag{4.9}$$

Moreover the feed-forward coefficient b is equal to 2.5, while the 2nd integrator is implemented in a forward-path delayed configuration. The zero-pole distribution of the equivalent DT loop-filter in z-plane is shown in Fig. 4.9. As can be seen, the zero placed at z=0.6 ensures that the loop-filter is always stable, while maintaining the 2nd-order behaviour [9]. It should be noticed that the time-constant of the first integrator is determined by the resistor implemented in the WB, together with the integration capacitor. While the value of the implemented resistor is equal to 135kΩ, an integration capacitor equal to 37pF is required.

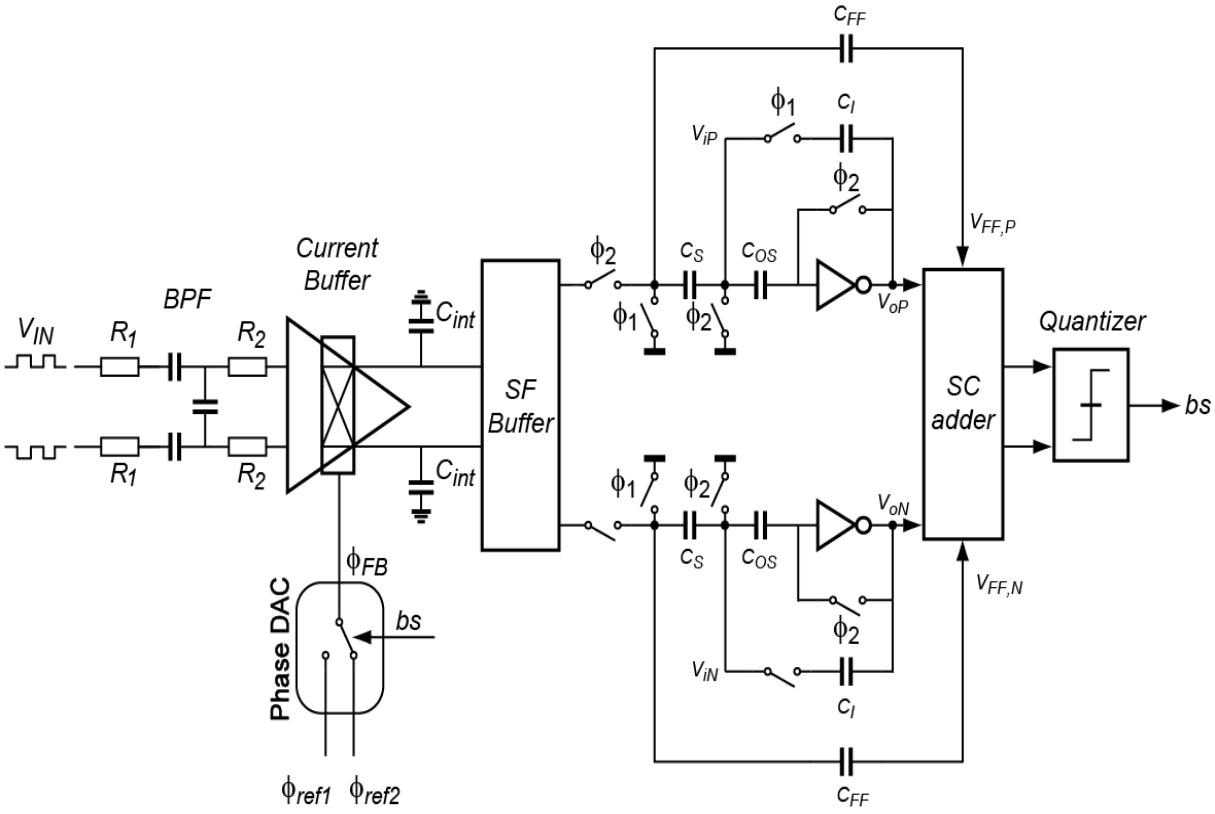

Figure 4.10. *Top-level implementation of the TDC using 2nd-order hybrid loop-filter sigma-delta*

4.5 Circuit Implementation

Figure 4.10 shows the 2nd-order hybrid PDSDM which incorporates a CT 1st-integrator and a DT 2nd-integrator. In order to minimize the power dissipation of the 1st integrator, it was implemented as a passive rather than an active integrator [2]. However, as discussed in Chapter 3, the passive integrator has an exponential leaky behaviour. Thus, it could not be directly connected to the following SC integrator. in order to tackle this problem a voltage-buffer is desired which buffers the output of the 1st integrator. The required voltage-buffer is implemented as a source-follower. The following DT stage is an energy-efficient pseudo-differential inverter-based integrator whose output will be added to the feed-forward signal by means of an SC adder [10, 11]. The output of the SC adder will be then fed into a quantizer whose output controls the charge-balancing feedback loop. As can be seen, the constituting blocks could be mainly classified as the current-buffer, a source-follower voltage-buffer between the 1st and 2nd integrator, a SC 2nd integrator, a SC adder, and a 1-bit quantizer. The circuit implementation and design considerations for the above mentioned blocks will be discussed in detail in the following section.

4.5.1 First Integrator

Figure 4.11 shows the modified current-buffer which operates in the same way as the passive integrator used in the first test chip (see Chapter 3). As the first integrator dominates

the noise performance of the ADC, this block limits the ultimate resolution of the whole system. As previously discussed, the noise performance of the current-buffer is improved by a factor of about 2x, while consumes about 2x less power equal to 18µW from a 1.8V supply. In order to make the noise contribution of the current-buffer to be the same as the implemented WB, the source degeneration resistors are chosen such a way that to have the same value as the resistors implemented in the WB. While looking at the Fig. 3.13 and using Eqn. 3.13, the noise performance of the first integrator could be extracted as follows:

$$S_{I_n} = \sqrt{4kT\left(\frac{2}{R_S} + \frac{1}{g_{mb}\times {R_{WB}}^2}\right)}\ {A}/{\sqrt{Hz}}. \tag{4.10}$$

While in this design, the transconductance of each current source is equal to $1/R_{WB}$, the transconductance of the gain-booster is equal to 100 µS, and the implemented resistor in the WB is 135 kΩ, the total noise could be calculated as follows:

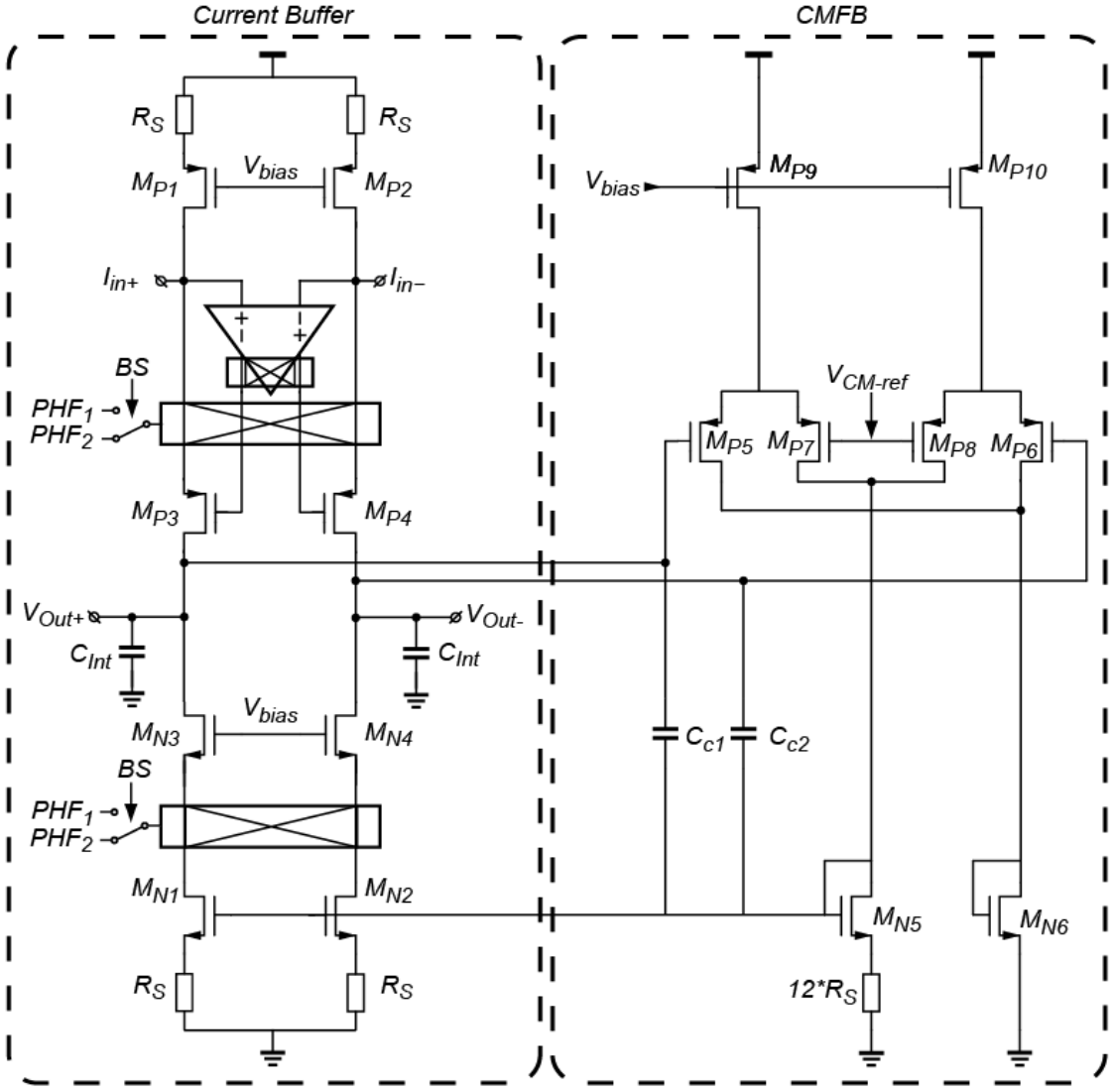

Figure 4.11. *Modified current-buffer, the implemented CT passive integrator*

$$S_{I_n} = \sqrt{4kT\left(\frac{2}{135k\Omega} + \frac{1}{100\ \mu S \times (135\ k\Omega)^2}\right)}\ {}^{A}/_{\sqrt{Hz}}. \quad (4.11)$$

where the total integrated noise in a 5Hz bandwidth is equal to:

$$\sigma_{I_n} = 1.38\ \text{pA (RMS)}. \quad (4.12)$$

which is about 1.7x more than the noise associated with the WB in the same bandwidth. This noise represents a temperature-sensing resolution of 369µK in a 5Hz bandwidth, while taking the sensitivity associated with the n-well resistor into account (see Chapter 2). Thus, the total temperature-sensing resolution in 5Hz bandwidth, while considering the WB's thermal noise incorporating n-well resistor, could be calculated as follows:

$$T_N \approx \sqrt{\left(T_{N,WB}\right)^2 + \left(T_{N,readout}\right)^2} = \sqrt{(176\mu K)^2 + (369\mu K)^2} = 407\mu K\ \text{(RMS)}. \quad (4.13)$$

Moreover, the source-degeneration technique together with the gain-boosting at the P-side (instead of N-side) of the current-buffer, its output impedance is increased by a factor of 10, compared with the previous design. However, due to the leakage associated with the passive integrator the quantization noise floor is still about 20dB higher than the thermal noise floor. In order to push the quantization noise much below the thermal noise floor, the 2nd integrator should provide with a minimum gain equal to 40dB.

The CMFB structure is the same as the one used in the previous design. However, in order to maintain the loop-gain provided by the CMFB, the diode-connected transistor M_{N5} should be also degenerated. In order to make a balance between area and power consumption, the degeneration resistor in CMFB is chosen to be 12 times larger than the degeneration resistor, while the CMFB consumes 500nA.

4.5.1.2 Gain Booster

Figure 4.12 illustrates the implemented booster amplifier which is a fully-differential telescopic configuration. As shown, input common-mode regulation is used to set the common-mode level of the booster's input terminal which also sets the DC bias voltage of the input terminal of the current-buffer [12]. A chopper is placed at the output of the booster which maintains the feedback polarity around the booster. Furthermore, it up-modulates the flicker noise associated with the booster. In order to compensate the loop around the booster, the same story as the previous design could be applied (See Chapter 3). The gain booster consumes 2.5µA, while having a unity-gain bandwidth of 75 MHz and a DC gain of 60dB. The gain-booster provides a gain of 50dB at the filter's driving frequency, which consequently reduces the current-buffer input impedance by about 200x. The telescopic implementation consumes 2x less power than the previous folded-cascode amplifier and its noise contribution is mitigated by connecting only one filter to the current-buffer, in the top-level chip implementation.

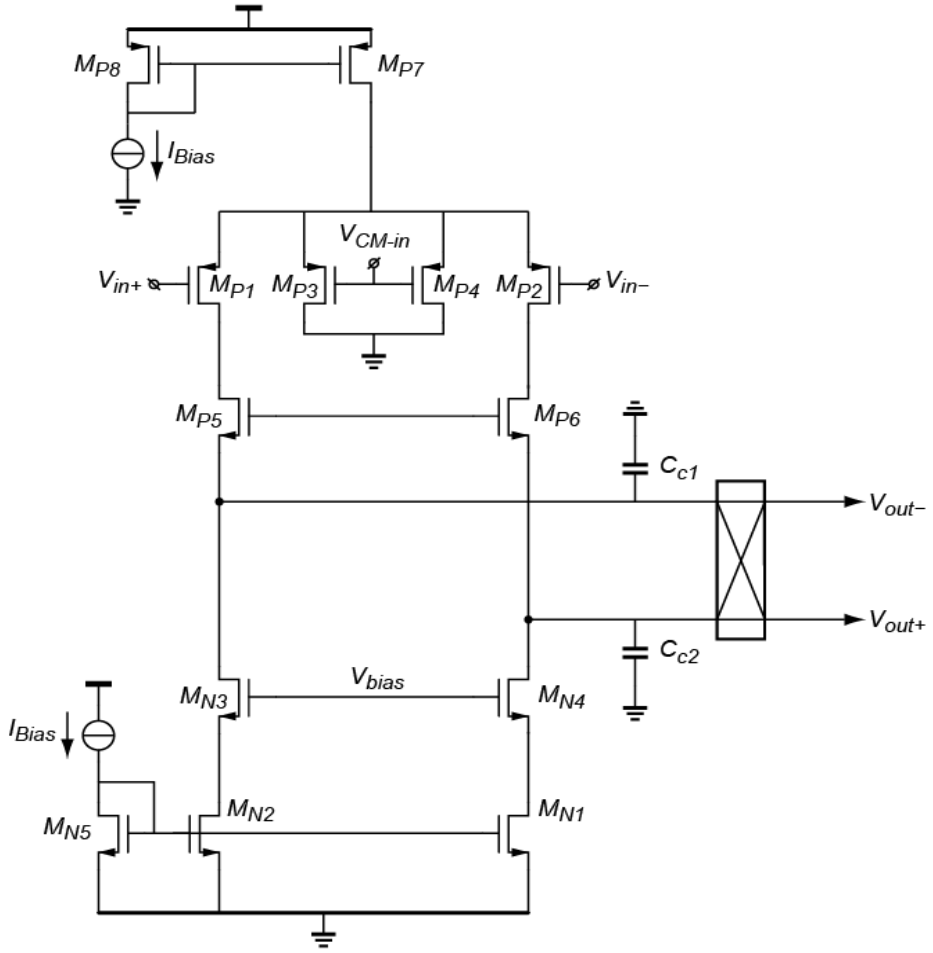

Figure 4.12. *Fully-differential telescopic gain-booster*

4.5.2 1st & 2nd Integrator Connection

Since the first integrator is implemented in a passive fashion, its output has to be buffered in order to prevent the integrator from being leaky [15]. A source-follower (SF) is chosen to buffer the 1st integrator's output (see Fig. 4.13). The main considerations for using a SF are its noise and non-linearity in order to be energy-efficient and prevent extra temperature inaccuracy, respectively. Although SF has a poor noise performance compared with other configurations, its noise will be high-pass filtered by the first integrator whose corner frequency is equal to few Hz. The non-linearity associated with the SF is caused by the non-linear dependence of V_{TH} upon the source potential. The non-linearity caused by the body-effect could be eliminated if the bulk is tied to the source. To do so, a PMOS input pair is chosen which its n-well substrate could be separated from the substrate of the other transistors. The voltage gain of the SF while considering the body-effect could be extracted as follows [3]:

$$A_V = \frac{g_m R_L}{1+(g_m+g_{mb})R_L}. \tag{4.14}$$

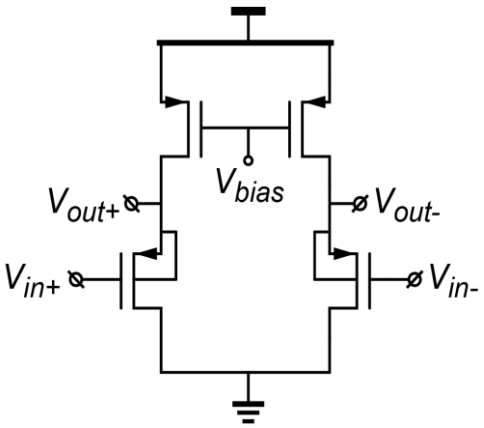

Figure 4.13. *Implemented source-follower to buffer the 1st integrator output voltage*

where g_m is the input transconductance, g_{mb} is the body transconductance, and R_L is the output resistance of the current source (see Fig. 4.13).

As mentioned before, the implemented source-follower should drive a SC circuit. In order to keep the settling-error of the source-follower to be about zero, it has to have a bandwidth of 5≈6 times more than the sampling frequency of the following DT integrator (500 kHz). Thus, the required bandwidth should be about 3MHz, Consequently, the required g_m for the input transistor could be extracted as follows:

$$g_m = C_{load}.BW. \tag{4.15}$$

where $g_m$is transconductance of the input transistor, C_{load} is the output load capacitance, and finally BW is the required bandwidth equal to 3MHz. To be concluded, assuming a load capacitance of 175fF, the required g_m should be higher than 3µS. The source-follower consumes 1 µA in total while satisfying the aforementioned requirements.

4.5.3 Second Integrator

As discussed before, the 2nd integrator requires a DC gain of more than 40dB. To be energy-efficient, it is employing a SC, pseudo-differential, inverter-based OTA as proposed in [11, 13]. As shown in Fig. 4.14, the inverter is implemented in a cascoded fashion which is dynamically biased in order to be more immune with respect to the PVT variations. During the sampling phase, M_1 & M_4 are biased with the floating current source made by M_5 & M_6 while the cascode transistors are biased in the off state. Using a floating current source ensures that the M_1 & M_2 are biased with exactly the same bias currents. Meanwhile, the offset-storage capacitors C_{OS}, store the operation biasing point. This auto-zeroing process also cancels the offset and flicker noise. During the integration phase, the floating current source will be disconnected from the inverter, while the cascode transistors M_2 & M_3 turned on with the appropriate biasing voltage. As a result, the inverter is configured as a high gain push-pull common-source amplifier with a well-defined bias-current. The output of the 2nd-integrator is connected to a SC passive adder which sums the feed-forward signal with the 2nd-integrator's output signal.

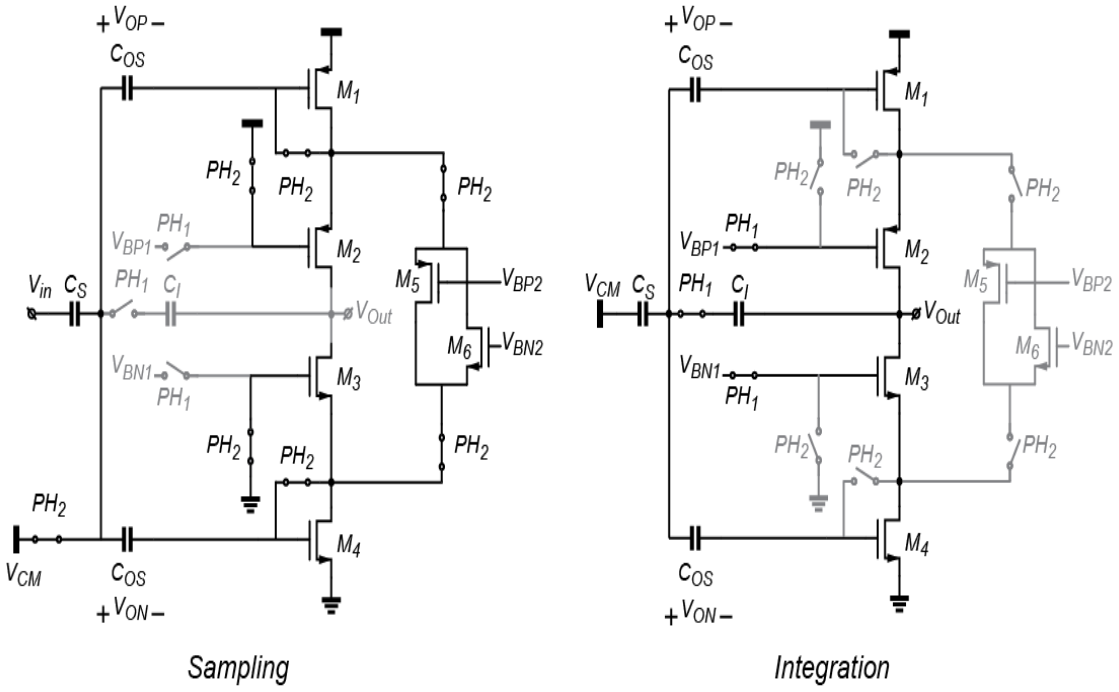

Figure 4.14. *Simplified circuit diagram of the inverter-based integrator in the sampling and integration phase*

As shown in Fig. 4.10, the 2nd integrator is implemented in a pseudo-differential configuration. Thus, a common-mode feedback (CMFB) is desired in order to maintain the output common-mode level as required. In this design a switched-capacitor CMFB is implemented, which samples the output and the desired common-mode voltages in charge packets. Then, subtract of these two charge packets will be fed back to the offset-storage capacitor at the input of the inverters.

The sampling capacitor could be as small as 5fF, since the noise associated with the 2nd integrator will be high-pass filtered. However, while considering the leakage current and charge injection associated with the switches, and moreover the parasitic effects, a sampling capacitor equal to 50fF is chosen. Thus, as discussed in system level implementation, a feed-forward and integration capacitor of 125fF and 50fF is required, respectively. The inverters draw 2µA while obtaining a DC gain greater than 60dB over PVT variations.

4.5.4 Comparator Implementation

The implemented comparator uses the same structure as the one implemented in the previous design. However, in order to prevent instability in the 2nd-order loop filter, the time-delay associated with the comparator should much lower than the delay of the 1st and 2nd integrator (2µsec). Moreover, since a 2nd order loop-filter is utilized, the effect of kick-back noise of the comparator is further mitigated. Thus, instead of three pre-amplifier stages, two pre-amps are used. However, lowering the time delay associated with the previously designed comparator requires more power. The comparator consumes 1µA in total, while the total delay of the comparator is less than 30nsec which represents a bandwidth more than 33MHz. Figure 4.15 shows the system level implementation of the modified comparator.

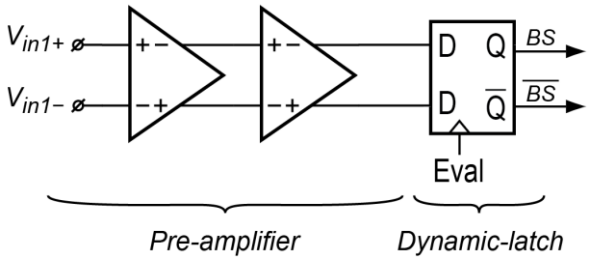

Figure 4.15. *Modified structure of the previously implemented comparator*

4.6 Simulation Results

As discussed before, the noise performance of the first test chip was dominated by the quantization noise. Since energy-efficiency is the main goal of this design, the quantization noise of the TDC should be lower than the thermal noise in the desired signal bandwidth. To do so, the thermal noise floor should be calculated and normalized with respect to the ADC's full-scale. As discussed in Chapter 2, the PDSDM requires a minimum full-scale equal to 30 degrees (radian) which defines the zero dB of the quantization noise PSD spectrum. This full-scale could be translated into a temperature full-scale of 270°C, while considering the phase-to-temperature sensitivity of the WB incorporating the n-well resistor. Consequently, the previously calculated temperature sensing resolution of 407 µK in 5Hz bandwidth represents a thermal noise floor of -124dB. As a result, to be thermal noise limited, the ADC should provide a dynamic range of more than 124dB.

A transient simulation is utilized in order to extract the quantization noise PSD spectrum of the implemented 2^{nd}-order hybrid PDSDM and prove that a quantization noise floor of lower than -124dB could be obtained. Figure 4.16 shows the simulated output spectrum of the implemented circuitry. In this simulation, only the quantization noise is shown which is normalized to the ADC's full-scale. The output spectrum is extracted from 16384-points FFT and applying a Hanning window, which represents a conversion time of about 30msec. As can be seen the ADC provides with a quantization noise much lower than the thermal noise floor equal to -124dB.

4.7 Chip Implementation

The chip was fabricated in the $0.18\mu m$ standard CMOS process with the Euro-Practice IC Multi-project wafer service, hosted by CSEM. Figure 4.17 shows the top level implementation of the chip. It consists of two WB incorporating the n-well resistor and another one using n-poly resistor. Following the WBs, the 2^{nd}-order hybrid PDSDM is placed. The filter's driving signal, the reference-phase signals, the 2^{nd} stage control signals together with the quantizer's sampling frequency are going to be generated from an FPGA. Furthermore, to have a lower phase-noise, all the above mentioned signals are synchronized with the crystal oscillator which drives the FPGA, by using on-chip D-FF (see Chapter 3).

Moreover, in order to possibly measure the targeted sub-mK resolution, two temperature sensors are placed on one die (see Chapter 3). In this way, the common-mode environmental thermal noise could be mitigated by the common-mode rejection property of the two temperature sensors.

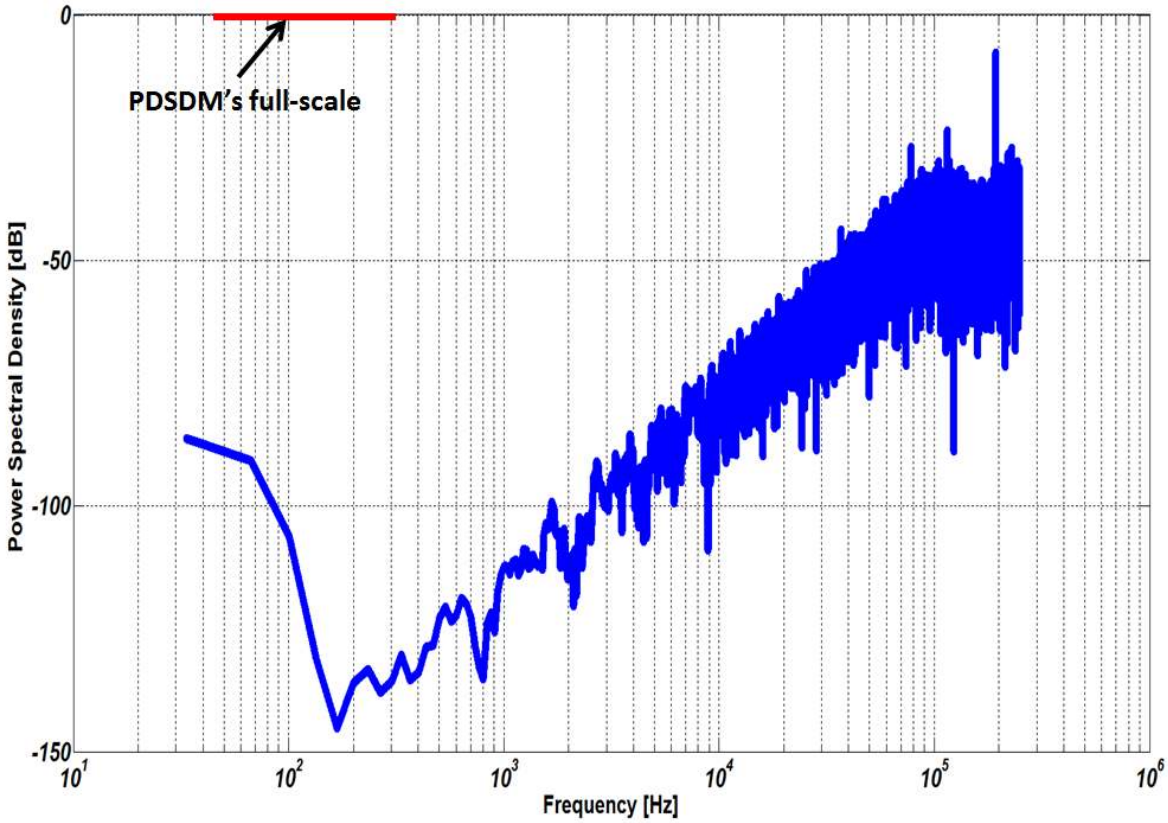

Figure 4.16. *simulated output spectrum of the temperature sensor using 2nd-order hybrid PDSDM (16384-point FFT, Hanning window)*

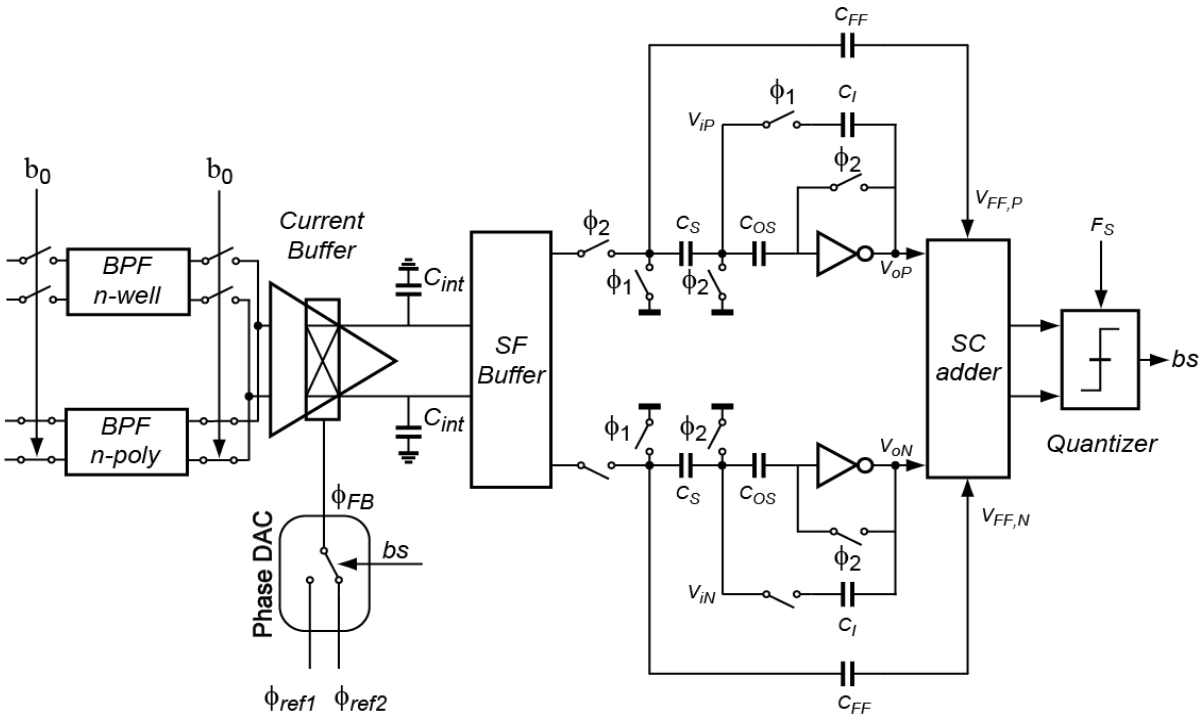

Figure 4.17. *Top-level implementation of the 2nd test chip*

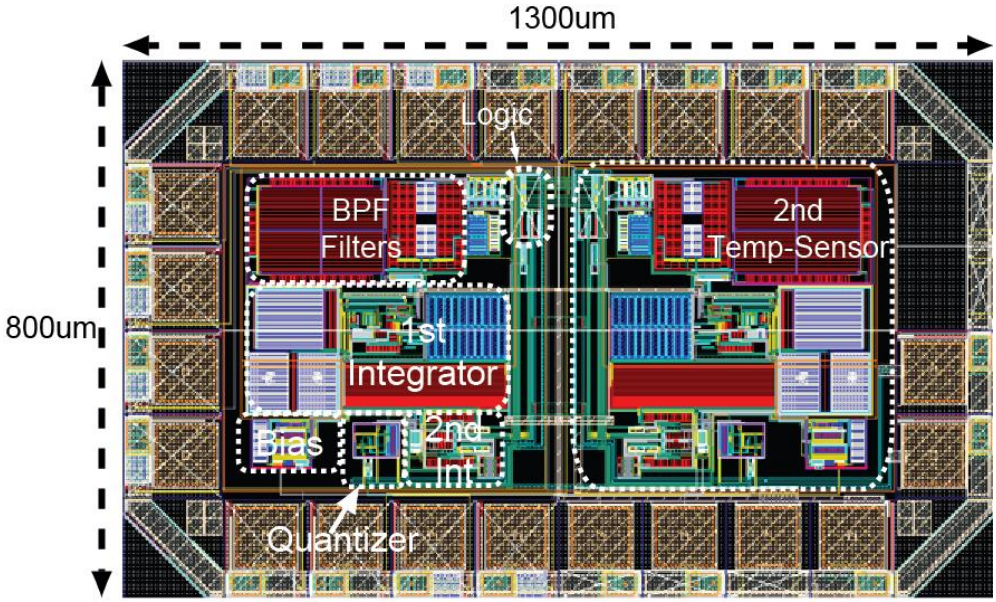

Figure 4.18. *2nd test chip top-level layout*

4.7.2 Layout

Figure 4.18 depicts the layout of this test chip with highlighted important parts. Since a low-noise readout circuitry is targeted, the on-chip logics are placed far apart from analog circuitry. On top of this, all the sensitive elements to noise such as degenerated resistors, WBs, and integration capacitor of the first stage are all shielded. Furthermore, in order to mitigate the input referred offset, interdigitated layout configuration is used specially for the source degeneration resistors, the input pair of the gain-booster together with the its current sources.

4.8 Expected Performance

As calculated before, the temperature-sensing resolution could be equal to 407µK in a conversion time of 100msec, while considering the phase-to-temperature sensitivity of the n-well under STI resistor. However, in this design, two resistor types namely n-poly and n-well under OD are implemented in the WB. The n-poly and n-well under OD have 2.1x less and 1.2x more sensitivity. Consequently, the resolution of n-poly and n-well under OD will be 854 µK and 339 µK in the same 100msec conversion time, respectively. The 2nd-order PDSDM enters the thermal noise limited region in about 10msec, which is the optimum operating point from the energy-efficiency point of view. Although, for a conversion time of 10msec, the bandwidth in which the noise is integrated will be larger by a factor equal to $\sqrt{10}$ compared with the 100msec conversion time. Moreover, the whole chip is expected to consume about 15µA from a 1.8V supply.

The temperature-inaccuracy extracted from the n-poly in previous design was less than 0.1°C, after a 2nd order fitting and over the industrial temperature range. However, by lowering the noise by about 10x, the 3σ of the noise could be removed which in case of n-poly resistor is about 0.018°C. The implemented n-well under OD, based on simulation

results, is expected to have higher temperature sensitivity, and better linearity performance compared with the n-well under STI. However, its temperature inaccuracy could be extracted after testing the chips. The sensor's performance, both for n-poly and n-well resistor, is summarized in Table 4.1 and compared to other energy-efficient designs. It draws 15μA from a 1.5V to 2.1V supply which provides a thermal noise limited resolution of less than 2mK in 10msec conversion time (5000 ΣΔ cycles).

Figure 4.19 shows the dissipated energy/conversion versus resolution for state-of-the-art designs, and including this work [2]. As shown, the designed sensor achieves sub-mk resolution while consumes about few hundreds nJ during a conversion. The sensor should have a resolution-FOM of less than 3pJ°K^2 which would rank it as the most energy-efficient temperature sensor among the state-of-the art designs.

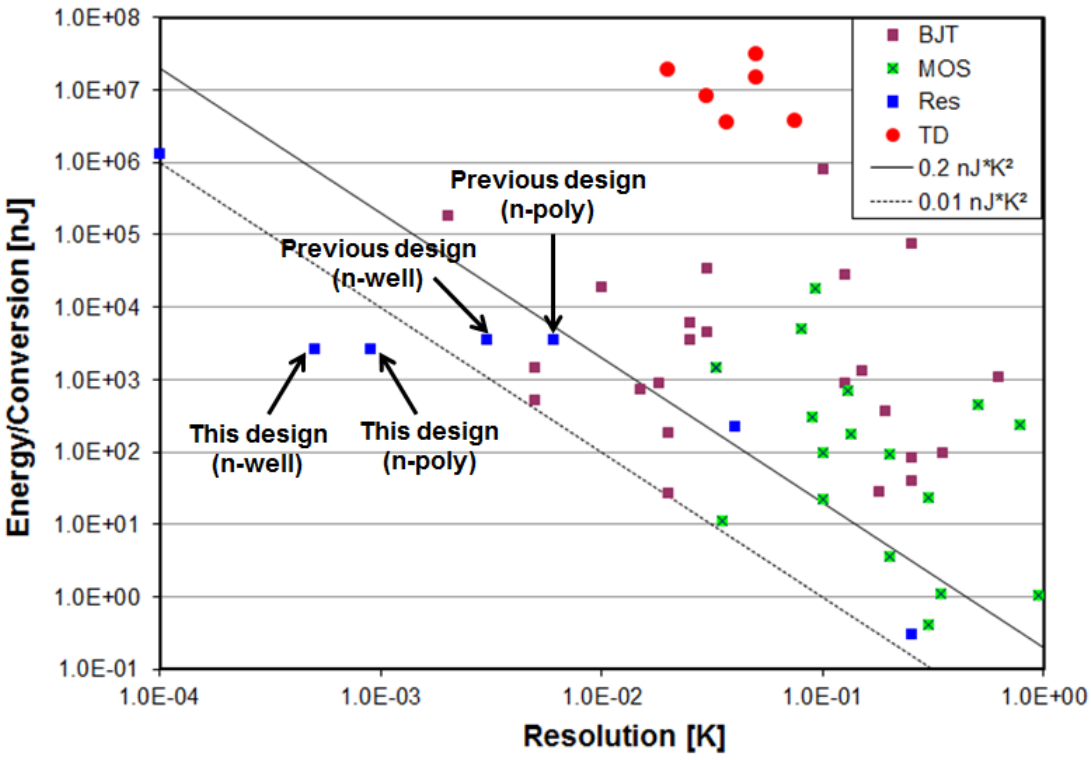

Figure 4.19. *Dissipated energy/conversion as a function of resolution[2]*

Table 4.1. *Performance Summary and Comparison to Previous Work*

	This work	This work	ESSCIRC Prev. work [1]	JSSC [5]	JSSC [10]	JSSC [14]
Sensor Type	Resistor (n-well)	Resistor (n-poly)	Resistor (n-poly)	Resistor	BJT	Resistor
Technology	0.18µm	0.18µm	0.18µm	0.18µm	0.16µm	0.18µm
Area	0.4mm^2	0.4mm^2	0.35mm^2	0.044mm^2	0.08mm^2	0.18mm^2
Supply dependency	<0.5°C/V	<0.5°C/V	0.65°C/V	-----	0.5°C/V	-----
Temp range	-40 to 85°C	-40 to 85°C	-40 to 85°C	-40 to 85°C	-55 to 125°C	0 to 100°C
Inaccuracy	-----	<0.05°C (expected)	0.1°C	0.03°C	0.15°C	3°C
Calibration (point)	-----	Thermal (3)	Thermal (3)	Thermal (6)	Voltage (1)	Thermal (1)
Resolution (Con. Time)	0.86mK (10msec)	1.5mK (10msec)	6mK (100msec)	0.1mK (100msec)	5mK (100msec)	40mK (7.5msec)
Power	27µW	27µW	36µW	10mW	7uW	30uW
Res. FOM (pJK^2)	0.68	2.2	80	13	11	360

4.9 Conclusion

Integrating the temperature sensors in battery powered applications has placed a stringent requirement on their energy-efficiency performance. Prior-art smart temperature sensors have shown an ultimate energy-efficiency performance limited to 10pJK^2. However, study of state-of-the-art energy-efficient temperature sensors revealed the fact that in all designs the TDC's resolution is off by about more than 5x than the ultimate resolution associated with the used sensing-element. However, while the readout circuitry dominated the noise performance of the TDC, the extra power and resolution of the sensing element degrades the energy-efficiency performance. In order to make a balance between the noise performance of the sensing element and the readout circuitry, a "*2nd-order Hybrid Phase Domain Sigma-Delta Modulator*" is implemented. The proposed approach efficiently combines the continuous-time and discrete-time integrator, while they are implemented in passive and active

configuration, respectively. The first CT passive integrator provides with about the same noise performance as the sensing element, while its power consumption is also in the same order as the sensing element. Moreover, CT implementation imposes no noise folding. Both these advantages are in-line with the targeted energy-efficient performance. On top of this, since also a high-resolution performance is targeted, a 2^{nd} order sigma-delta loop is implemented in order to provide with a thermal noise limited resolution. While again considering the energy-efficiency, the 2^{nd} stage is implemented as DT inverter-based, which also aims to improve the temperature inaccuracy by filtering out the non-idealities associated with the first integrator. While combining all the above mentioned performance together, a sub-mK resolution could be obtained in a low power fashion which corresponds to at least 5x to 15x improvement in energy-efficiency compared to state-of-the-art temperature sensors.

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5 *Conclusion*

5.1 Conclusion & Future Work

Several low-noise techniques such as source degeneration, CT sigma-delta, while incorporating a passive integrator have been employed to improve the energy-efficiency. However, the temperature inaccuracy of the proposed architecture is limited to the non-linear temperature dependence of the resistor. In order to achieve an inaccuracy of less than 0.1°C (3σ) over the industrial temperature-range, multipoint trimming is required. As extracted from the first test chip, the targeted inaccuracy could be achieved while using n-poly resistor. However, as the 2nd test chip provides 6x more resolution, the extracted inaccuracy could be improved by about 0.02°C. Furthermore, as shown in Chapter 2, the temperature-dependent gain error associated with the implemented WB is about 0.03°C after a 2nd order fitting. The non-linear gain error coefficients of the implemented TDC could be extracted by sweeping the WB's driving signal frequency, this technique is called room temperature frequency trimming. Then, the extracted coefficients could be subtracted from the measured temperature characteristic of the TDC which ideally removes this source of inaccuracy. Consequently, after doing the so-called frequency calibration together with the available high-resolution, the expected temperature-inaccuracy of the 2nd test chip while using n-poly resistor, should be less than 0.05°C (3σ) over the industrial temperature range and after a 2nd order fitting which represents 3-point trimming.

A substantial improvement in energy-efficiency compared to prior ultra-low energy temperature sensors has been achieved in this work. Further improvements, however, are still possible both in circuit and topology levels. For instance, an inaccuracy of about 0.05°C (3σ) could be achieved after 3-point trimming and employing a frequency trimming at room temperature. Moreover, energy-efficiency performance could be improved by possibly removing the source-follower while also implementing an ultra-low power and fast

comparator. Lastly, the idea of hybrid sigma-delta utilizing a first stage CT passive integrator could be adapted with other energy-efficient applications such as capacitor-to-digital converter used in humidity sensors and accelerometers.