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# An Equal Precision Programmed Cymometer Design Using Low-Power Technique

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**Abstract:** Based on equal precision frequency measurement and pulse counting technique, a multi-period synchronous frequency measurement method is proposed in this paper. A programmed cymometer is designed with a full frequency band with equal precision measurement and improved measurement accuracy. In addition to adopting a low-power gate-control clock technique, the strong stability of our design is also carried out through the filtering of interference signals. Finally, the designed circuit is implemented with FPGA. The experimental results show that the static power consumption of the programmable frequency meter testing platform designed after continuous operation for 100 h is only 0.56 W, and the input impedance is 1 M Ω/40 pF. At the same time, the errors of frequency, cycle measurement, duty cycle measurement, and time interval are within a reasonable range. In addition, the measurement accuracy requirements for various indicators can also be met at a maximum frequency of 100 MHz. Therefore, this work can provide a feasible design method for low-power consumption electrical systems that are easy to replicate.

**Keywords:** equal precision; cymometer; clock gating; pulse measurement



**Citation:** Liu, Y.; Tang, J.; Feng, C.; Zhang, C.; Xue, Y.; Zhang, L.; Xu, S.; Wang, J.; Dai, F.; Wang, N. An Equal Precision Programmed Cymometer Design Using Low-Power Technique. *Appl. Sci.* **2023**, *13*, 5173. https://doi.org/10.3390/app13085173

Academic Editors: Ernesto Limiti and Yitsen Ku

Received: 8 January 2023
Revised: 19 April 2023
Accepted: 20 April 2023
Published: 21 April 2023



## 1. Introduction

A digital cymometer is an instrument that can digitally measure frequencies, time, and physical quantities from sensors. Its basic work principle is to select a stable reference frequency and compare it to the frequency of other tested signals. After calculating the number of pulses per second of the tested signal, it can be converted to frequency and displayed digitally [1,2]. Due to massively adopting discrete components, the early cymometer designs face serial problems such as long clock cycle, poor stability, large finished product volume, and high power consumption [3–5]. Due to employing discrete electronic components, a long design period and poor stability are common factors accompanying cymometer design. In addition, the conducted products always have large volumes and high power consumption. Fortunately, the extensive improvement of digital electronic technology and integrated circuit technology promotes the wide application of digital cymometers [4]. As a result, a digital cymometer can be designed and realized by a unit circuit and Single Chip Microcomputer. Compared with the conventional discrete cymometer, the volume of the digital cymometer is greatly reduced, with improved stability. The development direction of future frequency meters is miniaturization, high accuracy, and a wide measurement range. With the development of integrated circuits, the emergence of FPGA makes it possible to reconstruct chip hardware circuits, overcoming the shortcomings of traditional hardware circuit design that are time-consuming and laborious. With the characteristics of FPGA parallel pipelines, using the "equal precision measurement method" can achieve high-precision, high-bandwidth, and efficient measurement functions. However, the range of frequency measurement that can be achieved for a single FPGA is

also limited, and FPGA chips with higher operating speeds tend to lead to high power consumption and expensive prices [6,7]. Additionally, it still faces a long design period due to its complex circuit. Furthermore, the measurement range of digital cymometers is always limited. Therefore, it is necessary to use a specially designed circuit to simplify the measurement process [8–10].

To solve this problem, this article introduces a method that uses a mixer to mix locally known high-frequency signals with the signal to be tested, and continuously reduce the frequency at a certain frequency by controlling a phase-locked loop module. After filtering by a low-pass filter, the down-converted signal is obtained, the signal power output is then detected by the low-pass filter to automatically select the appropriate frequency conversion signal. Next, the variable frequency signal is measured using the "equal precision measurement method" based on FPGA, and the measurement results are finally displayed on the OLED display screen through calculation. Compared with traditional frequency meters, this method reduces the threshold for circuit design, realizes miniaturization of the equipment, and expands the frequency measurement range while ensuring measurement accuracy [11,12].

## 2. Working Principles

### 2.1. Basic Structure

Figure 1 describes the control structure of the equal precision digital frequency meter. The structure is mainly composed of a pulse signal processing circuit, pulse width measurement circuit, frequency, and cycle measurement circuit, controlling and data-processing circuit, and displaying circuit. Among them, the pulse signal processing circuit is used to generate the measured signal [13]. After receiving the detecting signal from the duty cycle measuring circuit, the pulse width measuring circuit begins to measure the pulse width generated by the pulse signal processing circuit. During the process of pulse width detection and frequency processing, the reference frequency is supplied by the standard frequency signal generation circuit. By employing the waveform-shaping circuit, the input signal amplified by the preset amplifier module will be shaped for easy frequency acquisition. After the frequency input signal to be tested enters the signal amplification and shaping circuit for processing, it is distributed to the frequency and period measurement circuit together with the standard frequency signal for counting operation and measurement. At the same time, the input frequency signal to be tested and the standard frequency will also be linked to the pulse signal processing circuit for duty cycle measurement. Finally, the processed data are transmitted into the controlling and data-processing circuit for decoding and data processing, which will be displayed in real time by the display circuit [14]. The working process above is the basic equal precision measurement method. It should be noted that the biggest feature of the equal precision measurement method is that the preset gate time is not a fixed value, but a value related to the signal to be tested. Moreover, it is exactly an integer multiple of the period of the signal under test [15–17].

### 2.2. Frequency Measurement Design Methods

For the measurement frequency value, assuming that the standard frequency is $f_s$, the count value of the measurement signal is $N_x$, and the value of the standard signal is the count value set in the main preset gate time $T$, which is $N_s$; the measurement frequency $f_x$ is established as the following formula [18,19]:

$$f_x = (f_s \times N_x)/N_s \quad (1)$$

It can be seen from Formula (1) that if the error of standard frequency $f_s$ is ignored, the possible relative error $\delta$ of equal precision frequency measurement is shown in Formula (2):

$$\delta = (|f_{xe} - f_x|/f_{xe}) \times 100\% \quad (2)$$

where $f_{xe}$ is the accurate value of the measured signal frequency.

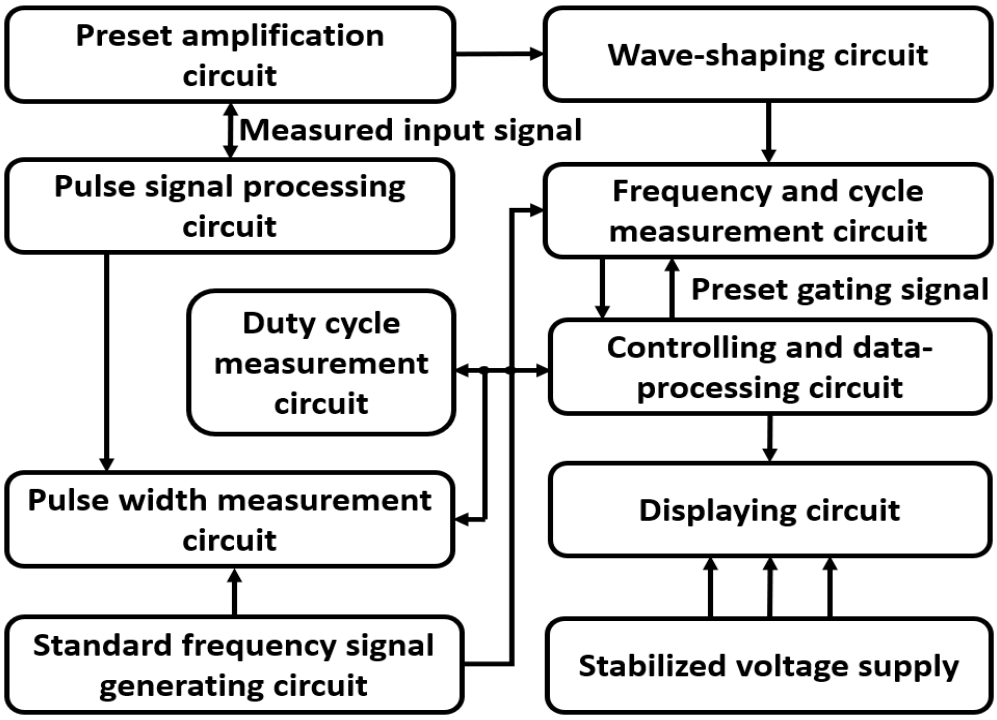



**Figure 1.** Structure diagram of the equal precision digital cymometer.

In the measurement, since the start and stop times of $f_x$ counting are triggered by the rising edge of the signal, there is no error in the $f_x$ counting $N_x$ within the preset gate time $T(T = N_x T_x)$. There is a counting error of $N_s$ for $f_s$, that is $|\Delta N_s| \leq 1$, and the measurement frequency is shown in Formula (3) [20]:

$$f_{xe} = [N_x/(N_s + \Delta N_s)] \times f_s \tag{3}$$

Substituting Formulas (1) and (3) into Formula (2), the relative error δ can be optimized as Formula (4):

$$\delta = |\Delta N_s|/N_s \leq 1/N_s = 1/(T \times f_s) \tag{4}$$

It can be seen from the Formula (4) that the relative error of the measured frequency is independent of the size of the measured signal frequency and is only related to the preset gate time and the standard signal frequency, that is, the equal precision measurement of the entire test frequency band can be achieved. The longer the time, the higher the standard frequency, and the smaller the relative error of frequency measurement [21,22].

## 3. Systematic Design Scheme

### *3.1. Equal Precision Digital Cymometer Design Principle*

In this work, an equal precision digital cymometer design is proposed as shown in Figure 2. It mainly consists of the self-calibration/frequency measurement selection module, counting/pulse width measurement status control module, gated clock selection module, and counter module. Among them, the self-calibration/frequency measurement selection module FIN is mainly controlled by the signal CHOIS. By setting signal CHOIS, the system will decide whether to start self-calibration or frequency measurement. The next module CONTRL is referred to as the frequency measurement state control. It mainly receives the signal START to select the frequency of the counter module and controls its counting end state through signal ENDD. In addition, the signal PUL will be received to count the upper and lower edges of the pulse signal in the pulse measurement control module CONTROL2. For the module of GATE, the function of pulse width measurement or frequency counting is dependent on the bit of CNL. Finally, the corresponding counting

results are obtained based on the input frequency in the two counter modules, CNT, which are processed by the single-chip microcomputer through the signal output signal. This equal precision measurement process is carried out by two channels of counting modules and a standard clock, and then the frequency to be tested can be calculated conveniently.

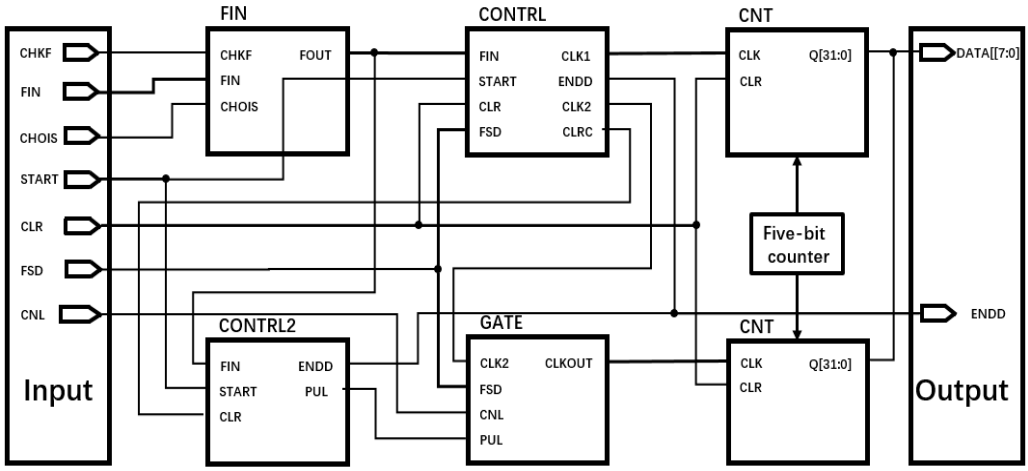



**Figure 2.** Equal precision digital cymometer circuit systematic diagram.

### *3.2. Circuit Design of Frequency Measurement Specialized Modules*

#### 3.2.1. Design of Self-Calibration/Frequency Measurement Selection Module

The implementation method of self-calibration/frequency is a comparative process. Figure 3 describes the self-calibration process and circuit implementation designed in this article. Based on CHKF, by adjusting the FIN output frequency, the output frequency is closer to the output frequency of CHKF. When the two do not have a different frequency, the accuracy of the FIN frequency reaches the accuracy of CHKF. Based on this principle, when the frequency difference between the two is less than a certain value, the FIN output frequency can meet the accuracy requirements, thereby achieving frequency calibration purposes. In addition, it should be noted that CHKF and FIN need to be calibrated after the circuit work is stable. At the same time, when FIN fails to meet the accuracy requirements, FOUT provides frequency sampling by the CHKF signal to ensure the reliability and stability of the system. As shown in Figure 3a, the compared results between FIN and CHKF will be transmitted into FPGA for data processing, which is used to judge whether the FIN frequency meets the accuracy requirement. Finally, the signal measurement with high accuracy can be carried out through the regulation and optimization of the DAC module.

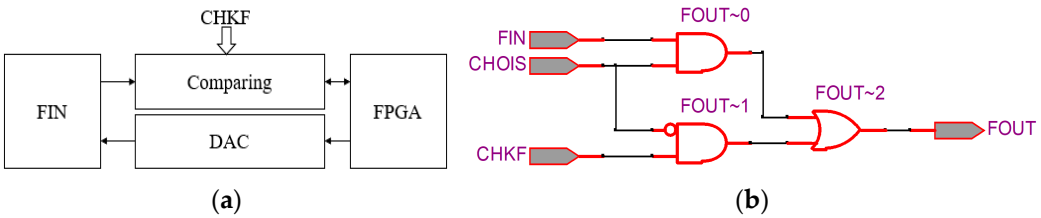



**Figure 3.** Self-Calibration/Frequency Measurement Selection Module. (**a**) Working cells, (**b**) designed circuit.

#### 3.2.2. Clock Control of Frequency and Period Measurement

As shown in Figure 4, the circuit design for the frequency and period measurement clock sources is presented. To prevent operating with error, START is triggered by using one D-type Flip-Flop register. It can also filter unnecessary burrs. Then, the two-channel clock sources including FIN and FSD can be selected with two AND2 gates by the clear signal in end Q. Among them, FIN is flowed into CLK1 for frequency measurement operation, while FSD flows into CLK2 for cyclical measurement operation. When the START signal at

the input end of the D flip-flop is high-level, the Q end will become high-level if there is a rising edge at the FIN end. Therefore, the clock of CLK1 is provided by the FIN-measured signal frequency, and the clock of CLK2 is provided by the FSD reference clock. At the same time, the high level of the Q terminal is also provided to EEND to display the frequency measurement status flag. CLRC in Figure 4 is the zero-clearing flag, where the circuit initialization is completed through the pulse signal.

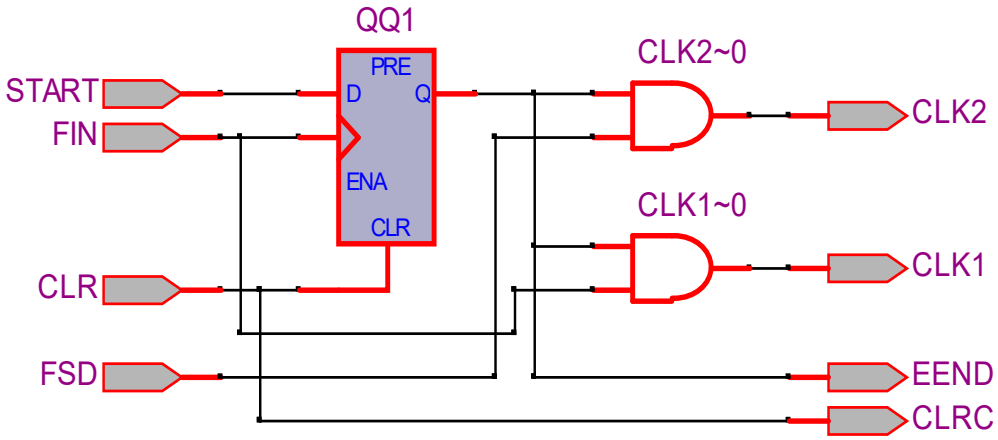



**Figure 4.** Clock control circuit of frequency measurement and period measurement.

3.2.3. Frequency Measurement and Counter Circuit Design

Figure 5 illustrates the circuit design and implementation ideas of the counting module. The key functional unit is the adder. Considering that the transmission delay brought by the 32-bit serial adder may lead to competition risks, this paper adopts the look-ahead carry algorithm to reduce the propagation delay. In addition, the frequency counting unit integrates a low-power circuit design method and reduces signal inversion through logic optimization methods such as decomposition and reduction in logic depth. Here, the carry generation logic will be transformed in the carryout logic cell, which can effectively eliminate false flip glitches and reduce the node switch activity rate. Further, the effect of path balance is achieved, thereby realizing the low-power consumption design of the counter combination logic. Finally, the counting final data are obtained after being triggered by the D flip-flop. This design approach is expected to reduce propagation delay and thus improve data accuracy, while also minimizing power consumption.

3.2.4. Double Precision High-Speed Pulse/Frequency Control Circuit

Figure 6 gives the ideas for high-speed pulse/frequency control circuit design. Its key functional unit is the equivalent trigger. In order to prevent signal interference in the circuit, a circuit to prevent misunderstanding is proposed. The signal is stabilized through the D trigger in the circuit, and the obtained result is then operated with the Q output end to improve the stability of the system. In addition, the method of generating the sign of the sampling signal by the equivalent trigger is generated by the equivalent trigger, thereby effectively improving the accuracy of the signal capture. In detail, pulse signals are sent to the signal CLR terminal for circuit initialization. The positive and negative pulse widths are measured by setting START. The Q-terminal value generated by the two D flip-flops is used to enter the equivalent flip-flop to generate the pulse measurement state end flag signal, ENDD, and the pulse counter switch flag PUL signal.

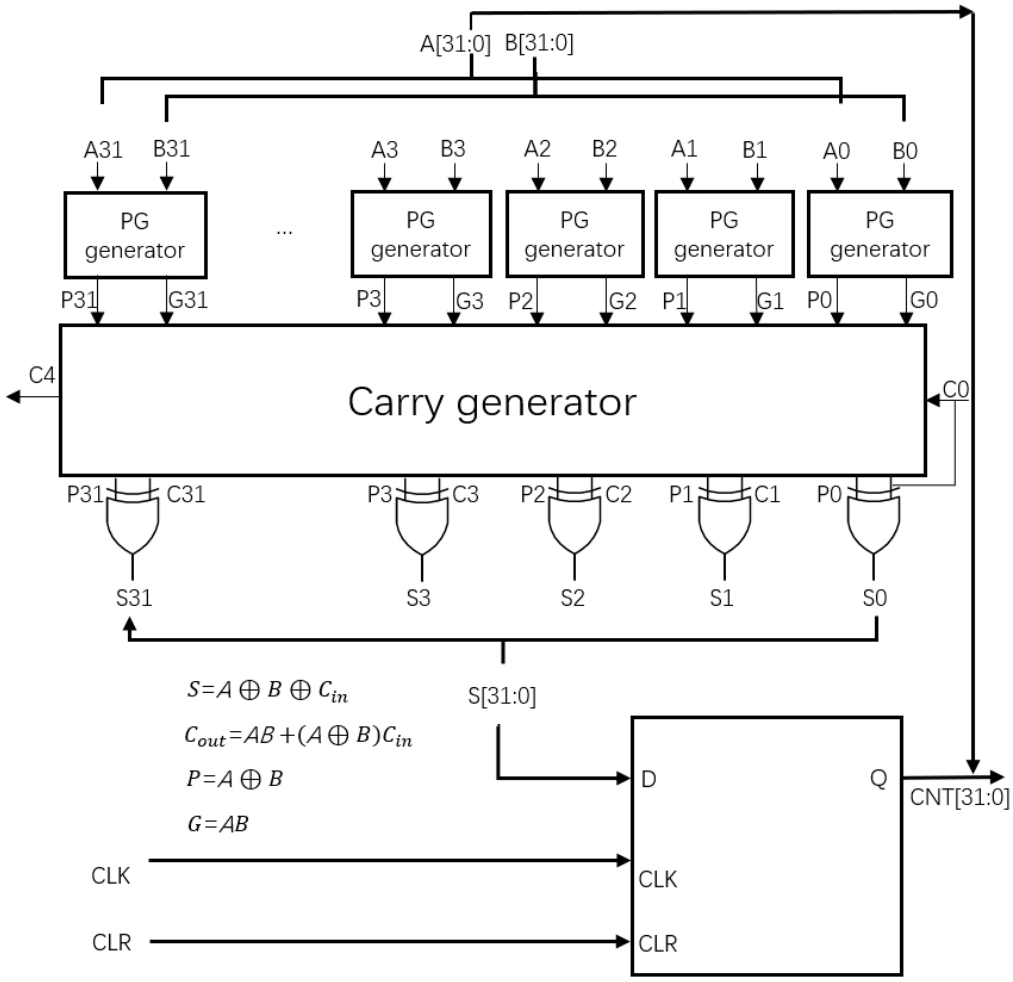



**Figure 5.** Counter circuit diagram.

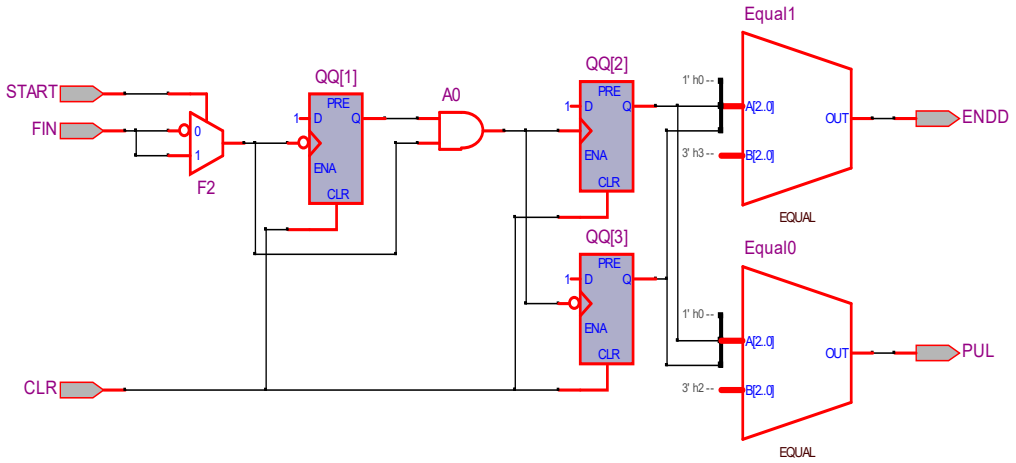


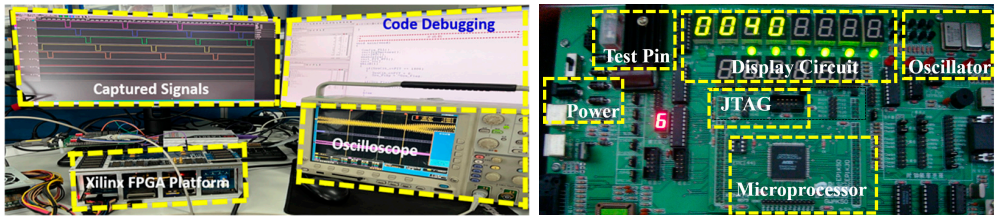

**Figure 6.** Pulse width measurement and duty cycle control block.

## 4. Results and Discussion

### *4.1. Experimental Setup*

Using the FPGA hardware prototype with the type of XILINX-XCVU440, the experimental verification system is built. Additionally, the control circuit with AT89C51 is employed to analyze and display data. Figure 7 describes experimental environments for testing and data processing in the corresponding signal; the circuit is verified and analyzed, and the data are in detail. Among them, the logic analyzer LA5016 with a sampling rate up

to 500 MHz/s and oscilloscope DSOX1102A with a sampling rate of up to 100 MHz/s are used to process and display the obtained signals in the AT89C51 control circuit. Based on this hardware platform, the internal clock signal can be frequently multiplied to 100 MHz when the active crystal oscillator of 20 MHz is inputted. In Figure 7, the code is burned to the microprocessor AT89C51 through the JTAG port of the microcontroller for data processing and conversion. Finally, the signal is outputted to the digital tube for real-time data display.




(**a**) (**b**)

**Figure 7.** (**a**) Test process observed from Xilinx FPGA. (**b**) Single-chip microcomputer data processing display circuit.

### *4.2. Function Verification*

The simulation results of the FPGA circuit module of the frequency meter are shown in Figures 8–12.

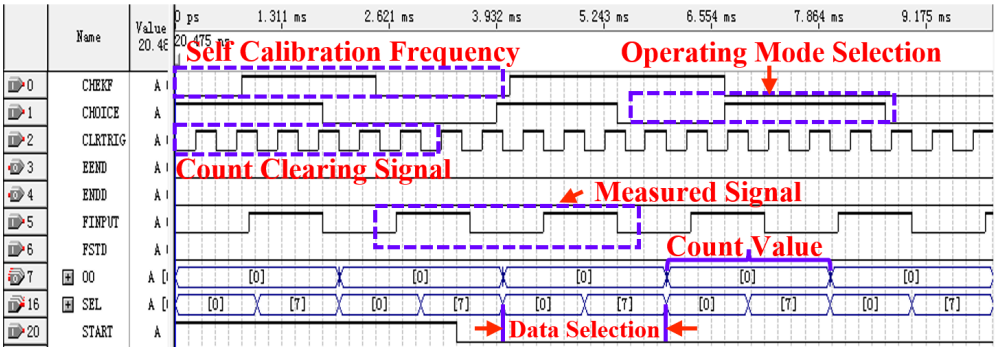



**Figure 8.** Waveform of top hierarchy module.

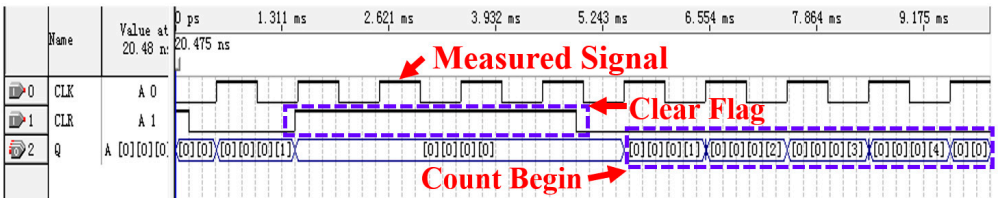



**Figure 9.** Waveform of counter block cnt.

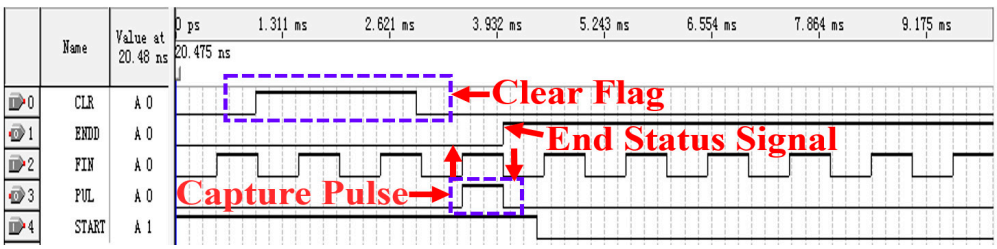



**Figure 10.** Pulse width measurement and duty cycle measurement.

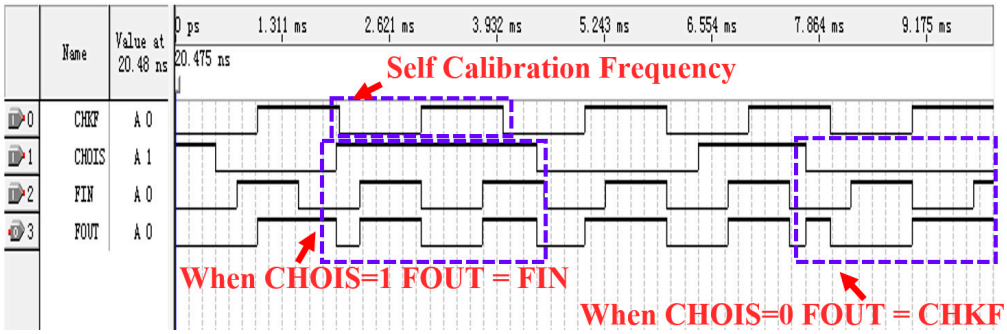



**Figure 11.** Self-calibration/test frequency selection circuit.

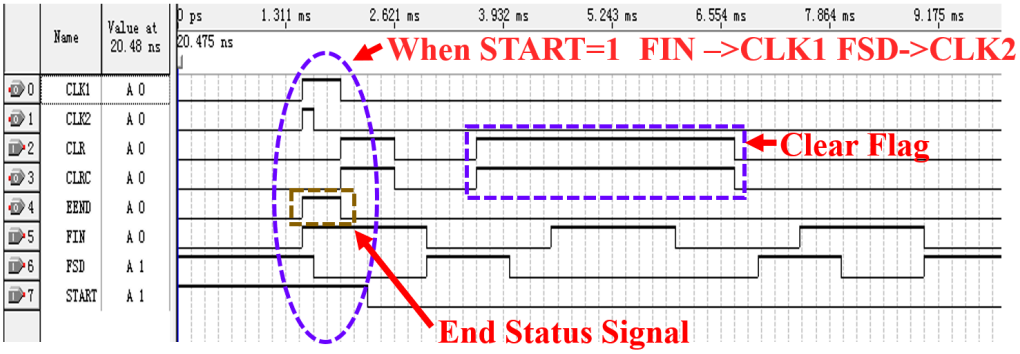



**Figure 12.** Frequency measurement/cycle control circuit.

Figure 8 shows the main functions of the frequency meter. Among them, when CLRTRIG = 0, the system is cleared and set. Herein, the CNT is started when the CLRTRIG is at the rising edge, where the pulse width test count is performed until the ENDD flips to a high-level count. The selection of self-calibration and frequency measurement modes is determined by the CHOICE signal. FINPUT can be provided by CHKF or FSTD. When START = 0, the counter is closed as a preset gate. When START = 1, the preset gate is opened, and the counter begins to work. Meanwhile, when START = 1 and 0, the positive and negative pulse widths are measured separately to obtain the duty cycle. Finally, SEL reads the selected count value and controls the data entering the microcontroller for processing and display. Through the choice of working mode in Figure 8, the circuit can be flexible, switching between self-calibration and frequency modulation modes, thereby improving the circuit sensitivity. When the measured frequency meets the requirements, the self-calibration frequency is in a closed state, which is beneficial to reduce power consumption.

Figure 9 shows the work case of the counting module. To initialize the test circuit state, a positive pulse signal is applied to the CLR end of the circuit, resulting in Q becoming low. When the CLR is recovered to a negative pulse, the Q-terminal begins to count. This process verifies the correctness of the counter circuit and meets the design requirements.

Figure 10 calculates the pulse width by capturing the rising and falling edges of signal FIN. Similarly, a positive pulse signal is applied to the CLR end in the CONTRL2 circuit, and then the test circuit enters the state initialization phase. After that, when the input START of the D flip-flop is set as high and the rising edge of the FIN signal is detected, the PUL side of the CONTRL2 outputs a high level. As a result, the standard frequency signal enters the counter CNT to complete the pulse width measurement. At the same time, the ENDD is set as high to complete the pulse width measurement.

Pulse width measurement and duty cycle measurement are conducted in Figure 11. The signal of FOUT can be configured as CHKF and FIN according to CHOIS. When the input CHOIS of the D flip-flop is high, the FIN channel is turned on to send the signal to the FOUT. When the input CHOIS of the D flip-flop is low, the CHKF channel is turned on

to send the signal to the FOUT. In the case of a mismatch of the measurement frequency, the circuit stability and flexibility can be improved by real-time switching operation.

Figure 12 shows the switching between the frequency acquisition and pulse width measurement. When the input START of the D flip-flop is set as high, FIN is turned on to transmit the signal to CLK1, and FSD is turned on to transmit the signal to CLK2 under the condition of the rising edge of FIN. After completing the above process, EEND is set to a high level as a symbol. When the input START of the D flip-flop is set as low, the data links of FIN → CLK1 and FSD → CLK2 are cut off under the condition of a rising edge of FIN. This process performs mode switching by configuring the high level of the START signal and tests the data link gating in time, which is helpful to verify the functional reliability of the circuit.

### *4.3. Performance Test*

#### 4.3.1. Adjustable High-Frequency Sine Signal Test

To measure the frequency characteristic of our proposed design, the test results of sine wave frequency meters are presented in Table 1 with different amplitudes and frequencies large than 1 MHz. The experimental results show that the maximum error is only 0.006% at 30 mV and 0.01% at 1 mV, respectively. After the adjustable high-frequency sine wave test, the error between the proposed design and the standard frequency is very small. This is because the frequency accuracy can be improved by the designed self-calibration module, and the error can be reduced by the equal precision frequency measurement.

**Table 1.** High-frequency sine channel test.

| Input Amplitude (mV) | Input Frequency (MHz) | 100 | 50 | 20 | 5 | 3 | 1 |
|---|---|---|---|---|---|---|---|
| 30 mV | Display Frequency (MHz) | 99.9940 | 49.9997 | 19.9997 | 4.9998 | 2.9999 | 1.0000 |
| | Error (%) | 0.0060 | 0.0006 | 0.0015 | 0.0040 | 0.0033 | 0.0000 |
| 1 mV | Display Frequency (MHz) | 99.9996 | 49.9998 | 19.9996 | 4.9997 | 2.9997 | 0.9999 |
| | Error (%) | 0.0004 | 0.0004 | 0.0020 | 0.0060 | 0.0100 | 0.0100 |

#### 4.3.2. Adjustable Low-Frequency Sine Signal Test

Similarly, the test results of sine wave frequency meters presented in Table 2 with different amplitudes and frequencies small than 500 KHz. After the low-frequency sine wave test, the error between the proposed design and the standard frequency is very small, which is lower than that of the high-frequency. The experimental results show that the maximum error is only 0.0075% at 30 mV and 0.0018% at 1 mV, respectively. This is due to the use of equal precision frequency measurement, which can greatly reduce the error. At the same time, it is also proven that the measured frequency accuracy is significantly improved through the self-calibration module optimization.

**Table 2.** Low-frequency sine channel test.

| Input Amplitude (mV) | Input Frequency (KHz) | 500 | 400 | 300 | 200 | 100 | 50 |
|---|---|---|---|---|---|---|---|
| 30 mV | Display Frequency (KHz) | 499.9960 | 399.9970 | 299.9996 | 199.9999 | 99.9998 | 49.9999 |
| | Error (%) | 0.0008 | 0.0075 | 0.0001 | 0.0001 | 0.0002 | 0.0002 |
| 1 mV | Display Frequency (KHz) | 499.9997 | 400.0070 | 300.0050 | 199.9990 | 99.9998 | 49.9999 |
| | Error (%) | 0.0001 | 0.0018 | 0.0017 | 0.0005 | 0.0002 | 0.0002 |

#### 4.3.3. Duty Cycle Test

Under the condition that the duty cycle is 40% and 60% at an amplitude of 1 volt, Table 3 shows the duty cycle test with the input frequency discretely changing. After testing, the duty cycle error between the proposed design and the standard frequency is very small. These results prove that the duty cycle accuracy can be significantly improved

by an equal precision frequency measurement method. In addition, in terms of error, the experimental results show that the maximum error is only 0.05% when the input duty cycle is 40%, and the maximum error is only 0.5% when the input duty cycle is 60%.

**Table 3.** Duty cycle test.

| Input Duty Cycle (%) | Input Frequency (KHz) | 500 | 400 | 300 | 200 | 100 | 50 |
|---|---|---|---|---|---|---|---|
| 40 | Display Duty Cycle (%) | 39.99 | 39.98 | 40.00 | 40.00 | 40.00 | 40.00 |
| | Error (%) | 0.030 | 0.050 | 0.000 | 0.000 | 0.000 | 0.000 |
| 60 | Display Duty Cycle (%) | 59.90 | 59.70 | 59.80 | 60.00 | 60.00 | 60.00 |
| | Error (%) | 0.170 | 0.500 | 0.330 | 0.000 | 0.000 | 0.000 |

#### 4.3.4. Power Consumption Evaluation

Using the XILINX chip, the obtained power consumption profiles are shown in Figure 13. It is measured in the case that the clock frequency multiplication reaches up to a maximum of 100 MHz. Note that the consumed power mainly comes from the RAM and cymometer. From the static power data listed in Table 4, the calculated total static power including the cymometer is only 0.56 W when the running time is more than 100 h. The small power is caused by the added gate-control clock in our design. When the input data of the register are invalid, the control clock stops the post-register signal from flipping, thus avoiding dynamic power consumption. In addition, the design of the carry look-ahead adder can reduce the additional power consumption caused by transmission delay.

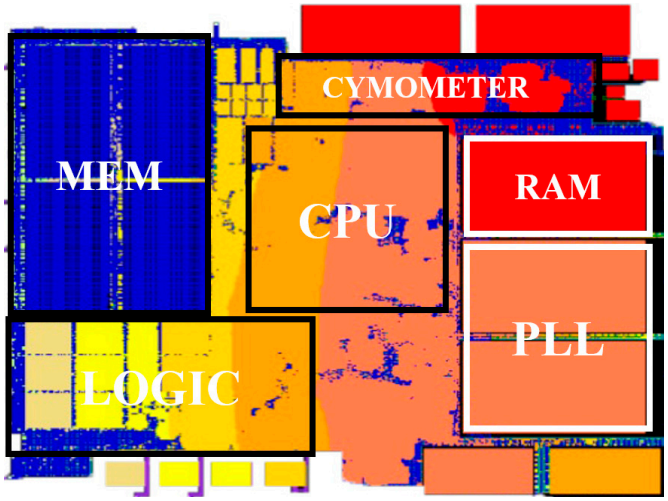



**Figure 13.** Simulate static power consumption distribution.

**Table 4.** Actual measured static power consumed by different modules.

| Resource | CYMOMETER | RAM | PLL | MEM | CPU | LOGIC |
|---|---|---|---|---|---|---|
| **Voltage (V)** | 0.720 | 0.850 | 0.850 | 1.800 | 1.800 | 0.050 |
| **Total (A)** | 0.164 | 0.035 | 0.003 | 0.195 | 0.033 | 0.020 |
| **Total (W)** | 0.118 | 0.029 | 0.003 | 0.351 | 0.059 | 0.001 |

The equal precision frequency measurement method eliminates quantization error and can maintain high accuracy throughout the test frequency band. Its accuracy will not change due to the high or low frequency of the measured signal. Through high-frequency and low-frequency experiments, it is known that the frequency acquisition measurement error is less than 1%, and the duty cycle measurement accuracy is less than 1%. The thermal scanner shows that the power consumption is lower than 0.56 W (Table 5).

**Table 5.** Performance comparison.

| / | Tang et al. 2020 [7] | Guo et al. 2021 [3] | This Work 2023 |
|---|---|---|---|
| **Method** | Periodic measurement | Frequency measurement | Equal precision measurement |
| **Measuring range** | Up to 100 KHz | Up to 50 MHz | Up to 100 MHz |
| **Frequency Stability of Crystal Oscillators (Crystal oscillator 20 MHz)** | 0.2 PPM | 0.1 PPM | 0.05 PPM |
| **Input sensitivity** | 30 mV RMS from 50 KHZ to 100 KHz | 20 mV RMS from 1 MHZ to 50 MHz | 15 mV RMS from 1 MHZ to 100 MHz |
| **Input high resistance/low resistance** | 1 MΩ/50 Ω | 1 MΩ/50 Ω | 1 MΩ/50 Ω |
| **Power Consumption** | 1 W | 0.8 W | 0.56 W |

## 5. Conclusions

In this paper, a programable digital frequency meter is designed based on the principle of equal precision frequency measurement with field-programmable gate array FPGA as the core. Using Verilog description language and a top-down design method, the MCU program is written to communicate with FPGA, and the PCB circuit is drawn to build the system. The errors of frequency, period measurement, duty cycle measurement, and time interval are within a reasonable range. The physical production proves that when the measured signal is within the range of 50 KHz~100 MHz, the circuit can operate stably, and the measurement accuracy of each index reaches the index. At the same time, power consumption and stability are also greatly improved.

**Author Contributions:** Conceptualization, L.Z. and J.W.; methodology, N.W. and J.T.; software, C.Z.; validation, C.F., Y.L. and N.W.; formal analysis, C.Z.; investigation, Y.L.; resources, N.W.; data curation, Y.X.; writing—original draft preparation, Y.L.; writing—review and editing, N.W.; visualization, C.F.; supervision, Y.L.; project administration, F.D. and Y.L.; funding acquisition, S.X. and N.W. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the Shanghai Natural Science Foundation, grant number 21ZR1446300.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** Not applicable.

**Conflicts of Interest:** The authors declare no conflict of interest.

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