An Event-Detection High Dynamic Range CMOS Image Sensor

Gözen Köklü[1,2], Dechao Sun[1], Yusuf Leblebici[2], Giovanni De Micheli[1], and Sandro Carrara[1]

[1]Integrated Systems Laboratory (LSI), Swiss Federal Institute of Technology (EPFL)
[2]Microelectronic Systems Laboratory (LSM), Swiss Federal Institute of Technology (EPFL)

***Abstract*—A novel CMOS image sensor is proposed to overcome the analog design limitations in *Active Pixel Sensors* - APS and large area overcome in *Digital Pixel Sensors* - DPS for use in bio-medical applications. The design includes a pixel level event generation mechanism by using a binary search technique. A ramp voltage generated by a combined block of 10-bit counter and DAC *Digital to Analog Converter* is compared with the pixel integrated voltage at each clock cycle at the same time allowing a fixed exposure time interval. The proposed design arrives to a total pixel array area of $1505.62\mu m \times 4566\mu m$ for a pixel array size of $160(H) \times 120(V)$. The photo-active area in each pixel is considered as the N-well area in a p+/n-well/p-sub type photo-transistor corresponding to a size of $11.24\mu m \times 10.76\mu m$. The overall pixel array reaches a fill factor of %34.**

I. Introduction

After the first introduction of electronic camera-on-a-chip concept [1], many techniques and designs have been proposed by scientists to overcome the disadvantages of the current designs in order to reach compatible results with *Charge-Coupled Devices* - CCDs, to add chip or pixel level new features and to design for more application specific constraints. Among these proposed designs, *Active Pixel Sensors* [2] have been the one that is used most due to its simplicity and low area cost which can be implemented by minimum a single transistor and a photo sensitive device. However, the APS designs suffer from the analog design limitations since the value of each pixel is represented in voltage and output as an analog signal. An alternative to APS designs is later proposed as *Digital Pixel Sensor* - DPS where the designs no longer suffer from analog design limitations and the pixel output is carried out as a digital signal and the design no longer requires an extra *Analog to Digital Convertor* (ADC) unit per column or per chip. DPS designs are known to achieve high speeds i.e. 10000 fps proposed in [3], and wide dynamic range of over 100 dB [4], and propose additional features such as adaptive dynamic range as in [5]. *Pulse Width Modulation* - PWM and *Pulse Frequency Modulation* - PFM image sensors are also considered within DPS architectures. Pulse modulation sensors, as opposed to APS designs where the output signal value is read after a certain time has passed, produces the output signal when the signal reaches a certain value. Similarly, these type of architectures no longer represent the pixel value in voltage domain but in time or frequency domain as presented in [6], [7], [8].

Similar to other digital pixel sensor designs, this design benefits from the inherited advantages of DPS architectures i.e. wide dynamic range and gets rids of the limitations of analog design and extra (ADC) unit while requiring less area than the related state of the art designs [3] and [9]. However, unlike the pulse modulation techniques, this design outputs the digital pixel value after a certain time. Moreover, due to the pixel output bus lines connected to each column level encoders, the design can be advantageous in terms of the area only for low array sizes (lower or equal to Q-QVGA). The fill factor of this design achieves better results than [3] and [9], where as mentioned earlier, in [3], an 8-bit Dynamic RAM is used for each pixel which is the limiting factor for the resolution of the sensor as well as the fill-factor. In [9], due to the large area of pixel control unit for communication with the *Address-Event Protocol* (AER), the pixel has reached again a large non-photosensitive area. In addition, since the memory in this proposed design is not a dynamic one but a static one, the sensor is appropriate for long-exposure times, which is of great importance for low-light bio-medical applications.

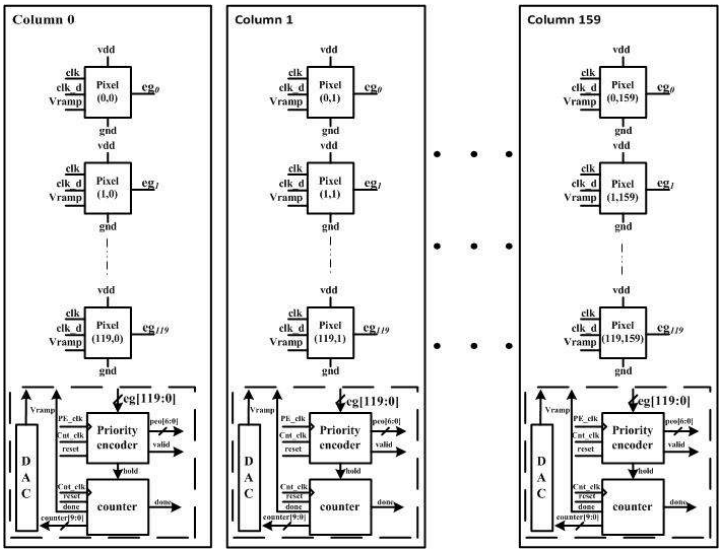
This design is implemented by using UMC $0.18\mu m$ Standard CMOS process. With this proposed design, each pixel continuously monitors its photo-voltage for events and the location of the corresponding pixel with the event is registered. The address of the pixel with the event is encoded by means of a priority encoder. The sensitivity (minimum detectable light) and the dynamic range of the image sensor are determined by the comparator and counter resolution, which are both 10-bits in this implementation. However, depending on the application the counter and the DAC can be designed with higher resolution without bringing a large area penalty since these blocks are present per column or per chip.

II. Design and Implementation

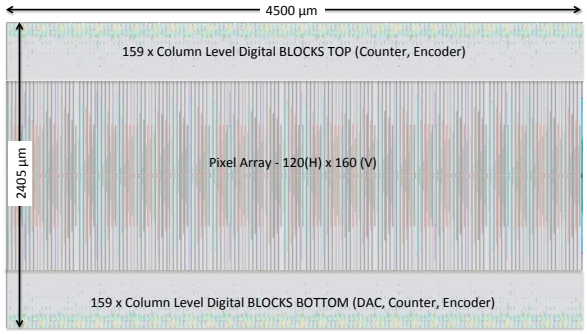
The top level schematic of the design is shown in Fig. 1. The proposed design targets a display resolution of Quarter - QVGA (QQVGA) which denotes a resolution of 120(H) x 160(V) or 160(H) x 120(V). In the proposed design, the chip includes 160(H) and 120(V) pixel arrays.

The working principle of the design is as follows. Each column includes 120 pixels, a priority encoder, a decrement counter and a DAC *Digital to Analog Converter*. The pixel architecture includes a photodiode, a reset transistor (RS), a latched-comparator and a novel photo voltage change monitoring system by means of a 1 bit register and an XOR gate as seen in Fig. 2. A ramp voltage is generated by the combined block of a 10-bit decrement counter and a DAC for each column independently. The design can also be realized by a common counter and DAC block for all columns

978-1-4673-4642-9/13/$31.00 ©2013 IEEE



(a) Top Level Schematic View of the Proposed Design



(b) Top Level Layout View of the Proposed Design

Figure 1: Top Level Design

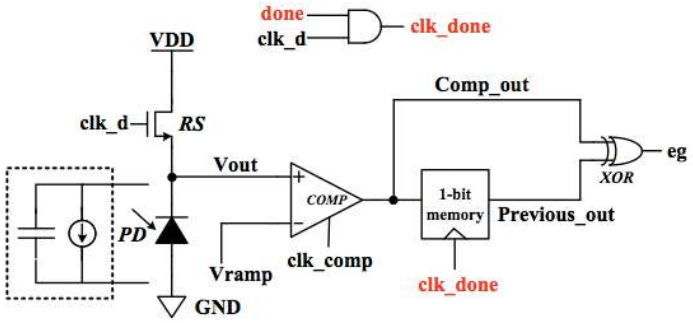


Figure 2: Schematic View of a Single Pixel

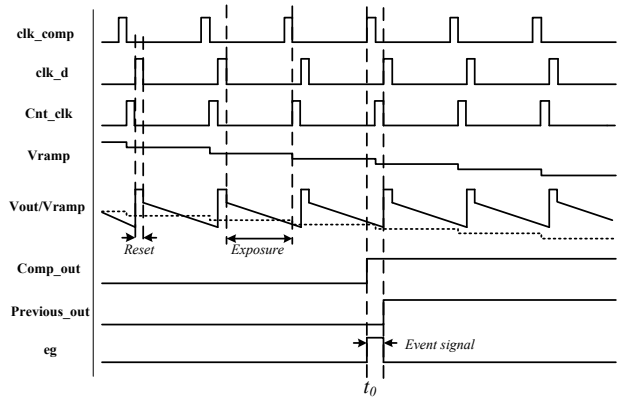


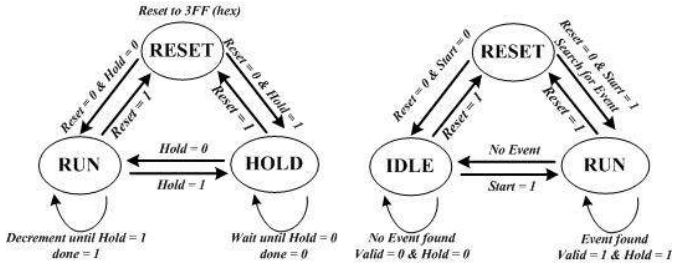
Figure 3: Timing Diagram of a Single Pixel

instead of per column counter-DAC blocks. The technique is based on binary search where the digital control logic (counter) decrements bits at each clock cycle. After each decrement, the input voltage of the pixels (which is the integrated pixel voltage in this case) is compared with the reference voltage generated by the Counter-DAC block. When the input voltage is higher than the generated ramp voltage, as seen in Fig. 3, the event detector in the pixel is triggered to 1 by means of a comparator, 1-bit register and XOR gate and the *event generation* (eg) signal becomes 1. In the next clock cycles, the pixel output (eg) will return to 0 since the value in the pixel will always stay higher than the ramp voltage after the first event and the XOR result of the first event (1) and the next output of the comparator (1) will result in 0.

In Fig. 2 and 3, *clk_comp* represents the comparator clock, *Cnt_clk* denotes for the counter clock and the *clk_d* represents the delayed version of *clk_comp* used for the reset transistor *RS* and the 1-bit memory cell. Later, the clock of the 1-bit register is modified to *clk_done* which is implemented by an *AND* operation with one of the outputs of the decrement counter, *Done* signal, and the *clk_d*.

Fig. 4 explains the finite state machine of the decrement counter and the encoder block to get a better insight on the corresponding input and output signals. The counter block has 3 phases as *Reset*, *Hold* and *Run*. In the reset phase, the value in the counter is reset to its initial value which is 1023 in decimal and initiated only when receiving a new frame and the counter has decremented to 0. The counter gets into *Hold* mode, only if multiple pixels are active and the priority has to be shifted from one to another until all the active pixel addresses are registered. The *Hold* signal of the counter is an input for the counter block and controlled by the *Hold* output of the encoder. Finally, in the *Run* mode, the counter decrements its value at each clock cycle. Similar to the counter phases, the encoder block has also 3 phases as *Reset*, *Idle* and *Run*. The *Reset* phase is controlled with the same signal as the counter, the *Idle* phase means no event has been found in any pixels and no address has to be registered and finally the *Run* mode means, single or multiple events have been found and the priority should be shifted and each priority encoder output should be registered which gives the address of the active pixel for the known counter value.

The working principle of each independent column in case



(a) FSM of decrement counter (b) FSM of priority encoder

Figure 4: Finite State Machines of Digital Blocks

of single (Fig. 5a) and multiple (Fig. 5b) event conditions is explained in more detail in Fig. 5.

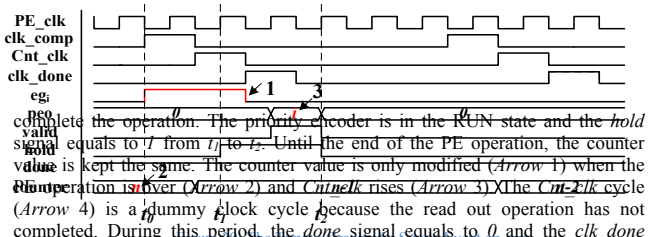
The single event case is trivial, where pointer *1* represents the generated event from one of the pixels in a column, pointer *2* represents the counter value at the time of the event or the value of the pixel with the event and the arrow *3* points the priority encoder output that represents the address of the active pixel.

For cases where multiple pixels are active at the same time, the priority encoder implementation is used to give priority to one pixel at a time in a column. In this case, first, the location of the pixel with highest priority is registered and all the other active pixels are queued until they receive the priority. The priority can be shifted from the least significant to most significant pixel or vice versa or other orders can be used. In this design, the first method has been implemented. As explained earlier, during priority shifting, the counter is in *Hold* mode as shown by pointer *2* and the ramp voltage value is no longer changed until the priority shifts to the lowest priority pixel. It is also seen that during the *Hold* mode, even if the counter's clock has risen (pointer *4*), until the next clock cycle of the counter (pointer *3*), the counter keeps its previous value (pointer *1*).

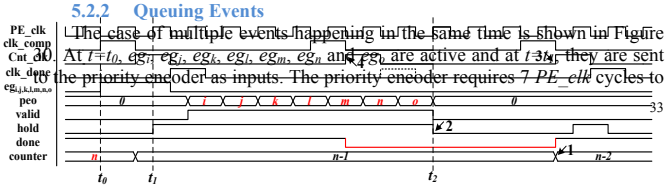
The idea of a priority encoder is similar to AER *Address Event Registration* protocol but the difference is that the pixels do not require acknowledge or request hand-shaking signals since each pixel uses a separate output line. After passing through the priority encoder, the location information of the pixels are represented by 7 bit data for 120 row lines. The read-out of each column output is considered to be serialized by multiplexing the column outputs with an 8-bit Multiplexer. The final output of the overall system should be considered to include the serialized priority encoder outputs together with the encoder's *Hold* and *Valid* and the counter's *Done* signal output. These signals will be used to regenerate the counter value at the time of each event for the corresponding active pixels when constructing the images. The clock of the counter, priority encoder and the main clock of the system is also expected to be known during this read-out.

The comparator, included in each pixel design is implemented by a two-stage comparator where the first stage is a pre-amplifier stage to ensure the 12-bit resolution which is larger than the resolution of the decrement counter and DAC block for future higher resolution targets and the second stage is a clocked comparator to sample the pixel value at the same time for each pixel with the determined clock - *clk_comp*. The schematic of the comparator is shown in Fig. 6 and the simulation results confirms

corresponds to the last counter value *n* (*Arrow* 2) and is sent to PE as an input at $t=t_1$. PE requires 2 *PE_clk* cycles to complete the operation and outputs the location of the event, *i* (*Arrow* 3). During the operation time of PE, from t_1 to t_2, the *hold* signal equals to *1*.



(a) Single Event Generation Mechanism



(b) Multiple Event Generation Mechanism

Figure 5: Event Generation and Priority Shifting Principle

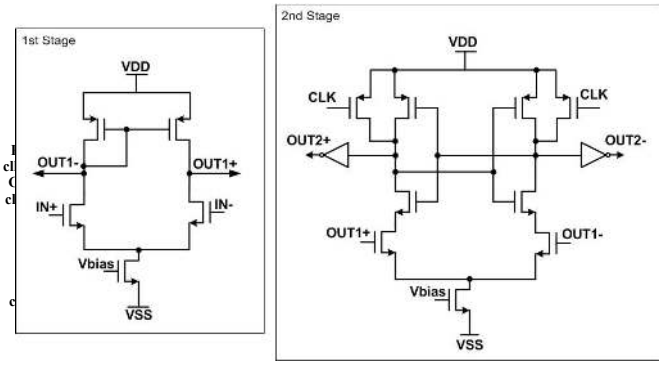
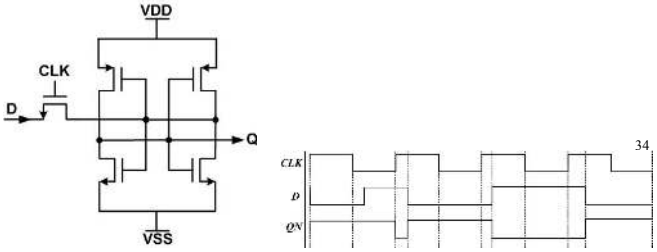


Figure 6: Schematic View of the 2-Stage Comparator

a minimum detectable voltage of 0.2mV with this design.



(a) Schematic View of the 5-T SRAM (b) Timing Diagram of the 5-T SRAM

Figure 7: 5-Transistor SRAM Cell

For the 1-bit register cell of each pixel, there are multiple ways of implementing the register where D-latch and 5-T or 6-T SRAM are some possible ways of doing it. For this design, 5-T SRAM is preferred due to its lower area as seen in Fig. 7a and the timing diagram of this cell can be found in Fig. 7b. The DRAM *Dynamic RAM* is not considered as an option for this design although it can be implemented by 3 transistors only, since DRAMs tends to discharge and loose their value during long exposure time.

The layout of a 2×2 pixel array together with the pixel output buses are shown in Fig. 8. The pixel array reaches a

fill factor of %34 where the photo active area is implemented by relatively large p+/n- well/psub type photo-transistors. This type of phototransistors are known to provide 4.5 times higher responsivity than n+/p-sub type photodiodes and 1.8 times higher responsivity than n-well/p-sub type photodiodes [10]. However, they have area draw back and lower sensitivity compared to n+/p-sub type photodiodes due to their large capacitance.

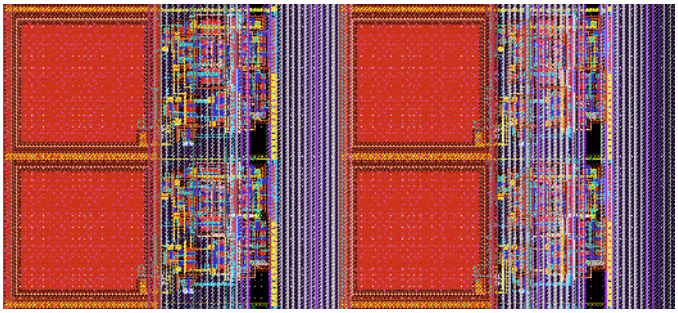


Figure 8: Layout View of 2x2 Pixel Array

The overall layout of the design has been shown in Fig. 1b. In this design, two counters and encoders are used per column at the top and the bottom of the pixel area as seen the figure in order to decrease the number of bus lines coming out of the pixels and going to the priority encoder as inputs. The large number of bus lines are the limiting factor of this design and makes this design compatible for only lower array sensors. During the layout of the design, special attention has been taken in order to limit the area cost by these lines by generating them with higher metal levels than the ones used in the pixel and by going over the pixel non-photosensitive areas with the bus lines in order not to limit the extra area caused by the bus lines.

III. Simulation Results

During this design, different analog, digital and mixed mode simulators and design environments are used. The photodiode, comparator, 5T-SRAM, the logic gates and the DAC blocks are designed in Full-Custom and simulated by using Cadence Analog Environment Spectre Simulator. The RTL level design of the counter and priority encoder parts are written in verilog and synthesized with Design Compiler Tool. The synthesized design is placed and routed by using Encounter Tool. For overall system simulations, first Cadence Analog Environment with mixed mode simulators (SpectreVerilog Simulator) and after importing the placed and routed digital designs to cadence, post synthesis simulations are done by Cadence Spectre Simulator. In Fig. 9, a mixed mode simulation is shown as an example where multiple pixels have the same voltage level and have been queued for the priority to be shifted.

IV. CONCLUSION

A novel event-generation high dynamic range CMOS image sensor is proposed to overcome design limitations in APS and DPS designs. A latched-comparator with a pre-amp is designed which resolves up to 0.2mV for voltage ranges from 0.35-1.45V arriving a resolution of 12-bits. A 5T-Static RAM is designed for use in the 1-bit register due to its low area. In this design,

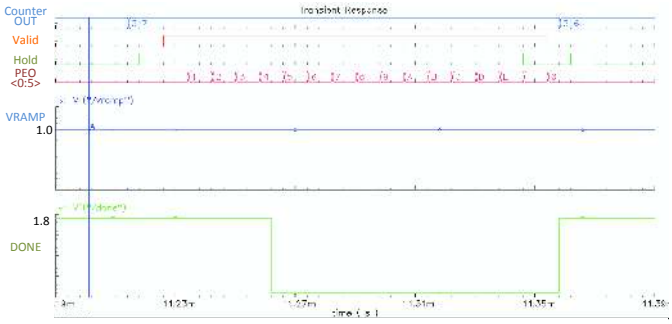


Figure 9: Mixed Mode Multiple Event Generation Simulation

two counters and encoders are used per column at the top and the bottom of the pixel area. This design has an array size of $160(H) \times 120(V)$ achieves 10 bit resolution. The overall area of the design, including the pixel array and the counter and encoder digital blocks, is $4500\mu m \times 2405\mu m$. The pixel array reaches a fill factor of %34. The future work includes the fabrication of this design and having a comparative chip test result with the simulation results, as well as a simulation level validation of an updated version of the current design with pixel hand-shaking protocol.

Acknowledgment

The research work presented in this paper was funded by the NutriCHIP project with a grant from the Swiss Nano-Tera.ch initiative, evaluated by the Swiss National Science Foundation. It was also partially supported by the NanoSys project (program ERC-2009-AdG-246810).

References

[1] Fossum, E. R. (1997). *CMOS image sensors: Electronic camera-on-a-chip.* Electron Devices, IEEE Transactions on, 44(10), 1689-1698.

[2] Mendis, S. K., Kemeny, S. E., Gee, R. C., Pain, B., Staller, C. O., Kim, Q., & Fossum, E. R. (1997). *CMOS active pixel image sensors for highly integrated imaging systems.* Solid-State Circuits, IEEE Journal of, 32(2), 187-197.

[3] Kleinfelder, S., Lim, S., Liu, X., & El Gamal, A. (2001). *A 10000 frames/s CMOS digital pixel sensor.* Solid-State Circuits, IEEE Journal of, 36(12), 2049-2059.

[4] Bidermann, W., El Gamal, A., Ewedemi, S., Reyneri, J., Tian, H., Wile, D., & Yang, D. (2003). *A 0.18 um high dynamic range NTSC/PAL imaging system-on-chip with embedded DRAM frame buffer.* In Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International (pp. 212-488).

[5] Kitchen, A., Bermak, A., & Bouzerdoum, A. (2005). *A digital pixel sensor array with programmable dynamic range.* Electron Devices, IEEE Transactions on, 52(12), 2591-2601.

[6] Nagata, M., Homma, M., Takeda, N., Morie, T., & Iwata, A. (1999). *A smart CMOS imager with pixel level PWM signal processing.* In VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on (pp. 141-144). IEEE.

[7] Shouho, M., Hashiguchi, K., Kagawa, K., & Ohta, J. (2005, June). *A low-voltage pulse-width-modulation image sensor.* In IEEE Workshop on Charge-Coupled Devices & Advanced Image Sensors (pp. 226-229).

[8] Yang, W. *Awide-dynamic-range,low-powerphotosensorarray.* InDig.Tech. Papers Int. Solid-State Circuits Conf. (ISSCC), pages 230-231, February 1994.

[9] Guo, X., Qi, X., & Harris, J. G. (2007). *A time-to-first-spike CMOS image sensor.* Sensors Journal, IEEE, 7(8), 1165-1175.

[10] Koklu, G., Etienne-Cummings, R., Leblebici, Y., De Micheli, G. & Carrara, S. *Characterization of Standard CMOS Compatible Photodiodes and Pixels for Lab-on-Chip Devices.* In Circuits and Systems (ISCAS), 2013 IEEE International Symposium on (pp. 1075-1078). 19-22 May, Beijing